Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101rgt6tr

Table 5. STM32F101xF/STM32F101xG pin definitions (continued)

Pins			Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
37	17	26	PA3	I/O	-	PA3	USART2_RX(8) / TIM5_CH4/ ADC_IN3 / TIM2_CH4(8)/ TIM9_CH2	-
38	18	27	V_{SS_4}	S	-	V_{SS_4}	-	-
39	19	28	V_{DD_4}	S	-	V_{DD_4}	-	-
40	20	29	PA4	I/O	-	PA4	SPI1_NSS/ DAC_OUT1 / ADC_IN4 / USART2_CK(8)	-
41	21	30	PA5	I/O	-	PA5	SPI1_SCK / DAC_OUT2 / ADC_IN5	-
42	22	31	PA6	I/O	-	PA6	SPI1_MISO / ADC_IN6 / TIM3_CH1(8) / TIM13_CH1	-
43	23	32	PA7	I/O	-	PA7	SPI1_MOSI / ADC_IN7 / TIM3_CH2(8)/ TIM14_CH1	-
44	24	33	PC4	I/O	-	PC4	ADC_IN14	-
45	25	34	PC5	I/O	-	PC5	ADC_IN15	-
46	26	35	PB0	I/O	-	PB0	ADC_IN8 / TIM3_CH3(8)	-
47	27	36	PB1	I/O	-	PB1	ADC_IN9 / TIM3_CH4(8)	-
48	28	37	PB2	I/O	FT	PB2/BOOT1	-	-
49	-	-	PF11	I/O	FT	PF11	FSMC_NIOS16	-
50	-	-	PF12	I/O	FT	PF12	FSMC_A6	-
51	-	-	V_{SS_6}	S	-	V_{SS_6}	-	-
52	-	-	V_{DD_6}	S	-	V_{DD_6}	-	-
53	-	-	PF13	I/O	FT	PF13	FSMC_A7	-
54	-	-	PF14	I/O	FT	PF14	FSMC_A8	-
55	-	-	PF15	I/O	FT	PF15	FSMC_A9	-
56	-	-	PG0	I/O	FT	PG0	FSMC_A10	-
57	-	-	PG1	I/O	FT	PG1	FSMC_A11	-
58	-	38	PE7	I/O	FT	PE7	FSMC_D4	-
59	-	39	PE8	I/O	FT	PE8	FSMC_D5	-
60	-	40	PE9	I/O	FT	PE9	FSMC_D6	-
61	-	-	V_{SS_7}	S	-	V_{SS_7}	-	-

Table 6. FSMC pin definition (continued)

Pins	FSMC					LQFP100[1]
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PD9	D14	D14	D14	DA14	D14	Yes
PD10	D15	D15	D15	DA15	D15	Yes
PD11	-	-	A16	A16	CLE	Yes
PD12	-	-	A17	A17	ALE	Yes
PD13	-	-	A18	A18		Yes
PD14	D0	D0	D0	DA0	D0	Yes
PD15	D1	D1	D1	DA1	D1	Yes
PG2	-	-	A12	-	-	-
PG3	-	-	A13	-	-	-
PG4	-	-	A14	-	-	-
PG5	-	-	A15	-	-	-
PG6	-	-	-	-	INT2	-
PG7	-	-	-	-	INT3	-
PD0	D2	D2	D2	DA2	D2	Yes
PD1	D3	D3	D3	DA3	D3	Yes
PD3	-	-	CLK	CLK	-	Yes
PD4	NOE	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7	-	-	NE1	NE1	NCE2	Yes
PG9	-	-	NE2	NE2	NCE3	-
PG10	NCE4_1	NCE4_1	NE3	NE3	-	-
PG11	NCE4_2	NCE4_2	-	-	-	-
PG12	-	-	NE4	NE4	-	-
PG13	-	-	A24	A24	-	-
PG14	-	-	A25	A25	-	-
PB7	-	-	NADV	NADV	-	Yes
PE0	-	-	NBL0	NBL0	-	Yes
PE1	-	-	NBL1	NBL1	-	Yes

1. Ports F and G are not available in devices delivered in 100-pin packages.

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 12* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 12. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(2)	Reset temporization	-	1.5	2.5	3.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design.

Figure 11. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

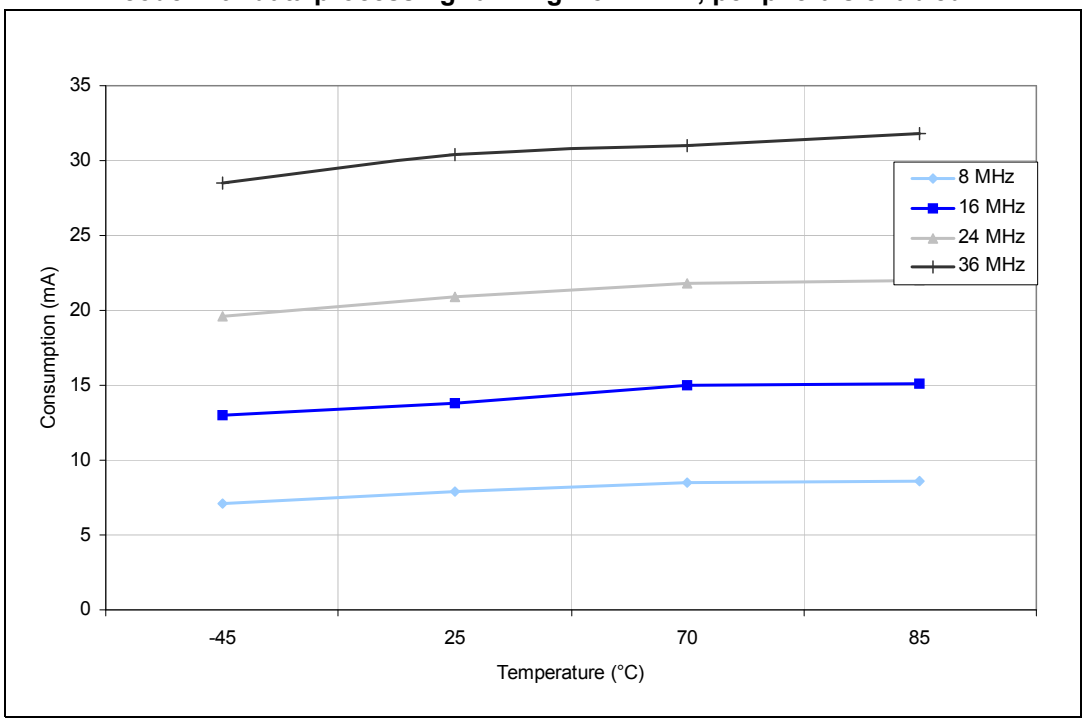


Figure 12. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled

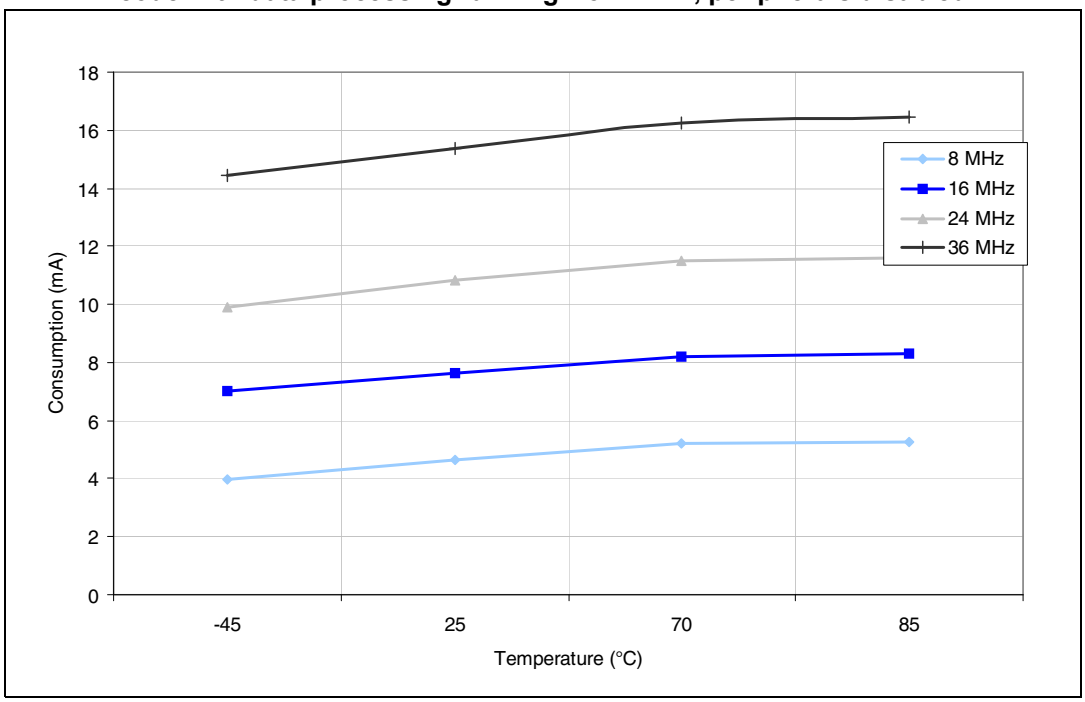


Figure 13. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values

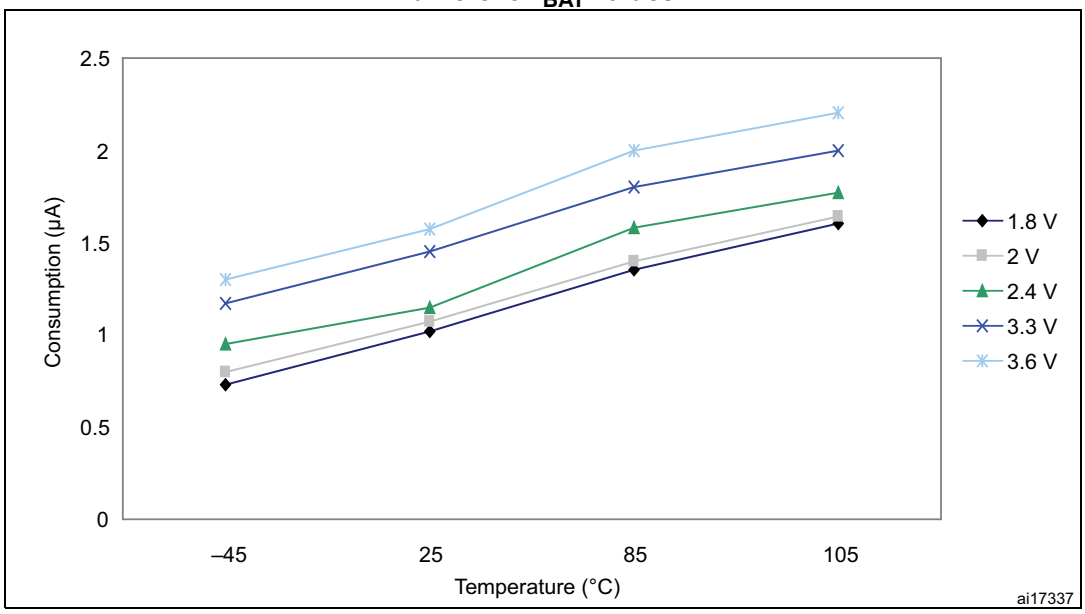
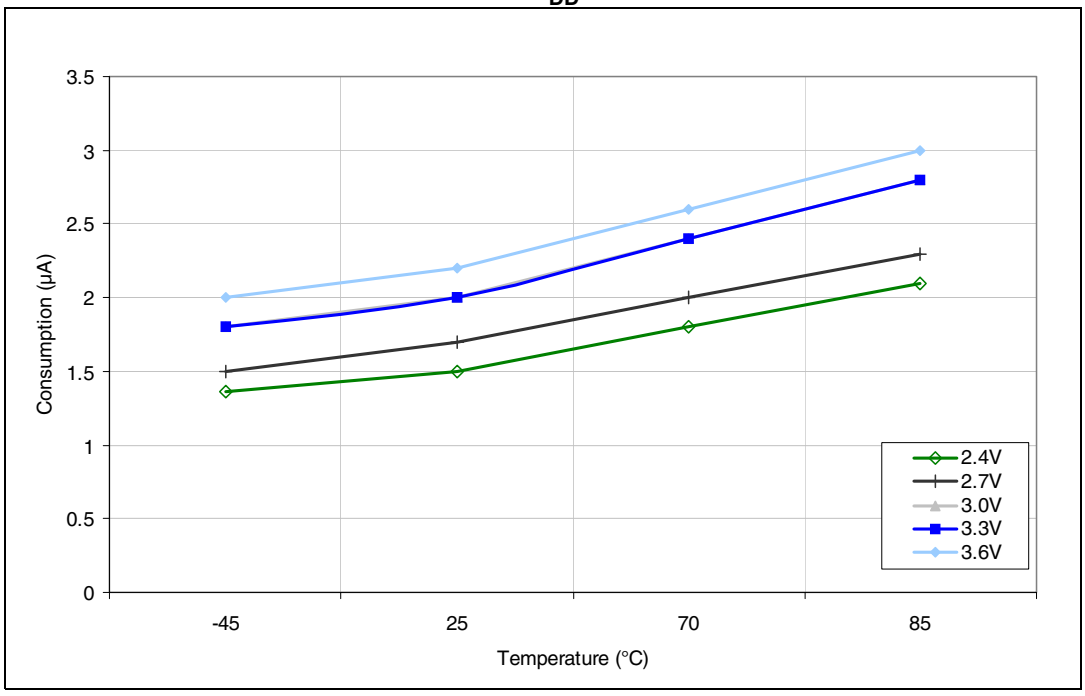


Figure 14. Typical current consumption in Standby mode versus temperature at different V_{DD} values



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)
- Prefetch is on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/4}$, $f_{PCLK2} = f_{HCLK/2}$, $f_{ADCCLK} = f_{PCLK2}/4$
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/2$

The parameters given in *Table 18* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 18. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1) All peripherals enabled(2)	Typ(1) All peripherals disabled	Unit
I_{DD}	Supply current in Run mode	External clock(3)	36 MHz	28.5	18.7	mA
			24 MHz	24.1	12.8	
			16 MHz	14	9.2	
			8 MHz	7.7	5.4	
			4 MHz	4.6	3.4	
			2 MHz	3	2.3	
			1 MHz	2.2	1.8	
			500 kHz	1.7	1.5	
			125 kHz	1.4	1.3	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	27.5	17.5	
			24 MHz	18.9	11.6	
			16 MHz	12.2	8.2	
			8 MHz	7.2	4.8	
			4 MHz	4	2.7	
			2 MHz	2.3	1.7	
			1 MHz	1.5	1.2	
			500 kHz	1.1	0.9	
			125 kHz	0.75	0.7	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

5.3.8 PLL characteristics

The parameters given in *Table 28* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 28. PLL characteristics

Symbol	Parameter	Value			Unit
		Min(1)	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	36	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 85 °C unless otherwise specified.

Table 29. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +85 °C	40	52.5	70	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +85 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +85 °C	20	-	40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 36 MHz with 1 wait state, V_{DD} = 3.3 V	-	-	28	mA
		Write mode f_{HCLK} = 36 MHz, V_{DD} = 3.3 V	-	-	7	mA
		Erase mode f_{HCLK} = 36 MHz, V_{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage	-	2	-	3.6	V

1. Guaranteed by design.

Figure 22. Asynchronous multiplexed NOR/PSRAM write waveforms

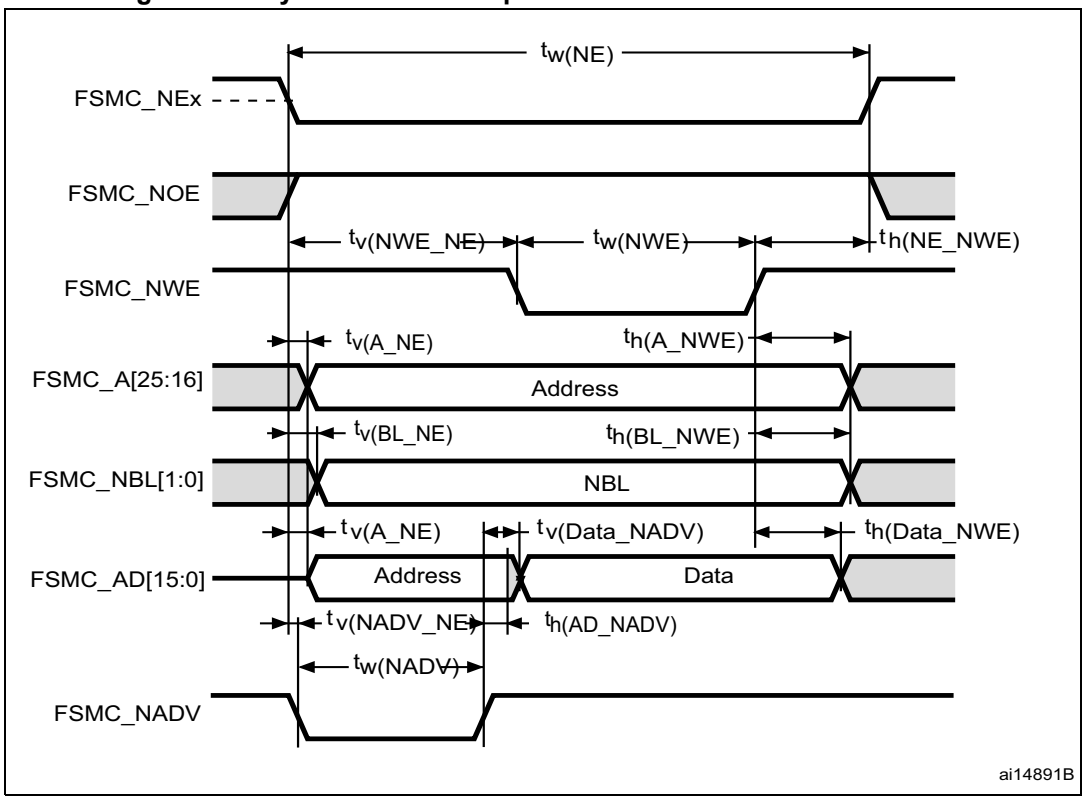


Table 34. Asynchronous multiplexed NOR/PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5t_{HCLK}$ + 0.5	$5t_{HCLK}$ + 2	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	t_{HCLK} + 1	t_{HCLK} + 1.5	ns
$t_{w(NWE)}$	FSMC_NWE low time	$3t_{HCLK}$ – 1	$3t_{HCLK}$ + 2	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	t_{HCLK} - 0.5	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	3.5	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	0	1	ns
$t_{w(NADV)}$	FSMC_NADV low time	t_{HCLK} + 0.5	t_{HCLK} + 1.5	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	t_{HCLK} – 0.5	-	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$4t_{HCLK}$ – 2	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	t_{HCLK} – 1.5	-	ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	t_{HCLK} + 6	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	t_{HCLK} – 0.5	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

Table 35. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	55.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	0.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	1	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0.5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	1.5	-	ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	14	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	11	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0.5	-	ns
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	2	-	ns
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	8	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

Table 36. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_Nex low (x = 0...2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	1	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	1	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	1	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1.5	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	10	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	1	-	ns
$t_{d(CLKL-Data)}$	FSMC_A/D[15:0] valid after FSMC_CLK low	-	6	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	1	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

2. Guaranteed by characterization results.

Figure 26. Synchronous non-multiplexed PSRAM write timings

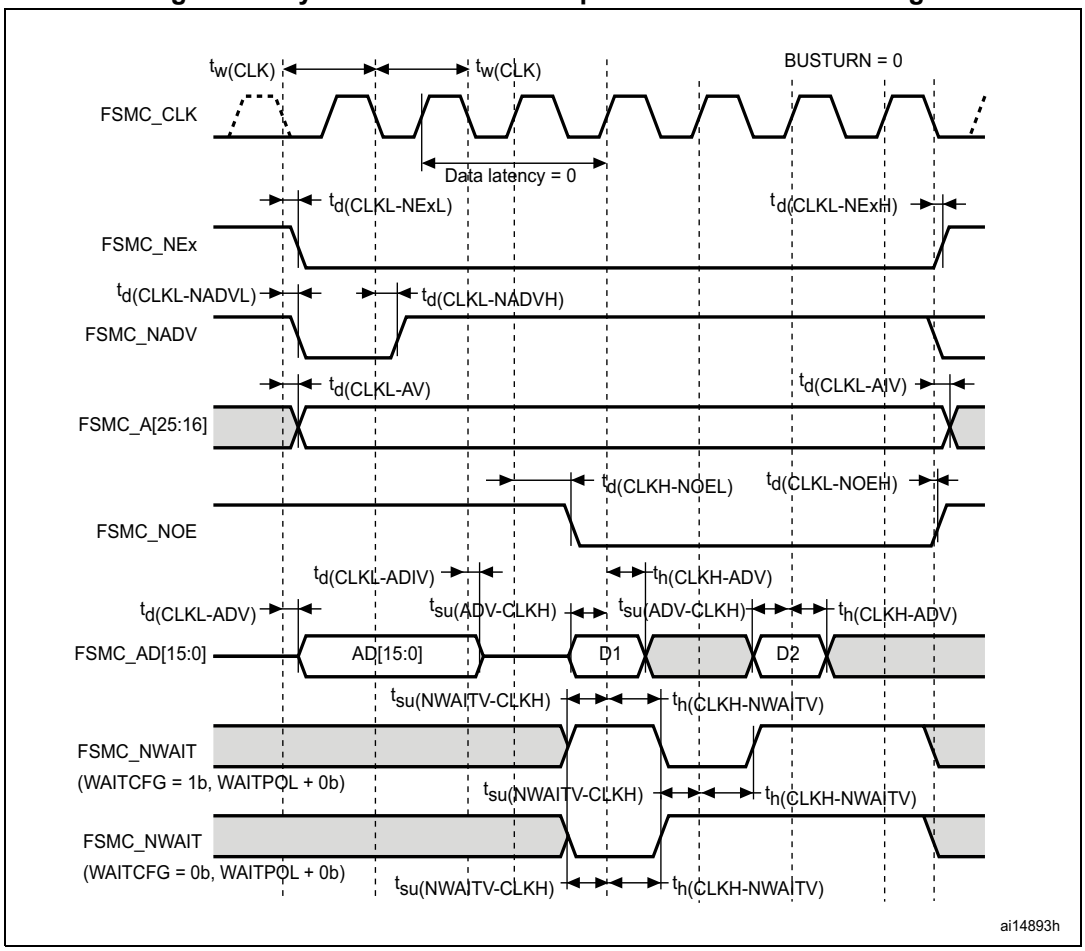
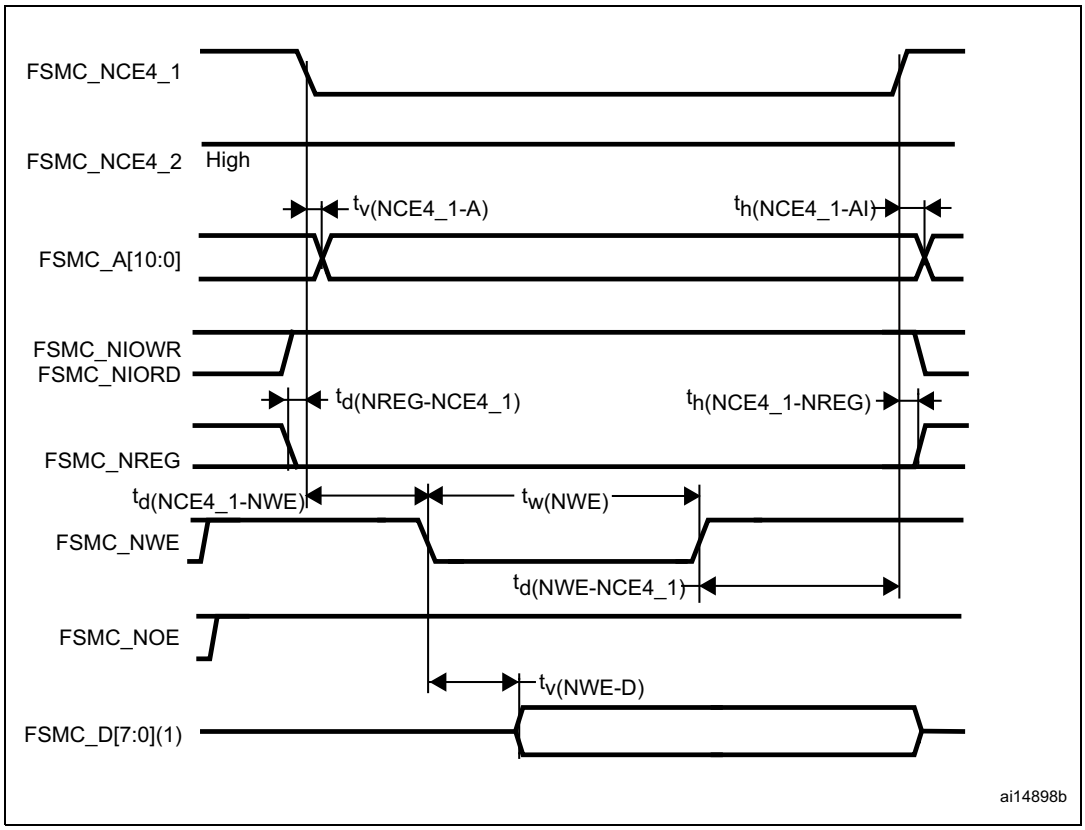


Table 38. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.6	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	0.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	1.5	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0.5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	1.5	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1.5	-	ns
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low	-	2.5	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	0.5	-	ns

Figure 30. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains HiZ).

Figure 31. PC Card/CompactFlash controller waveforms for I/O space read access

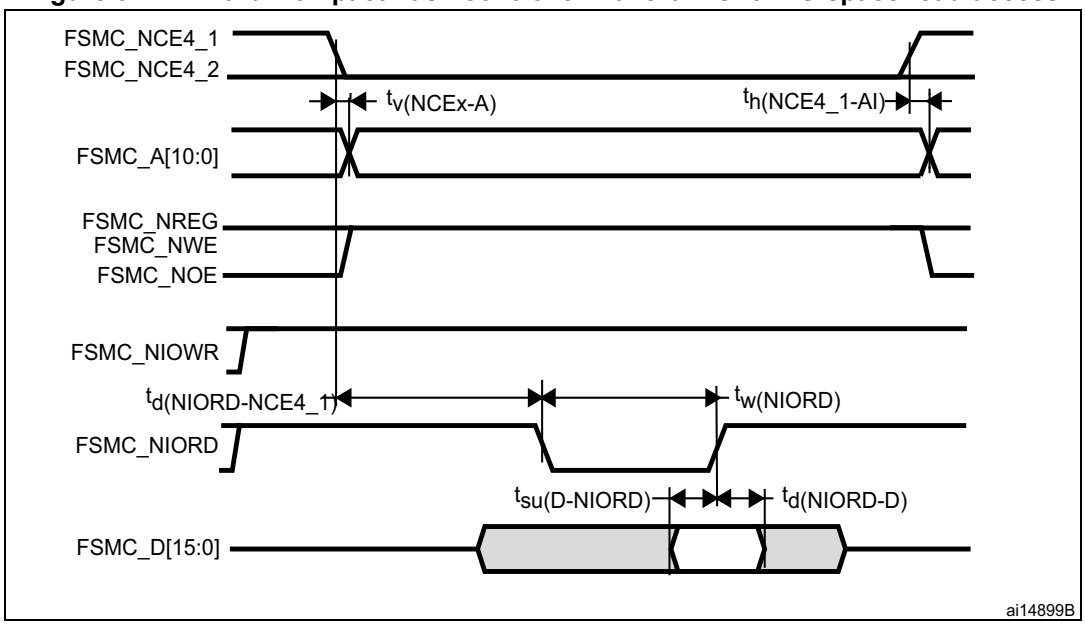


Table 40. Switching characteristics for PC Card/CF read and write cycles in I/O space

Symbol	Parameter	Min	Max	Unit
$tw_{(NIOWR)}$	FSMC_NIOWR low width	8 THCLK	-	ns
$tv_{(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	5 THCLK - 4	ns
$th_{(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	11THCLK - 7	-	ns
$td_{(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	5THCLK + 1	ns
$th_{(NCEx-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid	5THCLK - 2.5	-	ns
$td_{(NIORD-NCEx)}$	FSMC_NCEx low to FSMC_NIORD valid	-	5THCLK - 0.5	ns
$th_{(NCEx-NIORD)}$	FSMC_NCEx high to FSMC_NIORD) valid	5 THCLK - 0.5	-	ns
$tw_{(NIORD)}$	FSMC_NIORD low width	8THCLK	-	ns
$tsu_{(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	28	-	ns
$td_{(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	3	-	ns

NAND controller waveforms and timings

Figure 33 through *Figure 36* represent synchronous waveforms and *Table 40* and *Table 41* provide the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x00;
- COM.FSMC_WaitSetupTime = 0x02;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x02;
- ATT.FSMC_HoldSetupTime = 0x01;
- ATT.FSMC_HiZSetupTime = 0x00;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 36. NAND controller waveforms for common memory write access

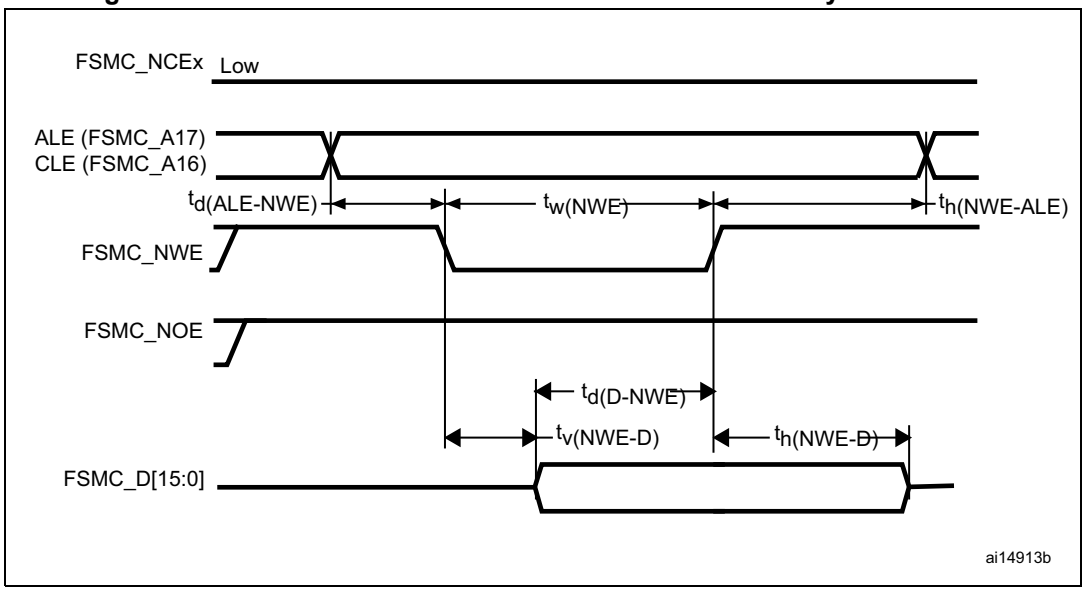


Table 41. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FSMC_NWE low width	$3t_{HCLK}$	$3t_{HCLK}$	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] invalid	$2t_{HCLK}$ + 2	-	ns
$t_{d(ALE-NWE)}$	FSMC_ALE valid before FSMC_NWE low	-	$3t_{HCLK}$ + 1.5	ns
$t_{h(NWE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3t_{HCLK}$ + 8	-	ns
$t_{d(ALE-NOE)}$	FSMC_ALE valid before FSMC_NOE low	-	$2t_{HCLK}$	ns
$t_{h(NOE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$2t_{HCLK}$	-	ns

1. C_L = 15 pF.

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 42*. They are based on the EMS levels and classes defined in application note AN1709.

Table 42. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK}= 36 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 36 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 43. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/36 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP144 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	8	dBµV
			30 MHz to 130 MHz	27	
			130 MHz to 1 GHz	26	
			SAE EMI Level	4	-

The test results are given in *Table 46*

Table 46. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 54Table 55* are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 10*.
Refer to *Section 5.3.13: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 54. STM32F10xxx SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	10	MHz
		Slave mode	-	10	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	73	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode - SPI1	3	-	
		Master mode - SPI2	5	-	
		Slave mode	4	-	
$t_{h(MI)}$ (1)	Data input hold time	Master mode - SPI1	4	-	
		Master mode - SPI2	6	-	
$t_{h(SI)}$ (1)		Slave mode	5	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 36 MHz, presc = 4	0	55	
		Slave mode, f_{PCLK} = 20 MHz	-	$4t_{PCLK}$	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	10	-	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	25	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	6	-	

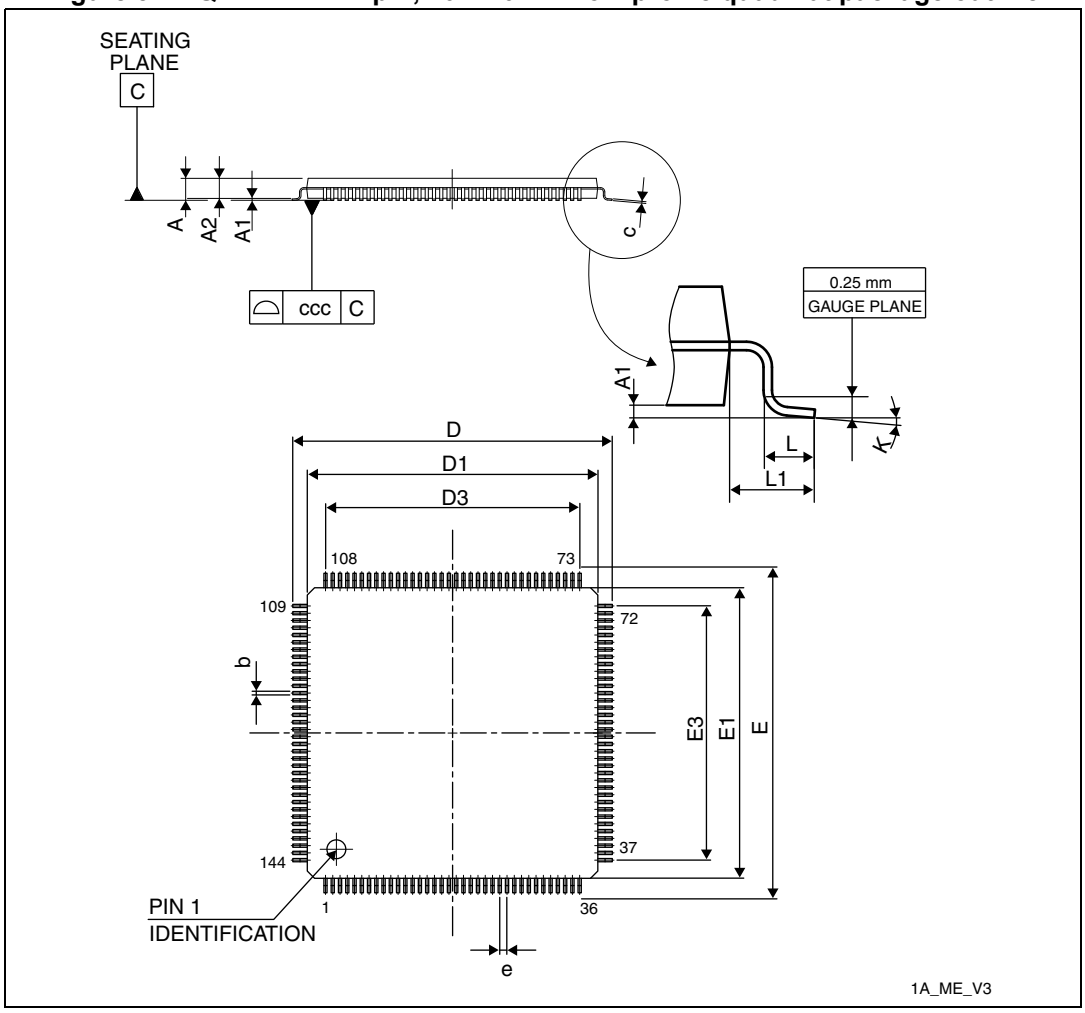
1. Guaranteed by characterization results.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.1 LQFP144 package information

Figure 52. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 67. Document revision history (continued)

Date	Revision	Changes
25-Nov-2014	3	Updated number of ADCs in *Table 2: STM32F101xF and STM32F101xG features and peripheral counts*. Modified *Section 2.3.22: GPIOs (general-purpose inputs/outputs) on page 21*. Added note below *Figure 3: LQFP144 pinout*, *Figure 4: LQFP100 pinout*, and *Figure 5: LQFP64 pinout*. Modified OSC_IN, OSC_OUT, PD0, PD1, PB8, PB9 and PF8 in *Table 5: STM32F101xF/STM32F101xG pin definitions on page 25*/ Updated notes related to parameters not tested in production in the whole document. Modified notes in *Table 7: Voltage characteristics on page 37* and *Table 8: Current characteristics on page 38*. Removed ADC2/3 and CAN from *Table 20: Peripheral current consumption on page 48*. Modified $t_{w(HSE)}$ value in *Table 21: High-speed external user clock characteristics on page 50*. Updated *Table 24: LSE oscillator characteristics (f_{LSE} = 32.768 kHz) on page 53*. Changed JESD22-C101 to ANSI/ESD STM5.3.1 in *Section : Electrostatic discharge (ESD)*. Updated *Section 5.3.10: FSMC characteristics on page 57*. Updated *Figure 41: I/O AC characteristics definition*. Updated conditions related to *Section : I^2C interface characteristics on page 87*. Modified *Table 52: I^2C characteristics on page 87*, updated *Figure 43: I^2C bus AC waveforms and measurement circuit(1)* and V_{DD}/V_{DD_I2C} conditions in *Table 53: SCL frequency (f_{PCLK1}= 36 MHz, V_{DD} = V_{DD_I2C} = 3.3 V) on page 88*. Modified *Section : Output driving current on page 82*. Modified *Table 52: I^2C characteristics on page 87* and updated *Figure 43: I^2C bus AC waveforms and measurement circuit(1)*. Modified *Figure 46: SPI timing diagram - master mode(1) on page 92*. Modified notes in *Table 56: ADC characteristics on page 93* and *Table 59: ADC accuracy on page 95*. Updated I_{DDA} definition in *Table 60: DAC characteristics on page 97* and removed comment related to the offset parameter for ±10 mV. Added Device marking information for all packages.