What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101vft6

Contents

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F101xF and STM32F101xG XL-density access line microcontrollers. For more details on the whole STMicroelectronics STM32F101xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The XL-density STM32F101xx datasheet should be read in conjunction with the STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the www.arm.com website.

2.3.10 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers are used to configure the AHB frequency, the high-speed APB (APB2) domain and the low-speed APB (APB1) domain. The maximum frequency of the AHB and APB domains is 36 MHz. See *Figure 2* for details on the clock tree.

2.3.11 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash: you have an option to boot from any of two memory banks. By default, boot from Flash memory bank 1 is selected. You can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The bootloader is located in system memory. It is used to reprogram the Flash memory by using USART1.

2.3.12 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 9: Power supply scheme*.

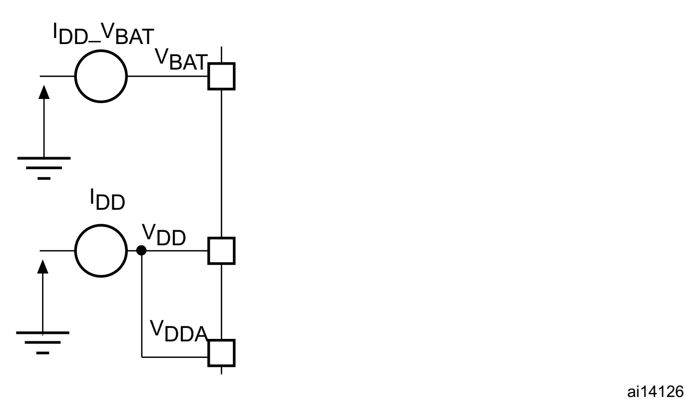
2.3.13 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 12: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and V_{PVD}.

5.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 7: Voltage characteristics*, *Table 8: Current characteristics*, and *Table 9: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD})[1]	–0.3	4.0	V
V_{IN}[2]	Input voltage on five volt tolerant pin	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins including V_{REF-}	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.12: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. V_{IN} maximum must always be respected. Refer to *Table 8: Current characteristics* for the maximum allowed injected current values.

Figure 11. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

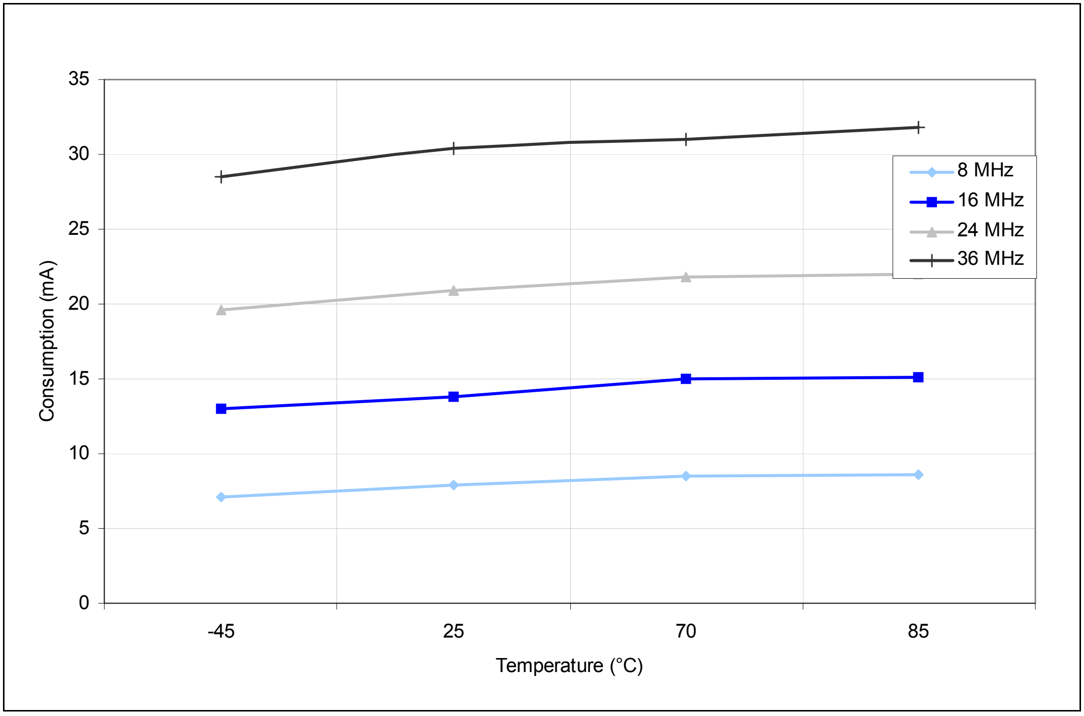
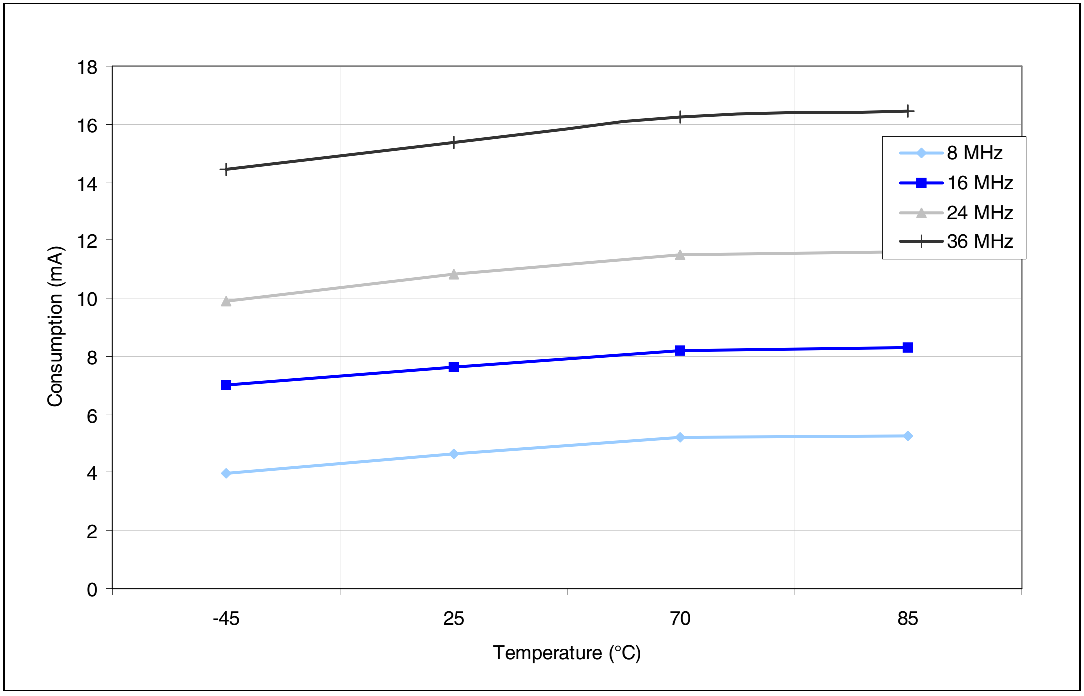


Figure 12. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)
- Prefetch is on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/4}$, $f_{PCLK2} = f_{HCLK/2}$, $f_{ADCCLK} = f_{PCLK2}/4$
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/2$

The parameters given in *Table 18* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 18. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ[1]	Typ[1]	Unit
				All peripherals enabled[2]	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock[3]	36 MHz	28.5	18.7	mA
			24 MHz	24.1	12.8	
			16 MHz	14	9.2	
			8 MHz	7.7	5.4	
			4 MHz	4.6	3.4	
			2 MHz	3	2.3	
			1 MHz	2.2	1.8	
			500 kHz	1.7	1.5	
			125 kHz	1.4	1.3	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	27.5	17.5	
			24 MHz	18.9	11.6	
			16 MHz	12.2	8.2	
			8 MHz	7.2	4.8	
			4 MHz	4	2.7	
			2 MHz	2.3	1.7	
			1 MHz	1.5	1.2	
			500 kHz	1.1	0.9	
			125 kHz	0.75	0.7	

1. Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 21. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Low-speed external user clock generated from an external source

The characteristics given in *Table 22* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

Table 22. Low-speed user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)	-	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)	-	-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

5.3.8 PLL characteristics

The parameters given in *Table 28* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 28. PLL characteristics

Symbol	Parameter	Value			Unit
		Min[1]	Typ	Max[1]	
f_{PLL_IN}	PLL input clock[2]	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	36	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 85 °C unless otherwise specified.

Table 29. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
t_{prog}	16-bit programming time	T_A = –40 to +85 °C	40	52.5	70	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +85 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +85 °C	20	-	40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 36 MHz with 1 wait state, V_{DD} = 3.3 V	-	-	28	mA
		Write mode f_{HCLK} = 36 MHz, V_{DD} = 3.3 V	-	-	7	mA
		Erase mode f_{HCLK} = 36 MHz, V_{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage	-	2	-	3.6	V

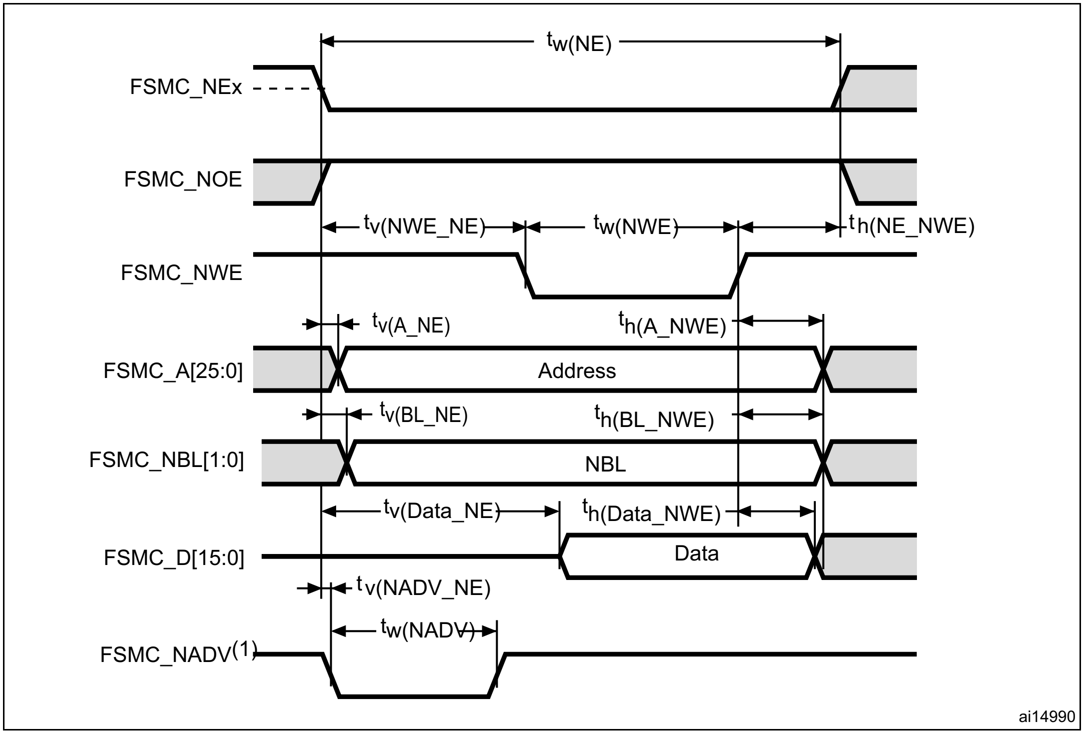
1. Guaranteed by design.

Table 31. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1) (2)

Symbol	Parameter	Min	Max	Unit
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	0	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	t_{HCLK} + 2	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

Figure 20. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

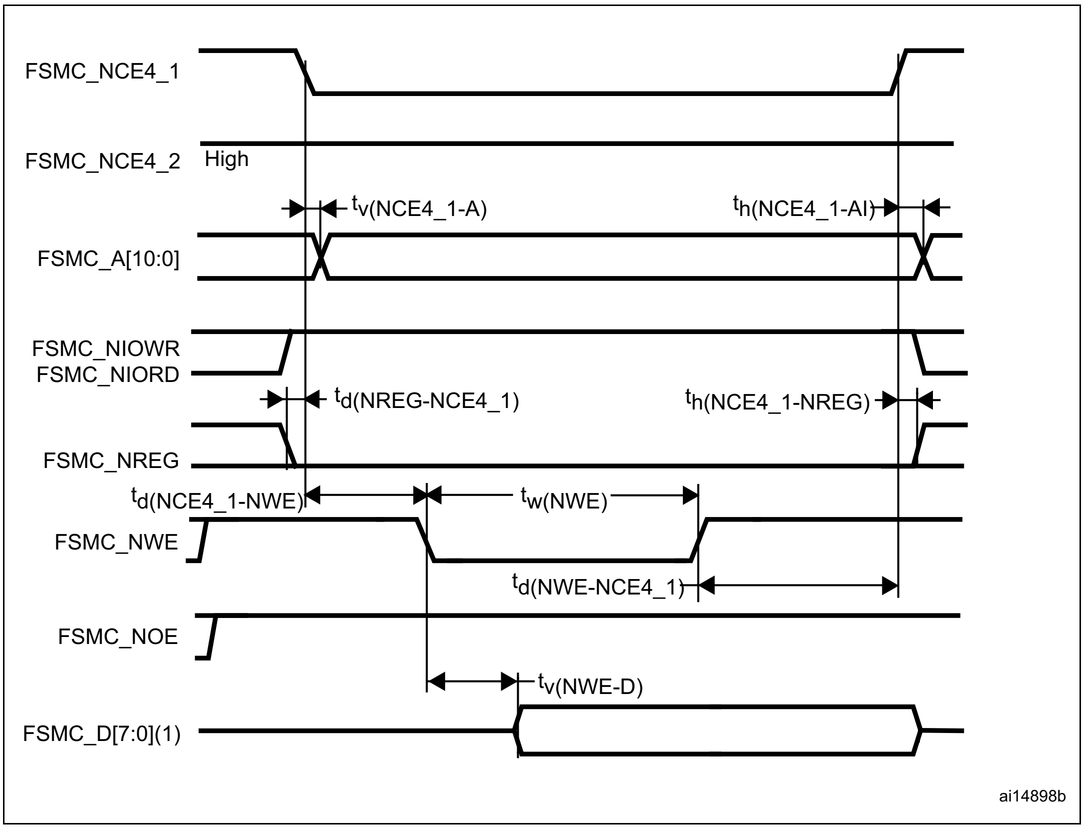


1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 32. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3t_{HCLK}$ + 0.5	$3t_{HCLK}$ + 1.5	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	t_{HCLK} + 0.5	t_{HCLK} + 1.5	ns
$t_{w(NWE)}$	FSMC_NWE low time	t_{HCLK} – 0.5	t_{HCLK} + 1	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	t_{HCLK} – 0.5	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	t_{HCLK}	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1.5	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	t_{HCLK} – 1.5	-	ns
$t_{v(Data\_NE)}$	FSMC_NEx low to Data valid	-	t_{HCLK}	ns

Figure 30. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains HiZ).

Figure 31. PC Card/CompactFlash controller waveforms for I/O space read access

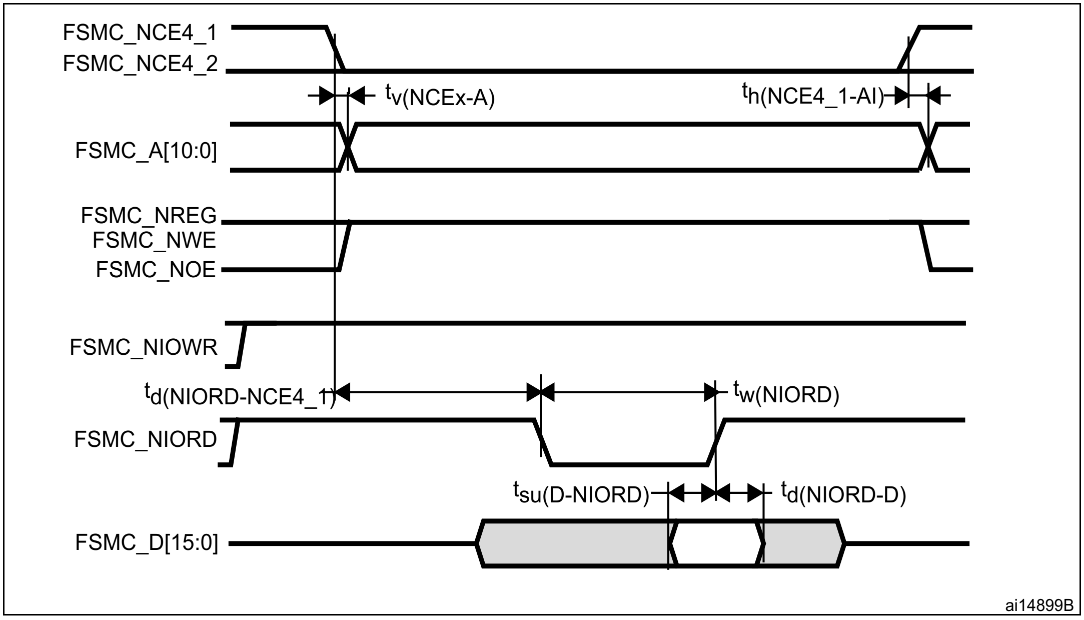


Figure 36. NAND controller waveforms for common memory write access

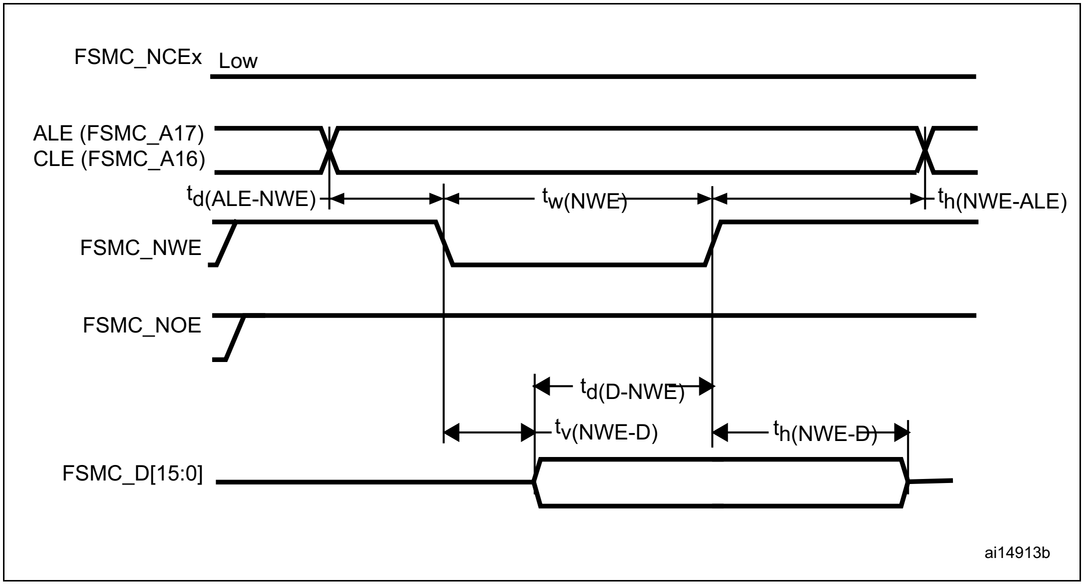


Table 41. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FSMC_NWE low width	$3t_{HCLK}$	$3t_{HCLK}$	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] invalid	$2t_{HCLK} + 2$	-	ns
$t_{d(ALE-NWE)}$	FSMC_ALE valid before FSMC_NWE low	-	$3t_{HCLK} + 1.5$	ns
$t_{h(NWE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3t_{HCLK} + 8$	-	ns
$t_{d(ALE-NOE)}$	FSMC_ALE valid before FSMC_NOE low	-	$2t_{HCLK}$	ns
$t_{h(NOE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$2t_{HCLK}$	-	ns

1. C_L = 15 pF.

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

Figure 39. 5 V tolerant I/O input characteristics - CMOS port

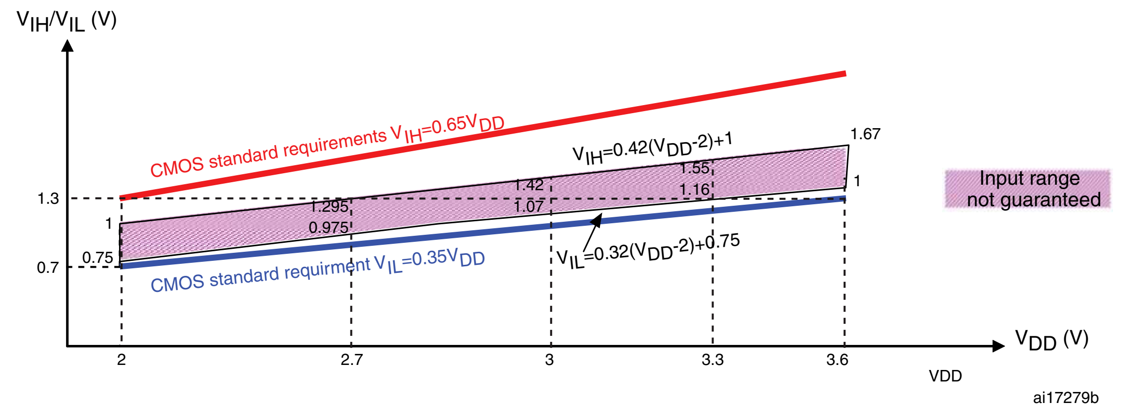
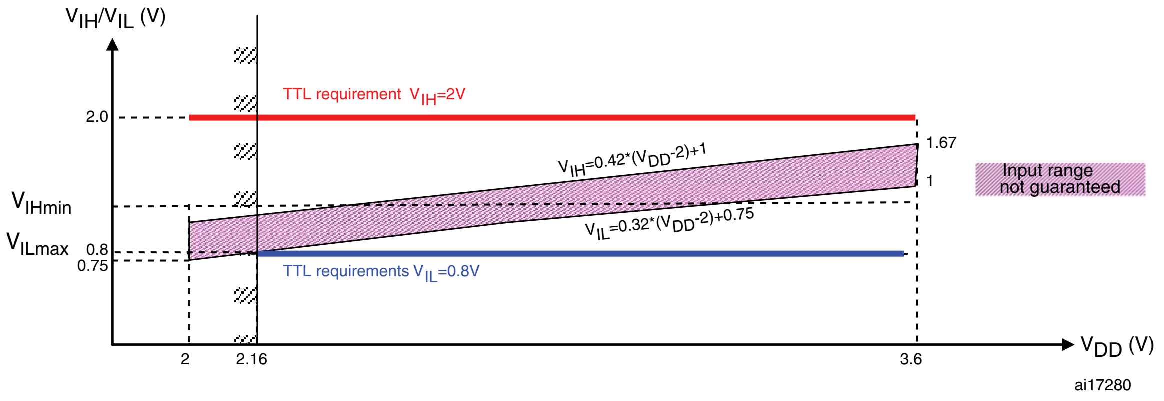


Figure 40. 5 V tolerant I/O input characteristics - TTL port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxedV_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ±3 mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 8*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 8*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*. All I/Os are CMOS and TTL compliant.

Table 48. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port(2), I_{IO} = +8 mA, 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +20 mA(4) 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–1.3	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +6 mA(4) 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 8* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 8* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results.

Figure 44. SPI timing diagram - slave mode and CPHA=0

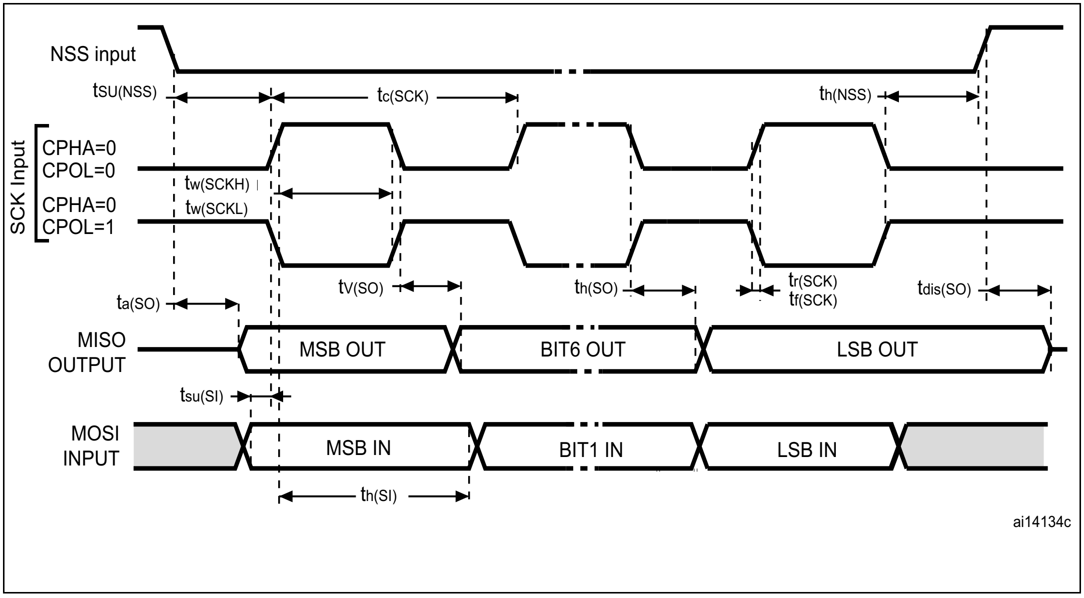
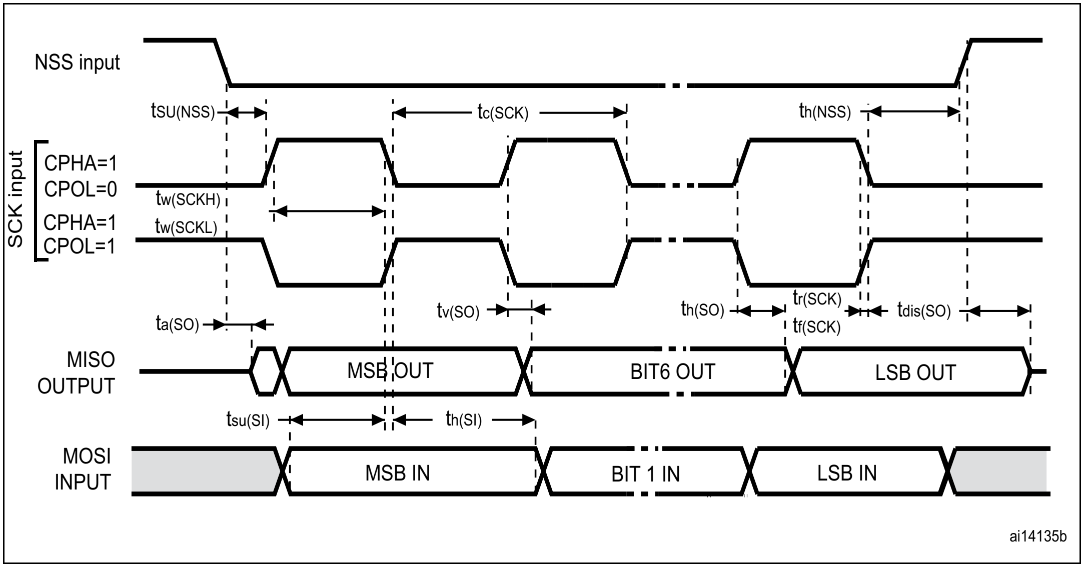


Figure 45. SPI timing diagram - slave mode and CPHA=1[1]



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 60. DAC characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max(1)	Unit	Comments
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON			0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x155) and (0xEAB) at V_{REF+} = 2.4 V.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON			-	-	V_{DDA} – 0.2	V	
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF			-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF			-	-	V_{REF+} – 1LSB	V	
$I_{DDVREF+}$	DAC DC current consumption in quiescent mode (Standby mode)			-	-	220	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs.
I_{DDA}	DAC DC current consumption in quiescent mode(3)			-	-	380	µA	With no load, middle code (0x800) on the inputs.
				-	-	480	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs.
DNL(1)	Differential non linearity Difference between two consecutive code-1LSB)			-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
				-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL(1)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)			-	-	±1	LSB	Given for the DAC in 10-bit configuration.
				-	-	±4	LSB	Given for the DAC in 12-bit configuration.
Offset(1)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)			-	-	±10	mV	-
				-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V.
				-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V.
Gain error(1)	Gain error			-	-	±0.5	%	Given for the DAC in 12bit configuration.

5.3.20 Temperature sensor characteristics

Table 61. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}(1)	Voltage at 25°C	1.34	1.43	1.52	V
t_{START}(2)	Startup time	4	-	10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

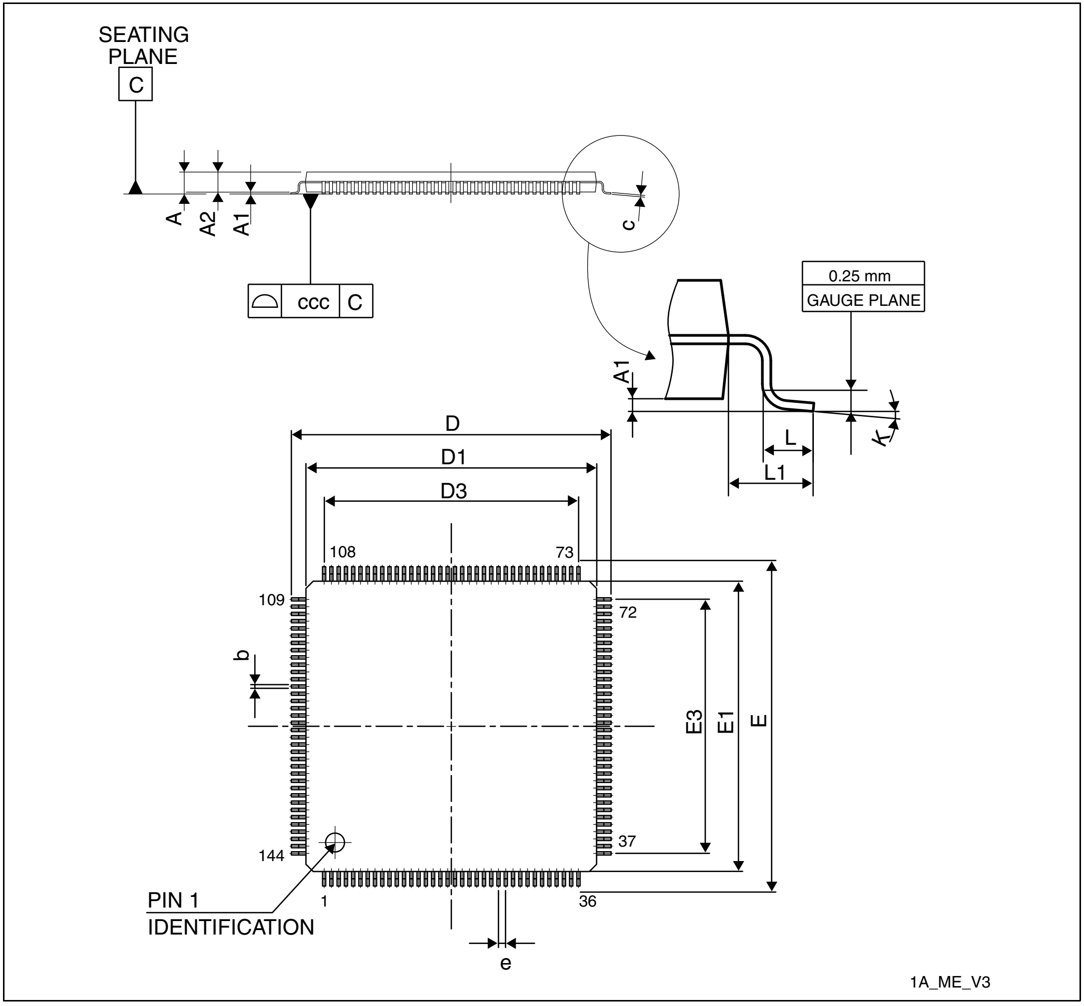
1. Preliminary values.
2. Guaranteed by design.
3. Shortest sampling time can be determined in the application by multiple iterations.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

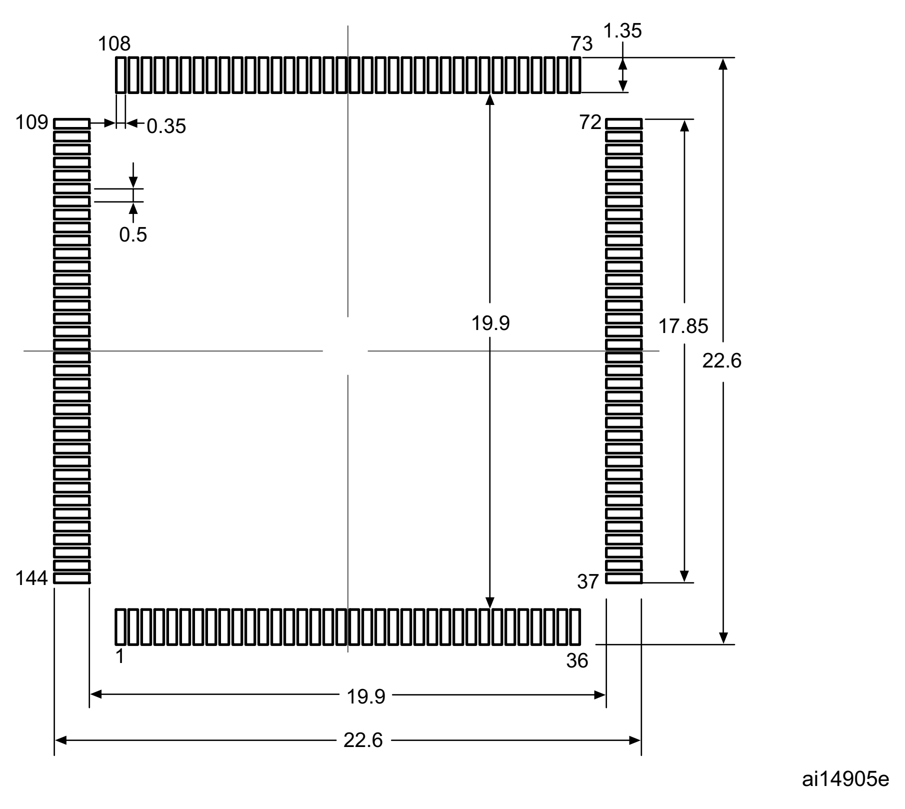
6.1 LQFP144 package information

Figure 52. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.

Figure 53. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package footprint



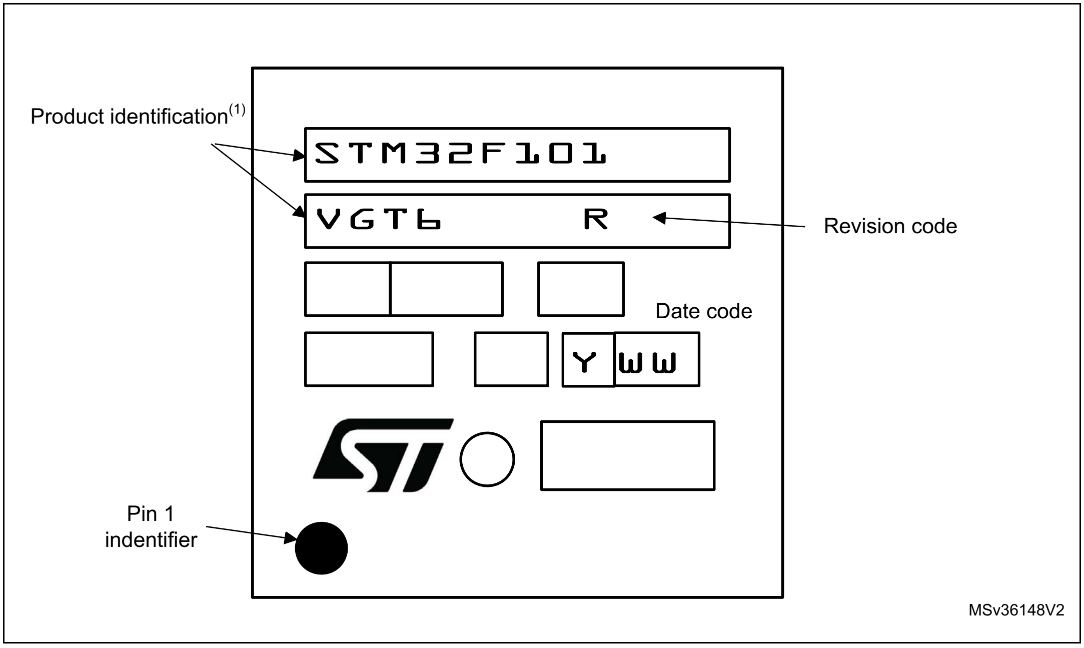
1. Dimensions are expressed in millimeters.

Device marking for LQFP100

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

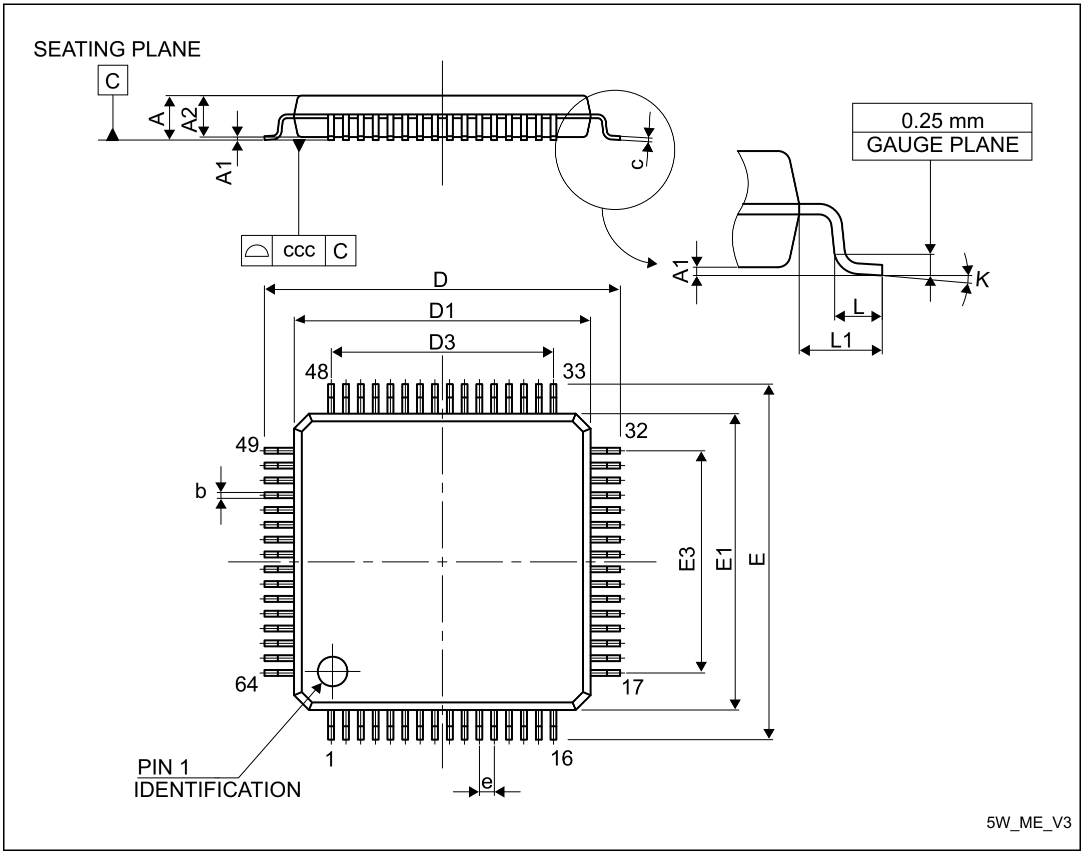
Figure 57. LQFP100 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.3 LQFP64 information

Figure 58. LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 64. LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-