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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	1MB (1M × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101vgt6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2 Description

The STM32F101xF and STM32F101xG access line family incorporates the highperformance ARM[®] Cortex[®]-M3 32-bit RISC core operating at a 36 MHz frequency, highspeed embedded memories (Flash memory up to 1 Mbyte and SRAM of 80 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer one 12-bit ADC, ten general-purpose 16-bit timers, as well as standard and advanced communication interfaces: up to two I²Cs, three SPIs and five USARTs.

The STM32F101xx XL-density access line family operates in the -40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

These features make the STM32F101xx XL-density access line microcontroller family suitable for a wide range of applications such as medical and handheld equipment, PC peripherals and gaming, GPS platforms, industrial applications, PLC, printers, scanners alarm systems, power meters, and video intercom.



2.3.17 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.18 Timers and watchdogs

The XL-density STM32F101xx access line devices include up to ten general-purpose timers, two basic timers, two watchdog timers and a SysTick timer.

Table 4: STM32F101xF and STM32F101xG timer feature comparison compares the features of the general-purpose and basic timers.

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9, TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No
TIM10, TIM11, TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Table 4. STM32F101xF and STM32F101xG timer feature comparison

General-purpose timers (TIMx)

There are 10 synchronizable general-purpose timers embedded in the STM32F101xF and STM32F101xG XL-density access line devices (see *Table 4* for differences).

• TIM2, TIM3, TIM4, TIM5

There are up to 4 synchronizable general-purpose timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F101xF and STM32F101xG access line devices.

These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or



4 Memory mapping

The memory map is shown in Figure 6.



Figure 6. Memory map

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Figure 11. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

Figure 12. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled





Symbol	Baramatar	Conditions	£	Max ⁽¹⁾	Unit
	Farameter	Conditions	HCLK	T _A = 85 °C	Unit
I _{DD}			36 MHz	27.5	
		External clock ⁽²⁾ all peripherals enabled	24 MHz	20	mA
			16 MHz	15	
	Supply current in		8 MHz	9	
	Sleep mode	External clock ⁽²⁾ , all peripherals disabled	36 MHz	6.9	
			24 MHz	5.9	
			16 MHz	5.4	
			8 MHz	4.7	

Table 16. Maximum current consumption in Sleep mode, code running from Flash or RAM

1. Guaranteed by characterization results, tested in production at V_{DD} max, f_{HCLK} max with peripherals enabled.

2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

				Typ ⁽¹⁾			
Symbol	Parameter	Conditions	V _{DD} / V _{BAT} = 2.0 V	V _{DD} / V _{BAT} = 2.4 V	V_{DD}/V_{BA} = 3.3 V	T _A = 85 °C	Unit
	Supply current	Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	34.5	35	379	
in Sto	in Stop mode	Regulator in Low-power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	24.5	25	365	
ייםסי	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	3	3.8	-	μA
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.8	3.6	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.9	2.1	5 ⁽²⁾	
I _{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.05	1.1	1.4	2 ⁽²⁾	

Table 17	Typical an	d maximum	current cor	nsumptions	in Stor	and Stan	dby modes
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1. Typical values are measured at T_A = 25 °C.

2. Guaranteed by characterization results.



Perip	oherals	μA/MHz
	DMA1	23.06
	DMA2	18.47
AHB (up to 36MHz)	FSMC	55.14
	CRC	2.08
	BusMatrix ⁽²⁾	11.67
	APB1-Bridge	8.61
	TIM2	37.22
	TIM3	36.39
	TIM4	35.56
	TIM5	33.61
	TIM6	7.78
	TIM7	7.78
	TIM12	19.17
	TIM13	12.22
	TIM14	13.33
	SPI2/I2S2 ⁽³⁾	8.33
APB1 (up to 18 MHz)	SPI3/I2S3 ⁽³⁾	8.33
	USART2	12.22
	USART3	12.22
	UART4	12.22
	UART5	12.22
	I2C1	10.28
	I2C2	10.28
	DAC ⁽⁴⁾	9.17
	WWDG	3.06
	PWR	2.50
	ВКР	2.78
	IWDG	4.44

Table 20. Peripheral current consumption⁽¹⁾





Figure 15. High-speed external clock source AC timing diagram







5.3.8 PLL characteristics

The parameters given in *Table 28* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Symbol	Poromotor	Value			Unit
Symbol	Farameter	Min ⁽¹⁾	Тур	Max ⁽¹⁾	Unit
f _{PLL_IN}	PLL input clock ⁽²⁾	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f _{PLL_OUT}	PLL multiplier output clock	16	-	36	MHz
t _{LOCK}	PLL lock time	-	-	200	μs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

	Table	28.	PLL	characteristics
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1. Guaranteed by characterization results.

2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by $f_{\mathsf{PLL}_\mathsf{OUT}}$.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at $T_A = -40$ to 85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max ⁽¹⁾	Unit
t _{prog}	16-bit programming time	$T_A = -40$ to +85 °C	40	52.5	70	μs
t _{ERASE}	Page (2 KB) erase time	$T_A = -40$ to +85 °C	20	-	40	ms
t _{ME}	Mass erase time	$T_A = -40$ to +85 °C	20	-	40	ms
		Read mode f _{HCLK} = 36 MHz with 1 wait state, V _{DD} = 3.3 V	-	-	28	mA
I _{DD}	Supply current	Write mode f_{HCLK} = 36 MHz, V _{DD} = 3.3 V	-	-	7	mA
		Erase mode f _{HCLK} = 36 MHz, V _{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V _{DD} = 3.0 to 3.6 V	-	-	50	μA
V _{prog}	Programming voltage	-	2	-	3.6	V

Table 29. Flash memory characteristics

1. Guaranteed by design.



Symbol	Parameter	Min	Max	Unit
t _{h(Data_NE)}	Data hold time after FSMC_NEx high	0	-	ns
t _{v(NADV_NE)}	FSMC_NEx low to FSMC_NADV low	-	0	ns
t _{w(NADV)}	FSMC_NADV low time	-	t _{HCLK} + 2	ns

Table 31. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings^{(1) (2)}

1. C_L = 15 pF.

2. Guaranteed by characterization results.

FSMC_NEx	
FSMC_NOE	
FSMC_NWE	-tv(NWE_NE) tw(NWE) th(NE_NWE)
FSMC_A[25:0]	<pre>tv(A_NE) th(A_NWE) Address</pre>
FSMC_NBL[1:0]	tv(BL_NE) th(BL_NWE) NBL
FSMC_D[15:0]	^t v(Data_NE)
FSMC_NADV ⁽¹⁾	tw(NADV) ►
	ai14990

Figure 20. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 32 As	unchronous non-multi	nloved SPAM/		write timings $(1)(2)$
Table 32. As	ynchronous non-multi	piexea SRAM/F	SKAW/NUK	write timings ⁽¹⁾⁽⁻⁾

	•		-	
Symbol	Parameter	Min	Max	Unit
t _{w(NE)}	FSMC_NE low time	3t _{HCLK} + 0.5	3t _{HCLK} + 1.5	ns
$t_{v(NWE_NE)}$	FSMC_NEx low to FSMC_NWE low	t _{HCLK} + 0.5	t _{HCLK} + 1.5	ns
t _{w(NWE)}	FSMC_NWE low time	t _{HCLK} – 0.5	t _{HCLK} + 1	ns
t _{h(NE_NWE)}	FSMC_NWE high to FSMC_NE high hold time	t _{HCLK} – 0.5	-	ns
t _{v(A_NE)}	FSMC_NEx low to FSMC_A valid	-	0	ns
t _{h(A_NWE)}	Address hold time after FSMC_NWE high	t _{HCLK}	-	ns
t _{v(BL_NE)}	FSMC_NEx low to FSMC_BL valid	-	1.5	ns
t _{h(BL_NWE)}	FSMC_BL hold time after FSMC_NWE high	t _{HCLK} – 1.5	-	ns
t _{v(Data_NE)}	FSMC_NEx low to Data valid	-	t _{HCLK}	ns



2. Guaranteed by characterization results.



Figure 26. Synchronous non-multiplexed PSRAM write timings

Table 38. Synchronous non-multiplexed PSRAM write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
t _{w(CLK)}	FSMC_CLK period	27.6	-	ns
t _{d(CLKL-NExL)}	FSMC_CLK low to FSMC_NEx low (x = 02)	-	0.5	ns
t _{d(CLKL-NExH)}	FSMC_CLK low to FSMC_NEx high (x = 02)	1.5	-	ns
t _{d(CLKL-NADVL)}	FSMC_CLK low to FSMC_NADV low	-	1	ns
t _{d(CLKL-NADVH)}	FSMC_CLK low to FSMC_NADV high	0.5	-	ns
t _{d(CLKL-AV)}	FSMC_CLK low to FSMC_Ax valid (x = 1625)	-	0	ns
t _{d(CLKL-AIV)}	FSMC_CLK low to FSMC_Ax invalid (x = 1625)	1.5	-	ns
t _{d(CLKL-NWEL)}	FSMC_CLK low to FSMC_NWE low	-	1	ns
t _{d(CLKL-NWEH)}	FSMC_CLK low to FSMC_NWE high	1.5	-	ns
t _{d(CLKL-Data)}	FSMC_D[15:0] valid data after FSMC_CLK low	-	2.5	ns
t _{d(CLKL-NBLH)}	FSMC_CLK low to FSMC_NBL high	0.5	-	ns





Figure 36. NAND controller waveforms for common memory write access

Table 41. Switching characteristics for NAND Flash write cycles⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t _{w(NWE)}	FSMC_NWE low width	3t _{HCLK}	3t _{HCLK}	ns
t _{v(NWE-D)}	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
t _{h(NWE-D)}	FSMC_NWE high to FSMC_D[15:0] invalid	2t _{HCLK} + 2	-	ns
t _{d(ALE-NWE)}	FSMC_ALE valid before FSMC_NWE low	-	3t _{HCLK} + 1.5	ns
t _{h(NWE-ALE)}	FSMC_NWE high to FSMC_ALE invalid	3t _{HCLK} + 8	-	ns
t _{d(ALE-NOE)}	FSMC_ALE valid before FSMC_NOE low	-	2t _{HCLK}	ns
t _{h(NOE-ALE)}	FSMC_NWE high to FSMC_ALE invalid	2t _{HCLK}	_	ns

1. C_L = 15 pF.

5.3.11 **EMC** characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.





Figure 46. SPI timing diagram - master mode⁽¹⁾

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.18 **12-bit ADC characteristics**

Unless otherwise specified, the parameters given in Table 56 are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in Table 10.

Note: It is recommended to perform a calibration after each power-up.





Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V _{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF^+}	Positive reference voltage	-	2.4	-	V _{DDA}	V
V _{REF-}	Negative reference voltage	-	-	0	-	V
I _{VREF}	Current on the V _{REF} input pin	-	-	160	220 ⁽¹⁾	μA
f _{ADC}	ADC clock frequency	-	0.6	-	14	MHz
$f_{S}^{(2)}$	Sampling rate	-	0.05	-	1	MHz
£ (2)	Extornal trigger frequency	f _{ADC} = 14 MHz	-	-	823	kHz
ITRIG ⁽⁼⁾	External trigger frequency	-	-	-	17	1/f _{ADC}
V _{AIN}	Conversion voltage range ⁽³⁾	-	0 (V _{SSA} or V _{REF-} tied to ground)	-	V _{REF+}	V
R _{AIN} ⁽²⁾	External input impedance	See Equation 1 and Table 57 for details	-	-	50	kΩ
$R_{ADC}^{(2)}$	Sampling switch resistance	-	-	-	1	kΩ
$C_{ADC}^{(2)}$	Internal sample and hold capacitor	-	-	I	8	pF
t (2)	Calibration time	f _{ADC} = 14 MHz	5.9			μs
'CAL		-	83			1/f _{ADC}
t. (2)	Injection trigger conversion	f _{ADC} = 14 MHz	-	-	0.214	μs
Yat	latency	-	-	-	3 ⁽⁴⁾	1/f _{ADC}
t. (2)	Regular trigger conversion	f _{ADC} = 14 MHz	-	-	0.143	μs
latr'-'	latency	-	-	-	2 ⁽⁴⁾	1/f _{ADC}
t _S ⁽²⁾	Sampling time	f _{ADC} = 14 MHz	0.107	-	17.1	μs
		-	1.5	-	239.5	1/f _{ADC}
t _{STAB} ⁽²⁾	Power-up time	-	0	0	1	μs
	Total conversion time	f _{ADC} = 14 MHz	1	-	18	μs
t _{CONV} ⁽²⁾	(including sampling time)	-	14 to 252 (t _S for sampling +12.5 for successive approximation)			1/f _{ADC}

 Table 56. ADC characteristics

1. Guaranteed by characterization results.

- 2. Guaranteed by design.
- V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to Section 3: Pinouts and pin descriptions for further details.
- 4. For external triggers, a delay of 1/f_{PCLK2} must be added to the latency specified in *Table 56*.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{I_{S}}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$





Figure 48. Typical connection diagram using the ADC

Refer to Table 56 for the values of RAIN, RADC and CADC. 1.

 $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced. 2.

General PCB design guidelines

Power supply decoupling should be performed as shown in Figure 49 or Figure 50, depending on whether $V_{\text{REF+}}$ is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.





1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.



STM32F101xF, STM32F101xG

Symbol	Parameter	Cond	itions	Min	Тур	Max ⁽¹⁾	Unit	Comments
tsettling	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB			-	3	4	μs	C _{LOAD} ≤50 pF, R _{LOAD} ≥ 5 kΩ
Update rate ⁽¹⁾	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)			-	-	1	MS/s	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ
t _{wakeup} (1)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)			-	6.5	10	μs	$C_{LOAD} \le 50 \text{ pF}, R_{LOAD} \ge 5 \text{ k}\Omega$ input code between lowest and highest possible ones.
PSRR+ ⁽²⁾	Power supply rejection ratio (to V _{DDA}) (static DC measurement			-	-67	-40	dB	No R _{LOAD} , C _{LOAD} = 50 pF

Table 60. DAC characteristics (continued)

1. Preliminary values.

2. Guaranteed by design.

3. Quiescent mode refers to the state of the DAC when a steady value is kept on the output so that no dynamic consumption is involved.



Figure 51. 12-bit buffered /non-buffered DAC

1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.



Symbol		millimeters		inches ⁽¹⁾		
Symbol	Min	Тур	Мах	Min	Тур	Мах
А	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
С	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.874
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.874
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-		0.689	
е	-	0.500	-		0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-		0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
CCC	-	-	0.080	-	-	0.0031

Table 62. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat packagemechanical data

1. Values in inches are converted from mm and rounded to 4 decimal digits.



publicage mechanical data (continued)							
Symbol	millimeters			inches ⁽¹⁾			
	Min	Тур	Мах	Min	Тур	Мах	
E3	-	12.000	-	-	0.4724	-	
е	-	0.500	-	-	0.0197	-	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295	
L1	-	1.000	-	-	0.0394	-	
k	0°	3.5°	7°	0°	3.5°	7°	
ccc	-	-	0.080	-	-	0.0031	

Table 63. LQPF100 – 14 x 14 mm, 100-pin low-profile quad flat package mechanical data (continued)

1. Values in inches are converted from mm and rounded to 4 decimal digits.





1. Dimensions are in millimeters.



Device marking for LQFP64

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.





 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



8 Revision history

Date	Revision	Changes
27-Oct-2009	1	Initial release.
15-Nov-2010	2	LQFP64 package mechanical data updated: see <i>Figure 58</i> : LQ <i>FP64</i> – 10 x 10 mm, 64 pin low-profile quad flat package outline and Table 64: LQ <i>FP64</i> – 10 x 10 mm, 64 pin low-profile quad flat package mechanical data. Internal code removed from <i>Table 66</i> : STM32 <i>F</i> 101 <i>xF</i> and STM32 <i>F</i> 101 <i>xG</i> ordering information scheme. Updated note 2 below <i>Table 52</i> : <i>I</i> ² C characteristics Updated Figure 43: <i>I</i> ² C bus AC waveforms and measurement circuit ⁽¹⁾ Updated <i>Figure 42</i> : Recommended NRST pin protection Updated note 1 below <i>Table 47</i> : <i>I/O</i> static characteristics Updated <i>Table 20</i> : Peripheral current consumption Updated <i>Table 20</i> : Peripheral current consumption in Run mode, code with data processing running from <i>Flash</i> Updated <i>Table 15</i> : Maximum current consumption in Sleep mode, code with data processing running from <i>RAM</i> Updated <i>Table 16</i> : Maximum current consumption in Sleep mode, code running from <i>Flash</i> or <i>RAM</i> Updated <i>Table 17</i> : Typical and maximum current consumptions in Stop and Standby modes Updated <i>Table 18</i> : Typical current consumption in Run mode, code with data processing running from <i>Flash</i> Updated <i>Table 19</i> : <i>Typical current consumption in Sleep mode, code</i> <i>running from Flash</i> or <i>RAM</i> Updated <i>Table 18</i> : Typical current consumption in Sleep mode, code running from <i>Flash</i> or <i>RAM</i> Updated <i>Table 19</i> : <i>Typical current consumption in Sleep mode, code</i> <i>running from Flash</i> or <i>RAM</i> Updated <i>Table 19</i> : <i>Typical current consumption in Sleep mode, code</i> <i>running from Flash</i> or <i>RAM</i> Updated <i>Table 24</i> : <i>LSE</i> oscillator characteristics (<i>f</i> _{LSE} = 32.768 kHz) Updated <i>Figure 19</i> : <i>Asynchronous non-multiplexed</i> <i>SRAM/PSRAM/NOR read</i> waveforms on page 58 Added Section 5.3.13: <i>I/O</i> current injection characteristics on page 99.

Table 67. Document revision history



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