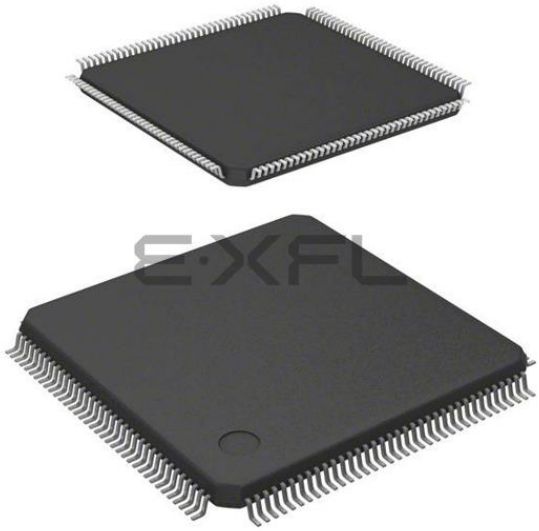

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	112
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101zft6

2.3 Overview

2.3.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM® Cortex®-M3 processor is the latest generation of ARM® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM® core in the memory size usually associated with 8- and 16-bit devices.

The STM32F101xF and STM32F101xG access line family having an embedded ARM® core, is therefore compatible with all ARM® tools and software.

Figure 1 shows the general block diagram of the device family.

2.3.2 Memory protection unit

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.3.3 Embedded Flash memory

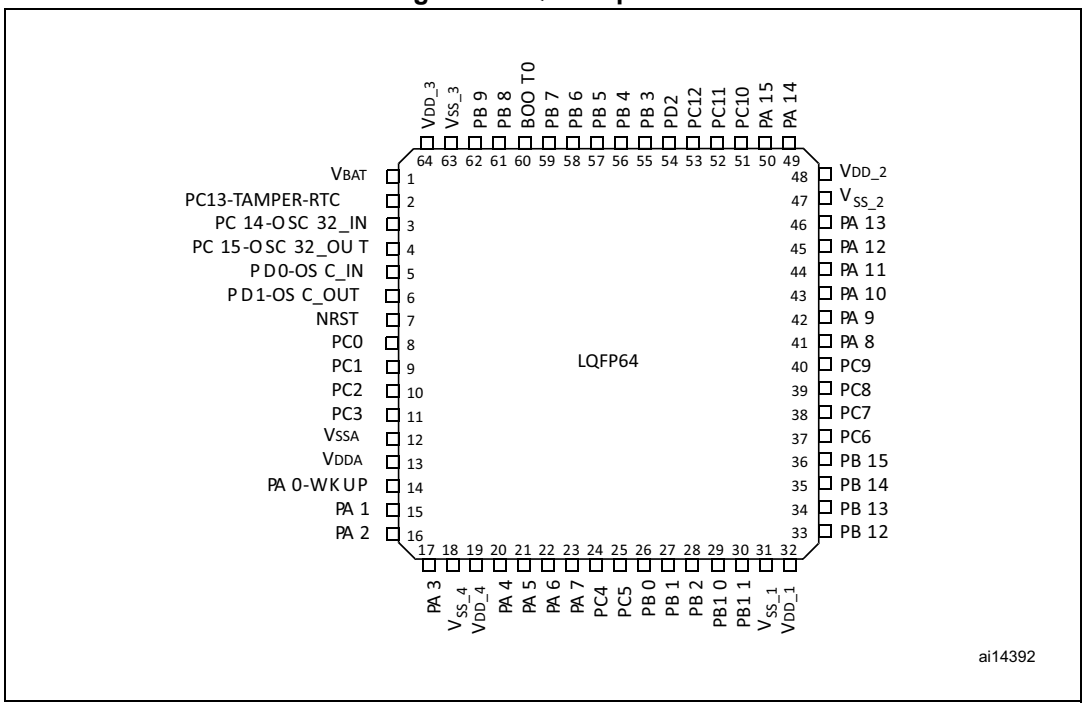
768 Kbytes to 1 Mbyte of embedded Flash are available for storing programs and data. The Flash memory is organized as two banks. The first bank has a size of 512 Kbytes. The second bank is either 256 or 512 Kbytes depending on the device. This gives the device the capability of writing to one bank while executing code from the other bank (read-while-write capability).

2.3.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

Figure 5. LQFP64 pinout



1. The above figure shows the package top view.

Table 5. STM32F101xF/STM32F101xG pin definitions

Pins			Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
1	-	1	PE2	I/O	FT	PE2	TRACECLK / FSMC_A23	-
2	-	2	PE3	I/O	FT	PE3	TRACED0 / FSMC_A19	-
3	-	3	PE4	I/O	FT	PE4	TRACED1 / FSMC_A20	-
4	-	4	PE5	I/O	FT	PE5	TRACED2 / FSMC_A21	TIM9_CH1
5	-	5	PE6	I/O	FT	PE6	TRACED3 / FSMC_A22	TIM9_CH2
6	1	6	V_{BAT}	S	-	V_{BAT}	-	-
7	2	7	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
8	3	8	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
9	4	9	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
10	-	-	PF0	I/O	FT	PF0	FSMC_A0	-
11	-	-	PF1	I/O	FT	PF1	FSMC_A1	-

Table 5. STM32F101xF/STM32F101xG pin definitions (continued)

Pins			Pin name	Type[1]	I / O level[2]	Main function[3] (after reset)	Alternate functions[4]	
LQFP144	LQFP64	LQFP100					Default	Remap
88	-	-	PG3	I/O	FT	PG3	FSMC_A13	-
89	-	-	PG4	I/O	FT	PG4	FSMC_A14	-
90	-	-	PG5	I/O	FT	PG5	FSMC_A15	-
91	-	-	PG6	I/O	FT	PG6	FSMC_INT2	-
92	-	-	PG7	I/O	FT	PG7	FSMC_INT3	-
93	-	-	PG8	I/O	FT	PG8	-	-
94	-	-	V_{SS_9}	S	-	V_{SS_9}	-	-
95	-	-	V_{DD_9}	S	-	V_{DD_9}	-	-
96	37	63	PC6	I/O	FT	PC6	-	TIM3_CH1
97	38	64	PC7	I/O	FT	PC7	-	TIM3_CH2
98	39	65	PC8	I/O	FT	PC8	-	TIM3_CH3
99	40	66	PC9	I/O	FT	PC9	-	TIM3_CH4
100	41	67	PA8	I/O	FT	PA8	USART1_CK / MCO	-
101	42	68	PA9	I/O	FT	PA9	USART1_TX[8]	-
102	43	69	PA10	I/O	FT	PA10	USART1_RX[8]	-
103	44	70	PA11	I/O	FT	PA11	USART1_CTS	-
104	45	71	PA12	I/O	FT	PA12	USART1_RTS	-
105	46	72	PA13	I/O	FT	JTMS-SWDIO	-	PA13
106	-	73	Not connected					
107	47	74	V_{SS_2}	S	-	V_{SS_2}	-	-
108	48	75	V_{DD_2}	S	-	V_{DD_2}	-	-
109	49	76	PA14	I/O	FT	JTCK-SWCLK	-	PA14
110	50	77	PA15	I/O	FT	JTDI	SPI3_NSS	TIM2_CH1_ETR/ PA15 /SPI1_NSS
111	51	78	PC10	I/O	FT	PC10	UART4_TX	USART3_TX
112	52	79	PC11	I/O	FT	PC11	UART4_RX	USART3_RX
113	53	80	PC12	I/O	FT	PC12	UART5_TX	USART3_CK
114	-	81	PD0	I/O	FT	-	FSMC_D2[9]	-
115	-	82	PD1	I/O	FT	-	FSMC_D3[9]	-

Figure 13. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values

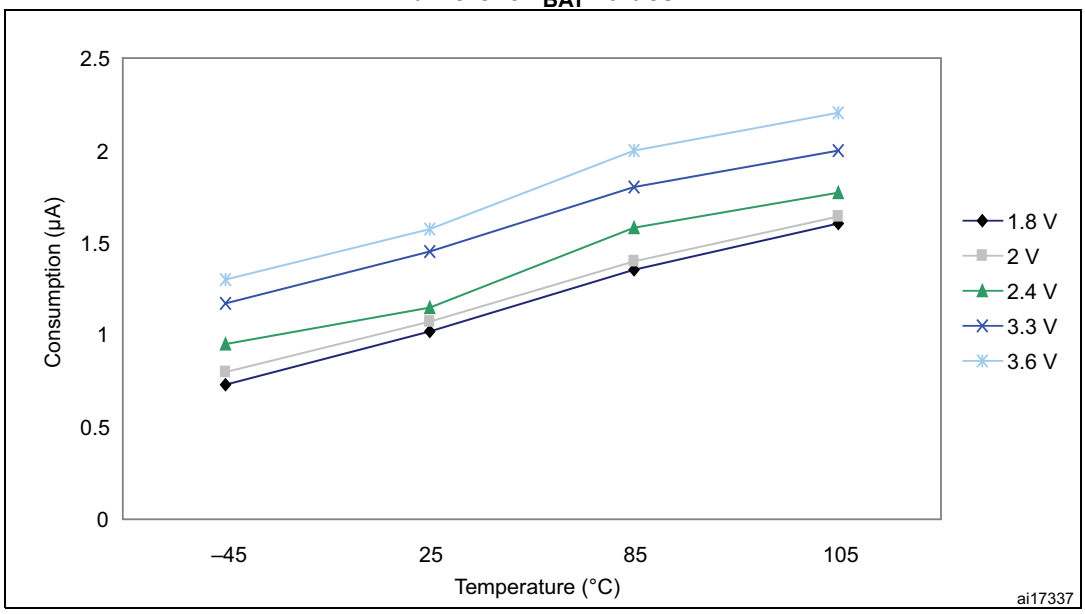
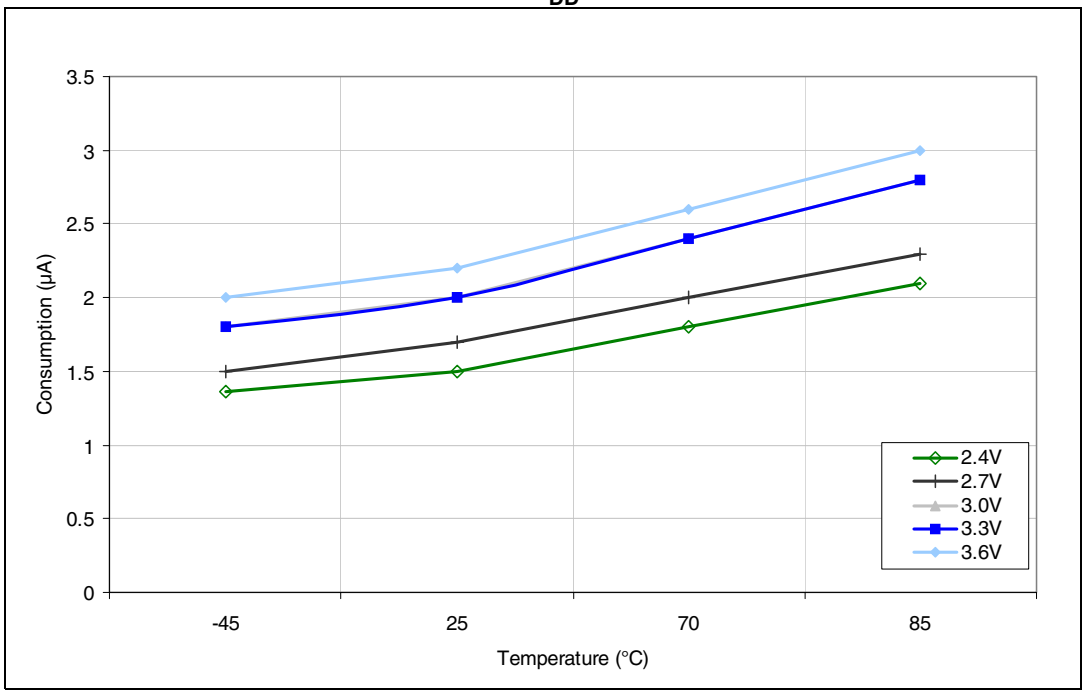


Figure 14. Typical current consumption in Standby mode versus temperature at different V_{DD} values



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 23. HSE 4-16 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Table 33. Asynchronous multiplexed NOR/PSRAM read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	t_{HCLK} -2	-	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0.5	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$4t_{HCLK}$ - 0.5	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	$4t_{HCLK}$ - 1	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

Figure 24. Synchronous multiplexed PSRAM write timings

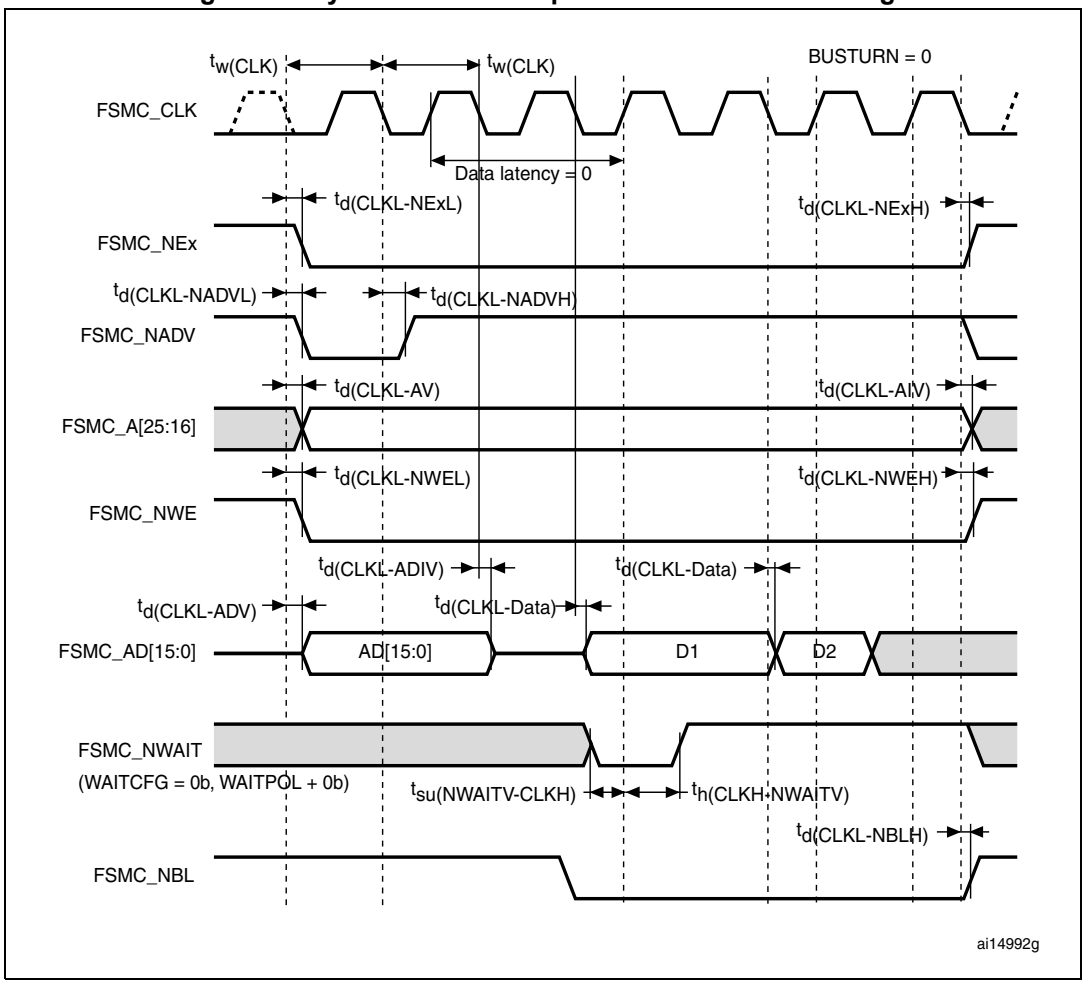


Figure 25. Synchronous non-multiplexed NOR/PSRAM read timings

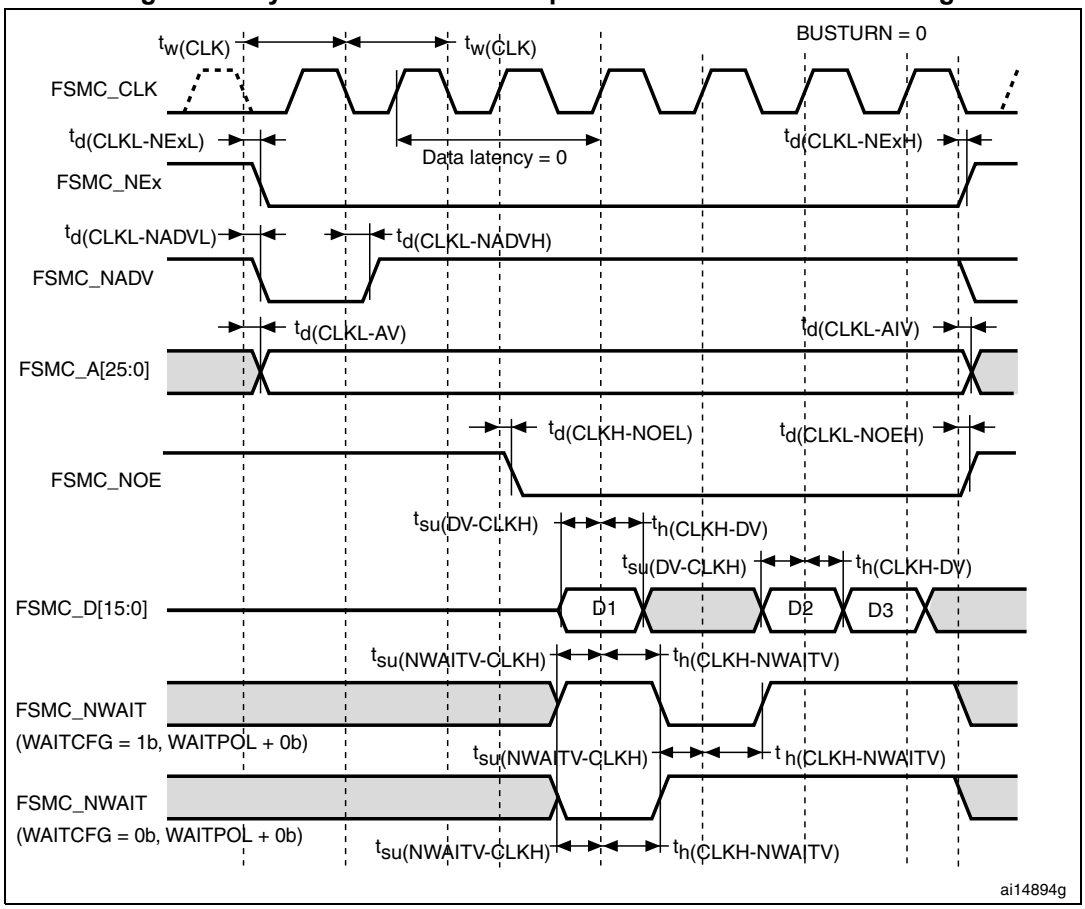


Table 37. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.6	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	1.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	0.5	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	1	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 0...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 0...25)	2	-	ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	t_{HCLK} + 1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	3.5	-	ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	0	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_SMCLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. C_L = 15 pF.

Table 38. Synchronous non-multiplexed PSRAM write timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results.

PC Card/CompactFlash controller waveforms and timings

Figure 27 through *Figure 32* represent synchronous waveforms and *Table 40* and *Table 41* provide the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x04;
- COM.FSMC_WaitSetupTime = 0x07;
- COM.FSMC_HoldSetupTime = 0x04;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x04;
- ATT.FSMC_WaitSetupTime = 0x07;
- ATT.FSMC_HoldSetupTime = 0x04;
- ATT.FSMC_HiZSetupTime = 0x00;
- IO.FSMC_SetupTime = 0x04;
- IO.FSMC_WaitSetupTime = 0x07;
- IO.FSMC_HoldSetupTime = 0x04;
- IO.FSMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

The test results are given in *Table 42*. They are based on the EMS levels and classes defined in application note AN1709.

Table 42. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK}= 36 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 36 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 43. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/36 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP144 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	8	dBµV
			30 MHz to 130 MHz	27	
			130 MHz to 1 GHz	26	
			SAE EMI Level	4	-

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 41* and *Table 49*, respectively.

Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 49. I/O AC characteristics(1)

MODEx [1:0] bit value(1)	Symbol	Parameter	Conditions	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		25(3)	
11	$F_{max(IO)out}$	Maximum Frequency(2)	C_L= 30 pF, V_{DD} = 2.7 V to 3.6 V	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 41*.
3. Guaranteed by design.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 54Table 55* are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 10*.
Refer to *Section 5.3.13: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 54. STM32F10xxx SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	10	MHz
		Slave mode	-	10	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	73	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode - SPI1	3	-	
		Master mode - SPI2	5	-	
		Slave mode	4	-	
$t_{h(MI)}$ (1)	Data input hold time	Master mode - SPI1	4	-	
		Master mode - SPI2	6	-	
$t_{h(SI)}$ (1)		Slave mode	5	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 36 MHz, presc = 4	0	55	
		Slave mode, f_{PCLK} = 20 MHz	-	$4t_{PCLK}$	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	10	-	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	25	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	6	-	

1. Guaranteed by characterization results.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Table 56. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	-	0	-	V
I_{VREF}	Current on the V_{REF} input pin	-	-	160	220(1)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 57* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Guaranteed by characterization results.
2. Guaranteed by design.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 3: Pinouts and pin descriptions* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 56*.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

Table 59. ADC accuracy(1) (2)(3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK2} = 28 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency, V_{REF} and temperature ranges.
3. ADC accuracy vs. negative injection current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.13* does not affect the ADC accuracy.
4. Preliminary values.

Figure 47. ADC accuracy characteristics

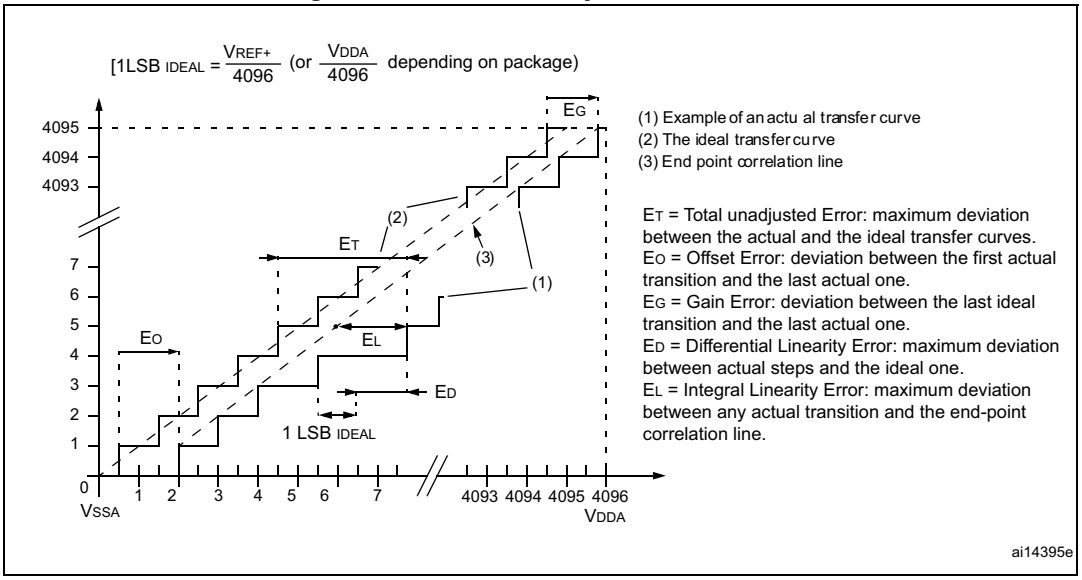


Table 62. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.874
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.874
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-		0.689	
e	-	0.500	-		0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-		0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.4 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 10: General operating conditions on page 39*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 65. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP144 - 20 x 20 mm / 0.5 mm pitch	30	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	45	

6.4.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air), available from www.jedec.org.

7 Part numbering

Table 66. STM32F101xF and STM32F101xG ordering information scheme

Example: STM32F 101 R F T 6 xxx

Device family

STM32 = ARM®-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

101 = access line

Pin count

R = 64 pins

V = 100 pins

Z = 144 pins

Flash memory size

F = 768 Kbytes of Flash memory

G = 1 Mbyte of Flash memory

Package

T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

Options

xxx = programmed parts

TR = tape and real

For a list of available options (speed, package, etc..) or for further information on any aspect of this device, please contact your nearest ST sales office.

8 Revision history

Table 67. Document revision history

Date	Revision	Changes
27-Oct-2009	1	Initial release.
15-Nov-2010	2	LQFP64 package mechanical data updated: see *Figure 58: LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package outline* and *Table 64: LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package mechanical data*. Internal code removed from *Table 66: STM32F101xF and STM32F101xG ordering information scheme*. Updated note 2 below *Table 52: I^2C characteristics* Updated *Figure 43: I^2C bus AC waveforms and measurement circuit*(1) Updated *Figure 42: Recommended NRST pin protection* Updated note 1 below *Table 47: I/O static characteristics* Updated *Table 20: Peripheral current consumption* Updated *Table 14: Maximum current consumption in Run mode, code with data processing running from Flash* Updated *Table 15: Maximum current consumption in Run mode, code with data processing running from RAM* Updated *Table 16: Maximum current consumption in Sleep mode, code running from Flash or RAM* Updated *Table 17: Typical and maximum current consumptions in Stop and Standby modes* Updated *Table 18: Typical current consumption in Run mode, code with data processing running from Flash* Updated *Table 19: Typical current consumption in Sleep mode, code running from Flash or RAM* Updated *Table 24: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)* Updated *Figure 19: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms on page 58* Added *Section 5.3.13: I/O current injection characteristics on page 99.*

Table 67. Document revision history (continued)

Date	Revision	Changes
25-Nov-2014	3	Updated number of ADCs in *Table 2: STM32F101xF and STM32F101xG features and peripheral counts*. Modified *Section 2.3.22: GPIOs (general-purpose inputs/outputs) on page 21*. Added note below *Figure 3: LQFP144 pinout*, *Figure 4: LQFP100 pinout*, and *Figure 5: LQFP64 pinout*. Modified OSC_IN, OSC_OUT, PD0, PD1, PB8, PB9 and PF8 in *Table 5: STM32F101xF/STM32F101xG pin definitions on page 25*/ Updated notes related to parameters not tested in production in the whole document. Modified notes in *Table 7: Voltage characteristics on page 37* and *Table 8: Current characteristics on page 38*. Removed ADC2/3 and CAN from *Table 20: Peripheral current consumption on page 48*. Modified $t_{w(HSE)}$ value in *Table 21: High-speed external user clock characteristics on page 50*. Updated *Table 24: LSE oscillator characteristics (f_{LSE} = 32.768 kHz) on page 53*. Changed JESD22-C101 to ANSI/ESD STM5.3.1 in *Section : Electrostatic discharge (ESD)*. Updated *Section 5.3.10: FSMC characteristics on page 57*. Updated *Figure 41: I/O AC characteristics definition*. Updated conditions related to *Section : I^2C interface characteristics on page 87*. Modified *Table 52: I^2C characteristics on page 87*, updated *Figure 43: I^2C bus AC waveforms and measurement circuit(1)* and V_{DD}/V_{DD_I2C} conditions in *Table 53: SCL frequency (f_{PCLK1}= 36 MHz, V_{DD} = V_{DD_I2C} = 3.3 V) on page 88*. Modified *Section : Output driving current on page 82*. Modified *Table 52: I^2C characteristics on page 87* and updated *Figure 43: I^2C bus AC waveforms and measurement circuit(1)*. Modified *Figure 46: SPI timing diagram - master mode(1) on page 92*. Modified notes in *Table 56: ADC characteristics on page 93* and *Table 59: ADC accuracy on page 95*. Updated I_{DDA} definition in *Table 60: DAC characteristics on page 97* and removed comment related to the offset parameter for ±10 mV. Added Device marking information for all packages.