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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	CPU12
Core Size	16-Bit
Speed	8MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc912dg128acpve

1.3 Devices Covered in this Document

The MC68HC912DG128A device is similar to the MC68HC912DT128A, but it has only two MSCAN12 modules. The entire databook applies to both devices, except where differences are noted.

The MC68HC912DT128C and MC68HC912DT128P are devices similar to the MC68HC912DT128A, but with different oscillator configurations. Sections of this book applicable to the MC68HC912DT128A also apply to the MC68HC912DT128C and MC68HC912DT128P, except for the differences highlighted in Section 13. Oscillator.

The MC68HC912DG128C and MC68HC912DG128P are devices similar to the MC68HC912DG128A, but with different oscillator configurations. Sections of this book applicable to the MC68HC912DG128A also apply to the MC68HC912DG128C and MC68HC912DG128P, except for the differences highlighted in Section 13. Oscillator.

NOTE: *The generic term MC68HC912DT128A is used throughout the document to mean all derivatives mentioned above, except in Section 13. Oscillator, where it refers only to the MC68HC912DT128A and MC68HC912DG128A devices.*

1.4 Features

- 16-bit CPU12
  - Upward compatible with M68HC11 instruction set
  - Interrupt stacking and programmer's model identical to M68HC11
  - 20-bit ALU
  - Instruction queue
  - Enhanced indexed addressing
- Multiplexed bus
  - Single chip or expanded
  - 16 address/16 data wide or 16 address/8 data narrow modes

Table 3-2. MC68HC912DT128A Signal Description Summary

Pin Name	Shared port	Pin Number 112-pin	Description
IRQ	PE1	55	Maskable interrupt request input provides a means of applying asynchronous interrupt requests to the MCU. Either falling edge-sensitive triggering or level-sensitive triggering is program selectable (INTCR register).
XIRQ	PE0	56	Provides a means of requesting asynchronous nonmaskable interrupt requests after reset initialization
SMODN/ BKGD/ $\overline{\text{TAGHI}}$	-	23	During reset, this pin determines special or normal operating mode. After reset, single-wire background interface pin is dedicated to the background debug function. Pin function $\overline{\text{TAGHI}}$ used in instruction tagging. See Development Support.
IX[2:0]	PK[2:0]	109-111	Page Index register emulation outputs.
ECS	PK7	108	Emulation Chip select.
PW[3:0]	PP[3:0]	112, 1–3	Pulse Width Modulator channel outputs.
SS	PS7	96	Slave select output for SPI master mode, input for slave mode or master mode.
SCK	PS6	95	Serial clock for SPI system.
SDO/MOSI	PS5	94	Master out/slave in pin for serial peripheral interface
SDI/MISO	PS4	93	Master in/slave out pin for serial peripheral interface
TxD1	PS3	92	SCI1 transmit pin
RxD1	PS2	91	SCI1 receive pin
TxD0	PS1	90	SCI0 transmit pin
RxD0	PS0	89	SCI0 receive pin
IOC[7:0]	PT[7:0]	18–15, 7–4	Pins used for input capture and output compare in the timer and pulse accumulator subsystem.
AN1[7:0]	PAD1[7:0]	84/82/80/ 78/76/74/ 72/70	Analog inputs for the analog-to-digital conversion module 1
AN0[7:0]	PAD0[7:0]	83/81/79/ 77/75/73/ 71/69	Analog inputs for the analog-to-digital conversion module 0
TEST	-	97	Used for factory test purposes. Do not connect in the application; may be bonded to 5.5 V max.
TxCAN2(1)	-	100	MSCAN2 transmit pin (MC68HC912DT128A only). Leave unconnected if MSCAN2 is not used.
RxCAN2(1)	-	101	MSCAN2 receive pin (MC68HC912DT128A only). Pin has internal pull-up; where msCAN module is not used, do not tie to VSS.
TxCAN1	-	102	MSCAN1 transmit pin. Leave unconnected if MSCAN1 is not used.
RxCAN1	-	103	MSCAN1 receive pin. Pin has internal pull-up; where msCAN module is not used, do not tie to VSS.
TxCAN0	-	104	MSCAN0 transmit pin. Leave unconnected if MSCAN0 is not used.
RxCAN0	-	105	MSCAN0 receive pin. Pin has internal pull-up; where msCAN module is not used, do not tie to VSS.
SCL	PIB7	98	I^2C bus serial clock line pin

while the MCU is in special peripheral mode as internal bus conflicts between BDM and the external master can cause improper operation of both functions.

	Bit 7	6	5	4	3	2	1	Bit 0	
	SMODN	MODB	MODA	ESTR	IVIS	EBSWAI	EMK	EME	
RESET:	0	0	0	1	1	0	1	1	Special Single Chip
RESET:	0	0	1	1	1	0	1	1	Special Exp Nar
RESET:	0	1	0	1	1	0	1	1	Peripheral
RESET:	0	1	1	1	1	0	1	1	Special Exp Wide
RESET:	1	0	0	1	0	0	0	0	Normal Single Chip
RESET:	1	0	1	1	0	0	0	0	Normal Exp Nar
RESET:	1	1	1	1	0	0	0	0	Normal Exp Wide

MODE — Mode Register **$000B**

The MODE register controls the MCU operating mode and various configuration options. This register is not in the map in peripheral mode

SMODN, MODB, MODA — Mode Select Special, B and A

These bits show the current operating mode and reflect the status of the BKGD, MODB and MODA input pins at the rising edge of reset.

Read anytime.

SMODN may only be written if SMODN = 0 (in special modes) but the first write is ignored.

MODB, MODA may be written once if SMODN = 1; anytime if SMODN = 0 but the first write is ignored and in special peripheral and reserved modes cannot be selected.

NDRF — Narrow Data Bus for Register-Following Map Space

This bit enables a narrow bus feature for the 1K byte Register-Following Map. This is useful for accessing 8-bit peripherals and allows 8-bit and 16-bit external memory devices to be mixed in a system. In Expanded Narrow (eight bit) modes, Single Chip Modes, and Peripheral mode, this bit has no effect.

0 = Makes Register-Following MAP space act as a full 16 bit data bus.

1 = Makes the Register-Following MAP space act the same as an 8 bit only external data bus (data only goes through port A externally).

The Register-Following space is mapped from $0400 to $07FF after reset, which is next to the register map. If the registers are moved this space follows.

RFSTR1, RFSTR0 — Register Following Stretch

This two bit field determines the amount of clock stretch on accesses to the 1K byte Register Following Map. It is valid regardless of the state of the NDRF bit. In Single Chip and Peripheral Modes this bit has no meaning or effect.

Table 6-5. RFSTR Stretch Bit Definition

RFSTR1	RFSTR0	Number of E Clocks Stretched
0	0	0
0	1	1
1	0	2
1	1	3

EXSTR1, EXSTR0 — External Access Stretch

This two bit field determines the amount of clock stretch on accesses to an external address space. In Single Chip and Peripheral Modes this bit has no meaning or effect.

Section 9. EEPROM Memory

9.1 Contents

9.2 Introduction

The MC68HC912DT128A EEPROM nonvolatile memory is arranged in a 16-bit configuration. The EEPROM array may be read as either bytes, aligned words or misaligned words. Access times are one bus cycle for byte and aligned word access and two bus cycles for misaligned word operations.

Programming is by byte or aligned word. Attempts to program or erase misaligned words will fail. Only the lower byte will be latched and programmed or erased. Programming and erasing of the user EEPROM can be done in normal modes.

Each EEPROM byte or aligned word must be erased before programming. The EEPROM module supports byte, aligned word, row (32 bytes) or bulk erase, all using the internal charge pump. The erased state is $FF. The EEPROM module has hardware interlocks which protect stored data from corruption by accidentally enabling the program/erase voltage. Programming voltage is derived from the internal V_{DD} supply with an internal charge pump.

10.5 Latching of Interrupts

$\overline{\text{XIRQ}}$ is always level triggered and $\overline{\text{IRQ}}$ can be selected as a level triggered interrupt. These level triggered interrupt pins should only be released during the appropriate interrupt service routine. Generally the interrupt service routine will handshake with the interrupting logic to release the pin. In this way, the MCU will never start the interrupt service sequence only to determine that there is no longer an interrupt source. In event that this does occur the trap vector will be taken.

If $\overline{\text{IRQ}}$ is selected as an edge triggered interrupt, the hold time of the level after the active edge is independent of when the interrupt is serviced. As long as the minimum hold time is met, the interrupt will be latched inside the MCU. In this case the IRQ edge interrupt latch is cleared automatically when the interrupt is serviced.

All of the remaining interrupts are latched by the MCU with a flag bit. These interrupt flags should be cleared during an interrupt service routine or when interrupts are masked by the I bit. By doing this, the MCU will never get an unknown interrupt source and take the trap vector.

$\overline{ACQ}$ — Not in Acquisition

If AUTO = 1 ($\overline{ACQ}$ is Read Only)

0 = PLL VCO is not within the desired tolerance of the target frequency. The loop filter is in high bandwidth, acquisition mode.

1 = After the phase lock loop circuit is turned on, indicates the PLL VCO is within the desired tolerance of the target frequency. The loop filter is in low bandwidth, tracking mode.

If AUTO = 0

0 = High bandwidth PLL loop selected

1 = Low bandwidth PLL loop selected

PSTP — Pseudo-STOP Enable

0 = Pseudo-STOP oscillator mode is disabled

1 = Pseudo-STOP oscillator mode is enabled

In Pseudo-STOP mode, the oscillator is still running while the MCU is maintained in STOP mode. This allows for a faster STOP recovery and reduces the mechanical stress and aging of the resonator in case frequent STOP conditions at the expense of a slightly increased power consumption.

LHIE — Limp-Home Interrupt Enable

0 = Limp-Home interrupt is disabled

1 = Limp-Home interrupt is enabled

Forced to 0 when VDDPLL is at VSS level.

NOLHM —No Limp-Home Mode

0 = Loss of reference clock forces the MCU in limp-home mode.

1 = Loss of reference clock causes standard Clock Monitor reset.

Read anytime; Normal modes: write once; Special modes: write anytime. Forced to 1 when VDDPLL is at VSS level.

variation or particle contamination).

3. Within this range, choose the EXTAL–VSS capacitance closest to ($C_{EXTAL–VSS}$ = 2*CL – 10pF).
4. If the ideal component is between two valid component values (the maximum ESR is sufficient for both component values), then choose the component with the highest maximum ESR or choose an available component between the two listed values.
5. Choose the size of the XTAL–VSS capacitance equal to EXTAL–VSS capacitance.
6. If the frequency of the crystal falls between listed values, determine the appropriate component for the listed frequency values on either side and extrapolate.
7. The maximum allowed capacitor is the highest listed component, and the minimum allowed capacitor is the lowest listed component. ‘NA’ or ‘Not Allowed’ means the listed component is not valid or allowed for the given frequency, Shunt Capacitance, and VDDPLL setting.

13.5.3.2 General Specifications

The following limitations apply to every system:

- Ceramic resonators with integrated components must have the integrated components accounted for in the total component value.
- Series cut resonators should not be used. Use parallel cut instead.
- The Load Capacitance should be 12pF or higher, preferably greater than 15pF.

16.3 Block diagram

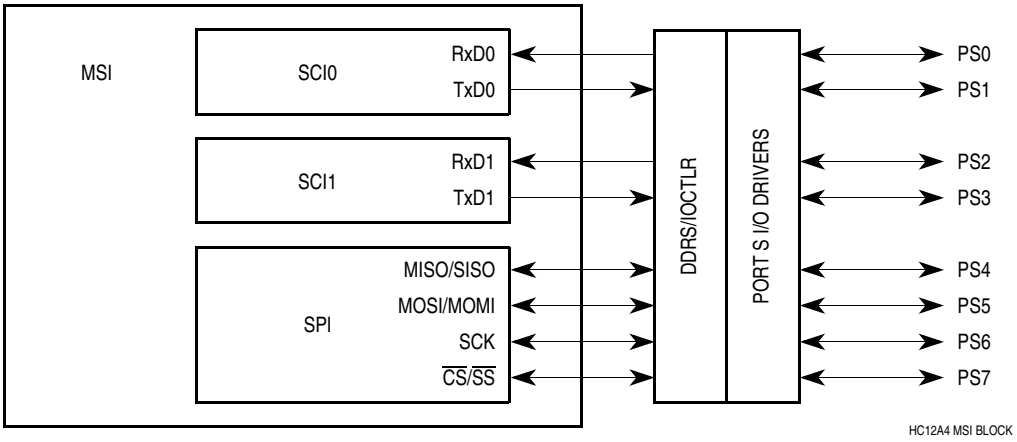


Figure 16-1. Multiple Serial Interface Block Diagram

16.4 Serial Communication Interface (SCI)

Two serial communication interfaces are available on the MC68HC912DT128A. These are NRZ format (one start, eight or nine data, and one stop bit) asynchronous communication systems with independent internal baud rate generation circuitry and SCI transmitters and receivers. They can be configured for eight or nine data bits (one of which may be designated as a parity bit, odd or even). If enabled, parity is generated in hardware for transmitted and received data. Receiver parity errors are flagged in hardware. The baud rate generator is based on a modulus counter, allowing flexibility in choosing baud rates. There is a receiver wake-up feature, an idle line detect feature, a loop-back mode, and various error detection features. Two port pins for each SCI provide the external interface for the transmitted data (TXD) and the received data (RXD).

For a faster wake-up out of WAIT mode by a received SCI message, both SCI have the capability of sending a receiver interrupt, if enabled, when RAF (receiver active flag) is set. For compatibility with other M68HC12 products, this feature is active only in WAIT mode and is disabled when VDDPLL supply is at V_{SS} level.

Table 17-2. IIC Divider and SDA Hold values

IBC5-0 (hex)	SCL Divider (clocks)	SDA Hold (clocks)
00	20	7
01	22	7
02	24	8
03	26	8
04	28	9
05	30	9
06	34	10
07	40	10
08	28	7
09	32	7
0A	36	9
0B	40	9
0C	44	11
0D	48	11
0E	56	13
0F	68	13
10	48	9
11	56	9
12	64	13
13	72	13
14	80	17
15	88	17
16	104	21
17	128	21
18	80	9
19	96	9
1A	112	17

IBC5-0 (hex)	SCL Divider (clocks)	SDA Hold (clocks)
20	160	17
21	192	17
22	224	33
23	256	33
24	288	49
25	320	49
26	384	65
27	480	65
28	320	33
29	384	33
2A	448	65
2B	512	65
2C	576	97
2D	640	97
2E	768	129
2F	960	129
30	640	65
31	768	65
32	896	129
33	1024	129
34	1152	193
35	1280	193
36	1536	257
37	1920	257
38	1280	129
39	1536	129
3A	1792	257

three bits in the identifier acceptance control register (see msCAN12 Identifier Acceptance Control Register (CIDAC)). These identifier hit flags (IDHIT2–0) clearly identify the filter section that caused the acceptance. They simplify the application software's task to identify the cause of the receiver interrupt. In case that more than one hit occurs (two or more filters match) the lower hit has priority.

A hit will also cause a receiver interrupt if enabled.

18.6 Interrupts

The msCAN12 supports four interrupt vectors mapped onto eleven different interrupt sources, any of which can be individually masked (for details see msCAN12 Receiver Flag Register (CRFLG) to msCAN12 Transmitter Control Register (CTCR)):

- *Transmit interrupt*: At least one of the three transmit buffers is empty (not scheduled) and can be loaded to schedule a message for transmission. The TXE flags of the empty message buffers are set.
- *Receive interrupt*: A message has been successfully received and loaded into the foreground receive buffer. This interrupt will be emitted immediately after receiving the EOF symbol. The RXF flag is set.
- *Wake-up interrupt*: An activity on the CAN bus occurred during msCAN12 internal SLEEP mode.
- *Error interrupt*: An overrun, error or warning condition occurred. The receiver flag register (CRFLG) will indicate one of the following conditions:
  - *Overrun:* an overrun condition as described in Receive Structures has occurred.
  - *Receiver warning*: the receive error counter has reached the CPU warning limit of 96.
  - *Transmitter warning*: the transmit error counter has reached the CPU warning limit of 96.

mode is required, the existing continuous sequence must be interrupted, the control registers modified, and a new conversion sequence initiated.

MULT — Multi-Channel Sample Mode

0 = Sample only the specified channel
1 = Sample across many channels

When MULT is 0, the ATD sequence controller samples only from the specified analog input channel for an entire conversion sequence. The analog channel is selected by channel selection code (control bits CC/CB/CA located in ATDCTL5).

When MULT is 1, the ATD sequence controller samples across channels. The number of channels sampled is determined by the sequence length value (S8C, S1C control bits). The first analog channel examined is determined by channel selection code (CC, CB, CA control bits); subsequent channels sampled in the sequence are determined by incrementing the channel selection code.

SC — Special Channel Conversion Mode

0 = Perform A/D conversion on an analog input channel
1 = Perform special channel A/D conversion

SC determines if the ATD module performs A/D conversions on any of the analog input channels (normal operation) or whether it performs a conversion on one of the defined, special channels. The special channels are normally used to test the A/D machine and include converting the high and low reference potentials for the module. The control bits CC/CB/CA are used to indicate which special channel is to be converted.

Table 19-8. Special Channel Conversion Select Coding

CC	CB	CA	Special	Expected
			Channel	Digital Result Code
0	X	X	reserved	–
1	0	0	VRH	$FF
1	0	1	VRL	$00
1	1	0	(VRH + VRL)/2	$7F
1	1	1	reserved	–

Resetting to idle mode defines the only exception of the reset control bit condition to the system reset condition. The reset control bit does not initialize the ADPU bit to its reset condition and therefore does not power down the module. This except allows the module to remain active for other test operations.

19.9.7 PORTAD Port Data Register

The input data port associated with the ATD module is input-only. The port pins are shared with the analog A/D inputs.

PORTAD0/PORTAD1 — Port AD Data Input Register **$006F/$01EF**

	Bit 7	6	5	4	3	2	1	Bit 0
	PADx7	PADx6	PADx5	PADx4	PADx3	PADx2	PADx1	PADx0
RESET:	-	-	-	-	-	-	-	-

PADx[7:0] — Port AD Data Input Bits

Reset: These pins reflect the state of the input pins.

The ATD input ports may be used for general purpose digital input. When the port data registers are read, they contain the digital levels appearing on the input pins at the time of the read. Input pins with signal potentials not meeting V_{IL} or V_{IH} specifications will have an indeterminate value.

Use of any Port pin for digital input does not preclude the use of any other Port pin for analog input.

Writes to this register have no meaning at any time.

19.9.8 ADRx A/D Conversion Result Registers (ADR0-15)

ADRx0H — A/D Converter Result Register 0	**$0070/$01F0**
ADRx0L — A/D Converter Result Register 0	**$0071/$01F1**
ADRx1H — A/D Converter Result Register 1	**$0072/$01F2**
ADRx1L — A/D Converter Result Register 1	**$0073/$01F3**
ADRx2H — A/D Converter Result Register 2	**$0074/$01F4**
ADRx2L — A/D Converter Result Register 2	**$0075/$01F5**
ADRx3H — A/D Converter Result Register 3	**$0076/$01F6**
ADRx3L — A/D Converter Result Register 3	**$0077/$01F7**
ADRx4H — A/D Converter Result Register 4	**$0078/$01F8**
ADRx4L — A/D Converter Result Register 4	**$0079/$01F9**
ADRx5H — A/D Converter Result Register 5	**$007A/$01FA**
ADRx5L — A/D Converter Result Register 5	**$007B/$01FB**
ADRx6H — A/D Converter Result Register 6	**$007C/$01FC**
ADRx6L — A/D Converter Result Register 6	**$007D/$01FD**
ADRx7H — A/D Converter Result Register 7	**$007E/$01FE**
ADRx7L — A/D Converter Result Register 7	**$007F/$01FF**

ADRxxH	Bit 15	6	5	4	3	2	1	Bit 8
ADRxxL	Bit 7	Bit 6	0	0	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

The A/D conversion results are stored in 8 result registers. These registers are designated ADR0 through ADR7.

The result data is formatted using the DJM control bit in ATDCTL2. For 8-bit result data, the result data maps between the high (left justified) and low (right justified) order bytes of the result register. For 10-bit result data, the result data maps between bits 6-15 (left justified) and bits 0-9 (right justified) of the result register.

These registers are normally read-only.

BKGD pin during host-to-target transmissions to speed up rising edges. Since the target does not drive the BKGD pin during this period, there is no need to treat the line as an open-drain signal during host-to-target transmissions.

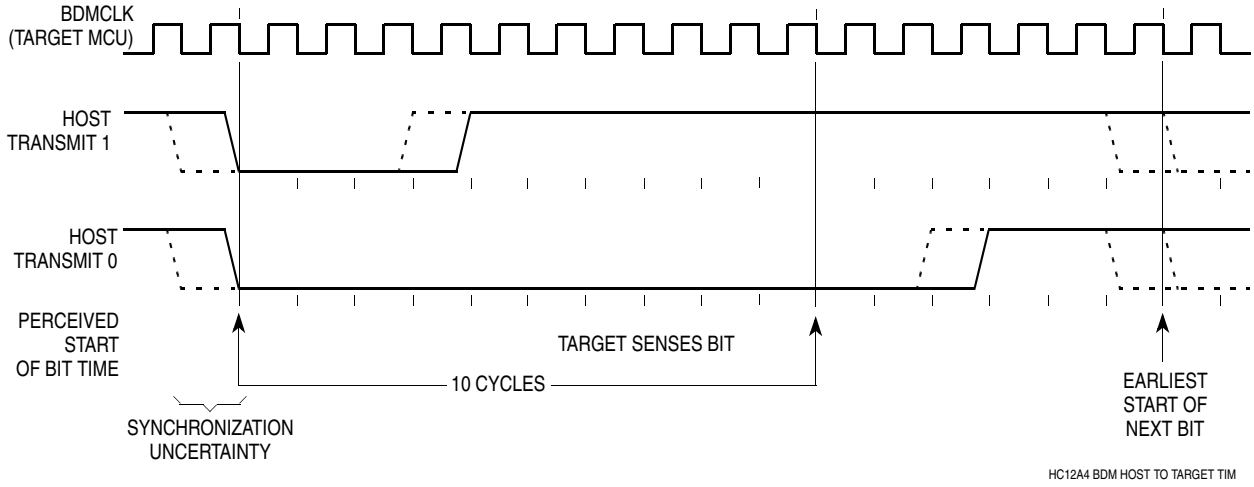


Figure 20-1. BDM Host to Target Serial Bit Timing

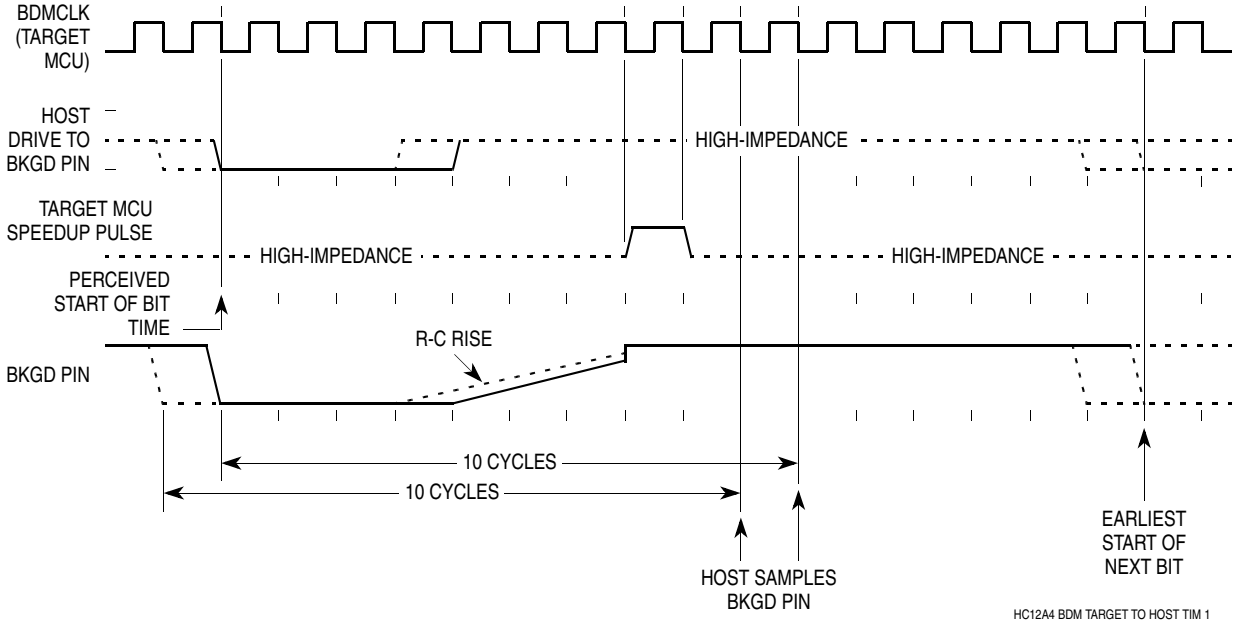
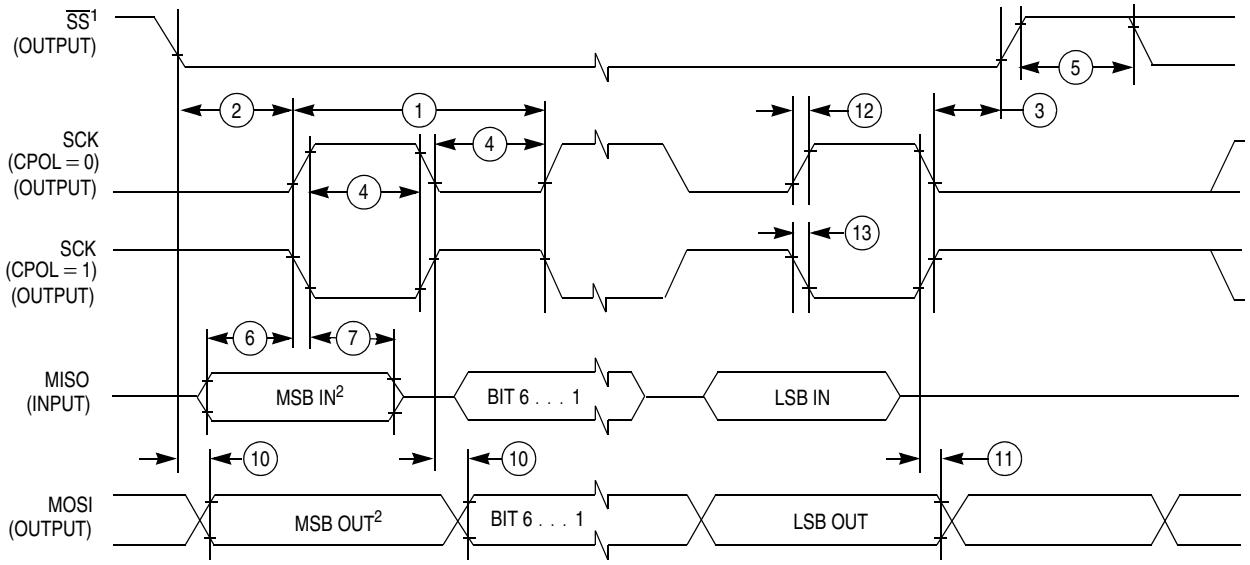
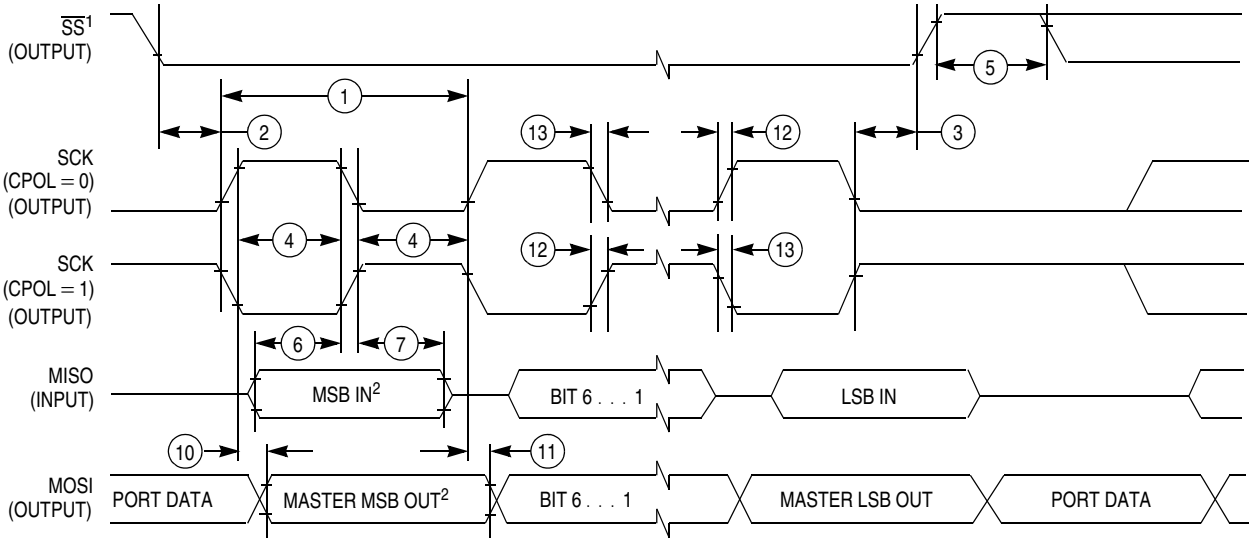


Figure 20-2. BDM Target to Host Serial Bit Timing (Logic 1)



1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

A) SPI Master Timing (CPHA = 0)



1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

B) SPI Master Timing (CPHA = 1)

Figure 21-9. SPI Timing Diagram (1 of 2)

Table 23-1. Suggested 8MHz Synthesis PLL Filter Elements (Tracking Mode)

Reference [MHz]	SYNR	Fbus [MHz]	C [nF]	R [kΩ]	Loop Bandwidth [kHz]	Bandwidth Limit [kHz]
0.614	$0C	7.98	100	4.3	1.1	157
0.614	$0C	7.98	4.7	20	5.3	157
0.614	$0C	7.98	1	43	11.5	157
0.614	$0C	7.98	0.33	75	20	157
0.8	$09	8.00	220	2.7	0.9	201
0.8	$09	8.00	10	12	4.2	201
0.8	$09	8.00	2.2	27	8.6	201
0.8	$09	8.00	0.47	56	19.2	201
1	$07	8.00	220	2.4	1	251
1	$07	8.00	10	11	4.7	251
1	$07	8.00	2.2	24	9.9	251
1	$07	8.00	0.47	51	21.4	251
1.6	$05	8.00	330	1.5	1	402
1.6	$05	8.00	10	9.1	5.9	402
1.6	$05	8.00	3.3	15	10.2	402
1.6	$05	8.00	1	27	18.6	402
2	$03	8.00	470	1.1	0.96	502
2	$03	8.00	22	5.1	4.4	502
2	$03	8.00	4.7	11	9.6	502
2	$03	8.00	1	24	20.8	502
2.66	$02	8.00	220	1.5	1.6	668
2.66	$02	8.00	22	4.7	5.1	668
2.66	$02	8.00	4.7	10	11	668
2.66	$02	8.00	1	22	24	668
4	$01	8.00	220	1.2	1.98	1005
4	$01	8.00	33	3	5.1	1005
4	$01	8.00	10	5.6	9.3	1005
4	$01	8.00	2.2	12	19.8	1005

Glossary