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Details	
Product Status	Not For New Designs
Core Processor	CPU12
Core Size	16-Bit
Speed	8MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc912dg128acpver

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Setting the RDPA bit in register RDRIV causes all port A outputs to have reduced drive level. RDRIV can be written once after reset. RDRIV is not in the address map in peripheral mode. Refer to Bus Control and Input/Output.

3.5.2 Port B

Port B pins are used for address and data in expanded modes. When this port is not used for external access such as in single-chip mode, these pins can be used as general purpose I/O. The port data register is not in the address map during expanded and peripheral mode operation. When it is in the map, port B can be read or written at anytime.

Register DDRB determines whether each port B pin is an input or output. DDRB is not in the address map during expanded and peripheral mode operation. Setting a bit in DDRB makes the corresponding bit in port B an output; clearing a bit in DDRB makes the corresponding bit in port B an input. The default reset state of DDRB is all zeroes.

When the PUPB bit in the PUCR register is set, all port B input pins are pulled-up internally by an active pull-up device. PUCR is not in the address map in peripheral mode.

Setting the RDPB bit in register RDRIV causes all port B outputs to have reduced drive level. RDRIV can be written once after reset. RDRIV is not in the address map in peripheral mode. Refer to Bus Control and Input/Output.

3.5.3 Port E

Port E pins operate differently from port A and B pins. Port E pins are used for bus control signals and interrupt service request signals. When a pin is not used for one of these specific functions, it can be used as general-purpose I/O. However, two of the pins (PE[1:0]) can only be used for input, and the states of these pins can be read in the port data register even when they are used for $\overline{\text{IRQ}}$ and $\overline{\text{XIRQ}}$.

The PEAR register determines pin function, and register DDRE determines whether each pin is an input or output when it is used for

Table 6-2. Program space Page Index

Page Index 2 (PPAGE bit 2)	Page Index 1 (PPAGE bit 1)	Page Index 0 (PPAGE bit 0)	16K Program space Page	Flash array
0	0	0	16K byte Page 0	00FEE32K
0	0	1	16K byte Page 1	00FEE32K
0	1	0	16K byte Page 2	01FEE32K
0	1	1	16K byte Page 3	01FEE32K
1	0	0	16K byte Page 4	10FEE32K
1	0	1	16K byte Page 5	10FEE32K
1	1	0	16K byte Page 6*	11FEE32K
1	1	1	16K byte Page 7*	11FEE32K

* The 16K byte flash in program space page 6 can also be accessed at a fixed location from $4000 to $7FFF. The 16K byte flash in program space page 7 can also be accessed at a fixed location from $C000 to $FFFF.

6.4.2 Flash register space expansion

There are four 32K Flash arrays for MC68HC912DT128A and each requires a 4-byte register block. A register space window is used to access one of the four 4-byte blocks and the PPAGE register to map each one into the window. The register space window is located from $00F4 to $00F7 after reset. Only two page indices are used to point to one of the four pages of the register space.

Table 6-3. Flash Register space Page Index

Page Index 2 (PPAGE bit 2)	Page Index 1 (PPAGE bit 1)	Page Index 0 (PPAGE bit 0)	Flash register space Page	Flash array
0	0	X	$00F4-$00F7 Page 0	00FEE32K
0	1	X	$00F4-$00F7 Page 1	01FEE32K
1	0	X	$00F4-$00F7 Page 2	10FEE32K
1	1	X	$00F4-$00F7 Page 3	11FEE32K

CALE — Calibration Reference Enable

Read and write anytime.

0 = Calibration reference is disabled and PE7 is general purpose I/O in single chip or peripheral modes or if NDBE bit is set.

1 = Calibration reference is enabled on PE7 in single chip and peripheral modes or if NDBE bit is set.

DBENE — $\overline{\text{DBE}}$ or Inverted E Clock on PE7

Normal modes: write once. Special modes: write anytime EXCEPT the first time. Read anytime.

DBENE controls which signal is output on PE7 when NDBE control bit is cleared. The inverted E clock output can be used to latch the address for de-multiplexing. It has the same behavior as the E clock, except it is inverted. Please note that in the case of idle expansion bus, the 'not E clock' signal could stay high for many cycles.

The DBENE bit has no effect in Single Chip or Peripheral Modes and PE7 is defaulted to the CAL function if CALE bit is set in PEAR register or to an I/O otherwise.

0 = PE7 pin used for $\overline{\text{DBE}}$ external control of data enable on memories in expanded modes when NDBE = 0

1 = PE7 pin used for inverted E clock output in expanded modes when NDBE = 0

PUCR — Pull-Up Control Register **$000C**

	Bit 7	6	5	4	3	2	1	Bit 0
	PUPK	PUPJ	PUPH	PUPE	0	0	PUPB	PUPA
RESET:	0	0	0	1	0	0	0	0

These bits select pull-up resistors for any pin in the corresponding port that is currently configured as an input. This register is not in the map in peripheral mode.

Read and write anytime.

PUPK — Pull-Up Port K Enable

0 = Port K pull-ups are disabled.

1 = Enable pull-up devices for all port K input pins.

9.8 Programming EEDIVH and EEDIVL Registers

The EEDIVH and EEDIVL registers must be correctly set according to the oscillator frequency before any EEPROM location can be programmed or erased.

9.8.1 Normal mode

The EEDIVH and EEDIVL registers are write once in normal mode. Upon system reset, the application program is required to write the correct divider value to EEDIVH and EEDIVL registers based on the oscillator frequency. After the first write, the value in the EEDIVH and EEDIVL registers is locked from being overwritten until the next reset. The EEPROM is then ready for standard program/erase routines.

CAUTION: *Runaway code can possibly corrupt the EEDIVH and EEDIVL registers if they are not initialized (write once registers).*

9.8.2 Special mode

If an existing application code with EEPROM program/erase routines is fixed and the system is already operating at a known oscillator frequency, it is recommended to initialize the shadow word with the corresponding EEDIVH and EEDIVL values in special mode. The shadow word initializes EEDIVH and EEDIVL registers upon system reset to ensure software compatibility with existing code. Initializing the EEDIVH and EEDIVL registers in special modes (SMODN=0) is accomplished by the following steps.

1. Write correct divider value to EEDIVH and EEDIVL registers based on the oscillator frequency as per Table 9-1.
2. Remove the SHADOW word protection by clearing SHPROT bit in EEPROT register.
3. Clear NOSHW bit in EEMCR register to make the SHADOW word visible at $0FC0-$0FC1.
4. Write NOSHW bit in EEMCR register to make the SHADOW word visible at $0FC0-$0FC1.

12.5 Acquisition and Tracking Modes

The lock detector compares the frequencies of the VCO feedback clock, DIVCLK, and the final reference clock, REFCLK. Therefore, the speed of the lock detector is directly proportional to the final reference frequency. The circuit determines the mode of the PLL and the lock condition based on this comparison.

The PLL filter is manually or automatically configurable into one of two operating modes:

- Acquisition mode — In acquisition mode, the filter can make large frequency corrections to the VCO. This mode is used at PLL start-up or when the PLL has suffered a severe noise hit and the VCO frequency is far off the desired frequency. This mode can also be desired in harsh environments when the leakage levels on the filter pin (XFC) can overcome the tracking currents of the PLL charge pump. When in acquisition mode, the $\overline{ACQ}$ bit in the PLL control register is clear.
- Tracking mode — In tracking mode, the filter makes only small corrections to the frequency of the VCO. The PLL enters tracking mode when the VCO frequency is nearly correct. The PLL is automatically in tracking mode when not in acquisition mode or when the $\overline{ACQ}$ bit is set.

The PLL can change the bandwidth or operational mode of the loop filter manually or automatically. With an identical filtering time constant, the PLL bandwidth is larger in acquisition mode than in tracking by a ratio of about 3.

In automatic bandwidth control mode (AUTO = 1), the lock detector automatically switches between acquisition and tracking modes. Automatic bandwidth control mode also is used to determine when the VCO clock, PLLCLK, is safe to use as the source for the base clock, SYSCLK. If PLL LOCK interrupt requests are enabled, the software can wait for an interrupt request and then check the LOCK bit. If CPU interrupts are disabled, software can poll the LOCK bit continuously (during PLL start-up, usually) or at periodic intervals. In either case, when the LOCK bit is set, the PLLCLK clock is safe to use as the source

13.4.3 Important Information For Calculating Component Values

Before attempting to apply the information in section 13.4.2.4 Key Parameters, the following data from the resonator vendor is required:

- **Resonator Frequency (f)**
- **Maximum ESR (R, ESR, or R1)**
- **Maximum Shunt Capacitance (C0)**
- **Load Capacitance (CL)** — this is not the external component values but rather the capacitance applied in parallel with the resonator during the tuning procedure.

13.4.3.1 How to Use This Information

The following tables provide Maximum ESR vs. component value for various frequencies. This table should be used in the following manner:

1. Choose the set of component values corresponding to the correct maximum shunt capacitance (equal to the sum of EXTAL–VSS parasitics in excess of 1pF, plus the C0 of the resonator) and VDDPLL setting.
2. Determine the range of components for which the Maximum ESR is greater than the absolute maximum ESR of the resonator (including ageing, power dissipation, temperature, process variation or particle contamination).
3. Within this range, choose the EXTAL–XTAL capacitance closest to ($C_{EXTAL–XTAL}$ = 2*CL – 1pF).
4. If the ideal component is between two valid component values (the maximum ESR is sufficient for both component values), then choose the component with the highest maximum ESR or choose an available component between the two listed values.
5. Choose the size of the XTAL–VSS capacitance equal to the closest available size to ($C_{XTAL–VSS}$ = 0.82*$C_{EXTAL–XTAL}$).

- **Minimize XTAL and EXTAL routing lengths** to reduce EMC issues.

NOTE: *EXTAL and XTAL routing resistances are less important than capacitances. Using minimum width traces is an acceptable trade-off to reduce capacitance.*

13.5 MC68HC912Dx128P Pierce Oscillator Specification

This section applies to the 2L05H mask set, which refers to the newest set of CGM fixes (to the MC68HC912DT128A) with the Pierce oscillator configuration enabled. The name for these devices is MC68HC912Dx128P.

13.5.1 MC68HC912Dx128P Oscillator Design Architecture

The Pierce oscillator architecture is shown in Figure 13-4. The component configuration for this oscillator is different to all previous MC68HC912DT128A configurations and the recommended components may be different.

Please note carefully the connection of external capacitors and the resonator in this diagram.

RIE — Receiver Interrupt Enable

0 = RDRF and OR interrupts disabled, RAF interrupt in WAIT mode disabled

1 = SCI interrupt will be requested whenever the RDRF or OR status flag is set, or when RAF is set while in WAIT mode with VDDPLL high.

ILIE — Idle Line Interrupt Enable

0 = IDLE interrupts disabled

1 = SCI interrupt will be requested whenever the IDLE status flag is set.

TE — Transmitter Enable

0 = Transmitter disabled

1 = SCI transmit logic is enabled and the TXD pin (Port S bit 1/bit 3) is dedicated to the transmitter. The TE bit can be used to queue an idle preamble.

RE — Receiver Enable

0 = Receiver disabled

1 = Enables the SCI receive circuitry.

RWU — Receiver Wake-Up Control

0 = Normal SCI Receiver

1 = Enables the wake-up function and inhibits further receiver interrupts. Normally hardware wakes the receiver by automatically clearing this bit.

SBK — Send Break

0 = Break generator off

1 = Generate a break code (at least 10 or 11 contiguous zeros).

As long as SBK remains set the transmitter will send zeros. When SBK is changed to zero, the current frame of all zeros is finished before the TxD line goes to the idle state. If SBK is toggled on and off, the transmitter will send only 10 (or 11) zeros and then revert to mark idle or sending data.

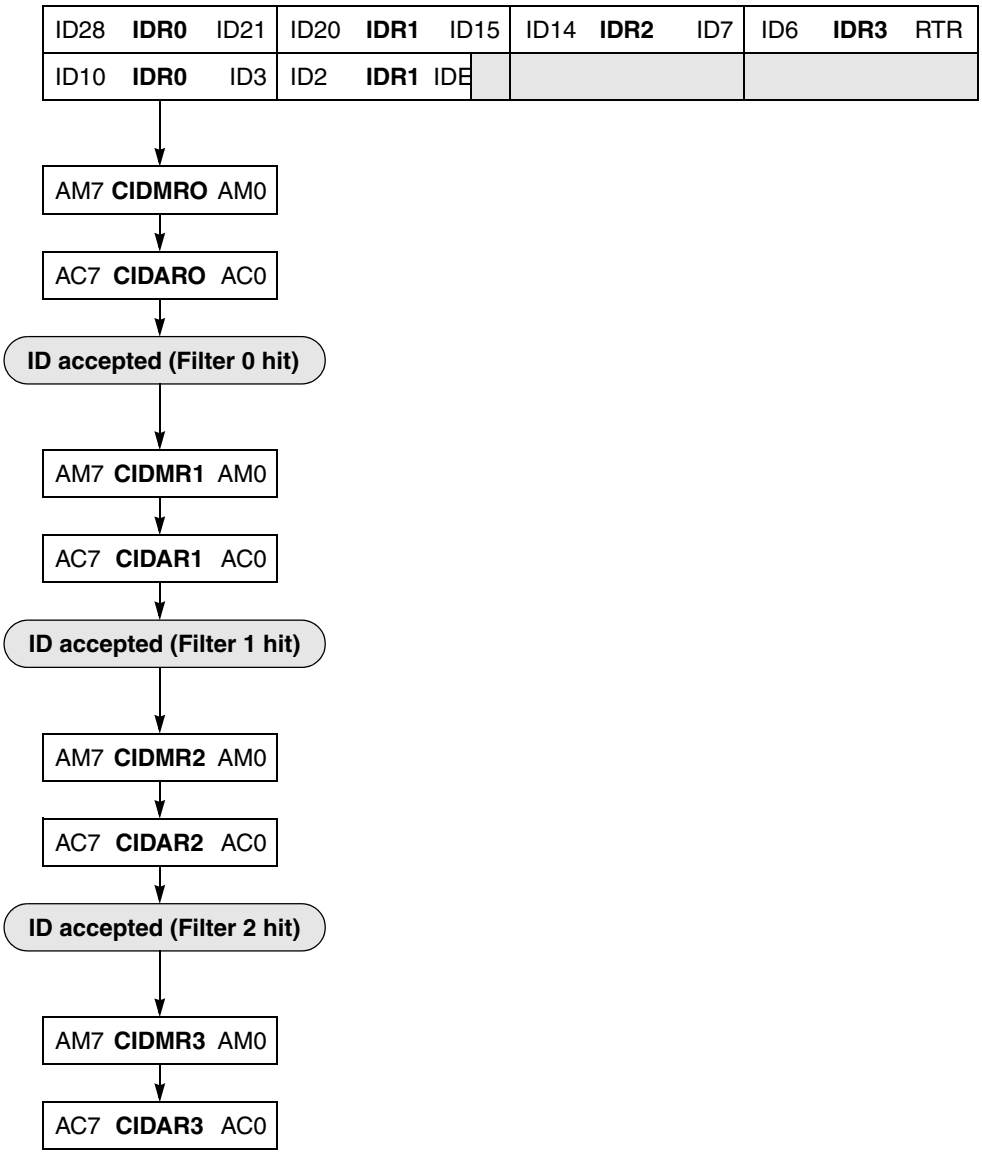


Figure 18-5. 8-bit Maskable Acceptance Filters

The identifier acceptance registers (CIDAR0–7) define the acceptable patterns of the standard or extended identifier (ID10–ID0 or ID28–ID0). Any of these bits can be marked don't care in the identifier mask registers (CIDMR0–7).

A filter hit is indicated to the application software by a set RXF (receive buffer full flag, see msCAN12 Receiver Flag Register (CRFLG)) and

18.12.4 Data Segment Registers (DSRn)

The eight data segment registers contain the data to be transmitted or being received. The number of bytes to be transmitted or being received is determined by the data length code in the corresponding DLR.

18.12.5 Transmit Buffer Priority Registers (TBPR)

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TBPR(1)	R	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
$01xD	W								
RESET		-	-	-	-	-	-	-	-

1. x is 5, 6, or 7 depending on which buffer Tx0, Tx1, or Tx2 respectively.

PRIO7 – PRIO0 — Local Priority

This field defines the local priority of the associated message buffer. The local priority is used for the internal prioritizing process of the msCAN12 and is defined to be highest for the smallest binary number. The msCAN12 implements the following internal priorization mechanism:

- All transmission buffers with a cleared TXE flag participate in the priorisation right before the SOF (Start of Frame) is sent.
- The transmission buffer with the lowest local priority field wins the priorisation.
- In case of more than one buffer having the same lowest priority the message buffer with the lower index number wins.

NOTE: *To ensure data integrity, no registers of the transmit buffers shall be written while the associated TXE flag is cleared.*
To ensure data integrity, no registers of the receive buffer shall be read while the RXF flag is cleared.

programmable constant in order to generate the ATD module's internal clock. One additional benefit of the prescaled clock feature is that it allows the user further control over the sample period (note that changing the module clock also affects conversion time).

The prescaler is based on a 5 bit modulus counter and divides the PCLK by an integer value between 1 and 32. The final clock frequency is obtained with a further division by 2.

The internal ATD module clock and the system PCLK have a direct phase relationship, however the ATD module operates as if it is effectively asynchronous to MCU bus clock cycles.

19.5 ATD Operational Modes

19.5.1 Power Down Mode

The ATD module can be powered down under program control. This is done by turning the clock signals off to the digital electronics of the module and eliminating the quiescent current draw of the analog electronics.

Power down control is implemented in one of three ways.

1. Using the ADPU bit in control register ATDCTL2.
2. When STOP instruction is executed, the module will power down for the duration of the STOP function.
3. If the module WAIT enable bit (ASWAI) is set and a WAIT instruction is executed, the module will power down for the duration of the WAIT function.

Note that the reset default for the ADPU bit is zero. Therefore, when this module is reset, it is reset into the power down state.

Once the command to power down has been received, the ATD module aborts any conversion sequence in progress and enters lower power mode. When the module is powered up again, the bias settings in the analog electronics must be given time to stabilize before conversions

Input Signal Vrl = 0 Volts Vrh = 5.12 Volts	8-Bit Codes	10-Bit Codes
5.120 Volts	FF	FFC0
5.100	FF	FF00
5.080	FE	FE00
2.580	81	8100
2.560	80	8000
2.540	7F	7F00
0.020	01	0100
0.000	00	0000

Table 19-2. Left Justified ATD Output Codes

ASCIE — ATD Sequence Complete Interrupt Enable

0 = Disables ATD interrupt

1 = Enables ATD interrupt on Sequence Complete

The sequence complete interrupt function signals the MCU when a conversion sequence is complete. At this time, the result registers contain the result data generated by the conversion sequence. If this interrupt function is disabled, then the conversion complete flags must be polled to determine when a conversion or a conversion sequence is complete. Note that reset clears pending interrupts.

ASCIF — ATD Sequence Complete Interrupt Flag

0 = No ATD sequence complete interrupt occurred

1 = ATD sequence complete interrupt occurred

The sequence complete interrupt flag. This flag is not cleared until the interrupt is serviced (by reading the result data in such a way that the conversion complete flag is cleared), a new conversion sequence is initiated, or the module is reset. This bit is not writable in any mode.

19.9.6 ATDTEST Module Test Register (ATDTEST)

The test registers implement various special (test) modes used to test the ATD module. The reset bit in ATDTEST1 is always read/write. The SAR (successive approximation register) can always be read but only written in special (test) mode.

The functions implemented by the test registers are reserved for factory test.

ATD0TESTH/ATD1TESTH — ATD Test Register **$0068/$01E8**

	Bit 7	6	5	4	3	2	1	Bit 0
	SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2
RESET:	0	0	0	0	0	0	0	0

ATD0TESTL/ATD1TESTL — ATD Test Register **$0069/$01E9**

	Bit 7	6	5	4	3	2	1	Bit 0
	SAR1	SAR0	RST	0	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

SAR[9:0] — Successive Approximation Register

This ten bit value represents the contents of the AD machine's successive approximation register. This value can always be read. It can only be written in special (test) mode. Note that ATDTEST0 acts as a ten bit register since the entire SAR is read/written when accessing this address.

RST — Test Mode Reset Bit

0 = No reset

1 = Reset the ATD module

When set, this bit causes the ATD module to reset itself. This sets all registers to their reset state (note the reset state of the reset bit is zero), the current conversion and conversion sequence are aborted, pending interrupts are cleared, and the module is placed in an idle mode.

1 = BDM system operates with ECLK.

The WRITE_BD_BYTE@FF01 command that changes CLKSW including 150 cycles after the data portion of the command should be timed at the old speed. Beginning with the start of the next BDM command, the new clock can be used for timing BDM communications.

If ECLK rate is slower than BDMCLK rate, CLKSW is ignored and BDM system is forced to operate with ECLK.

20.4.5.2 INSTRUCTION - Hardware Instruction Decode

The INSTRUCTION register is written by the BDM hardware as a result of serial data shifted in on the BKGD pin. It is readable and writable in Special Peripheral mode on the parallel bus. It is discussed here for two conditions: when a **hardware** command is executed and when a **firmware** command is executed.

Read and write: all modes

. The hardware clears the INSTRUCTION register if 512 BDMCLK cycles occur between falling edges from the host.

INSTRUCTION— BDM Instruction Register (hardware command explanation) **$FF00**

	BIT 7	6	5	4	3	2	1	BIT 0
	H/F	DATA	R/W	BKGND	W/B	BD/U	0	0
RESET:	0	0	0	0	0	0	0	0

The bits in the BDM instruction register have the following meanings when a **hardware** command is executed.

H/F — Hardware/Firmware Flag

0 = Firmware command

1 = Hardware command

To trace program flow, setting the BKPM bit causes address comparison of program data only. Control bits are also available that allow checking read/write matches.

BRKCT0 — Breakpoint Control Register 0 **$0020**

	Bit 7	6	5	4	3	2	1	Bit 0
	BKEN1	BKEN0	BKPM	0	BK1ALE	BK0ALE	0	0
RESET:	0	0	0	0	0	0	0	0

Read and write anytime.
This register is used to control the breakpoint logic.

BKEN1, BKEN0 — Breakpoint Mode Enable

Table 20-7. Breakpoint Mode Control

BKEN1	BKEN0	Mode Selected	BRKAH/L Usage	BRKDH/L Usage	R/W	Range
0	0	Breakpoints Off	—	—	—	—
0	1	SWI — Dual Address Mode	Address Match	Address Match	No	Yes
1	0	BDM — Full Breakpoint Mode	Address Match	Data Match	Yes	Yes
1	1	BDM — Dual Address Mode	Address Match	Address Match	Yes	Yes

BKPM — Break on Program Addresses

This bit controls whether the breakpoint will cause a break on a match (next instruction boundary) or on a match that will be an executable opcode. Data and non-executed opcodes cannot cause a break if this bit is set. This bit has no meaning in SWI dual address mode. The SWI mode only performs program breakpoints.

0 = On match, break at the next instruction boundary
1 = On match, break if the match is an instruction that will be executed. This uses tagging as its breakpoint mechanism.

BK1ALE — Breakpoint 1 Range Control

Only valid in dual address mode.

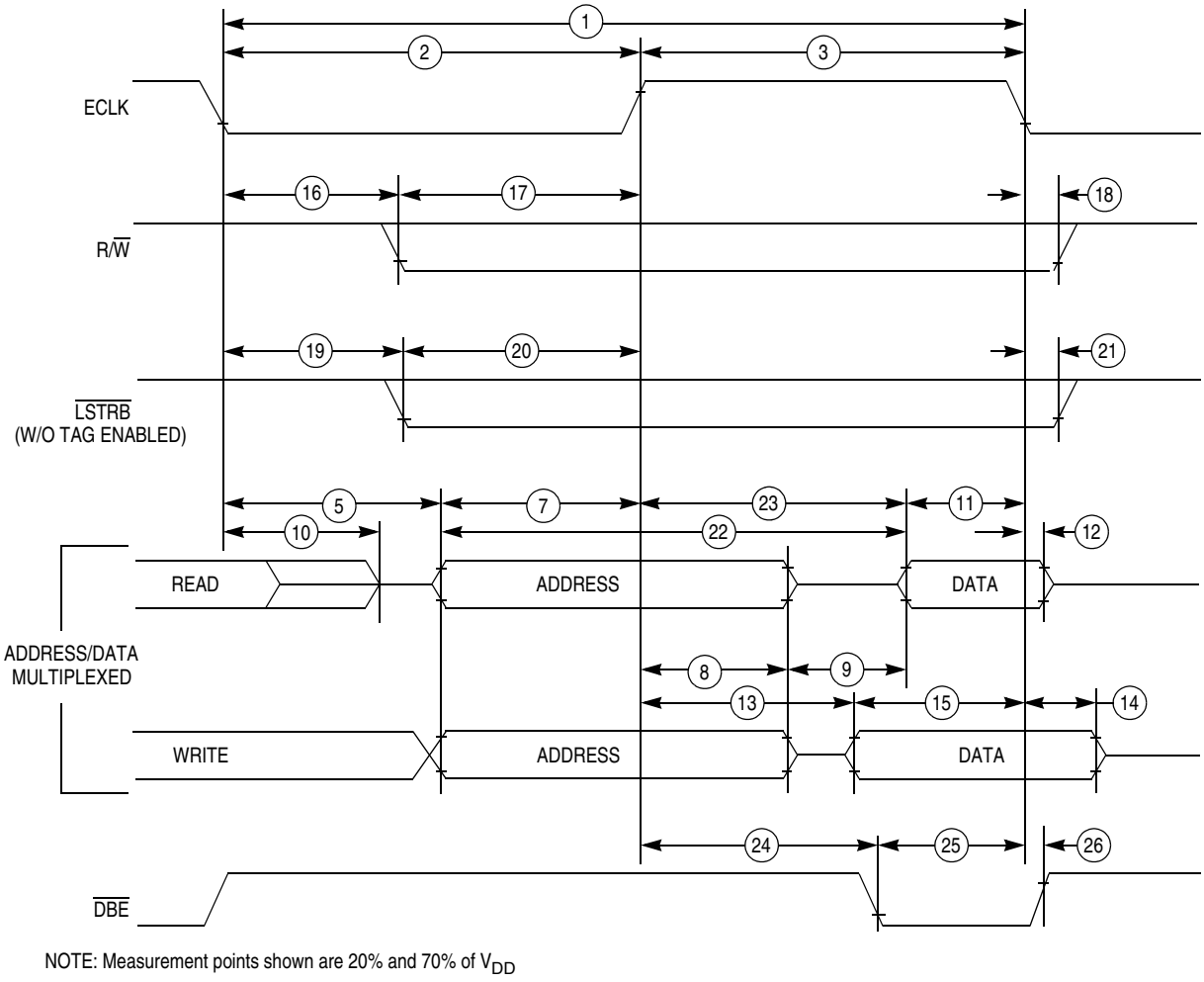
0 = BRKDL will not be used to compare to the address bus.
1 = BRKDL will be used to compare to the address bus.

Section 21. Electrical Specifications

21.1 Contents

21.2 Introduction

The MC68HC912DT128A microcontroller unit (MCU) is a16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (CPU12), 128-Kbyte flash EEPROM, 8K byte RAM, 2K byte EEPROM, two asynchronous serial communications interfaces (SCI), a serial peripheral interface (SPI), an 8-channel, 16-bit timer, two16-bit pulse accumulators and 16-bit down counter (ECT), two 10-bit analog-to-digital converter (ADC), a four-channel pulse-width modulator (PWM), an IIC interface module, and three MSCAN modules. The chip is the first 16-bit microcontroller to include both byte-erasable EEPROM and flash EEPROM on the same device. System resource mapping, clock generation, interrupt control and bus interfacing are managed by the Lite integration module (LIM). The MC68HC912DT128A has full 16-bit data paths throughout, however, the multiplexed external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems.



NOTE: Measurement points shown are 20% and 70% of V_{DD}

Figure 21-8. Multiplexed Expansion Bus Timing Diagram

In addition to the above general pieces of advice, the following guidelines should be followed for the CGM pins (but also more generally for any sensitive analog circuitry):

- Parasitic capacitance on EXTAL is absolutely critical – probably the most critical layout consideration. The XTAL pin is not as sensitive. All routing from the EXTAL pin through the resonator and the blocking cap to the actual connection to VSS must be considered.
- For minimum capacitance there should ideally be no ground / power plane around the EXTAL pin and associated routing. However, practical EMC considerations obviously should be taken into consideration for each application.
- The clock input circuitry is sensitive to noise so excellent supply routing and decoupling is mandatory. Connect the ground point of the oscillator circuit directly to the VSSPLL pin.
- Good isolation of PLL / Oscillator Power supply is critical. Use 1nF+ 100nF and keep tracks as low impedance as possible
- Load capacitors should be low leakage and stable across temperature – use NPO or C0G types.
- The load capacitors may ‘pull’ the target frequency by a few ppm. Crystal manufacturer specs show symmetrical values but the series device capacitance on EXTAL and XTAL are not symmetrical. It may be possible to adjust this by changing the values of the load capacitors – start-up conditions should be evaluated.
- Keep the adjacent Port H / Port E and RESET signals noise free. Don’t connect these to external signals and / or add series filtering – a series resistor is probably adequate.
- Any DC-blocking capacitor should be as low ESR as possible – for the range of crystals we are looking at anything over 1 Ohm is too much.
- Mount oscillator components on MCU side of board – avoid using vias in the oscillator circuitry.

Glossary