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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CPU12
Core Size	16-Bit
Speed	8MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc912dg128avpve

Table 3-4. Port Pull-Up, Pull-Down and Reduced Drive Summary

Port Name	Resistive Input Loads	Enable Bit			Reduced Drive Control Bit		
		Register (Address)	Bit Name	Reset State	Register (Address)	Bit Name	Reset State
Port IB[5:4](1)	Pull-up	IBPURD ($00E5)	PUPIB	Disabled	IBPURD ($00E5)	RDPIB	Full drive
Port AD0	None	—			—		
Port AD1	None	—			—		
Port CAN2[1](2)	None	—			—		
Port CAN2[0](2)	Pull-up	Always enabled			—		
Port CAN1[1]	None	—			—		
Port CAN1[0]	Pull-up	Always enabled			—		
Port CAN0[1]	None	—			—		
Port CAN0[0]	Pull-up	Always enabled			—		

1. MC68HC912DG128A only

2. MC68HC912DT128A only

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
$00A2	Bit 7	6	5	4	3	2	1	Bit 0	PACN3
$00A3	Bit 7	6	5	4	3	2	1	Bit 0	PACN2
$00A4	Bit 7	6	5	4	3	2	1	Bit 0	PACN1
$00A5	Bit 7	6	5	4	3	2	1	Bit 0	PACN0
$00A6	MCZI	MODMC	RDMCL	ICLAT	FLMC	MCEN	MCPR1	MCPR0	MCCTL
$00A7	MCZF	0	0	0	POLF3	POLF2	POLF1	POLF0	MCFLG
$00A8	0	0	0	0	PA3EN	PA2EN	PA1EN	PA0EN	ICPAR
$00A9	0	0	0	0	0	0	DLY1	DLY0	DLYCT
$00AA	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0	ICOVW
$00AB	SH37	SH26	SH15	SH04	TFMOD	PACMX	BUFEN	LATQ	ICSYS
$00AC	0	0	0	0	0	0	0	0	Reserved
$00AD	0	0	0	0	0	0	TCBYP	0	TIMTST
$00AE	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0	PORTT
$00AF	DDT7	DDT6	DDT5	DDT4	DDT3	DDT2	DDT1	DDT0	DDRT
$00B0	0	PBEN	0	0	0	0	PBOVI	0	PBCTL
$00B1	0	0	0	0	0	0	PBOVF	0	PBFLG
$00B2	Bit 7	6	5	4	3	2	1	Bit 0	PA3H
$00B3	Bit 7	6	5	4	3	2	1	Bit 0	PA2H
$00B4	Bit 7	6	5	4	3	2	1	Bit 0	PA1H
$00B5	Bit 7	6	5	4	3	2	1	Bit 0	PA0H
$00B6	Bit 15	14	13	12	11	10	9	Bit 8	MCCNTH
$00B7	Bit 7	6	5	4	3	2	1	Bit 0	MCCNTL
$00B8	Bit 15	14	13	12	11	10	9	Bit 8	TC0H
$00B9	Bit 7	6	5	4	3	2	1	Bit 0	TC0H
$00BA	Bit 15	14	13	12	11	10	9	Bit 8	TC1H
$00BB	Bit 7	6	5	4	3	2	1	Bit 0	TC1H
$00BC	Bit 15	14	13	12	11	10	9	Bit 8	TC2H
$00BD	Bit 7	6	5	4	3	2	1	Bit 0	TC2H
$00BE	Bit 15	14	13	12	11	10	9	Bit 8	TC3H
$00BF	Bit 7	6	5	4	3	2	1	Bit 0	TC3H
$00C0	BTST	BSPL	BRLD	SBR12	SBR11	SBR10	SBR9	SBR8	SC0BDH
$00C1	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	SC0BDL
$00C2	LOOPS	WOMS	RSRC	M	WAKE	ILT	PE	PT	SC0CR1
$00C3	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SC0CR2
$00C4	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF	SC0SR1
$00C5	0	0	0	0	0	0	0	RAF	SC0SR2
$00C6	R8	T8	0	0	0	0	0	0	SC0DRH
$00C7	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SC0DRL

Table 4-1. Register Map (Sheet 5 of 11)

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
$031A	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	C1IDAR6
$031B	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	C1IDAR7
$031C	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0	C1IDMR4
$031D	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0	C1IDMR5
$031E	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0	C1IDMR6
$031F	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0	C1IDMR7
$0320–$033C	Unimplemented(4)								Reserved
$033D	0	0	0	0	0	0	PUPCAN	RDPCAN	PCTLCAN1
$033E	PCAN7	PCAN6	PCAN5	PCAN4	PCAN3	PCAN2	TxCAN	RxCAN	PORTCAN1
$033F	DDCAN7	DDCAN6	DDCAN5	DDCAN4	DDCAN3	DDCAN2	0	0	DDRCAN1
$0340–$034F	FOREGROUND RECEIVE BUFFER 1								RxFG1
$0350–$035F	TRANSMIT BUFFER 10								Tx10
$0360–$036F	TRANSMIT BUFFER 11								Tx11
$0370–$037F	TRANSMIT BUFFER 12								Tx12
$0380-$03FF	Unimplemented(4)								Reserved

= Reserved or unimplemented bits.

Table 4-1. Register Map (Sheet 11 of 11)

1. Port A, port B and data direction registers DDRA, DDRB are not in map in expanded and peripheral modes.
2. Port E and DDRE not in the map in peripheral and expanded modes with EME set.
3. Registers also not in map in peripheral mode.
4. Data read at these locations is undefined.
5. The FPOPEN bit is available only on the 0L05H and later mask sets. For previous masks, this bit is reserved.
6. Port K and DDRK not in the map in peripheral and expanded modes with EMK set.
7. MC68HC912DT128A only. Locations are unimplemented on the MC68HC912DG128A.

Section 5. Operating Modes

5.1 Contents

5.2 Introduction

Eight possible operating modes determine the operating configuration of the MC68HC912DT128A. Each mode has an associated default memory map and external bus configuration.

5.3 Operating Modes

The operating mode out of reset is determined by the states of the BKGD, MODB, and MODA pins during reset.

The SMODN, MODB, and MODA bits in the MODE register show current operating mode and provide limited mode switching during operation. The states of the BKGD, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal.

A steady internal self-time clock is required to provide accurate counts to meet EEPROM program/erase requirements. This clock is generated via by a programmable 10-bit prescaler register. Automatic program/erase termination is also provided.

In ordinary situations, with crystal operating properly, the steady internal self-time clock is derived from the input clock source (EXTALi). The divider value is as in EEDIVH:EEDIVL. In limp-home mode, where the oscillator clock has malfunctioned or is unavailable, the self-time clock is derived from the PLL at a nominal f_{VCOMIN} using a predefined divider value of $0023. Program/erase operation is not guaranteed in limp-home mode.

CAUTION: *It is strongly recommended that program/erase operation is terminated in the event of loss of crystal, either by the application software (clearing EEPGM & EELAT bits) when entering limp home mode or by enabling the clock monitor to generate a clock monitor reset. This will prevent unnecessary stress on the emulated EEPROM during oscillator failure.*

9.5 EEPROM Control Registers

EEDIVH — EEPROM Modulus Divider **$00EE**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	0	0	EEDIV9	EEDIV8
RESET:	0	0	0	0	0	0	—(1)	—(1)

1. Loaded from SHADOW word.

EEDIVL — EEPROM Modulus Divider **$00EF**

	Bit 7	6	5	4	3	2	1	Bit 0
	EEDIV7	EEDIV6	EEDIV5	EEDIV4	EEDIV3	EEDIV2	EEDIV1	EEDIV0
RESET:	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)

1. Loaded from SHADOW word.

12.3 Clock Sources

A compatible external clock signal can be applied to the EXTAL pin or the MCU can generate a clock signal using an on-chip oscillator circuit and an external crystal or ceramic resonator. The MCU uses several types of internal clock signals derived from the primary clock signal:

TxCLK clocks are used by the CPU.

ECLK and PCLK are used by the bus interfaces, SPI, PWM, ATD0 and ATD1.

MCLK is either PCLK or XCLK, and drives on-chip modules such as SCI0, SCI1 and ECT.

XCLK drives on-chip modules such as RTI, COP and restart-from-stop delay time.

SLWCLK is used as a calibration output signal.

The MSCAN module is clocked by EXTALi or SYSCLK, under control of an MSCAN bit.

The clock monitor is clocked by EXTALi.

The BDM system is clocked by BCLK or ECLK, under control of a BDM bit.

A slow mode clock divider is included to deliver a lower clock frequency for the SCI baud rate generators, the ECT timer module, and the RTI and COP clocks. The slow clock bus frequencies divide the crystal frequency in a programmable range of 4 to 252, with steps of 4. This is very useful for low power operation.

See the Clock Divider Chains section for further details. Figure 12-1 shows some of the timing relationships.

Where the crystal start-up time is longer than the initial count of 4096 XCLK cycles, or in the absence of an external clock, the MCU recovers from STOP following the 4096 count in limp-home mode with both the LHOME flag set and the LHIF limp-home interrupt request set to indicate it is not operating at the desired frequency. Each time the 13-stage counter reaches a count of 4096 XCLK cycles, a check of the clock monitor status is performed.

When the presence of an external clock is detected, limp-home mode is exited and the LHOME flag is cleared. This sets the limp-home interrupt flag and if enabled by the LHIE bit, the limp-home mode interrupt is requested.

CAUTION: *The clock monitor circuit can be misled by EXTALi clock into reporting a good signal before it has fully stabilised. Under these conditions, improper EXTALi clock cycles can occur on SYSCLK. This may lead to a code runaway.*

12.6.7 STOP exit in Limp Home mode without Delay (Fast Stop Recovery)

(NOLHM=0, CME=X, DLY=0)

Fast STOP recovery refers to any exit from STOP using DLY=0.

If the NOLHM bit is cleared, then the CME (or FCME) bit is masked when a STOP instruction is executed to prevent a clock monitor failure. When coming out of STOP mode, the MCU goes into limp-home mode where CME and FCME signals are asserted.

When using a crystal oscillator, it is possible to exit STOP with the DLY bit cleared. In this case, STOP is de-asserted without delay and the MCU will execute software in limp-home mode, giving the crystal oscillator time to stablise.

CAUTION: *This mode is not recommended since the risk of the clock monitor detecting incorrect clocks is high.*

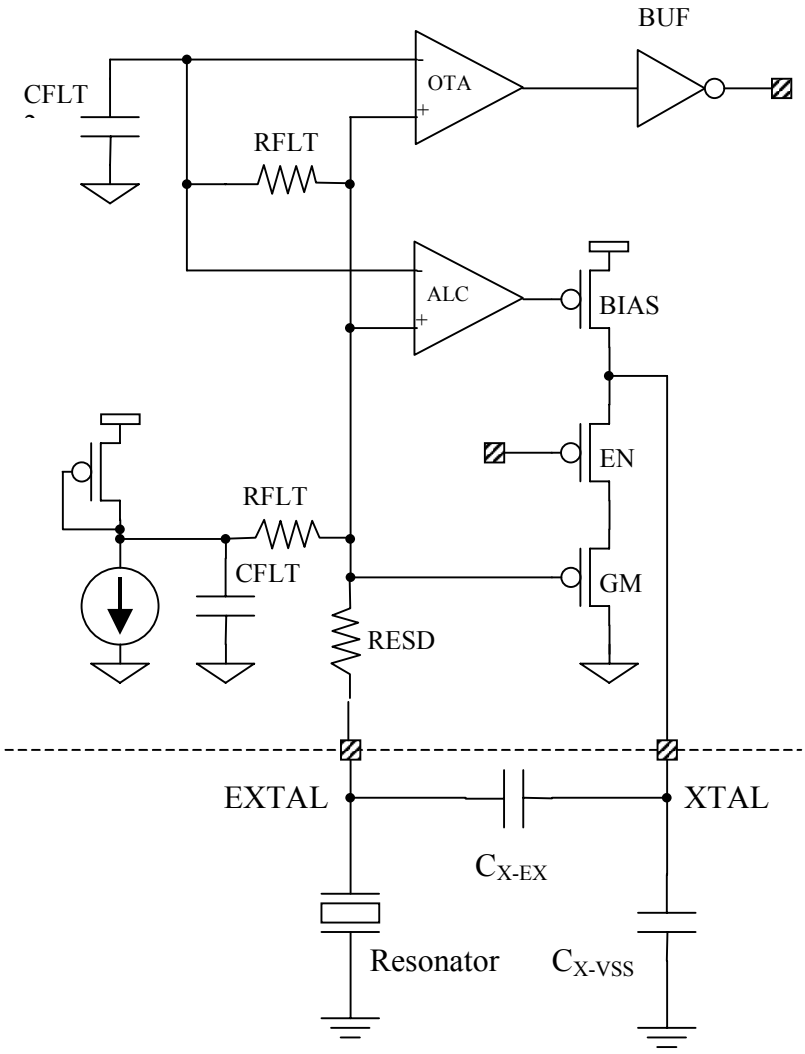

Figure 13-1. MC68HC912DT128A Colpitts Oscillator Architecture

13.3.2 MC68HC912DT128A Oscillator Design Guidelines

Proper and robust operation of the oscillator circuit requires excellent board layout design practice. Poor layout of the application board can contribute to EMC susceptibility, noise generation, slow starting oscillators, and reaction to noise on the clock input buffer. In addition to published errata for the MC68HC912DT128A, the following guidelines must be followed or failure in operation may occur.

- **Minimize Capacitance to VSS on EXTAL pin** — The Colpitts oscillator architecture is sensitive to capacitance in parallel with the resonator (from EXTAL to VSS). Follow these techniques:
  i. Remove ground plane from all layers around resonator and EXTAL route
  ii. Observe a minimum spacing from the EXTAL trace to all other traces of at least three times the design rule minimum (until the microcontroller's pin pitch prohibits this guideline)
  iii. Where possible, use XTAL as a shield between EXTAL and VSS
  iv. Keep EXTAL capacitance to less than 1pF (2pF absolute maximum)
- **Shield all oscillator components from all noisy traces** (while observing above guideline).
- **Keep the VSSPLL pin and the VSS reference to the oscillator as identical as possible**. Impedance between these signals must be minimum.
- **Observe best practice supply bypassing** on all MCU power pins. The oscillator's supply reference is VDD, not VDPLL.
- **Account for XTAL–VSS and EXTAL–XTAL parasitics in component values.**

NOTE: *An increase in the EXTAL–XTAL parasitic as a result of reducing EXTAL–VSS parasitic is acceptable provided component value is reduced by the appropriate value.*

- **Minimize XTAL and EXTAL routing lengths** to reduce EMC issues.

lower amplitude for the Pierce. The amplitude will still be sufficient for robust operation across process, temperature, and voltage variance.

13.5.1.2 Clock Buffer Hysteresis

The input clock buffer uses an Operational Transconductance Amplifier (labeled ‘OTA’ in the figure above) followed by a digital buffer to amplify the input signal on the EXTAL pin into a full-swing clock for use by the clock generation section of the microcontroller. There is an internal R-C filter (composed of components RFLT2 and CFLT2 in the figure above), which creates the DC value to which the EXTAL signal is compared. In this manner, the clock input buffer can track changes in the EXTAL DC offset voltage due to process variation as well as external factors such as leakage.

Because the purpose of the clock input buffer is to amplify relatively low-swing signals into a full-rail output, the gain of the OTA is very high. In the configuration shown, this means that very small levels of noise can be coupled onto the input of the clock buffer resulting in noise amplification.

To remedy this issue, hysteresis was added to the OTA so that the circuit could still provide the tolerance to leakage and the high gain required without the noise sensitivity. Approximately 150mV of hysteresis was added with a maximum hysteresis over process variation of 350mV. As such, the clock input buffer will not respond to input signals until they exceed the hysteresis level. At this point, the input signal due to oscillation will dominate the total input waveform and narrow clock pulses due to noise will be eliminated.

This circuit will limit the overall performance of the oscillator block only in cases where the amplitude of oscillation is less than the level of hysteresis. The minimum amplitude of oscillation is expected to be in excess of 750mV and the maximum hysteresis is expected to be less than 350mV, providing a factor of safety in excess of two.

RIE — Receiver Interrupt Enable

0 = RDRF and OR interrupts disabled, RAF interrupt in WAIT mode disabled

1 = SCI interrupt will be requested whenever the RDRF or OR status flag is set, or when RAF is set while in WAIT mode with VDDPLL high.

ILIE — Idle Line Interrupt Enable

0 = IDLE interrupts disabled

1 = SCI interrupt will be requested whenever the IDLE status flag is set.

TE — Transmitter Enable

0 = Transmitter disabled

1 = SCI transmit logic is enabled and the TXD pin (Port S bit 1/bit 3) is dedicated to the transmitter. The TE bit can be used to queue an idle preamble.

RE — Receiver Enable

0 = Receiver disabled

1 = Enables the SCI receive circuitry.

RWU — Receiver Wake-Up Control

0 = Normal SCI Receiver

1 = Enables the wake-up function and inhibits further receiver interrupts. Normally hardware wakes the receiver by automatically clearing this bit.

SBK — Send Break

0 = Break generator off

1 = Generate a break code (at least 10 or 11 contiguous zeros).

As long as SBK remains set the transmitter will send zeros. When SBK is changed to zero, the current frame of all zeros is finished before the TxD line goes to the idle state. If SBK is toggled on and off, the transmitter will send only 10 (or 11) zeros and then revert to mark idle or sending data.

19.2.1 Features

- 8/10 Bit Resolution
- 10 μs, 10-Bit Single Conversion Time
- Sample and Transfer Buffer Amplifier
- Programmable Sample Time
- Left/Right Justified Result Data
- Conversion Completion Interrupt
- Analog Input Multiplexer for 8 Analog Input Channels
- Analog/Digital Input Pin Multiplexing
- 1, 4, 8 Conversion Sequence Lengths
- Continuous Conversion Mode
- Multiple Channel Scans

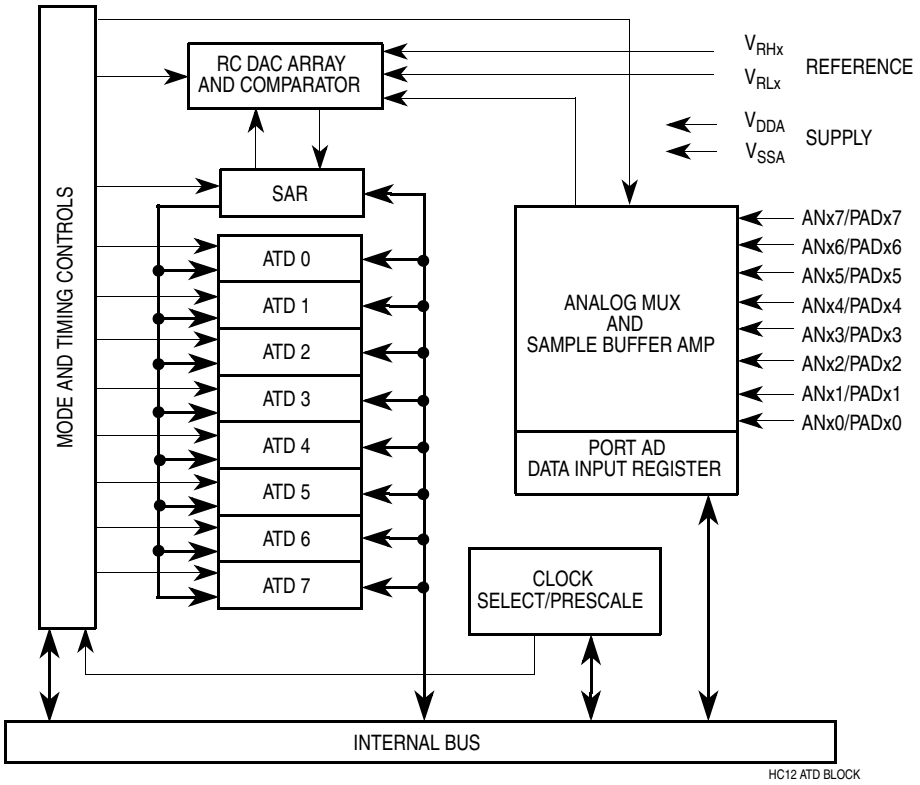

Figure 19-1. Analog-to-Digital Converter Block Diagram

programmable constant in order to generate the ATD module's internal clock. One additional benefit of the prescaled clock feature is that it allows the user further control over the sample period (note that changing the module clock also affects conversion time).

The prescaler is based on a 5 bit modulus counter and divides the PCLK by an integer value between 1 and 32. The final clock frequency is obtained with a further division by 2.

The internal ATD module clock and the system PCLK have a direct phase relationship, however the ATD module operates as if it is effectively asynchronous to MCU bus clock cycles.

19.5 ATD Operational Modes

19.5.1 Power Down Mode

The ATD module can be powered down under program control. This is done by turning the clock signals off to the digital electronics of the module and eliminating the quiescent current draw of the analog electronics.

Power down control is implemented in one of three ways.

1. Using the ADPU bit in control register ATDCTL2.
2. When STOP instruction is executed, the module will power down for the duration of the STOP function.
3. If the module WAIT enable bit (ASWAI) is set and a WAIT instruction is executed, the module will power down for the duration of the WAIT function.

Note that the reset default for the ADPU bit is zero. Therefore, when this module is reset, it is reset into the power down state.

Once the command to power down has been received, the ATD module aborts any conversion sequence in progress and enters lower power mode. When the module is powered up again, the bias settings in the analog electronics must be given time to stabilize before conversions

19.9.5 ATDSTAT A/D Status Register

The ATD Status registers contain the conversion complete flags and the conversion sequence counter. The status registers are read-only.

ATD0STAT0/ATD1STAT0 — ATD Status Register **$0066/$01E6**

	Bit 7	6	5	4	3	2	1	Bit 0
	SCF	0	0	0	0	CC2	CC1	CC0
RESET:	0	0	0	0	0	0	0	0

ATD0STAT1/ATD1STAT1 — ATD Status Register **$0067/$01E7**

	Bit 7	6	5	4	3	2	1	Bit 0
	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
RESET:	0	0	0	0	0	0	0	0

SCF — Sequence Complete Flag

This flag is set upon completion of a conversion sequence. If conversion sequences are continuously performed (SCAN=1), the flag is set after each one is completed. How this flag is cleared depends on the setting of the fast flag clear bit. When AFFC=0, SCF is cleared when a new conversion sequence is initiated (write to register ATDCTL4/5). When AFFC=1, SCF is cleared after reading the first (any) result register.

CC[2:0] — Conversion Counter

This 3-bit value represents the contents of the result register counter; the result register counter points to the result register that will receive the result of the current conversion. If not in FIFO mode, the register counter is initialized to zero when a new conversion sequence is begun.

If in FIFO mode, the register counter is not initialized. The result register count wraps around when its maximum value is reached.

CCF[7:0] — Conversion Complete Flags

A conversion complete flag is set at the end of each conversion in a conversion sequence. The flags are associated with the conversion position in a sequence and the result register number. Therefore, CCF0 is set when the first conversion in a sequence is complete and

Table 20-1. IPIPE Decoding

Data Movement — IPIPE[1:0] Captured at Rising Edge of E Clock(1)		
IPIPE[1:0]	**Mnemonic**	**Meaning**
0:0	—	No Movement
0:1	LAT	Latch Data From Bus
1:0	ALD	Advance Queue and Load From Bus
1:1	ALL	Advance Queue and Load From Latch
Execution Start — IPIPE[1:0] Captured at Falling Edge of E Clock(2)		
IPIPE[1:0]	**Mnemonic**	**Meaning**
0:0	—	No Start
0:1	INT	Start Interrupt Sequence
1:0	SEV	Start Even Instruction
1:1	SOD	Start Odd Instruction

1. Refers to data that was on the bus at the previous E falling edge.
2. Refers to bus cycle starting at this E falling edge.

Program information is fetched a few cycles before it is used by the CPU. In order to monitor cycle-by-cycle CPU activity, it is necessary to externally reconstruct what is happening in the instruction queue. Internally the MCU only needs to buffer the data from program fetches. For system debug it is necessary to keep the data and its associated address in the reconstructed instruction queue. The raw signals required for reconstruction of the queue are ADDR, DATA, R/$\overline{W}$, ECLK, and status signals IPIPE[1:0].

The instruction queue consists of two 16-bit queue stages and a holding latch on the input of the first stage. To advance the queue means to move the word in the first stage to the second stage and move the word from either the holding latch or the data bus input buffer into the first stage. To start even (or odd) instruction means to execute the opcode in the high-order (or low-order) byte of the second stage of the instruction queue.

DATA — Data Flag - Shows that data accompanies the command.
0 = No data
1 = Data follows the command

R/W — Read/Write Flag
0 = Write
1 = Read

BKGND — Hardware request to enter active background mode
0 = Not a hardware background command
1 = Hardware background command (INSTRUCTION = $90)

W/B — Word/Byte Transfer Flag
0 = Byte transfer
1 = Word transfer

BD/U — BDM Map/User Map Flag

Indicates whether BDM registers and ROM are mapped to addresses $FF00 to $FFFF in the standard 64-Kbyte address space. Used only by hardware read/write commands.
0 = BDM resources not in map
1 = BDM ROM and registers in map

INSTRUCTION — BDM Instruction Register (firmware command bit explanation) **$FF00**

Bit 7	6	5	4	3	2	1	Bit 0
H/F	DATA	R/W	TTAGO		REGN		

The bits in the BDM instruction register have the following meanings when a **firmware** command is executed.

H/F — Hardware/Firmware Flag
0 = Firmware command
1 = Hardware command

DATA — Data Flag – Shows that data accompanies the command.
0 = No data
1 = Data follows the command

20.5.1 Breakpoint Modes

Three modes of operation determine the type of breakpoint in effect.

- Dual address-only breakpoints, each of which will cause a software interrupt (SWI)
- Single full-feature breakpoint which will cause the part to enter background debug mode (BDM)
- Dual address-only breakpoints, each of which will cause the part to enter BDM

Breakpoints will not occur when BDM is active.

20.5.1.1 SWI Dual Address Mode

In this mode, dual address-only breakpoints can be set, each of which cause a software interrupt. This is the only breakpoint mode which can force the CPU to execute a SWI. Program fetch tagging is the default in this mode; data breakpoints are not possible. In the dual mode each address breakpoint is affected by the BKPM bit and the BKALE bit. The BKxRW and BKxRWE bits are ignored. In dual address mode the BKDBE becomes an enable for the second address breakpoint. The BKSZ8 bit will have no effect when in a dual address mode.

20.5.1.2 BDM Full Breakpoint Mode

A single full feature breakpoint which causes the part to enter background debug mode. BDM mode may be entered by a breakpoint only if an internal signal from the BDM indicates background debug mode is enabled.

- Breakpoints are not allowed if the BDM mode is already active. Active mode means the CPU is executing out of the BDM ROM.
- BDM should not be entered from a breakpoint unless the ENABLE bit is set in the BDM. This is important because even if the ENABLE bit in the BDM is negated the CPU actually does execute the BDM ROM code. It checks the ENABLE and returns if not set. If the BDM is not serviced by the monitor then the breakpoint would be re-asserted when the BDM returns to normal CPU flow.

to be set by programming an 10-bit time base pre-scalar into bits spread over two new registers, EEDIVH and EEDIVL.

The EEDIVH and EEDIVL registers are volatile. However, they are loaded upon reset by the contents of the non-volatile SHADOW word much in the same way as the EEPROM module control register (EEMCR) bits interact with the SHADOW word for configuration control on the existing revision.

22.2.2.3 EEPROM AUTO programming & erasing

The second major change to the EEPROM is the inclusion in the EEPROM control register (EEPROG) of an AUTO function using the previously unused bit 5 of this register.

The AUTO function enables the logic of the MCU to automatically use the optimum programming or erasing time for the EEPROM. If using AUTO, the user does not need to wait for the normal minimum specified programming or erasing time. After setting the EEPGM bit as normal the user just has to poll that bit again, waiting for the MCU to clear it indicating that programming or erasing is complete.

22.2.2.4 EEPROM Selective Write More Zeros

For some applications it may be advantageous to track more than 10k events with a single byte of EEPROM by programming one bit at a time. For that purpose, a special selective bit programming technique is available.

When this technique is utilized, a program / erase cycle is defined as multiple writes (up to eight) to a unique location followed by a single erase sequence.

22.2.3 STOP mode

This new version will correctly exit STOP mode without having to synchronize the start of STOP with the RTI clock.

22.2.4 WAIT mode

This new version will correctly exit WAIT mode using short XIRQ or IRQ inputs.

22.2.5 KWU Filter

The KWU filter will now ignore pulses shorter than 2 microseconds.

22.2.6 Port ADx

Power must be applied to VDDA at all times even if the ADC is not being used. This is necessary for port AD0 and port AD1 to function correctly as digital inputs.

22.2.7 ATD

22.2.7.1 Channel Selection

Any channel can be selected for the first conversion of a multiple channel conversion. Bits CA, CB & CC in ATDxCTL5 do not get masked but are used to select which channel is used to start the sequential conversion sequence. **For compatibilty, ensure that the appropriate bits are cleared in the software.** See Table 19-8.

Bit CC of ATDxCTL5 is not masked when bit S8CM = 1.

22.2.7.2 CD bit

Bit CD in ATDxCTL5 is renamed SC to differentiate it from extended functionality of bits CA, CB & CC. Functionality is unchanged as it still selects conversion from the internal reference sources but when doing a multiple channel scan, bits CA, CB & CC must be cleared as appropriate for compatible reference selection.

The filter components values are chosen from standard series (e.g. E12 for resistors). The operating voltage is assumed to be 5V (although there is only a minor difference between 3V and 5V operation). The smoothing capacitor Cp in parallel with R and C is set to be 1/10 of the value of C. The reference frequencies mentioned in this table correspond to the output of the fine granularity divider controlled by the REFDV register. This means that the calculations are irrespective of the way the reference frequency is generated (directly for the crystal oscillator or after division). The target frequency value also has an influence on the calculations of the filter components because the VCO gain is NOT constant over its operating range.

The bandwidth limit corresponds to the so-called Gardner's criteria. It corresponds to the maximum value that can be chosen before the continuous time approximation ceases to be justified. It is of course advisable to stay far away from this limit.