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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CPU12
Core Size	16-Bit
Speed	8MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	67
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc912dt128acpve

Section 3. Pinout and Signal Descriptions

Section 4. Registers

Section 5. Operating Modes

Section 6. Resource Mapping

List of Tables

- Memory
  - 128K byte flash EEPROM, made of four 32K byte modules with 8K bytes protected BOOT section in each module
  - 2K byte EEPROM
  - 8K byte RAM with Vstby, made of two 4K byte modules.
- Two Analog-to-digital converters
  - 2 times 8-channels, 10-bit resolution
- Three 1M bit per second, CAN 2.0 A, B software compatible modules on the MC68HC912DT128A (two on the MC68HC912DG128A)
  - Two receive and three transmit buffers per CAN
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up per CAN
  - Low-pass filter wake-up function
  - Loop-back for self test operation
  - Programmable link to a timer input capture channel, for time-stamping and network synchronization.
- Enhanced capture timer (ECT)
  - 16-bit main counter with 7-bit prescaler
  - 8 programmable input capture or output compare channels; 4 of the 8 input captures with buffer
  - Input capture filters and buffers, three successive captures on four channels, or two captures on four channels with a capture/compare selectable on the remaining four
  - Four 8-bit or two 16-bit pulse accumulators
  - 16-bit modulus down-counter with 4-bit prescaler
  - Four user-selectable delay counters for signal filtering

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
$004C	Bit 7	6	5	4	3	2	1	Bit 0	PWPER0
$004D	Bit 7	6	5	4	3	2	1	Bit 0	PWPER1
$004E	Bit 7	6	5	4	3	2	1	Bit 0	PWPER2
$004F	Bit 7	6	5	4	3	2	1	Bit 0	PWPER3
$0050	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY0
$0051	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY1
$0052	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY2
$0053	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY3
$0054	0	0	0	PSWAI	CENTR	RDPP	PUPP	PSBCK	PWCTL
$0055	DISCR	DISCP	DISCAL	0	0	0	0	0	PWTST
$0056	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0	PORTP
$0057	DDP7	DDP6	DDP5	DDP4	DDP3	DDP2	DDP1	DDP0	DDRP
$0058-$005F	0	0	0	0	0	0	0	0	Reserved
$0060	Reserved								ATD0CTL0
$0061	Reserved								ATD0CTL1
$0062	ADPU	AFFC	ASWAI	DJM	DSGN	Reserved	ASCIE	ASCIF	ATD0CTL2
$0063	0	0	0	0	S1C	FIFO	FRZ1	FRZ0	ATD0CTL3
$0064	RES10	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0	ATD0CTL4
$0065	0	S8C	SCAN	MULT	CD	CC	CB	CA	ATD0CTL5
$0066	SCF	0	0	0	0	CC2	CC1	CC0	ATD0STAT0
$0067	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0	ATD0STAT1
$0068	SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2	ATD0TESTH
$0069	SAR1	SAR0	RST	TSTOUT	TST3	TST2	TST1	TST0	ATD0TESTL
$006A–$006E	0	0	0	0	0	0	0	0	Reserved
$006F	PAD07	PAD06	PAD05	PAD04	PAD03	PAD02	PAD01	PAD00	PORTAD0
$0070	Bit 15	14	13	12	11	10	9	Bit 8	ADR00H
$0071	Bit 7	Bit 6	0	0	0	0	0	0	ADR00L
$0072	Bit 15	14	13	12	11	10	9	Bit 8	ADR01H
$0073	Bit 7	Bit 6	0	0	0	0	0	0	ADR01L
$0074	Bit 15	14	13	12	11	10	9	Bit 8	ADR02H
$0075	Bit 7	Bit 6	0	0	0	0	0	0	ADR02L
$0076	Bit 15	14	13	12	11	10	9	Bit 8	ADR03H
$0077	Bit 7	Bit 6	0	0	0	0	0	0	ADR03L
$0078	Bit 15	14	13	12	11	10	9	Bit 8	ADR04H
$0079	Bit 7	Bit 6	0	0	0	0	0	0	ADR04L
$007A	Bit 15	14	13	12	11	10	9	Bit 8	ADR05H
$007B	Bit 7	Bit 6	0	0	0	0	0	0	ADR05L

Table 4-1. Register Map (Sheet 3 of 11)

Section 6. Resource Mapping

6.1 Contents

6.2 Introduction

After reset, most system resources can be mapped to other addresses by writing to the appropriate control registers.

6.3 Internal Resource Mapping

The internal register block, RAM, and EEPROM have default locations within the 64K byte standard address space but may be reassigned to other locations during program execution by setting bits in mapping registers INITRG, INITRM, and INITEE. During normal operating modes these registers can be written once. It is advisable to explicitly establish these resource locations during the initialization phase of program execution, even if default values are chosen, in order to protect the registers from inadvertent modification later.

Writes to the mapping registers go into effect between the cycle that follows the write and the cycle after that. To assure that there are no

Resource Mapping

PEAR — Port E Assignment Register **$000A**

	BIT 7	6	5	4	3	2	1	BIT 0	
	NDBE	CGMTE	PIPOE	NECLK	LSTRE	RDWE	CALE	DBENE	
RESET:	0	0	0	0	0	0	0	0	Normal Expanded
RESET:	0	0	1	0	1	1	0	0	Special Expanded
RESET:	1	1	0	1	0	0	0	0	Peripheral
RESET:	1	0	0	1	0	0	0	0	Normal single chip
RESET:	0	0	1	0	1	1	0	0	Special single chip

Port E serves as general purpose I/O lines or as system and bus control signals. The PEAR register is used to choose between the general-purpose I/O functions and the alternate bus control functions. When an alternate control function is selected, the associated DDRE bits are overridden.

The reset condition of this register depends on the mode of operation because bus control signals are needed immediately after reset in some modes.

In normal single-chip mode, no external bus control signals are needed so all of port E is configured for general-purpose I/O.

In normal expanded modes, the reset vector is located in external memory. The $\overline{DBE}$ and E clock are required for de-multiplexing address and data but $\overline{LSTRB}$ and R/$\overline{W}$ are only needed by the system when there are external writable resources. Therefore in normal expanded modes, the $\overline{DBE}$ and the E clock are configured for their alternate bus control functions and the other bits of port E are configured for general-purpose I/O. If the normal expanded system needs any other bus control signals, PEAR would need to be written before any access that needed the additional signals.

In special expanded modes, $\overline{DBE}$, IPIPE1, IPIPE0, E, $\overline{LSTRB}$, and R/$\overline{W}$ are configured as bus-control signals.

In special single chip modes, $\overline{DBE}$, IPIPE1, IPIPE0, E, $\overline{LSTRB}$, R/$\overline{W}$, and CALE are configured as bus-control signals.

In peripheral mode, the PEAR register is not accessible for reads or writes. However, the CGMTE control bit is reset to one to configure PE6 as a test output for the CGM module.

NDBE — No Data Bus Enable

Normal: write once; Special: write anytime EXCEPT the first. Read anytime.

0 = PE7 is used for $\overline{\text{DBE}}$, external control of data enable on memories, or inverted E clock.

1 = PE7 is CAL function if CALE bit is set in PEAR register or general-purpose I/O otherwise.

The NDBE bit has no effect in Single Chip or Peripheral Modes and PE7 is defaulted to the CAL function if CALE bit is set in PEAR register or to an I/O otherwise.

CGMTE — Clock Generator Module Testing Enable

Normal: write never; Special: write anytime EXCEPT the first time. Read anytime.

0 = PE6 is general-purpose I/O or pipe output.

1 = PE6 is a test signal output from the CGM module (no effect in single chip or normal expanded modes). PIPOE = 1 overrides this function and forces PE6 to be a pipe status output signal.

PIPOE — Pipe Status Signal Output Enable

Normal: write once; Special: write anytime EXCEPT the first time. Read anytime.

0 = PE[6:5] are general-purpose I/O (if CGMTE = 1, PE6 is a test output signal from the CGM module).

1 = PE[6:5] are outputs and indicate the state of the instruction queue (only effective in expanded modes).

NECLK — No External E Clock

Normal single chip: write once; special single chip: write anytime; all other modes: write never.

Read anytime. In peripheral mode, E is an input and in all other modes, E is an output.

VCO clock at its minimum frequency, f_{VCOMIN}, is provided as the system clock, allowing the MCU to continue operating.

The MCU is said to be operating in **"limp-home" mode** with the forced VCO clock as the system clock. PLLON and BCSP ('bus clock select PLL') signals are forced high and the MCS ('module clock select') signal is forced low. The LHOME flag in the PLLFLG register is set to indicate that the MCU is running in limp-home mode. A change of this flag sets the limp-home interrupt flag, LHIF, and if enabled by the LHIE bit, the limp-home mode interrupt is requested. The Clock Monitor is enabled irrespective of CME and FCME bit settings. Module clocks to the RTI & COP (XCLK), BDM (BCLK) and ECT & SCI (MCLK) are forced to be PCLK (at f_{VCOMIN}) and ECLK is also equal to f_{VCOMIN}. MSCAN clock select is unaffected.

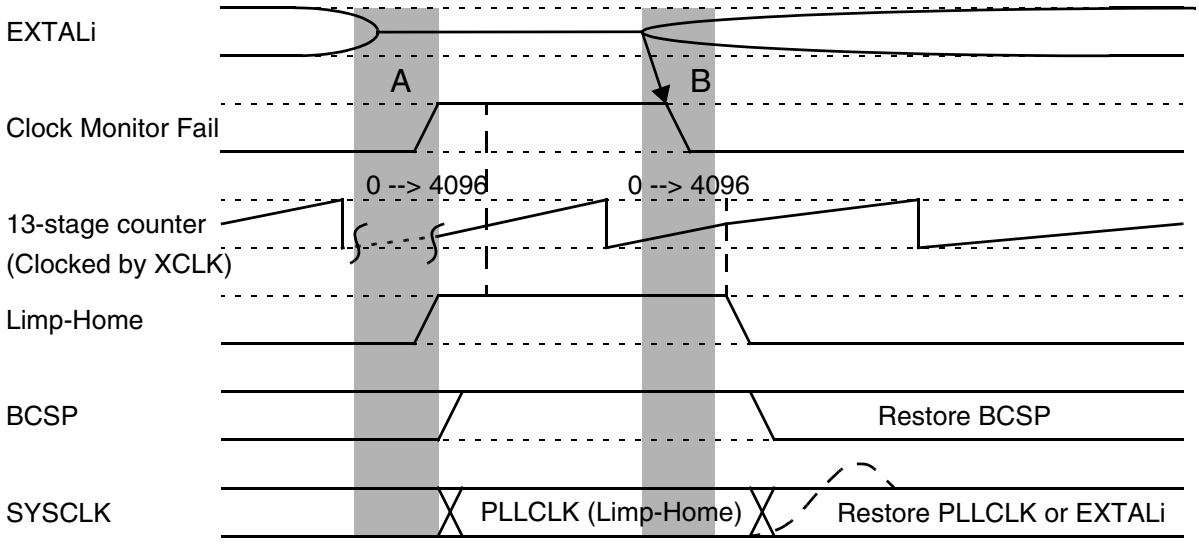

Figure 12-3. Clock Loss during Normal Operation

The clock monitor is polled each time the 13-stage free running counter reaches a count of 4096 XCLK cycles i.e. mid-count, hence the clock status gets checked once every 8192 XCLK cycles. When the presence of an external clock is detected, the MCU exits limp-home mode, clearing the LHOME flag and setting the limp-home interrupt flag. Upon leaving limp-home mode, BCSP and MCS signals are restored to their

. .

Table 12-1. Summary of STOP Mode Exit Conditions

Mode	Conditions	Summary
STOP exit without Limp Home mode, clock monitor disabled	NOLHM=1 CME=0 DLY=X	Oscillator must be stable within 4096 XCLK cycles. XCLK can be modified by SLOW divider register. Use of DLY=0 only recommended with external clock.
Executing the STOP instruction without Limp Home mode, clock monitor enabled	NOLHM=1 CME=1 DLY=X	When a STOP instruction is executed the MCU resets via the clock monitor reset vector.
STOP exit in Limp Home mode with Delay	NOLHM=0 CME=X DLY=1	Oscillator must be stable within 4096 f_{VCOMIN} cycles or there is a possibility of code runaway as the clock monitor circuit can be misled by EXTALi clock into reporting a good signal before it has fully stabilised
STOP exit in Limp Home mode without Delay (Fast Stop Recovery)	NOLHM=0 CME=X DLY=0	This mode is only recommended for use with an external clock source.

Table 12-2. Summary of Pseudo STOP Mode Exit Conditions

Mode	Conditions	Summary
Pseudo-STOP exit in Limp Home mode with Delay	NOLHM=0 CME=X DLY=1	CPU exits stop in limp home mode and oscillator running. If the oscillator fails during pseudo-STOP and then recovers there is a possibility of code runaway as the clock monitor circuit can be misled by EXTALi clock into reporting a good signal before it has fully stabilised
Pseudo-STOP exit in Limp Home mode without Delay (Fast Stop Recovery)	NOLHM=0 CME=X DLY=0	This mode is not recommended as it is possible that the initial VCO clock frequency may be high enough to cause code runaway.
Pseudo-STOP exit without Limp Home mode, clock monitor enabled	NOLHM=1 CME=1 DLY=X	When a STOP instruction is executed the MCU resets via the clock monitor reset vector.
Pseudo-STOP exit without Limp Home mode, clock monitor disabled, with Delay	NOLHM=1 CME=0 DLY=1	Oscillator starts operation following 4096 XCLK cycles (actual controlled by SLOW mode divider).
Pseudo-STOP exit without Limp Home mode, clock monitor disabled, without Delay	NOLHM=1 CME=0 DLY=0	This mode is only recommended for use with an external clock source.

Technical Data — MC68HC912DT128A

Section 13. Oscillator

13.1 Contents

13.2 Introduction

The oscillator implementation on the original 0.65µ (non-suffix) HC12 D-family is a ‘Colpitts Oscillator with Translated Ground’. This design was carried over to the first 0.5µ devices (A-suffix), up to the 0L05H mask set, and is described in Section 13.3 MC68HC912DT128A Oscillator Specification. In this section of the document, the term MC68HC912DT128A refers only to the MC68HC912DT128A and MC68HC912DG128A devices.

On mask set 1L05H, the Colpitts oscillator was updated, primarily to improve its performance. To maximise the benefit of this change, different external component values are required. However, the oscillator will perform at least as well as the MC68HC912DT128A version with the same components. This implementation and the changes are described in section 13.4 MC68HC912Dx128C Colpitts Oscillator Specification. In this section of the document, the term MC68HC912Dx128C refers only to the MC68HC912DT128C and MC68HC912DG128C devices.

In order to make the HC12 D-family oscillator options more flexible, a Pierce oscillator configuration has been implemented on the 2L05H

Similarly, if meeting a traditional NRM optimization criteria is important, then the components determined by this method are acceptable if the same components yield a maximum allowed ESR greater than the maximum ESR of the crystal while maintaining the worst case Gain Margin of 2. There is no guarantee that components chosen through traditional NRM optimization techniques will yield acceptable results across all expected variations.

13.4.2.4 Key Parameters

The following items are of critical importance to the operation of the oscillator:

- **EXTAL–XTAL capacitor value** — The value of the component plus external (board) parasitic in excess of 0.1pF between EXTAL and XTAL.
- **XTAL–VSS capacitor value** — The value of the component plus external (board) parasitic in excess of 1.0pF between XTAL and VSS.
- **Maximum Shunt Capacitance** — The maximum value of the resonator's shunt capacitance (C0) plus the external (board) parasitics in excess of 1pF from EXTAL to VSS.
- **VDDPLL Setting** — The Voltage applied to the VDDPLL pin (Logic 1 means VDDPLL is tied to the same potential as VDD).
- **Resonator Frequency** — The frequency of oscillation of the resonator.
- **Maximum ESR** — The maximum effective series resistance (ESR) of the resonator. This figure must include any increases due to ageing, power dissipation, temperature, process variation or particle contamination.

possible to know where the count is with respect to the duty value and software can be used to make adjustments by turning the enable bit off and on.

The four PWM channel outputs share general-purpose port P pins. Enabling PWM pins takes precedence over the general-purpose port. When PWM are not in use, the port pins may be used for discrete input/output.

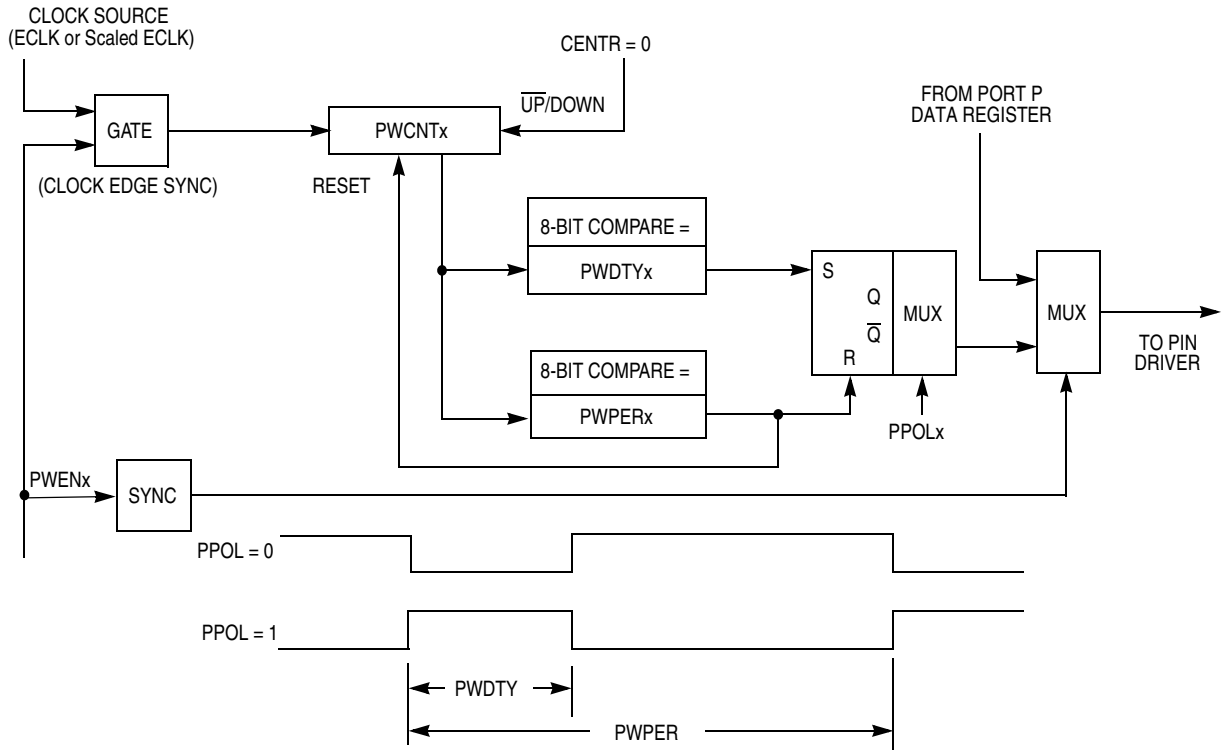

Figure 14-1. Block Diagram of PWM Left-Aligned Output Channel

PAxEN — 8-Bit Pulse Accumulator ‘x’ Enable
0 = 8-Bit Pulse Accumulator is disabled.
1 = 8-Bit Pulse Accumulator is enabled.

DLYCT — Delay Counter Control Register **$00A9**

	BIT 7	6	5	4	3	2	1	BIT 0
	0	0	0	0	0	0	DLY1	DLY0
RESET:	0	0	0	0	0	0	0	0

Read or write any time.

If enabled, after detection of a valid edge on input capture pin, the delay counter counts the pre-selected number of M clock (module clock) cycles, then it will generate a pulse on its output. The pulse is generated only if the level of input signal, after the preset delay, is the opposite of the level before the transition.This will avoid reaction to narrow input pulses.

After counting, the counter will be cleared automatically.

Delay between two active edges of the input signal period should be longer than the selected counter delay.

DLYx — Delay Counter Select

DLY1	DLY0	Delay
0	0	Disabled (bypassed)
0	1	256M clock cycles
1	0	512M clock cycles
1	1	1024 M clock cycles

ICOVW — Input Control Overwrite Register **$00AA**

	BIT 7	6	5	4	3	2	1	BIT 0
	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0
RESET:	0	0	0	0	0	0	0	0

Read or write any time.

some slave devices are very simple and either accept data from the master without returning data to the master or pass data to the master without requiring data from the master.

16.6 Port S

In all modes, port S bits PS[7:0] can be used for either general-purpose I/O, or with the SCI and SPI subsystems. During reset, port S pins are configured as high-impedance inputs (DDRS is cleared).

PORTS — Port S Data Register **$00D6**

	Bit 7	6	5	4	3	2	1	Bit 0
	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0
MSI	$\overline{SS}$ $\overline{CS}$	SCK	MOSI MOMI	MISO SISO	TXD1	RXD1	TXD0	RXD0
RESET:	-	-	-	-	-	-	-	-

Read anytime (inputs return pin level; outputs return pin driver input level). Write data stored in internal latch (drives pins only if configured for output). Writes do not change pin state when pin configured for SPI or SCI output.

After reset all bits are configured as general-purpose inputs.

Port S shares function with the on-chip serial systems (SPI and SCI0/1).

DDRS — Data Direction Register for Port S **$00D7**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDS7	DDS6	DDS5	DDS4	DDS3	DDS2	DDS1	DDS0
RESET:	0	0	0	0	0	0	0	0

Read or write anytime.
After reset, all general-purpose I/O are configured for input only.

0 = Configure the corresponding I/O pin for input only
1 = Configure the corresponding I/O pin for output

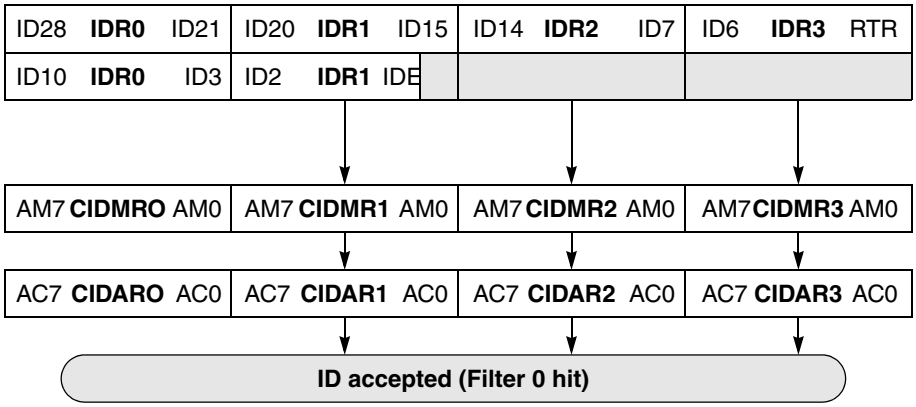

Figure 18-3. 32-bit Maskable Identifier Acceptance Filters

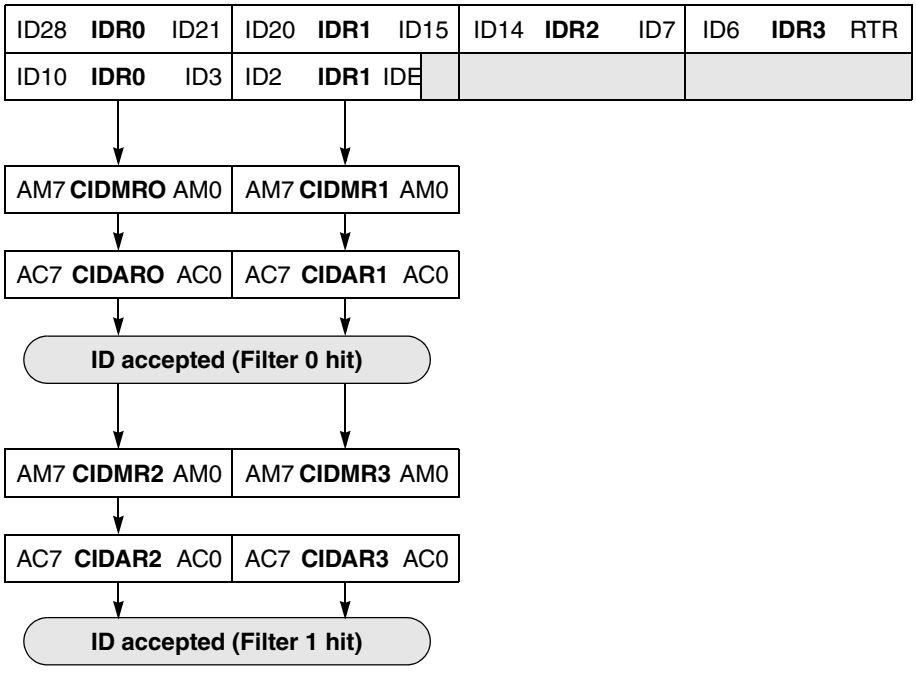

Figure 18-4. 16-bit Maskable Acceptance Filters

exited, the ATD module powers up and continues operation. The module is not reset; the register file is not reinitialized; the conversion sequence is not restarted.

When the module comes out of wait, it is recommended that a stabilization delay (t_{SR}) is allowed before new conversions are started.

DJM — Result Register Data Justification Mode

0 = Left justified mode

1 = Right justified mode

For 10-bit resolution, left justified mode maps a result register into data bus bits 6 through 15; bit 15 is the MSB. In right justified mode, the result registers maps onto data bus bits 0 through 9; bit 9 is the MSB.

For 8-bit resolution, left justified mode maps a result into the high byte (bits 8 though 15; bit 15 is the MSB). Right justified maps a result into the low byte (bits 0 through 7; bit 7 is the MSB).

Table 19-1 summarizes the result data formats available and how they are set up using the control bits.

Table 19-2 illustrates left justified output codes for an input signal range between 0 and 5.1 Volts.

RES10	DJM	Result Data Formats Description and Bus Bit Mapping
0	0	8-bit/left justified - bits 8-15
0	1	8-bit/right justified - bits 0-7
1	0	10-bit/left justified - bits 6-15
1	1	10-bit/right justified - bits 0-9

Table 19-1. Result Data Formats Available

Input Signal Vrl = 0 Volts Vrh = 5.12 Volts	8-Bit Codes	10-Bit Codes
5.120 Volts	FF	FFC0
5.100	FF	FF00
5.080	FE	FE00
2.580	81	8100
2.560	80	8000
2.540	7F	7F00
0.020	01	0100
0.000	00	0000

Table 19-2. Left Justified ATD Output Codes

ASCIE — ATD Sequence Complete Interrupt Enable

0 = Disables ATD interrupt

1 = Enables ATD interrupt on Sequence Complete

The sequence complete interrupt function signals the MCU when a conversion sequence is complete. At this time, the result registers contain the result data generated by the conversion sequence. If this interrupt function is disabled, then the conversion complete flags must be polled to determine when a conversion or a conversion sequence is complete. Note that reset clears pending interrupts.

ASCIF — ATD Sequence Complete Interrupt Flag

0 = No ATD sequence complete interrupt occurred

1 = ATD sequence complete interrupt occurred

The sequence complete interrupt flag. This flag is not cleared until the interrupt is serviced (by reading the result data in such a way that the conversion complete flag is cleared), a new conversion sequence is initiated, or the module is reset. This bit is not writable in any mode.

RES10 — A/D Resolution Select

0 = 8-bit resolution selected

1 = 10-bit resolution selected

This bit determines the resolution of the A/D converter: 8-bits or 10-bits. The A/D converter has the accuracy of a 10-bit converter. However, if low resolution is adequate, the conversion can be speeded up by selecting 8-bit resolution.

SMP[1:0] — Sample Time Select

These two bits select the length of the third phase of the sample period (in internal ATD clock cycles) which occurs after the buffered sample and transfer. During this phase, the external analog signal is connected directly to the storage node for final charging and improved accuracy. Note that the ATD clock period is itself a function of the prescaler value (bits PRS0–4). **Table 19-4** lists the lengths available for the third sample phase.

Table 19-4. Final Sample Time Selection

SMP1	SMP0	Final Sample Time
0	0	2 A/D clock periods
0	1	4 A/D clock periods
1	0	8 A/D clock periods
1	1	16 A/D clock periods

PRS[4:0] — ATD Clock Prescaler

The binary prescaler value (0 to 31) plus one (1 to 32) becomes the divide-by-factor for a modulus counter used to prescale the system PCLK frequency. The resulting scaled clock is further divided by 2 before the ATD internal clock is generated. This clock is used to drive the S/H and A/D machines.

Note that the maximum ATD clock frequency is half of the system clock. The default prescaler value is 00001 which results in a default ATD clock frequency that is quarter of the system clock i.e. with 8MHz bus the ATD module clock is 2MHz. **Table 19-5** illustrates the divide-by operation and the appropriate range of system clock frequencies.

BK0ALE — Breakpoint 0 Range Control

Valid in all modes.

0 = BRKAL will not be used to compare to the address bus.

1 = BRKAL will be used to compare to the address bus.

Table 20-8. Breakpoint Address Range Control

BK1ALE	BK0ALE	Address Range Selected
–	0	Upper 8-bit address only for full mode or dual mode BKP0
–	1	Full 16-bit address for full mode or dual mode BKP0
0	–	Upper 8-bit address only for dual mode BKP1
1	–	Full 16-bit address for dual mode BKP1

BRKCT1 — Breakpoint Control Register 1 **$0021**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	BKDBE	BKMBH	BKMBL	BK1RWE	BK1RW	BK0RWE	BK0RW
RESET:	0	0	0	0	0	0	0	0

This register is read/write in all modes.

BKDBE — Enable Data Bus

Enables comparing of address or data bus values using the BRKDH/L registers.

0 = The BRKDH/L registers are not used in any comparison

1 = The BRKDH/L registers are used to compare address or data (depending upon the mode selections BKEN1,0)

BKMBH — Breakpoint Mask High

Disables the comparing of the high byte of data when in full breakpoint mode. Used in conjunction with the BKDBE bit (which should be set)

0 = High byte of data bus (bits 15:8) are compared to BRKDH

1 = High byte is not used to in comparisons