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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	CPU12
Core Size	16-Bit
Speed	8MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	67
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc912dt128ccpve

Setting the RDPH bit in register RDRIV causes all port H outputs to have reduced drive level. RDRIV can be written once after reset. RDRIV is not in the address map in peripheral mode. Refer to Bus Control and Input/Output.

3.5.5 Port J

Port J pins are used for key wake-ups that can be used with the pins configured as inputs or outputs. The key wake-ups are triggered with either a rising or falling edge signal (KWPJ). An interrupt is generated if the corresponding bit is enabled (KWIEJ). If any of the interrupts is not enabled, the corresponding pin can be used as a general purpose I/O pin. Refer to I/O Ports with Key Wake-up.

Register DDRJ determines whether each port J pin is an input or output. Setting a bit in DDRJ makes the corresponding bit in port J an output; clearing a bit in DDRJ makes the corresponding bit in port J an input. The default reset state of DDRJ is all zeroes.

Register KWPJ not only determines what type of edge the key wake ups are triggered, but it also determines what type of resistive load is used for port J input pins when PUPJ bit is set in the PUCR register. Setting a bit in KWPJ makes the corresponding key wake up input pin trigger at rising edges and loads a pull down in the corresponding port J input pin. Clearing a bit in KWPJ makes the corresponding key wake up input pin trigger at falling edges and loads a pull up in the corresponding port J input pin. The default state of KWPJ is all zeroes.

Setting the RDPJ bit in register RDRIV causes all port J outputs to have reduced drive level. RDRIV can be written once after reset. RDRIV is not in the address map in peripheral mode. Refer to Bus Control and Input/Output.

3.5.6 Port K

Port K pins are used for page index emulation in expanded or peripheral modes. When page index emulation is not enabled, EMK is not set in MODE register, or the part is in single chip mode, these pins can be used

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
$00C8	BTST	BSPL	BRLD	SBR12	SBR11	SBR10	SBR9	SBR8	SC1BDH
$00C9	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	SC1BDL
$00CA	LOOPS	WOMS	RSRC	M	WAKE	ILT	PE	PT	SC1CR1
$00CB	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SC1CR2
$00CC	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF	SC1SR1
$00CD	0	0	0	0	0	0	0	RAF	SC1SR2
$00CE	R8	T8	0	0	0	0	0	0	SC1DRH
$00CF	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SC1DRL
$00D0	SPIE	SPE	SWOM	MSTR	CPOL	CPHA	SSOE	LSBF	SP0CR1
$00D1	0	0	0	0	PUPS	RDPS	SSWAI	SPC0	SP0CR2
$00D2	0	0	0	0	0	SPR2	SPR1	SPR0	SP0BR
$00D3	SPIF	WCOL	0	MODF	0	0	0	0	SP0SR
$00D4	0	0	0	0	0	0	0	0	Reserved
$00D5	Bit 7	6	5	4	3	2	1	Bit 0	SP0DR
$00D6	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	PORTS
$00D7	DDS7	DDS6	DDS5	DDS4	DDS3	DDS2	DDS1	DDS0	DDRS
$00D8–$00DF	0	0	0	0	0	0	0	0	Reserved
$00E0	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0	IBAD
$00E1	0	0	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0	IBFD
$00E2	IBEN	IBIE	MS/$\overline{SL}$	Tx/$\overline{Rx}$	TXAK	RSTA	0	IBSWAI	IBCR
$00E3	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK	IBSR
$00E4	D7	D6	D5	D4	D3	D2	D1	D0	IBDR
$00E5	0	0	0	RDPIB	0	0	0	PUPIB	IBPURD
$00E6	PIB7	PIB6	PIB5	PIB4	PIB3	PIB2	PIB1	PIB0	PORTIB
$00E7	DDRIB7	DDRIB6	DDRIB5	DDRIB4	DDRIB3	DDRIB2	DDRIB1	DDRIB0	DDRIB
$00E8–$00EB	Unimplemented[4]								Reserved
$00EC–$00ED	0	0	0	0	0	0	0	0	Reserved
$00EE	0	0	0	0	0	0	EEDIV9	EEDIV8	EEDIVH
$00EF	EEDIV7	EEDIV6	EEDIV5	EEDIV4	EEDIV3	EEDIV2	EEDIV1	EEDIV0	EEDIVL
$00F0	NOBDML	NOSHW	Reserved	FPOPEN[5]	1	EESWAI	PROTLCK	EERC	EEMCR
$00F1	SHPROT	1	BPROT5	BPROT4	BPROT3	BPROT2	BPROT1	BPROT0	EEPROT
$00F2	0	EREVTN	0	0	0	ETMSD	ETMR	ETMSE	EETST
$00F3	BULKP	0	AUTO	BYTE	ROW	ERASE	EELAT	EEPGM	EEPROG
$00F4	0	0	0	0	0	0	0	LOCK	FEELCK
$00F5	0	0	0	0	0	0	0	BOOTP	FEEMCR
$00F6	STRE	REVTUN	0	0	0	TMSD	TMR	TMSE	FEETST

Table 4-1. Register Map (Sheet 6 of 11)

6.4.3 Test mode Program space expansion

In special mode and for test purposes only, the 128K bytes of Flash EEPROM for MC68HC912DT128A can be accessed through a test program space window of 32K bytes. This window replaces the user's program space window to be able to access an entire array. In special mode and with ROMTST bit set in MISC register, a program space is located from $8000 to $FFFF. Only two page indices are used to point to one of the four 32K byte arrays. These indices can be viewed as expanded addresses X16 and X15.

Table 6-4. Test mode program space Page Index

Page Index 2 (PPAGE bit 2)	Page Index 1 (PPAGE bit 1)	Page Index 0 (PPAGE bit 0)	Flash register space Page	Flash array
0	0	X	32K byte array Page 0	00FEE32K
0	1	X	32K byte array Page 1	01FEE32K
1	0	X	32K byte array Page 2	10FEE32K
1	1	X	32K byte array Page 3	11FEE32K

6.4.4 Page Index register descriptions

PORTK — Port K Data Register **$00FC**

	Bit 7	6	5	4	3	2	1	Bit 0
PORT	PK7	0	0	0	PK3	PK2	PK1	PK0
Emulation	$\overline{ECS}$	0	0	0	-	PIX2	PIX1	PIX0
RESET:	-	0	0	0	-	-	-	-

Read and write anytime

Writes do not change pin state when pin configured for page index emulation output.

This port is associated with page index emulation pins. When the port is not enabled to emulate page index, the port pins are used as general-purpose I/O. Port K bit 3 is used as a general purpose I/O pin only. This register is not in the map in peripheral or expanded modes while the EMK control bit in MODE register is set.

6.7 Memory Maps

The following diagrams illustrate the memory map for each mode of operation immediately after reset.

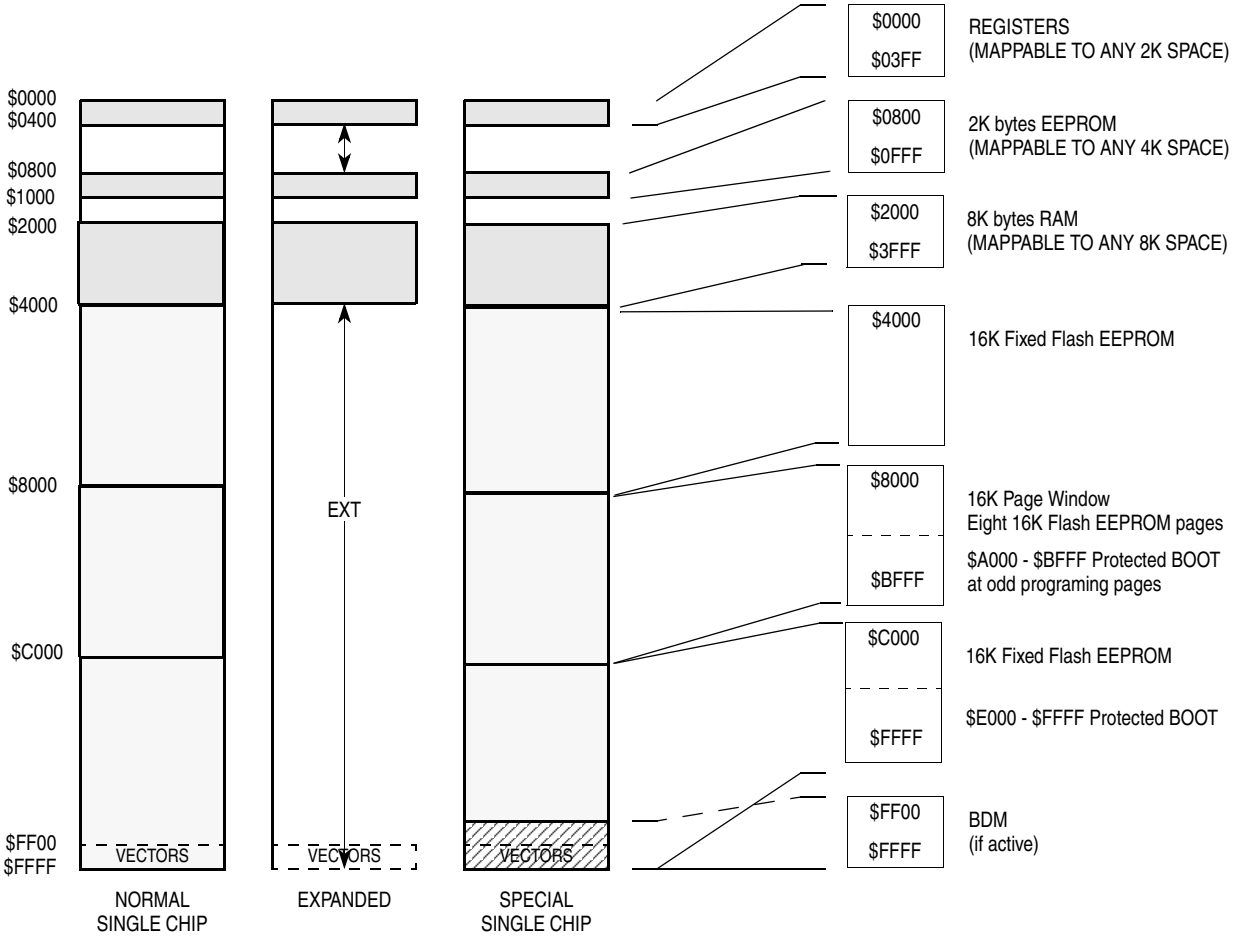

Figure 6-1. MC68HC912DT128A Memory Map after reset

The following diagram illustrates the memory paging scheme.

(R/$\overline{W}$), $\overline{IRQ}$, and $\overline{XIRQ}$. When the associated pin is not used for one of these specific functions, the pin can be used as general-purpose I/O. The port E assignment register (PEAR) selects the function of each pin. DDRE determines the primary direction of each port E pin when configured to be general-purpose I/O.

Some of these pins have software selectable pull-ups ($\overline{DBE}$, $\overline{LSTRB}$, R/$\overline{W}$, $\overline{IRQ}$ and $\overline{XIRQ}$). A single control bit enables the pull-ups for all these pins which are configured as inputs.

This register is not in the map in peripheral mode or expanded modes when the EME bit is set.

Read and write anytime.

DDRE — Port E Data Direction Register **$0009**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	0	0
RESET:	0	0	0	0	0	0	0	0

This register determines the primary direction for each port E pin configured as general-purpose I/O.

0 = Associated pin is a high-impedance input

1 = Associated pin is an output

PE[1:0] are associated with $\overline{XIRQ}$ and $\overline{IRQ}$ and cannot be configured as outputs. These pins can be read regardless of whether the alternate interrupt functions are enabled.

This register is not in the map in peripheral mode and expanded modes while the EME control bit is set.

Read and write anytime.

In peripheral mode, the PEAR register is not accessible for reads or writes. However, the CGMTE control bit is reset to one to configure PE6 as a test output for the CGM module.

NDBE — No Data Bus Enable

Normal: write once; Special: write anytime EXCEPT the first. Read anytime.

0 = PE7 is used for $\overline{\text{DBE}}$, external control of data enable on memories, or inverted E clock.

1 = PE7 is CAL function if CALE bit is set in PEAR register or general-purpose I/O otherwise.

The NDBE bit has no effect in Single Chip or Peripheral Modes and PE7 is defaulted to the CAL function if CALE bit is set in PEAR register or to an I/O otherwise.

CGMTE — Clock Generator Module Testing Enable

Normal: write never; Special: write anytime EXCEPT the first time. Read anytime.

0 = PE6 is general-purpose I/O or pipe output.

1 = PE6 is a test signal output from the CGM module (no effect in single chip or normal expanded modes). PIPOE = 1 overrides this function and forces PE6 to be a pipe status output signal.

PIPOE — Pipe Status Signal Output Enable

Normal: write once; Special: write anytime EXCEPT the first time. Read anytime.

0 = PE[6:5] are general-purpose I/O (if CGMTE = 1, PE6 is a test output signal from the CGM module).

1 = PE[6:5] are outputs and indicate the state of the instruction queue (only effective in expanded modes).

NECLK — No External E Clock

Normal single chip: write once; special single chip: write anytime; all other modes: write never.

Read anytime. In peripheral mode, E is an input and in all other modes, E is an output.

8.11 Flash protection bit FPOPEN

The FPOPEN bit is located in EEMCR – EEPROM Module Configuration Register, bit 4.

FPOPEN – Opens the Flash array for program or erase

0 = The whole Flash array is protected.

1 = The whole Flash array is enabled for program or erase

FPOPEN can be read at anytime.

FPOPEN can be written only to ’0’ for protection but not to ’1’ for un-protect in normal mode.

FPOPEN can be written ’0’ and ’1’ in special mode only.

FPOPEN is loaded at reset from EEPROM SHADOW word bit 4.

When FPOPEN is cleared to ’0’, the Flash array cannot be reprogrammed in normal modes.

CAUTION: *Programming the NVM FPOPEN bit in the SHADOW word ($_FC0, bit 4) means that the FPOPEN bit in the EEMCR register will always be ’0’ in normal modes. The flash array can no longer be modified in normal modes.*

10.5 Latching of Interrupts

$\overline{\text{XIRQ}}$ is always level triggered and $\overline{\text{IRQ}}$ can be selected as a level triggered interrupt. These level triggered interrupt pins should only be released during the appropriate interrupt service routine. Generally the interrupt service routine will handshake with the interrupting logic to release the pin. In this way, the MCU will never start the interrupt service sequence only to determine that there is no longer an interrupt source. In event that this does occur the trap vector will be taken.

If $\overline{\text{IRQ}}$ is selected as an edge triggered interrupt, the hold time of the level after the active edge is independent of when the interrupt is serviced. As long as the minimum hold time is met, the interrupt will be latched inside the MCU. In this case the IRQ edge interrupt latch is cleared automatically when the interrupt is serviced.

All of the remaining interrupts are latched by the MCU with a flag bit. These interrupt flags should be cleared during an interrupt service routine or when interrupts are masked by the I bit. By doing this, the MCU will never get an unknown interrupt source and take the trap vector.

software failing to execute the sequence properly causes a COP reset to occur. In addition, windowed COP operation can be selected. In this mode, a write to the COPRST register must occur in the last 25% of the selected period. A premature write will also reset the part.

10.8.4 Clock Monitor Reset

If clock frequency falls below a predetermined limit when the clock monitor is enabled, a reset occurs.

10.9 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states, as follows.

10.9.1 Operating Mode and Memory Map

Operating mode and default memory mapping are determined by the states of the BKGD, MODA, and MODB pins during reset. The SMODN, MODA, and MODB bits in the MODE register reflect the status of the mode-select inputs at the rising edge of reset. Operating mode and default maps can subsequently be changed according to strictly defined rules.

10.9.2 Clock and Watchdog Control Logic

The COP watchdog system is enabled, with the CR[2:0] bits set for the longest duration time-out. The clock monitor is disabled. The RTIF flag is cleared and automatic hardware interrupts are masked. The rate control bits are cleared, and must be initialized before the RTI system is used. The DLY control bit is set to specify an oscillator start-up delay upon recovery from STOP mode.

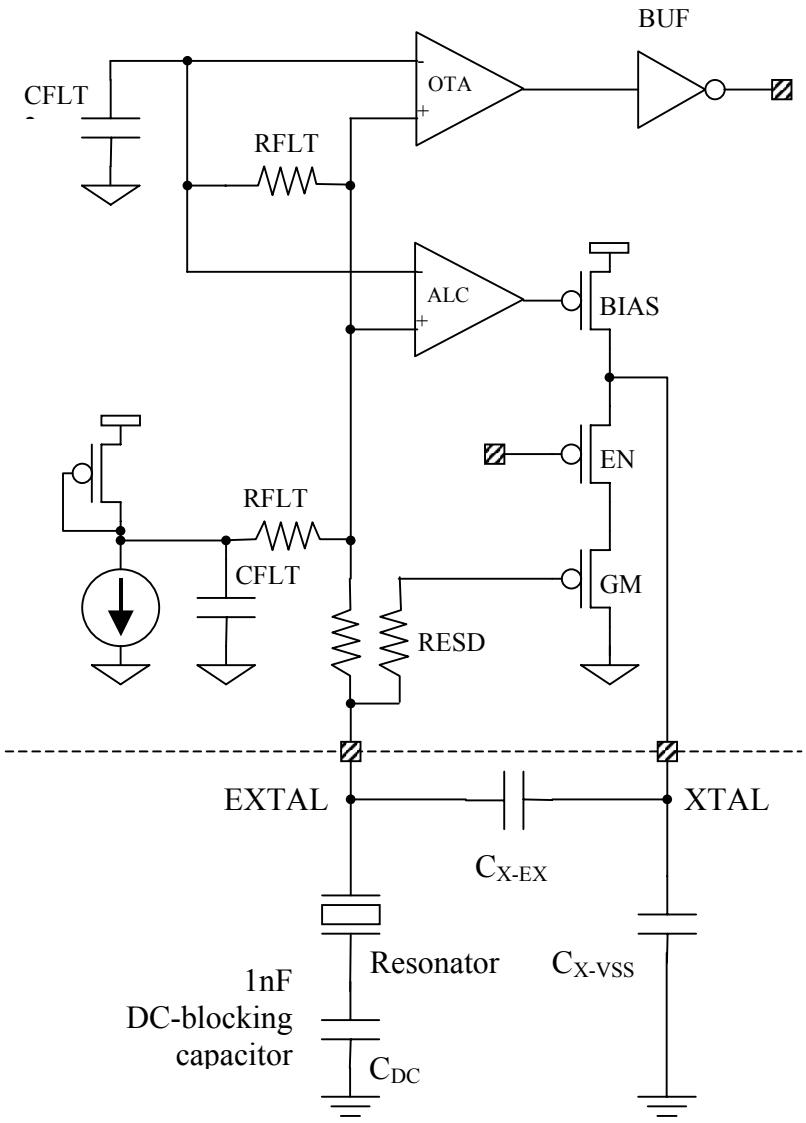

Figure 13-3. MC68HC912Dx128C Crystal with DC Blocking Capacitor

variation or particle contamination).

3. Within this range, choose the EXTAL–VSS capacitance closest to ($C_{EXTAL–VSS}$ = 2*CL – 10pF).
4. If the ideal component is between two valid component values (the maximum ESR is sufficient for both component values), then choose the component with the highest maximum ESR or choose an available component between the two listed values.
5. Choose the size of the XTAL–VSS capacitance equal to EXTAL–VSS capacitance.
6. If the frequency of the crystal falls between listed values, determine the appropriate component for the listed frequency values on either side and extrapolate.
7. The maximum allowed capacitor is the highest listed component, and the minimum allowed capacitor is the lowest listed component. ‘NA’ or ‘Not Allowed’ means the listed component is not valid or allowed for the given frequency, Shunt Capacitance, and VDDPLL setting.

13.5.3.2 General Specifications

The following limitations apply to every system:

- Ceramic resonators with integrated components must have the integrated components accounted for in the total component value.
- Series cut resonators should not be used. Use parallel cut instead.
- The Load Capacitance should be 12pF or higher, preferably greater than 15pF.

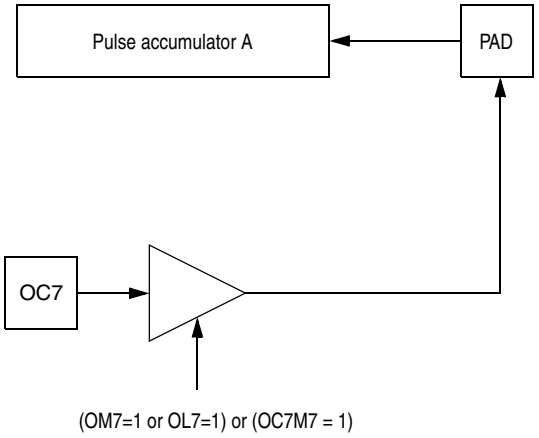

Figure 15-5. Block Diagram for Port7 with Output compare / Pulse Accumulator A

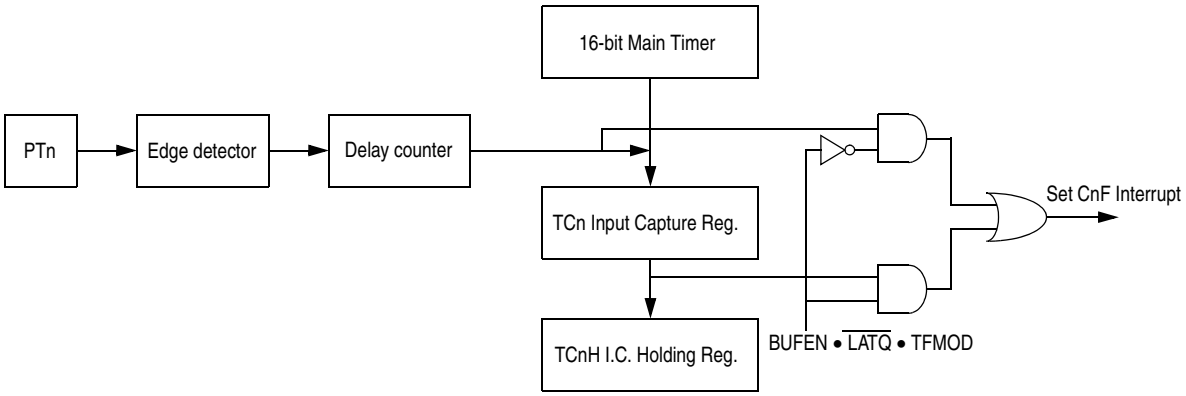

Figure 15-6. C3F-C0F Interrupt Flag Setting

15.3 Enhanced Capture Timer Modes of Operation

The Enhanced Capture Timer has 8 Input Capture, Output Compare (IC/OC) channels same as on the HC12 standard timer (timer channels TC0 to TC7). When channels are selected as input capture by selecting the IOSx bit in TIOS register, they are called Input Capture (IC) channels.

15.4 Timer Register Descriptions

Input/output pins default to general-purpose I/O lines until an internal function which uses that pin is specifically enabled. The timer overrides the state of the DDR to force the I/O state of each associated port line when an output compare using a port line is enabled. In these cases the data direction bits will have no affect on these lines.

When a pin is assigned to output an on-chip peripheral function, writing to this PORTT bit does not affect the pin but the data is stored in an internal latch such that if the pin becomes available for general-purpose output the driven level will be the last value written to the PORTT bit.

TIOS — Timer Input Capture/Output Compare Select **$0080**

	Bit 7	6	5	4	3	2	1	Bit 0
	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
RESET:	0	0	0	0	0	0	0	0

Read or write anytime.

IOS[7:0] — Input Capture or Output Compare Channel Configuration
0 = The corresponding channel acts as an input capture
1 = The corresponding channel acts as an output compare.

CFORC — Timer Compare Force Register **$0081**

	Bit 7	6	5	4	3	2	1	Bit 0
	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
RESET:	0	0	0	0	0	0	0	0

Read anytime but will always return $00 (1 state is transient). Write anytime.

SC0SR1/SC1SR1 — SCI Status Register 1 **$00C4/$00CC**

	Bit 7	6	5	4	3	2	1	Bit 0
	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
RESET:	1	1	0	0	0	0	0	0

The bits in these registers are set by various conditions in the SCI hardware and are automatically cleared by special acknowledge sequences. The receive related flag bits in SCxSR1 (RDRF, IDLE, OR, NF, FE, and PF) are all cleared by a read of the SCxSR1 register followed by a read of the transmit/receive data register low byte. However, only those bits which were set when SCxSR1 was read will be cleared by the subsequent read of the transmit/receive data register low byte. The transmit related bits in SCxSR1 (TDRE and TC) are cleared by a read of the SCxSR1 register followed by a write to the transmit/receive data register low byte.

Read anytime (used in auto clearing mechanism). Write has no meaning or effect.

TDRE — Transmit Data Register Empty Flag

New data will not be transmitted unless SCxSR1 is read before writing to the transmit data register. Reset sets this bit.

0 = SCxDR busy

1 = Any byte in the transmit data register is transferred to the serial shift register so new data may now be written to the transmit data register.

TC — Transmit Complete Flag

Flag is set when the transmitter is idle (no data, preamble, or break transmission in progress). Clear by reading SCxSR1 with TC set and then writing to SCxDR.

0 = Transmitter busy

1 = Transmitter is idle

SP0BR — SPI Baud Rate Register **$00D2**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	0	SPR2	SPR1	SPR0
RESET:	0	0	0	0	0	0	0	0

Read anytime. Write anytime.

At reset, E Clock divided by 2 is selected.

SPR[2:0] — SPI Clock (SCK) Rate Select Bits

These bits are used to specify the SPI clock rate.

Table 16-4. SPI Clock Rate Selection

SPR2	SPR1	SPR0	E Clock Divisor	Frequency at E Clock = 4 MHz	Frequency at E Clock = 8 MHz
0	0	0	2	2.0 MHz	4.0 MHz
0	0	1	4	1.0 MHz	2.0 MHz
0	1	0	8	500 kHz	1.0 MHz
0	1	1	16	250 kHz	500 KHz
1	0	0	32	125 kHz	250 KHz
1	0	1	64	62.5 kHz	125 KHz
1	1	0	128	31.3 kHz	62.5 KHz
1	1	1	256	15.6 kHz	31.3 KHz

SP0SR — SPI Status Register **$00D3**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIF	WCOL	0	MODF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

Read anytime. Write has no meaning or effect.

SPIF — SPI Interrupt Request

SPIF is set after the eighth SCK cycle in a data transfer and it is cleared by reading the SP0SR register (with SPIF set) followed by an access (read or write) to the SPI data register.

18.8.2 msCAN12 SOFT_RESET Mode

In SOFT_RESET mode, the msCAN12 is stopped. Registers can still be accessed. This mode is used to initialize the module configuration, bit timing, and the CAN message filter. See msCAN12 Module Control Register (CMCR0) for a complete description of the SOFT_RESET mode.

When setting the SFTRES bit, the msCAN12 immediately stops all ongoing transmissions and receptions, potentially causing the CAN protocol violations. The user is responsible to take care that the msCAN12 is not active when SOFT_RESET mode is entered. The recommended procedure is to bring the msCAN12 into SLEEP mode before the SFTRES bit is set.

18.8.3 msCAN12 POWER_DOWN Mode

The msCAN12 is in POWER_DOWN mode when

- the CPU is in STOP mode or
- the CPU is in WAIT mode and the CSWAI bit is set (see msCAN12 Module Control Register (CMCR0)).

When entering the POWER_DOWN mode, the msCAN12 immediately stops all ongoing transmissions and receptions, potentially causing CAN protocol violations. The user is responsible to take care that the msCAN12 is not active when POWER_DOWN mode is entered. The recommended procedure is to bring the msCAN12 into SLEEP mode before the STOP instruction (or the WAI instruction, if CSWAI is set) is executed.

To protect the CAN bus system from fatal consequences of violations to above rule, the msCAN12 will drive the TxCAN pin into recessive state.

In POWER_DOWN mode, no registers can be accessed.

18.13 Programmer's Model of Control Registers

18.13.1 Overview

The programmer's model has been laid out for maximum simplicity and efficiency.

18.13.2 msCAN12 Module Control Register (CMCR0)

		Bit 7	6	5	4	3	2	1	Bit 0
CMCR0	R	0	0	CSWAI	SYNCH	TLNKEN	SLPAK	SLPRQ	SFTRES
$0100	W								
RESET		0	0	1	0	0	0	0	1

CSWAI — CAN Stops in Wait Mode

0 = The module is not affected during WAIT mode.

1 = The module ceases to be clocked during WAIT mode.

SYNCH — Synchronized Status

This bit indicates whether the msCAN12 is synchronized to the CAN bus and as such can participate in the communication process.

0 = msCAN12 is not synchronized to the CAN bus

1 = msCAN12 is synchronized to the CAN bus

TLNKEN — Timer Enable

This flag is used to establish a link between the msCAN12 and the on-chip timer (see Timer Link).

0 = The port is connected to the timer input.

1 = The msCAN12 timer signal output is connected to the timer input.

SLPAK — SLEEP Mode Acknowledge

This flag indicates whether the msCAN12 is in module internal SLEEP Mode. It shall be used as a handshake for the SLEEP Mode request (see msCAN12 SLEEP Mode).

0 = Wake-up – The msCAN12 is not in SLEEP Mode.

1 = SLEEP – The msCAN12 is in SLEEP Mode.

Resetting to idle mode defines the only exception of the reset control bit condition to the system reset condition. The reset control bit does not initialize the ADPU bit to its reset condition and therefore does not power down the module. This except allows the module to remain active for other test operations.

19.9.7 PORTAD Port Data Register

The input data port associated with the ATD module is input-only. The port pins are shared with the analog A/D inputs.

PORTAD0/PORTAD1 — Port AD Data Input Register **$006F/$01EF**

	Bit 7	6	5	4	3	2	1	Bit 0
	PADx7	PADx6	PADx5	PADx4	PADx3	PADx2	PADx1	PADx0
RESET:	-	-	-	-	-	-	-	-

PADx[7:0] — Port AD Data Input Bits

Reset: These pins reflect the state of the input pins.

The ATD input ports may be used for general purpose digital input. When the port data registers are read, they contain the digital levels appearing on the input pins at the time of the read. Input pins with signal potentials not meeting V_{IL} or V_{IH} specifications will have an indeterminate value.

Use of any Port pin for digital input does not preclude the use of any other Port pin for analog input.

Writes to this register have no meaning at any time.

20.4.5.5 CCRSAV

The CCRSAV register is used to save the CCR of the users program when entering BDM. It is also used for temporary storage in the BDM firmware.

Read and write: all modes

CCRSAV— BDM CCR Holding Register **$FF06**

	BIT 7	6	5	4	3	2	1	BIT 0
	CCR7	CCR6	CCR5	CCR4	CCR3	CCR2	CCR1	CCR0
RESET: NOTE 1 (1)	X	X	X	X	X	X	X	X

1. Initialized to equal the CPU12 CCR register by the firmware.

20.5 Breakpoints

Hardware breakpoints are used to debug software on the MC68HC912DT128A by comparing actual address and data values to predetermined data in setup registers. A successful comparison will place the CPU in background debug mode (BDM) or initiate a software interrupt (SWI). Breakpoint features designed into the MC68HC912DT128A include:

- Mode selection for BDM or SWI generation
- Program fetch tagging for cycle of execution breakpoint
- Second address compare in dual address modes
- Range compare by disable of low byte address
- Data compare in full feature mode for non-tagged breakpoint
- Byte masking for high/low byte data compares
- R/$\overline{W}$ compare for non-tagged compares
- Tag inhibit on BDM TRACE

Glossary

A — See “accumulators (A and B or D).”

accumulators (A and B or D) — Two 8-bit (A and B) or one 16-bit (D) general-purpose registers in the CPU. The CPU uses the accumulators to hold operands and results of arithmetic and logic operations.

acquisition mode — A mode of PLL operation with large loop bandwidth. Also see ’tracking mode’.

address bus — The set of wires that the CPU or DMA uses to read and write memory locations.

addressing mode — The way that the CPU determines the operand address for an instruction. The M68HC12 CPU has 15 addressing modes.

ALU — See “arithmetic logic unit (ALU).”

analogue-to-digital converter (ATD) — The ATD module is an 8-channel, multiplexed-input successive-approximation analog-to-digital converter.

arithmetic logic unit (ALU) — The portion of the CPU that contains the logic circuitry to perform arithmetic, logic, and manipulation operations on operands.

asynchronous — Refers to logic circuits and operations that are not synchronized by a common reference signal.

ATD — See “analogue-to-digital converter”.

B — See “accumulators (A and B or D).”

baud rate — The total number of bits transmitted per unit of time.

BCD — See “binary-coded decimal (BCD).”