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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 33x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk22fn256vll12r

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1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	−55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	−2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	−500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	−100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

General

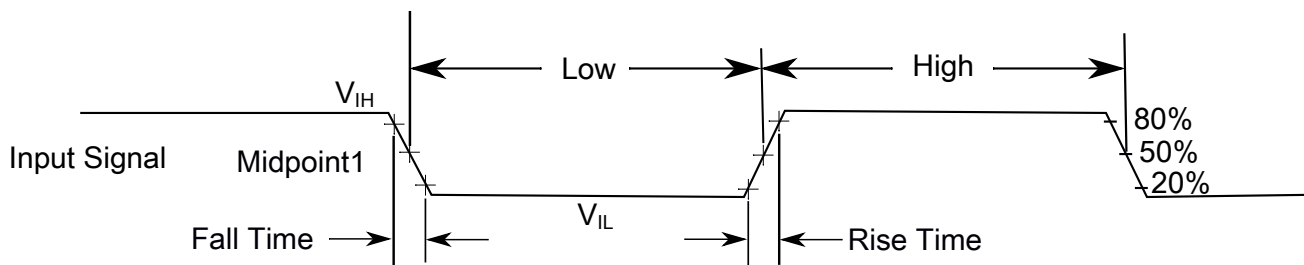
Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	158	mA
V_{DIO}	Digital input voltage	-0.3	$V_{DD} + 0.3$	V
V_{AIO}	Analog ¹	-0.3	$V_{DD} + 0.3$	V
I_D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{USB0_DP}	USB0_DP input voltage	-0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	-0.3	3.63	V
VREGIN	USB regulator input	-0.3	6.0	V
V_{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

Table 7. Low power mode peripheral adders—typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
	entering all modes with the crystal enabled.							
	VLLS1	440	490	540	560	570	580	nA
	VLLS3	440	490	540	560	570	580	
	LLS	490	490	540	560	570	680	
	VLPS	510	560	560	560	610	680	
	STOP	510	560	560	560	610	680	
I _{48MIRC}	48 Mhz internal reference clock	350	350	350	350	350	350	μA
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I _{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	μA
	>OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I _{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	μA
I _{ADC}	ADC peripheral adder combining the measured values at V _{DD} and V _{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	42	42	42	42	42	42	μA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

Table 10. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f _{BUS}	Bus clock	—	4	MHz	
f _{FLASH}	Flash clock	—	1	MHz	
f _{ERCLK}	External reference clock	—	16	MHz	
f _{LPTMR_pin}	LPTMR clock	—	25	MHz	
f _{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
f _{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f _{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 11. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	4
	Mode select (EZP_CS) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time • Slew disabled • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ • Slew enabled • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$	— — — —	10 5 30 16	ns ns ns ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.

3.3.2 IRC48M specifications

Table 17. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DD48M}	Supply current	—	400	500	μA	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m_ol_hv}$	Open loop total deviation of IRC48M frequency at high voltage ($V_{DD}=1.89V-3.6V$) over $0^{\circ}C$ to $70^{\circ}C$ Regulator enable (<code>USB_CLK_RECOVER_IRC_EN[REG_EN]=1</code>)	—	± 0.2	± 0.5	$\%f_{irc48m}$	1
$\Delta f_{irc48m_ol_hv}$	Open loop total deviation of IRC48M frequency at high voltage ($V_{DD}=1.89V-3.6V$) over full temperature Regulator enable (<code>USB_CLK_RECOVER_IRC_EN[REG_EN]=1</code>)	—	± 0.4	± 1.0	$\%f_{irc48m}$	1
$\Delta f_{irc48m_ol_lv}$	Open loop total deviation of IRC48M frequency at low voltage ($V_{DD}=1.71V-1.89V$) over full temperature Regulator disable (<code>USB_CLK_RECOVER_IRC_EN[REG_EN]=0</code>) Regulator enable (<code>USB_CLK_RECOVER_IRC_EN[REG_EN]=1</code>)	—	± 0.4 ± 0.5	± 1.0 ± 1.5	$\%f_{irc48m}$	1
Δf_{irc48m_cl}	Closed loop total deviation of IRC48M frequency over voltage and temperature	—	—	± 0.1	$\%f_{host}$	2
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	μs	3

1. The maximum value represents characterized results equivalent to the mean plus or minus three times the standard deviation (mean ± 3 sigma).
2. Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (`USB_CLK_RECOVER_IRC_CTRL[CLOCK_RECOVER_EN]=1`, `USB_CLK_RECOVER_IRC_EN[IRC_EN]=1`).
3. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by one of the following settings:
 - `USB_CLK_RECOVER_IRC_EN[IRC_EN]=1` or
 - MCG operating in an external clocking mode and `MCG_C7[OSCSEL]=10` or `MCG_C5[PLLCLKEN0]=1`, or
 - `SIM_SOPT2[PLLFLSEL]=11`

3.3.3 Oscillator electrical specifications

Table 18. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x and C_y can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

3.3.3.2 Oscillator frequency specifications

Table 19. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f _{osc_hi_1}	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
f _{osc_hi_2}	Oscillator crystal or resonator frequency — high-frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f _{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t _{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t _{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.

- Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

3.3.4 32 kHz oscillator electrical characteristics

3.3.4.1 32 kHz oscillator DC electrical specifications

Table 20. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	$M\Omega$
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp} ¹	Peak-to-peak amplitude of oscillation	—	0.6	—	V

- When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.4.2 32 kHz oscillator frequency specifications

Table 21. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$V_{ec_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

- Proper PC board layout procedures must be followed to achieve specifications.
- This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
- The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

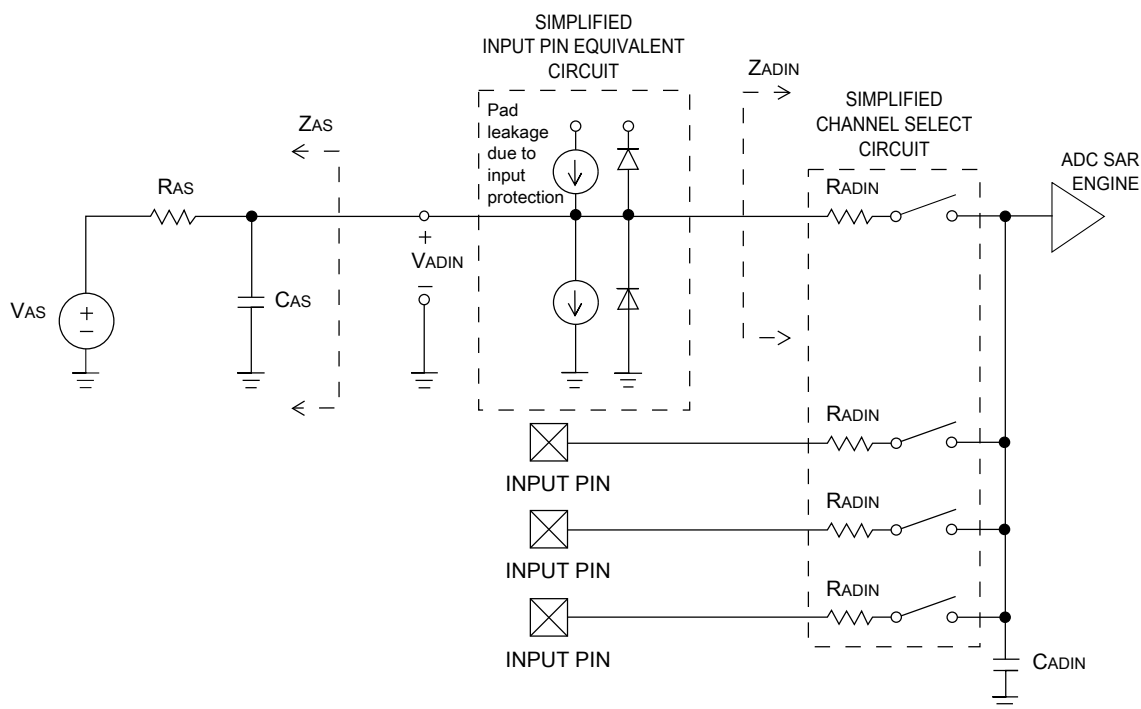


Figure 12. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	± 4 ± 1.4	± 6.8 ± 2.1	LSB ⁴	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	± 0.7 ± 0.2	-1.1 to +1.9 -0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	• 12-bit modes	—	± 1.0	-2.7 to +1.9	LSB ⁴	5

Table continues on the next page...

3.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit usb.org.

NOTE

The MCGPLLCLK meets the USB jitter and signaling rate specifications for certification with the use of an external clock/crystal for both Device and Host modes.

The MCGFLLCLK does not meet the USB jitter or signaling rate specifications for certification.

The IRC48M meets the USB jitter and signaling rate specifications for certification in Device mode when the USB clock recovery mode is enabled. It does not meet the USB signaling rate specifications for certification in Host mode operation.

3.8.2 USB VREG electrical specifications

Table 36. USB VREG electrical specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I _{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	μA	
I _{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	μA	
I _{DDoff}	Quiescent current — Shutdown mode - VREGIN = 5.0 V and temperature=25 °C - Across operating voltage and temperature	—	650	—	nA	
		—	—	4	μA	
I _{LOADrun}	Maximum load current — Run mode	—	—	120	mA	
I _{LOADstby}	Maximum load current — Standby mode	—	—	1	mA	
V _{Reg33out}	Regulator output voltage — Input supply (VREGIN) > 3.6 V - Run mode - Standby mode	3	3.3	3.6	V	
		2.1	2.8	3.6	V	

Table continues on the next page...

**Table 36. USB VREG electrical specifications
(continued)**

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
V _{Reg33out}	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C _{OUT}	External output capacitor	1.76	2.2	8.16	μF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I _{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.

2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

3.8.3 DSPI switching specifications (limited voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 37. Master mode DSPI timing (limited voltage range)

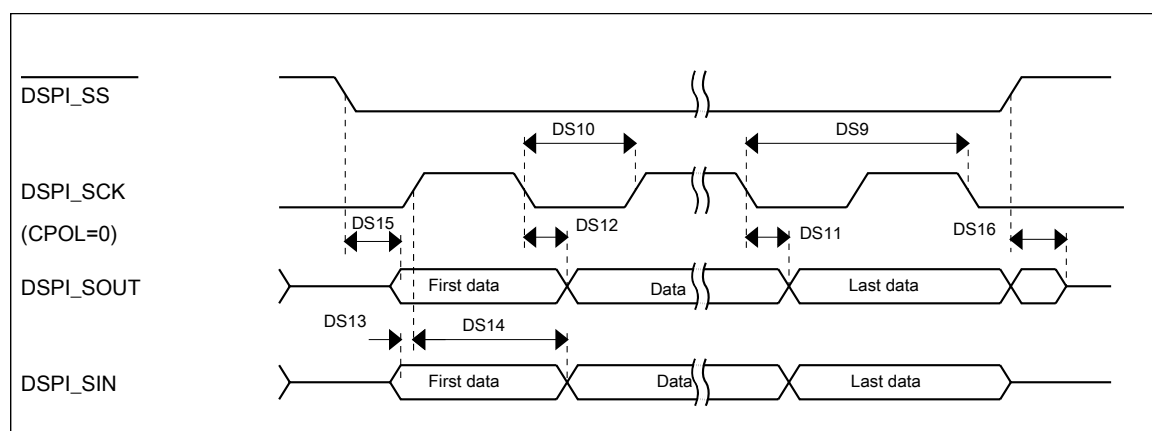
Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
DS1	DSPI_SCK output cycle time	2 × t _{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns	
DS3	DSPI_PCS _n valid to DSPI_SCK delay	(t _{BUS} × 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS _n invalid delay	(t _{BUS} × 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	16.2	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Table 40. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{\text{BUS}}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}}/2) - 4$	$(t_{\text{SCK}}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	29.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	25	ns </td
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	25	ns

**Figure 22. DSPI classic SPI timing — slave mode**

3.8.5 Inter-Integrated Circuit Interface (I²C) timing

Table 41. I²C timing

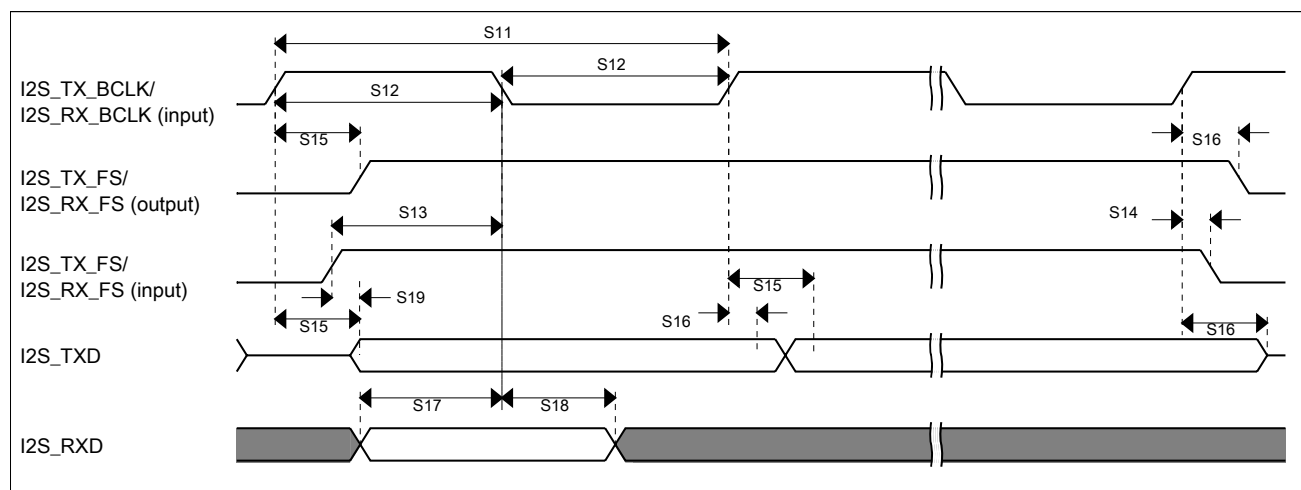
Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400 ¹	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD} ; STA	4	—	0.6	—	μs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	μs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	t_{SU} ; STA	4.7	—	0.6	—	μs

Table continues on the next page...

Table 46. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	28.5	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	5.8	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	26.3	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

**Figure 27. I2S/SAI timing — slave modes**

3.8.7.3 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 47. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns

Table continues on the next page...

Table 48. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	4	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

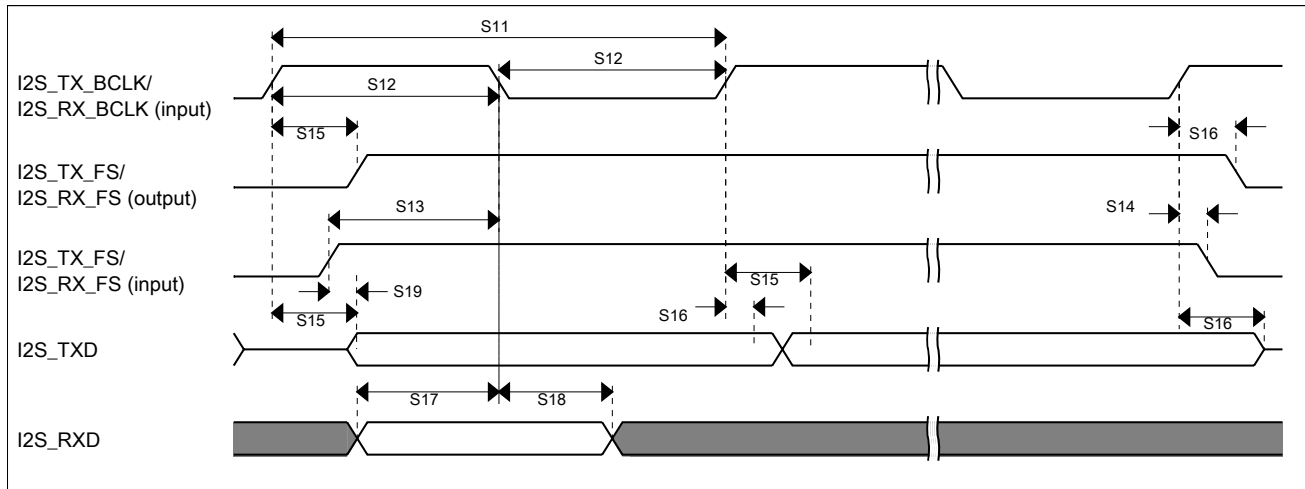


Figure 29. I2S/SAI timing — slave modes

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
64-pin LQFP	98ASS23234W
64-pin MAPBGA	98ASA00420D
100-pin LQFP	98ASS23308W
121-pin XFBGA	98ASA00595D

Pinout

121 BGA	100 LQFP	64 LQFP	64 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
K1	18	9	G1	ADC0_ DP0/ ADC1_DP3	ADC0_ DP0/ ADC1_DP3	ADC0_ DP0/ ADC1_DP3								
K2	19	10	F1	ADC0_ DM0/ ADC1_ DM3	ADC0_ DM0/ ADC1_ DM3	ADC0_ DM0/ ADC1_ DM3								
L1	20	11	G2	ADC1_ DP0/ ADC0_DP3	ADC1_ DP0/ ADC0_DP3	ADC1_ DP0/ ADC0_DP3								
L2	21	12	F2	ADC1_ DM0/ ADC0_ DM3	ADC1_ DM0/ ADC0_ DM3	ADC1_ DM0/ ADC0_ DM3								
F5	22	13	F4	VDDA	VDDA	VDDA								
G5	23	14	G4	VREFH	VREFH	VREFH								
G6	24	15	G3	VREFL	VREFL	VREFL								
F6	25	16	F3	VSSA	VSSA	VSSA								
L3	26	17	H1	VREF_ OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_ SE18	VREF_ OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_ SE18	VREF_ OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_ SE18								
K5	27	18	H2	DAC0_ OUT/ CMP1_IN3/ ADC0_ SE23	DAC0_ OUT/ CMP1_IN3/ ADC0_ SE23	DAC0_ OUT/ CMP1_IN3/ ADC0_ SE23								
K4	—	—	—	CMP0_IN4/ ADC1_ SE23	CMP0_IN4/ ADC1_ SE23	CMP0_IN4/ ADC1_ SE23								
L7	—	—	—	RTC_ WAKEUP_ B	RTC_ WAKEUP_ B	RTC_ WAKEUP_ B								
L4	28	19	H3	XTAL32	XTAL32	XTAL32								
L5	29	20	H4	EXTAL32	EXTAL32	EXTAL32								
K6	30	21	H5	VBAT	VBAT	VBAT								
H5	31	—	—	PTE24	ADC0_ SE17	ADC0_ SE17	PTE24				I2C0_SCL	EWM_ OUT_b		
J5	32	—	—	PTE25	ADC0_ SE18	ADC0_ SE18	PTE25				I2C0_SDA	EWM_IN		
H6	33	—	—	PTE26/ CLKOUT32 K	DISABLED		PTE26/ CLKOUT32 K					RTC_ CLKOUT	USB_ CLKIN	

Pinout

121 BGA	100 LQFP	64 LQFP	64 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
G8	56	38	E8	PTB3	ADC0_ SE13	ADC0_ SE13	PTB3	I2C0_SDA	UART0_ CTS_b			FTM0_ FLT0		
F11	—	—	—	PTB6	ADC1_ SE12	ADC1_ SE12	PTB6							
E11	—	—	—	PTB7	ADC1_ SE13	ADC1_ SE13	PTB7							
D11	—	—	—	PTB8	DISABLED		PTB8		LPUART0_ RTS_b					
E10	57	—	—	PTB9	DISABLED		PTB9	SPI1_ PCS1	LPUART0_ CTS_b					
D10	58	—	—	PTB10	ADC1_ SE14	ADC1_ SE14	PTB10	SPI1_ PCS0	LPUART0_ RX			FTM0_ FLT1		
C10	59	—	—	PTB11	ADC1_ SE15	ADC1_ SE15	PTB11	SPI1_SCK	LPUART0_ TX			FTM0_ FLT2		
—	60	—	—	VSS	VSS	VSS								
—	61	—	—	VDD	VDD	VDD								
B10	62	39	E6	PTB16	DISABLED		PTB16	SPI1_ SOUT	UART0_RX	FTM_ CLKIN0		EWM_IN		
E9	63	40	D7	PTB17	DISABLED		PTB17	SPI1_SIN	UART0_TX	FTM_ CLKIN1		EWM_ OUT_b		
D9	64	41	D6	PTB18	DISABLED		PTB18		FTM2_CH0	I2S0_TX_ BCLK		FTM2_QD_ PHA		
C9	65	42	C7	PTB19	DISABLED		PTB19		FTM2_CH1	I2S0_TX_ FS		FTM2_QD_ PHB		
F10	66	—	—	PTB20	DISABLED		PTB20					CMP0_ OUT		
F9	67	—	—	PTB21	DISABLED		PTB21					CMP1_ OUT		
F8	68	—	—	PTB22	DISABLED		PTB22							
E8	69	—	—	PTB23	DISABLED		PTB23		SPI0_ PCS5					
B9	70	43	D8	PTC0	ADC0_ SE14	ADC0_ SE14	PTC0	SPI0_ PCS4	PDB0_ EXTRG	USB_SOF_ OUT				
D8	71	44	C6	PTC1/ LLWU_P6	ADC0_ SE15	ADC0_ SE15	PTC1/ LLWU_P6	SPI0_ PCS3	UART1_ RTS_b	FTM0_CH0		I2S0_TXD0	LPUART0_ RTS_b	
C8	72	45	B7	PTC2	ADC0_ SE4b/ CMP1_IN0	ADC0_ SE4b/ CMP1_IN0	PTC2	SPI0_ PCS2	UART1_ CTS_b	FTM0_CH1		I2S0_TX_ FS	LPUART0_ CTS_b	
B8	73	46	C8	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_ PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_ BCLK	LPUART0_ RX	
—	74	47	E3	VSS	VSS	VSS								
—	75	48	E4	VDD	VDD	VDD								
A8	76	49	B8	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_ PCS0	UART1_TX	FTM0_CH3		CMP1_ OUT	LPUART0_ TX	

Table 49. Recommended connection for unused analog interfaces (continued)

Pin Type		Short recommendation	Detailed recommendation
GPIO/Analog	PTA18/EXTAL0	Float	Analog input - Float
GPIO/Analog	PTA19/XTAL0	Float	Analog output - Float
GPIO/Analog	PTx/ADCx	Float	Float (default is analog input)
GPIO/Analog	PTx/CMPx	Float	Float (default is analog input)
GPIO/Digital	PTA0/JTAG_TCLK	Float	Float (default is JTAG with pulldown)
GPIO/Digital	PTA1/JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA2/JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA3/JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA4/NMI_b	10k Ω pullup or disable and float	Pull high or disable in PCR & FOPT and float
GPIO/Digital	PTx	Float	Float (default is disabled)
USB	USB0_DP	Float	Float
USB	USB0_DM	Float	Float
USB	VOUT33	Tie to input and ground through 10k Ω	Tie to input and ground through 10k Ω
USB	VREGIN	Tie to output and ground through 10k Ω	Tie to output and ground through 10k Ω
VBAT	VBAT	Float	Float
VDDA	VDDA	Always connect to VDD potential	Always connect to VDD potential
VREFH	VREFH	Always connect to VDD potential	Always connect to VDD potential
VREFL	VREFL	Always connect to VSS potential	Always connect to VSS potential
VSSA	VSSA	Always connect to VSS potential	Always connect to VSS potential

5.3 K22F Pinouts

The following figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

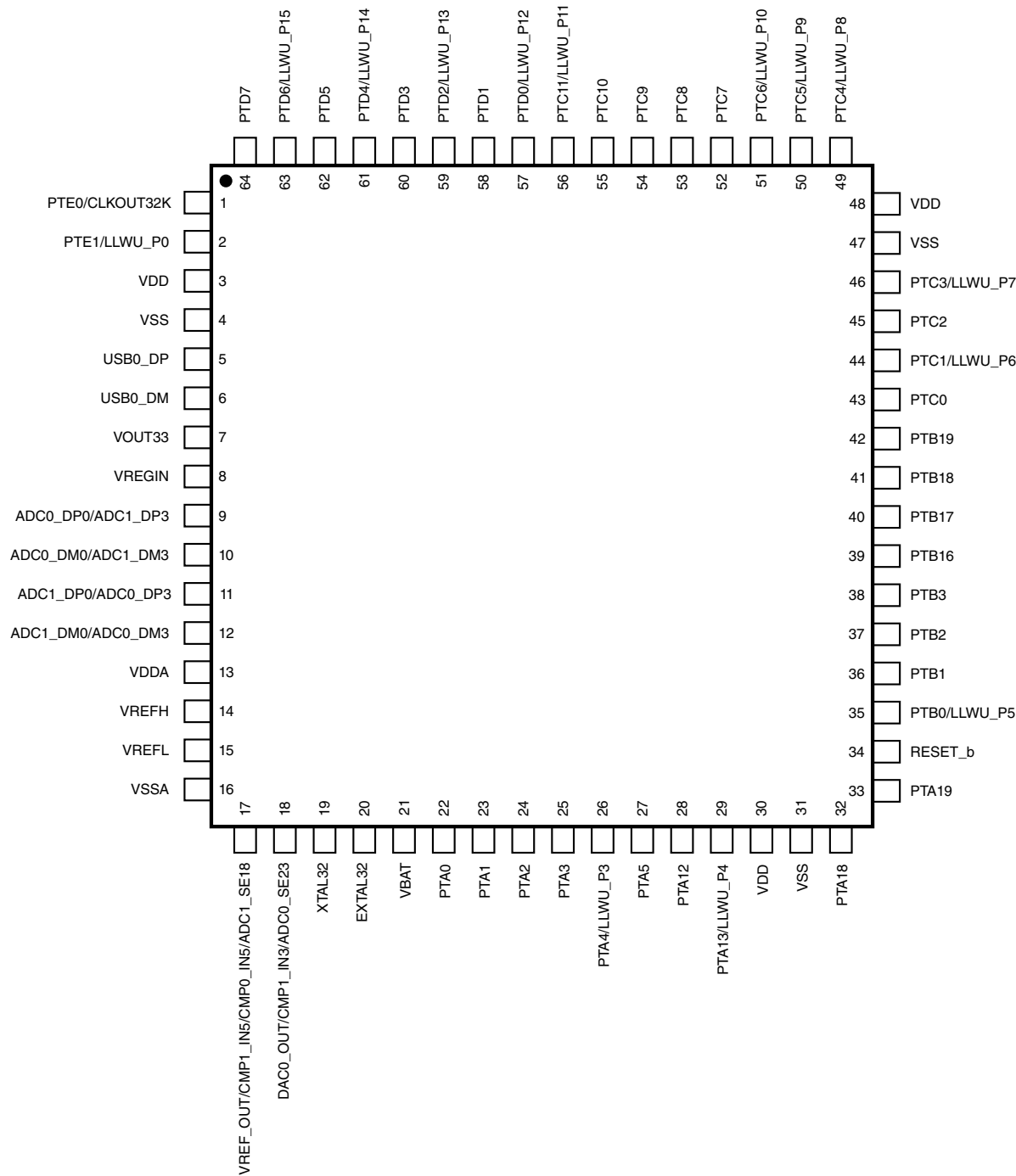


Figure 30. K22F 64 LQFP Pinout Diagram (top view)

Term	Definition
	NOTE: The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: - Lies within the range of values specified by the operating behavior - Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions NOTE: Typical values are provided as design guidelines and are neither tested nor guaranteed.

7.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	-0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

7.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

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