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Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

#### Applications of [Embedded - Microcontroller,](#)

#### Details

Product Status	Active
Module/Board Type	FPGA Core
Core Processor	Spartan-6 LX-150
Co-Processor	-
Speed	125MHz
Flash Size	16MB
RAM Size	256MB
Connector Type	Samtec LSHM
Size / Dimension	1.97" x 1.57" (50mm x 40mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	<a href="https://www.e-xfl.com/product-detail/trenz-electronic/te0600-03ivfn">https://www.e-xfl.com/product-detail/trenz-electronic/te0600-03ivfn</a>

Table 3: eFUSE Programming Conditions<sup>(1)</sup>

Symbol	Description	Min	Typ	Max	Units
$V_{FS}^{(2)}$	External voltage supply	3.2	3.3	3.4	V
$I_{FS}$	$V_{FS}$ supply current	–	–	40	mA
$V_{CCAUX}$	Auxiliary supply voltage relative to GND	3.2	3.3	3.45	V
$R_{FUSE}^{(3)}$	External resistor from $R_{FUSE}$ pin to GND	1129	1140	1151	$\Omega$
$V_{CCINT}$	Internal supply voltage relative to GND	1.14	1.2	1.26	V
$t_j$	Temperature range	15	–	85	$^{\circ}\text{C}$

**Notes:**

1. These specifications apply during programming of the eFUSE AES key. Programming is only supported through JTAG. The AES key is only supported in the following devices: LX75, LX75T, LX100, LX100T, LX150, and LX150T.
2. When programming eFUSE,  $V_{FS}$  must be less than or equal to  $V_{CCAUX}$ . When not programming or when eFUSE is not used, Xilinx recommends connecting  $V_{FS}$  to GND. However,  $V_{FS}$  can be between GND and 3.45 V.
3. An  $R_{FUSE}$  resistor is required when programming the eFUSE AES key. When not programming or when eFUSE is not used, Xilinx recommends connecting the  $R_{FUSE}$  pin to  $V_{CCAUX}$  or GND. However,  $R_{FUSE}$  can be unconnected.

Table 5: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
I <sub>CCAUXQ</sub>	Quiescent V <sub>CCAUX</sub> supply current	LX4	2.5	2.5	2.5	2.5	mA
		LX9	2.5	2.5	2.5	2.5	mA
		LX16	3.0	3.0	3.0	3.0	mA
		LX25	4.0	4.0	4.0	4.0	mA
		LX25T	4.0	4.0	4.0	N/A	mA
		LX45	5.0	5.0	5.0	5.0	mA
		LX45T	5.0	5.0	5.0	N/A	mA
		LX75	7.0	7.0	7.0	7.0	mA
		LX75T	7.0	7.0	7.0	N/A	mA
		LX100	9.0	9.0	9.0	9.0	mA
		LX100T	9.0	9.0	9.0	N/A	mA
		LX150	12.0	12.0	12.0	12.0	mA
		LX150T	12.0	12.0	12.0	N/A	mA

**Notes:**

1. Typical values are specified at nominal voltage, 25°C junction temperatures (T<sub>j</sub>). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 25°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. Nominal V<sub>CCINT</sub> is 1.20V; use the XPE tool to calculate 1.23V values for the nominal V<sub>CCINT</sub> of the extended performance range.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 6: Power Supply Ramp Time

Symbol	Description	Speed Grade	Ramp Time	Units
V <sub>CCINTR</sub>	Internal supply voltage ramp time	-3, -3N, -2	0.20 to 50.0	ms
		-1L	0.20 to 40.0	ms
V <sub>CCO2</sub> <sup>(1)</sup>	Output drivers bank 2 supply voltage ramp time	All	0.20 to 50.0	ms
V <sub>CCAUXR</sub>	Auxiliary supply voltage ramp time	All	0.20 to 50.0	ms

**Notes:**

1. The minimum V<sub>CCO2</sub> for power-on reset and configuration is 1.65V.
2. Spartan-6 FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply. Use the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools to estimate current drain on these supplies. Spartan-6 devices do not have a required power-on sequence.

## SelectIO™ Interface DC Input and Output Levels

Table 7: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

I/O Standard	V <sub>CCO</sub> for Drivers <sup>(1)</sup>			V <sub>REF</sub> for Inputs		
	V, Min	V, Nom	V, Max	V, Min	V, Nom	V, Max
LVTTTL	3.0	3.3	3.45	V <sub>REF</sub> is not used for these I/O standards		
LVC MOS33	3.0	3.3	3.45			
LVC MOS25	2.3	2.5	2.7			
LVC MOS18	1.65	1.8	1.95			
LVC MOS18_JEDEC	1.65	1.8	1.95			
LVC MOS15	1.4	1.5	1.6			
LVC MOS15_JEDEC	1.4	1.5	1.6			
LVC MOS12	1.1	1.2	1.3			
LVC MOS12_JEDEC	1.1	1.2	1.3			
PCI33_3 <sup>(2)</sup>	3.0	3.3	3.45			
PCI66_3 <sup>(2)</sup>	3.0	3.3	3.45			
I2C	2.7	3.0	3.45			
SMBUS	2.7	3.0	3.45			
SDIO	3.0	3.3	3.45			
MOBILE_DDR	1.7	1.8	1.9			
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_II	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_III	1.4	1.5	1.6	–	0.9	–
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–
HSTL_III_18	1.7	1.8	1.9	–	1.1	–
SSTL3_I	3.0	3.3	3.45	1.3	1.5	1.7
SSTL3_II	3.0	3.3	3.45	1.3	1.5	1.7
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38
SSTL18_I	1.7	1.8	1.9	0.833	0.9	0.969
SSTL18_II	1.7	1.8	1.9	0.833	0.9	0.969
SSTL15_II	1.425	1.5	1.575	0.69	0.75	0.81

### Notes:

1. V<sub>CCO</sub> range required when using I/O standard for an output. Also required for MOBILE\_DDR, PCI33\_3, LVC MOS18\_JEDEC, LVC MOS15\_JEDEC, and LVC MOS12\_JEDEC inputs, and for LVC MOS25 inputs when V<sub>CCAUX</sub> = 3.3V.
2. For PCI systems, the transmitter and receiver should have common supplies for V<sub>CCO</sub>.

Table 8: Recommended Operating Conditions for User I/Os Using Differential Signal Standards

I/O Standard	V <sub>CCO</sub> for Drivers		
	V, Min	V, Nom	V, Max
LVDS_33	3.0	3.3	3.45
LVDS_25	2.25	2.5	2.75
BLVDS_25	2.25	2.5	2.75
MINI_LVDS_33	3.0	3.3	3.45
MINI_LVDS_25	2.25	2.5	2.75
LVPECL_33 <sup>(1)</sup>	N/A—Inputs Only		
LVPECL_25	N/A—Inputs Only		
RSDS_33	3.0	3.3	3.45
RSDS_25	2.25	2.5	2.75
TMDS_33 <sup>(1)</sup>	3.14	3.3	3.45
PPDS_33	3.0	3.3	3.45
PPDS_25	2.25	2.5	2.75
DISPLAY_PORT	2.3	2.5	2.7
DIFF_MOBILE_DDR	1.7	1.8	1.9
DIFF_HSTL_I	1.4	1.5	1.6
DIFF_HSTL_II	1.4	1.5	1.6
DIFF_HSTL_III	1.4	1.5	1.6
DIFF_HSTL_I_18	1.7	1.8	1.9
DIFF_HSTL_II_18	1.7	1.8	1.9
DIFF_HSTL_III_18	1.7	1.8	1.9
DIFF_SSTL3_I	3.0	3.3	3.45
DIFF_SSTL3_II	3.0	3.3	3.45
DIFF_SSTL2_I	2.3	2.5	2.7
DIFF_SSTL2_II	2.3	2.5	2.7
DIFF_SSTL18_I	1.7	1.8	1.9
DIFF_SSTL18_II	1.7	1.8	1.9
DIFF_SSTL15_II	1.425	1.5	1.575

**Notes:**

1. LVPECL\_33 and TMDS\_33 inputs require V<sub>CCAUX</sub> = 3.3V nominal.

Table 10: Differential I/O Standard DC Input and Output Levels

I/O Standard	V <sub>ID</sub>		V <sub>ICM</sub>		V <sub>OD</sub>		V <sub>OCM</sub>		V <sub>OH</sub>	V <sub>OL</sub>
	mV, Min	mV, Max	V, Min	V, Max	mV, Min	mV, Max	V, Min	V, Max	V, Min	V, Max
LVDS_33 <sup>(2)(3)</sup>	100	600	0.3	2.35	247	454	1.125	1.375	–	–
LVDS_25 <sup>(2)(3)</sup>	100	600	0.3	2.35	247	454	1.125	1.375	–	–
BLVDS_25 <sup>(2)(3)</sup>	100	–	0.3	2.35	240	460	Typical 50% V <sub>CCO</sub>		–	–
MINI_LVDS_33	200	600	0.3	1.95	300	600	1.0	1.4	–	–
MINI_LVDS_25	200	600	0.3	1.95	300	600	1.0	1.4	–	–
LVPECL_33 <sup>(2)(3)</sup>	100	1000	0.3	2.8 <sup>(1)</sup>	Inputs only					
LVPECL_25 <sup>(2)(3)</sup>	100	1000	0.3	1.95	Inputs only					
RSDS_33 <sup>(2)(3)</sup>	100	–	0.3	1.5	100	400	1.0	1.4	–	–
RSDS_25 <sup>(2)(3)</sup>	100	–	0.3	1.5	100	400	1.0	1.4	–	–
TMDS_33	150	1200	2.7	3.23 <sup>(1)</sup>	400	800	V <sub>CCO</sub> – 0.405	V <sub>CCO</sub> – 0.190	–	–
PPDS_33 <sup>(2)(3)</sup>	100	400	0.2	2.3	100	400	0.5	1.4	–	–
PPDS_25 <sup>(2)(3)</sup>	100	400	0.2	2.3	100	400	0.5	1.4	–	–
DISPLAY_PORT	190	1260	0.3	2.35	–	–	Typical 50% V <sub>CCO</sub>		–	–
DIFF_MOBILE_DDR	100	–	0.78	1.02	–	–	–	–	90% V <sub>CCO</sub>	10% V <sub>CCO</sub>
DIFF_HSTL_I	100	–	0.68	0.9	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_HSTL_II	100	–	0.68	0.9	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_HSTL_III	100	–	0.68	0.9	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_HSTL_I_18	100	–	0.8	1.1	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_HSTL_II_18	100	–	0.8	1.1	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_HSTL_III_18	100	–	0.8	1.1	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_SSTL3_I	100	–	1.0	1.9	–	–	–	–	V <sub>TT</sub> + 0.6	V <sub>TT</sub> – 0.6
DIFF_SSTL3_II	100	–	1.0	1.9	–	–	–	–	V <sub>TT</sub> + 0.8	V <sub>TT</sub> – 0.8
DIFF_SSTL2_I	100	–	1.0	1.5	–	–	–	–	V <sub>TT</sub> + 0.61	V <sub>TT</sub> – 0.61
DIFF_SSTL2_II	100	–	1.0	1.5	–	–	–	–	V <sub>TT</sub> + 0.81	V <sub>TT</sub> – 0.81
DIFF_SSTL18_I	100	–	0.7	1.1	–	–	–	–	V <sub>TT</sub> + 0.47	V <sub>TT</sub> – 0.47
DIFF_SSTL18_II	100	–	0.7	1.1	–	–	–	–	V <sub>TT</sub> + 0.6	V <sub>TT</sub> – 0.6
DIFF_SSTL15_II	100	–	0.55	0.95	–	–	–	–	V <sub>TT</sub> + 0.4	V <sub>TT</sub> – 0.4

**Notes:**

1. LVPECL\_33 and TMDS\_33 maximum V<sub>ICM</sub> is the lower of V (maximum) or V<sub>CCAUX</sub> – (V<sub>ID</sub>/2)
2. When V<sub>CCAUX</sub> = 3.3V, the DCD can be higher than 5% for V<sub>ICM</sub> < 0.7V when using these I/O standards: LVDS\_25, LVDS\_33, BLVDS\_25, LVPECL\_25, LVPECL\_33, RSDS\_25, RSDS\_33, PPDS\_25, and PPDS\_33.
3. The -1L devices require V<sub>CCAUX</sub> = 2.5V when using the LVDS\_25, LVDS\_33, BLVDS\_25, LVPECL\_25, RSDS\_25, RSDS\_33, PPDS\_25, and PPDS\_33 I/O standards on inputs. LVPECL\_33 is not supported in the -1L devices.

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [Switching Characteristics, page 19](#).

Table 25: Interface Performances

Description	I/O Resource	Clock Buffer	Data Width	Speed Grade				Units
				-3	-3N	-2	-1L	
<b>Networking Applications<sup>(1)</sup></b>								
SDR LVDS transmitter or receiver	IOB SDR register	BUFG	–	400	400	375	250	Mb/s
DDR LVDS transmitter or receiver	ODDR2/IDDR2 register	2 BUFGs	–	800	800	750	500	Mb/s
SDR LVDS transmitter	OSERDES2	BUFPLL	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
DDR LVDS transmitter	OSERDES2	2 BUFIO2s	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
SDR LVDS receiver	ISERDES2 in RETIMED mode	BUFPLL	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
DDR LVDS receiver	ISERDES2 in RETIMED mode	2 BUFIO2s	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
<b>Memory Interfaces (Implemented using the Spartan-6 FPGA Memory Controller Block)<sup>(2)</sup></b>								
<b>Standard Performance (Standard V<sub>CCINT</sub>)</b>								
DDR				400	<a href="#">Note 4</a>	400	350	Mb/s
DDR2				667	<a href="#">Note 4</a>	625	400	Mb/s
DDR3				800	<a href="#">Note 4</a>	667	—	Mb/s
LPDDR (Mobile_DDR)				400	<a href="#">Note 4</a>	400	350	Mb/s
<b>Extended Performance (Requires Extended Performance V<sub>CCINT</sub>)<sup>(3)</sup></b>								
DDR2				800	<a href="#">Note 4</a>	667	—	Mb/s

**Notes:**

1. Refer to [XAPP1064](#), *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)* and [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.
2. Refer to [UG388](#), *Spartan-6 FPGA Memory Controller User Guide*.
3. Extended Memory Controller block performance for DDR2 can be achieved using the extended performance V<sub>CCINT</sub> range from [Table 2](#).
4. The LX4 device, all devices in the TQG144 and CPG196 packages, and the -3N speed grade do not support a Memory Controller Block.

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T <sub>IOPI</sub>				T <sub>IOOP</sub>				T <sub>IOTP</sub>				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	
PPDS_33	1.17	1.29	1.42	1.68	1.57	1.71	1.91	2.43	3000	3000	3000	3000	ns
PPDS_25	1.01	1.13	1.26	1.56	1.68	1.82	2.02	2.47	3000	3000	3000	3000	ns
PCI33_3	1.07	1.19	1.32	1.57 <sup>(2)</sup>	3.51	3.65	3.85	4.38 <sup>(2)</sup>	3.51	3.65	3.85	4.38 <sup>(1)</sup>	ns
PCI66_3	1.07	1.19	1.32	1.57 <sup>(2)</sup>	3.53	3.67	3.87	4.39 <sup>(2)</sup>	3.53	3.67	3.87	4.39 <sup>(1)</sup>	ns
DISPLAY_PORT	1.02	1.14	1.27	1.56	3.15	3.29	3.49	4.08	3.15	3.29	3.49	4.08	ns
I2C	1.33	1.45	1.58	1.82	11.56	11.70	11.90	12.52	11.56	11.70	11.90	12.52	ns
SMBUS	1.33	1.45	1.58	1.82	11.56	11.70	11.90	12.52	11.56	11.70	11.90	12.52	ns
SDIO	1.36	1.48	1.61	1.84	2.64	2.78	2.98	3.60	2.64	2.78	2.98	3.60	ns
MOBILE_DDR	0.94	1.06	1.19	1.43	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns
HSTL_I	0.90	1.02	1.15	1.39	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
HSTL_II	0.91	1.03	1.16	1.40	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
HSTL_III	0.95	1.07	1.20	1.44	1.67	1.81	2.01	2.61	1.67	1.81	2.01	2.61	ns
HSTL_I_18	0.94	1.06	1.19	1.43	1.77	1.91	2.11	2.73	1.77	1.91	2.11	2.73	ns
HSTL_II_18	0.94	1.06	1.19	1.43	1.85	1.99	2.19	2.81	1.85	1.99	2.19	2.81	ns
HSTL_III_18	0.99	1.11	1.24	1.47	1.79	1.93	2.13	2.72	1.79	1.93	2.13	2.72	ns
SSTL3_I	1.58	1.70	1.83	2.16	1.83	1.97	2.17	2.72	1.83	1.97	2.17	2.72	ns
SSTL3_II	1.58	1.70	1.83	2.16	2.01	2.15	2.35	2.94	2.01	2.15	2.35	2.94	ns
SSTL2_I	1.30	1.42	1.55	1.87	1.77	1.91	2.11	2.69	1.77	1.91	2.11	2.69	ns
SSTL2_II	1.30	1.42	1.55	1.88	1.86	2.00	2.20	2.82	1.86	2.00	2.20	2.82	ns
SSTL18_I	0.92	1.04	1.17	1.41	1.63	1.77	1.97	2.59	1.63	1.77	1.97	2.59	ns
SSTL18_II	0.92	1.04	1.17	1.41	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
SSTL15_II	0.92	1.04	1.17	1.41	1.67	1.81	2.01	2.63	1.67	1.81	2.01	2.63	ns
DIFF_HSTL_I	0.94	1.06	1.19	1.46	1.77	1.91	2.11	2.62	1.77	1.91	2.11	2.62	ns
DIFF_HSTL_II	0.93	1.05	1.18	1.45	1.72	1.86	2.06	2.54	1.72	1.86	2.06	2.54	ns
DIFF_HSTL_III	0.93	1.05	1.18	1.46	1.69	1.83	2.03	2.53	1.69	1.83	2.03	2.53	ns
DIFF_HSTL_I_18	0.97	1.09	1.22	1.50	1.79	1.93	2.13	2.63	1.79	1.93	2.13	2.63	ns
DIFF_HSTL_II_18	0.97	1.09	1.22	1.49	1.69	1.83	2.03	2.51	1.69	1.83	2.03	2.51	ns
DIFF_HSTL_III_18	0.97	1.09	1.22	1.50	1.69	1.83	2.03	2.53	1.69	1.83	2.03	2.53	ns
DIFF_SSTL3_I	1.18	1.30	1.43	1.68	1.81	1.95	2.15	2.64	1.81	1.95	2.15	2.64	ns
DIFF_SSTL3_II	1.19	1.31	1.44	1.68	1.80	1.94	2.14	2.63	1.80	1.94	2.14	2.63	ns
DIFF_SSTL2_I	1.02	1.14	1.27	1.57	1.80	1.94	2.14	2.62	1.80	1.94	2.14	2.62	ns
DIFF_SSTL2_II	1.02	1.14	1.27	1.57	1.76	1.90	2.10	2.57	1.76	1.90	2.10	2.57	ns
DIFF_SSTL18_I	0.97	1.09	1.22	1.51	1.72	1.86	2.06	2.56	1.72	1.86	2.06	2.56	ns
DIFF_SSTL18_II	0.98	1.10	1.23	1.50	1.68	1.82	2.02	2.52	1.68	1.82	2.02	2.52	ns
DIFF_SSTL15_II	0.94	1.06	1.19	1.46	1.67	1.81	2.01	2.50	1.67	1.81	2.01	2.50	ns
DIFF_MOBILE_DDR	0.97	1.09	1.22	1.51	1.75	1.89	2.09	2.57	1.75	1.89	2.09	2.57	ns



Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T <sub>IOPI</sub>				T <sub>IOOP</sub>				T <sub>IOTP</sub>				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	
LVC MOS33, Fast, 8 mA	1.34	1.46	1.59	1.82	2.07	2.21	2.41	3.03	2.07	2.21	2.41	3.03	ns
LVC MOS33, Fast, 12 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns
LVC MOS33, Fast, 16 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns
LVC MOS33, Fast, 24 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns
LVC MOS25, QUIETIO, 2 mA	0.82	0.94	1.07	1.31	4.81	4.95	5.15	5.79	4.81	4.95	5.15	5.79	ns
LVC MOS25, QUIETIO, 4 mA	0.82	0.94	1.07	1.31	3.70	3.84	4.04	4.66	3.70	3.84	4.04	4.66	ns
LVC MOS25, QUIETIO, 6 mA	0.82	0.94	1.07	1.31	3.46	3.60	3.80	4.38	3.46	3.60	3.80	4.38	ns
LVC MOS25, QUIETIO, 8 mA	0.82	0.94	1.07	1.31	3.20	3.34	3.54	4.12	3.20	3.34	3.54	4.12	ns
LVC MOS25, QUIETIO, 12 mA	0.82	0.94	1.07	1.31	2.83	2.97	3.17	3.75	2.83	2.97	3.17	3.75	ns
LVC MOS25, QUIETIO, 16 mA	0.82	0.94	1.07	1.31	2.64	2.78	2.98	3.64	2.64	2.78	2.98	3.64	ns
LVC MOS25, QUIETIO, 24 mA	0.82	0.94	1.07	1.31	2.45	2.59	2.79	3.42	2.45	2.59	2.79	3.42	ns
LVC MOS25, Slow, 2 mA	0.82	0.94	1.07	1.31	3.78	3.92	4.12	4.76	3.78	3.92	4.12	4.76	ns
LVC MOS25, Slow, 4 mA	0.82	0.94	1.07	1.31	2.79	2.93	3.13	3.73	2.79	2.93	3.13	3.73	ns
LVC MOS25, Slow, 6 mA	0.82	0.94	1.07	1.31	2.73	2.87	3.07	3.66	2.73	2.87	3.07	3.66	ns
LVC MOS25, Slow, 8 mA	0.82	0.94	1.07	1.31	2.48	2.62	2.82	3.42	2.48	2.62	2.82	3.42	ns
LVC MOS25, Slow, 12 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.95	2.01	2.15	2.35	2.95	ns
LVC MOS25, Slow, 16 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.95	2.01	2.15	2.35	2.95	ns
LVC MOS25, Slow, 24 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.94	2.01	2.15	2.35	2.94	ns
LVC MOS25, Fast, 2 mA	0.82	0.94	1.07	1.31	3.35	3.49	3.69	4.31	3.35	3.49	3.69	4.31	ns
LVC MOS25, Fast, 4 mA	0.82	0.94	1.07	1.31	2.25	2.39	2.59	3.22	2.25	2.39	2.59	3.22	ns
LVC MOS25, Fast, 6 mA	0.82	0.94	1.07	1.31	2.09	2.23	2.43	3.05	2.09	2.23	2.43	3.05	ns
LVC MOS25, Fast, 8 mA	0.82	0.94	1.07	1.31	2.02	2.16	2.36	2.98	2.02	2.16	2.36	2.98	ns
LVC MOS25, Fast, 12 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns
LVC MOS25, Fast, 16 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns
LVC MOS25, Fast, 24 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns
LVC MOS18, QUIETIO, 2 mA	1.18	1.30	1.43	2.04	5.92	6.06	6.26	6.80	5.92	6.06	6.26	6.80	ns
LVC MOS18, QUIETIO, 4 mA	1.18	1.30	1.43	2.04	4.74	4.88	5.08	5.63	4.74	4.88	5.08	5.63	ns
LVC MOS18, QUIETIO, 6 mA	1.18	1.30	1.43	2.04	4.05	4.19	4.39	4.96	4.05	4.19	4.39	4.96	ns
LVC MOS18, QUIETIO, 8 mA	1.18	1.30	1.43	2.04	3.71	3.85	4.05	4.63	3.71	3.85	4.05	4.63	ns
LVC MOS18, QUIETIO, 12 mA	1.18	1.30	1.43	2.04	3.35	3.49	3.69	4.27	3.35	3.49	3.69	4.27	ns
LVC MOS18, QUIETIO, 16 mA	1.18	1.30	1.43	2.04	3.20	3.34	3.54	4.14	3.20	3.34	3.54	4.14	ns
LVC MOS18, QUIETIO, 24 mA	1.18	1.30	1.43	2.04	2.96	3.10	3.30	3.98	2.96	3.10	3.30	3.98	ns
LVC MOS18, Slow, 2 mA	1.18	1.30	1.43	2.04	4.62	4.76	4.96	5.54	4.62	4.76	4.96	5.54	ns
LVC MOS18, Slow, 4 mA	1.18	1.30	1.43	2.04	3.69	3.83	4.03	4.60	3.69	3.83	4.03	4.60	ns
LVC MOS18, Slow, 6 mA	1.18	1.30	1.43	2.04	3.00	3.14	3.34	3.94	3.00	3.14	3.34	3.94	ns
LVC MOS18, Slow, 8 mA	1.18	1.30	1.43	2.04	2.19	2.33	2.53	3.17	2.19	2.33	2.53	3.17	ns
LVC MOS18, Slow, 12 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVC MOS18, Slow, 16 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns

**Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices<sup>(1)</sup>**

I/O Standard	T <sub>IOPI</sub>		T <sub>IOOP</sub>		T <sub>IOTP</sub>		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVDS_33	1.24	1.42	1.69	1.89	3000	3000	ns
LVDS_25	1.08	1.26	1.79	1.99	3000	3000	ns
BLVDS_25	1.09	1.27	1.86	2.06	1.86	2.06	ns
MINI_LVDS_33	1.25	1.43	1.71	1.91	3000	3000	ns
MINI_LVDS_25	1.08	1.26	1.79	1.99	3000	3000	ns
LVPECL_33	1.25	1.43	N/A	N/A	N/A	N/A	ns
LVPECL_25	1.09	1.27	N/A	N/A	N/A	N/A	ns
RSDS_33 (point to point)	1.24	1.42	1.71	1.91	3000	3000	ns
RSDS_25 (point to point)	1.08	1.26	1.79	1.99	3000	3000	ns
TMDS_33	1.29	1.47	1.68	1.88	3000	3000	ns
PPDS_33	1.25	1.43	1.71	1.91	3000	3000	ns
PPDS_25	1.08	1.26	1.82	2.02	3000	3000	ns
PCI33_3	1.14	1.32	3.81	4.01	3.81	4.01	ns
PCI66_3	1.14	1.32	3.81	4.01	3.81	4.01	ns
DISPLAY_PORT	1.09	1.27	3.29	3.49	3.29	3.49	ns
I2C	1.40	1.58	11.70	11.90	11.70	11.90	ns
SMBUS	1.40	1.58	11.70	11.90	11.70	11.90	ns
SDIO	1.43	1.61	2.78	2.98	2.78	2.98	ns
MOBILE_DDR	1.01	1.19	2.50	2.70	2.50	2.70	ns
HSTL_I	1.01	1.19	1.80	2.00	1.80	2.00	ns
HSTL_II	1.01	1.19	1.86	2.06	1.86	2.06	ns
HSTL_III	1.07	1.25	1.81	2.01	1.81	2.01	ns
HSTL_I_18	1.05	1.23	1.91	2.11	1.91	2.11	ns
HSTL_II_18	1.05	1.23	1.99	2.19	1.99	2.19	ns
HSTL_III_18	1.13	1.31	1.93	2.13	1.93	2.13	ns
SSTL3_I	1.65	1.83	1.97	2.17	1.97	2.17	ns
SSTL3_II	1.65	1.83	2.15	2.35	2.15	2.35	ns
SSTL2_I	1.37	1.55	1.91	2.11	1.91	2.11	ns
SSTL2_II	1.37	1.55	2.00	2.20	2.00	2.20	ns
SSTL18_I	0.99	1.17	1.77	1.97	1.77	1.97	ns
SSTL18_II	1.00	1.18	1.80	2.00	1.80	2.00	ns
SSTL15_II	1.00	1.18	1.81	2.01	1.81	2.01	ns
DIFF_HSTL_I	1.01	1.19	1.91	2.11	1.91	2.11	ns
DIFF_HSTL_II	1.00	1.18	1.86	2.06	1.86	2.06	ns
DIFF_HSTL_III	1.00	1.18	1.83	2.03	1.83	2.03	ns
DIFF_HSTL_I_18	1.04	1.22	1.93	2.13	1.93	2.13	ns
DIFF_HSTL_II_18	1.04	1.22	1.83	2.03	1.83	2.03	ns
DIFF_HSTL_III_18	1.04	1.22	1.83	2.03	1.83	2.03	ns

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices<sup>(1)</sup> (Cont'd)

I/O Standard	T <sub>IOPI</sub>		T <sub>IOOP</sub>		T <sub>IOTP</sub>		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS33, Slow, 6 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVC MOS33, Slow, 8 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVC MOS33, Slow, 12 mA	1.41	1.59	2.53	2.73	2.53	2.73	ns
LVC MOS33, Slow, 16 mA	1.41	1.59	2.45	2.65	2.45	2.65	ns
LVC MOS33, Slow, 24 mA	1.41	1.59	2.42	2.62	2.42	2.62	ns
LVC MOS33, Fast, 2 mA	1.41	1.59	4.05	4.25	4.05	4.25	ns
LVC MOS33, Fast, 4 mA	1.41	1.59	2.66	2.86	2.66	2.86	ns
LVC MOS33, Fast, 6 mA	1.41	1.59	2.46	2.66	2.46	2.66	ns
LVC MOS33, Fast, 8 mA	1.41	1.59	2.21	2.41	2.21	2.41	ns
LVC MOS33, Fast, 12 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVC MOS33, Fast, 16 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVC MOS33, Fast, 24 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVC MOS25, QUIETIO, 2 mA	0.89	1.07	5.00	5.20	5.00	5.20	ns
LVC MOS25, QUIETIO, 4 mA	0.89	1.07	3.85	4.05	3.85	4.05	ns
LVC MOS25, QUIETIO, 6 mA	0.89	1.07	3.60	3.80	3.60	3.80	ns
LVC MOS25, QUIETIO, 8 mA	0.89	1.07	3.34	3.54	3.34	3.54	ns
LVC MOS25, QUIETIO, 12 mA	0.89	1.07	2.98	3.18	2.98	3.18	ns
LVC MOS25, QUIETIO, 16 mA	0.89	1.07	2.79	2.99	2.79	2.99	ns
LVC MOS25, QUIETIO, 24 mA	0.89	1.07	2.64	2.84	2.64	2.84	ns
LVC MOS25, Slow, 2 mA	0.89	1.07	3.96	4.16	3.96	4.16	ns
LVC MOS25, Slow, 4 mA	0.89	1.07	2.96	3.16	2.96	3.16	ns
LVC MOS25, Slow, 6 mA	0.89	1.07	2.88	3.08	2.88	3.08	ns
LVC MOS25, Slow, 8 mA	0.89	1.07	2.63	2.83	2.63	2.83	ns
LVC MOS25, Slow, 12 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVC MOS25, Slow, 16 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVC MOS25, Slow, 24 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVC MOS25, Fast, 2 mA	0.89	1.07	3.52	3.72	3.52	3.72	ns
LVC MOS25, Fast, 4 mA	0.89	1.07	2.43	2.63	2.43	2.63	ns
LVC MOS25, Fast, 6 mA	0.89	1.07	2.23	2.43	2.23	2.43	ns
LVC MOS25, Fast, 8 mA	0.89	1.07	2.16	2.36	2.16	2.36	ns
LVC MOS25, Fast, 12 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVC MOS25, Fast, 16 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVC MOS25, Fast, 24 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVC MOS18, QUIETIO, 2 mA	1.25	1.43	6.11	6.31	6.11	6.31	ns
LVC MOS18, QUIETIO, 4 mA	1.25	1.43	4.88	5.08	4.88	5.08	ns
LVC MOS18, QUIETIO, 6 mA	1.25	1.43	4.20	4.40	4.20	4.40	ns
LVC MOS18, QUIETIO, 8 mA	1.25	1.43	3.86	4.06	3.86	4.06	ns
LVC MOS18, QUIETIO, 12 mA	1.25	1.43	3.49	3.69	3.49	3.69	ns

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices<sup>(1)</sup> (Cont'd)

I/O Standard	T <sub>IOPI</sub>		T <sub>IOOP</sub>		T <sub>IOTP</sub>		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS12, QUIETIO, 6 mA	0.98	1.16	4.79	4.99	4.79	4.99	ns
LVC MOS12, QUIETIO, 8 mA	0.98	1.16	4.43	4.63	4.43	4.63	ns
LVC MOS12, QUIETIO, 12 mA	0.98	1.16	4.18	4.38	4.18	4.38	ns
LVC MOS12, Slow, 2 mA	0.98	1.16	5.12	5.32	5.12	5.32	ns
LVC MOS12, Slow, 4 mA	0.98	1.16	3.00	3.20	3.00	3.20	ns
LVC MOS12, Slow, 6 mA	0.98	1.16	2.91	3.11	2.91	3.11	ns
LVC MOS12, Slow, 8 mA	0.98	1.16	2.51	2.71	2.51	2.71	ns
LVC MOS12, Slow, 12 mA	0.98	1.16	2.25	2.45	2.25	2.45	ns
LVC MOS12, Fast, 2 mA	0.98	1.16	3.60	3.80	3.60	3.80	ns
LVC MOS12, Fast, 4 mA	0.98	1.16	2.49	2.69	2.49	2.69	ns
LVC MOS12, Fast, 6 mA	0.98	1.16	1.94	2.14	1.94	2.14	ns
LVC MOS12, Fast, 8 mA	0.98	1.16	1.82	2.02	1.82	2.02	ns
LVC MOS12, Fast, 12 mA	0.98	1.16	1.80	2.00	1.80	2.00	ns
LVC MOS12_JEDEC, QUIETIO, 2 mA	1.57	1.75	6.53	6.73	6.53	6.73	ns
LVC MOS12_JEDEC, QUIETIO, 4 mA	1.57	1.75	5.12	5.32	5.12	5.32	ns
LVC MOS12_JEDEC, QUIETIO, 6 mA	1.57	1.75	4.81	5.01	4.81	5.01	ns
LVC MOS12_JEDEC, QUIETIO, 8 mA	1.57	1.75	4.44	4.64	4.44	4.64	ns
LVC MOS12_JEDEC, QUIETIO, 12 mA	1.57	1.75	4.20	4.40	4.20	4.40	ns
LVC MOS12_JEDEC, Slow, 2 mA	1.57	1.75	5.14	5.34	5.14	5.34	ns
LVC MOS12_JEDEC, Slow, 4 mA	1.57	1.75	2.99	3.19	2.99	3.19	ns
LVC MOS12_JEDEC, Slow, 6 mA	1.57	1.75	2.90	3.10	2.90	3.10	ns
LVC MOS12_JEDEC, Slow, 8 mA	1.57	1.75	2.50	2.70	2.50	2.70	ns
LVC MOS12_JEDEC, Slow, 12 mA	1.57	1.75	2.26	2.46	2.26	2.46	ns
LVC MOS12_JEDEC, Fast, 2 mA	1.57	1.75	3.60	3.80	3.60	3.80	ns
LVC MOS12_JEDEC, Fast, 4 mA	1.57	1.75	2.49	2.69	2.49	2.69	ns
LVC MOS12_JEDEC, Fast, 6 mA	1.57	1.75	1.94	2.14	1.94	2.14	ns
LVC MOS12_JEDEC, Fast, 8 mA	1.57	1.75	1.83	2.03	1.83	2.03	ns
LVC MOS12_JEDEC, Fast, 12 mA	1.57	1.75	1.80	2.00	1.80	2.00	ns

**Notes:**

1. The Spartan-6Q FPGA -1L values are listed in Table 28.

Table 30 summarizes the value of T<sub>IOTPHZ</sub>. T<sub>IOTPHZ</sub> is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). These delays are measured using LVC MOS25, Fast, 12 mA.

Table 30: IOB 3-state ON Output Switching Characteristics (T<sub>IOTPHZ</sub>)

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T <sub>IOTPHZ</sub>	T input to Pad high-impedance	1.39	1.59	1.59	1.91	ns

Table 34: SSO Limit per V<sub>CC0</sub>/GND Pair (Cont'd)

V <sub>CC0</sub>	I/O Standard	Drive	Slew	SSO Limit per V <sub>CC0</sub> /GND Pair					
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324			
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5		
1.5V	LVCMOS15, LVCMOS15_JEDEC	2	Fast	33	40	33	41		
			Slow	57	62	57	56		
			QuietIO	70	67	70	66		
		4	Fast	19	21	19	21		
			Slow	30	30	30	24		
			QuietIO	38	33	38	30		
		6	Fast	14	16	14	16		
			Slow	18	19	18	17		
			QuietIO	27	24	27	21		
		8	Fast	11	13	11	12		
			Slow	16	16	16	14		
			QuietIO	23	20	23	17		
		12	Fast	N/A	5	N/A	4		
			Slow	N/A	8	N/A	5		
			QuietIO	N/A	10	N/A	9		
		16	Fast	N/A	5	N/A	4		
			Slow	N/A	8	N/A	8		
			QuietIO	N/A	10	N/A	9		
		HSTL_I				9	10	9	10
		HSTL_II				N/A	5	N/A	6
HSTL_III				7	9	7	9		
DIFF_HSTL_I				27	30	27	30		
DIFF_HSTL_II				N/A	15	N/A	18		
DIFF_HSTL_III				21	27	21	27		
SSTL_15_II <sup>(3)</sup>				N/A	5	N/A	4		
DIFF_SSTL_15_II <sup>(3)</sup>				N/A	15	N/A	12		

Table 34: SSO Limit per V<sub>CCO</sub>/GND Pair (Cont'd)

V <sub>CCO</sub>	I/O Standard	Drive	Slew	SSO Limit per V <sub>CCO</sub> /GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
Various	LVDS_33			16	N/A	16	N/A
	LVDS_25			20	N/A	20	N/A
	BLVDS_25			20	48	20	20
	MINI_LVDS_33			13	N/A	13	N/A
	MINI_LVDS_25			18	N/A	18	N/A
	RSDS_33			12	N/A	12	N/A
	RSDS_25			15	N/A	15	N/A
	TMDS_33			83	N/A	83	N/A
	PPDS_33			12	N/A	12	N/A
	PPDS_25			16	N/A	16	N/A
	DISPLAY_PORT			42	40	42	30
	I2C			47	55	47	42
	SMBUS			44	52	44	40

**Notes:**

1. SSO limits greater than the number of I/O per V<sub>CCO</sub>/GND pair (Table 33) indicate No Limit for the given I/O standard. They are provided in this table to calculate limits when using multiple I/O standards in a bank.
2. Not available (N/A) indicates that the I/O standard is not available in the given bank.
3. When used with the MCB, these signals are exempt from SSO analysis due to the known activity of the MCB switching patterns. SSO performance is validated for all MCB instances. MCB outputs can, in some cases, exceed the SSO limits.

## DCM Switching Characteristics

Table 53: Operating Frequency Ranges and Conditions for the Delay-Locked Loop (DLL)<sup>(1)</sup>

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
<b>Input Frequency Ranges</b>										
CLKIN_FREQ_DLL	Frequency of the CLKIN clock input when the CLKDV output is not used.	5 <sup>(2)</sup>	280 <sup>(3)</sup>	5 <sup>(2)</sup>	280 <sup>(3)</sup>	5 <sup>(2)</sup>	250 <sup>(3)</sup>	5 <sup>(2)</sup>	175 <sup>(3)</sup>	MHz
	Frequency of the CLKIN clock input when using the CLKDV output.	5 <sup>(2)</sup>	280 <sup>(3)</sup>	5 <sup>(2)</sup>	280 <sup>(3)</sup>	5 <sup>(2)</sup>	250 <sup>(3)</sup>	5 <sup>(2)</sup>	133 <sup>(3)</sup>	MHz
<b>Input Pulse Requirements</b>										
CLKIN_PULSE	CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL < 150 MHz	40	60	40	60	40	60	40	60	%
	CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL > 150 MHz	45	55	45	55	45	55	45	55	%
<b>Input Clock Jitter Tolerance and Delay Path Variation<sup>(4)</sup></b>										
CLKIN_CYC_JITT_DLL_LF	Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL < 150 MHz	–	±300	–	±300	–	±300	–	±300	ps
CLKIN_CYC_JITT_DLL_HF	Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL > 150 MHz.	–	±150	–	±150	–	±150	–	±150	ps
CLKIN_PER_JITT_DLL	Period jitter at the CLKIN input.	–	±1	–	±1	–	±1	–	±1	ns
CLKFB_DELAY_VAR_EXT	Allowable variation of the off-chip feedback delay from the DCM output to the CLKFB input.	–	±1	–	±1	–	±1	–	±1	ns

**Notes:**

1. DLL specifications apply when using any of the DLL outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV.
2. When operating independently of the DLL, the DFS supports lower CLKIN\_FREQ\_DLL frequencies. See Table 55.
3. The CLKIN\_DIVIDE\_BY\_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the F<sub>MAX</sub> (see Table 48 and Table 49 for BUFG and BUFIO2 limits). When used with CLK\_FEEDBACK=2X, the input clock frequency matches the frequency for CLK2X, and is limited to CLKOUT\_FREQ\_2X.
4. CLKIN\_FREQ\_DLL input jitter beyond these limits can cause the DCM to lose LOCK, indicated by the LOCKED output deasserting. The user must then reset the DCM.
5. When using both DCMs in a CMT, both DCMs must be LOCKED.

Table 56: Switching Characteristics for the Digital Frequency Synthesizer (DFS) for DCM\_SP<sup>(1)</sup>

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
<b>Output Frequency Ranges</b>										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz
<b>Output Clock Jitter<sup>(2)(3)</sup></b>										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN < 20 MHz	Use the Clocking Wizard								ps
	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN > 20 MHz	Typical = ±(1% of CLKFX period + 100)								ps
<b>Duty Cycle<sup>(4)(5)</sup></b>										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±(1% of CLKFX period + 350)								ps
<b>Phase Alignment<sup>(5)</sup></b>										
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used	-	±200	-	±200	-	±200	-	±250	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used	Maximum = ±(1% of CLKFX period + 200)								ps
<b>LOCKED Time</b>										
LOCK_FX <sup>(2)</sup>	When FCLKIN < 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	-	5	-	5	-	5	-	5	ms
	When FCLKIN > 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	-	0.45	-	0.45	-	0.45	-	0.60	ms

**Notes:**

1. The values in this table are based on the operating conditions described in Table 2 and Table 55.
2. For optimal jitter tolerance and a faster LOCK time, use the CLKIN\_PERIOD attribute.
3. Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
5. Some duty cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.



**Table 66: Global Clock Input to Output Delay With PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> PLL in System-Synchronous Mode.							
T <sub>ICKOFFPLL</sub>	Global Clock and OUTFF <i>with</i> PLL	XC6SLX4	4.57	N/A	6.25	7.34	ns
		XC6SLX9	4.57	5.25	6.25	7.34	ns
		XC6SLX16	4.41	4.64	5.39	6.92	ns
		XC6SLX25	4.03	4.32	4.91	7.64	ns
		XC6SLX25T	4.03	4.32	4.91	N/A	ns
		XC6SLX45	4.63	4.96	5.75	7.36	ns
		XC6SLX45T	4.63	4.96	5.75	N/A	ns
		XC6SLX75	4.01	4.30	4.88	7.15	ns
		XC6SLX75T	4.01	4.30	4.88	N/A	ns
		XC6SLX100	4.02	4.33	4.90	7.37	ns
		XC6SLX100T	4.06	4.33	4.90	N/A	ns
		XC6SLX150	3.65	3.98	4.58	6.94	ns
		XC6SLX150T	3.65	3.98	4.58	N/A	ns
		XA6SLX4	4.88	N/A	6.13	N/A	ns
		XA6SLX9	4.88	N/A	6.13	N/A	ns
		XA6SLX16	4.74	N/A	5.27	N/A	ns
		XA6SLX25	4.43	N/A	4.78	N/A	ns
		XA6SLX25T	4.43	N/A	4.88	N/A	ns
		XA6SLX45	4.94	N/A	5.62	N/A	ns
		XA6SLX45T	4.94	N/A	5.62	N/A	ns
		XA6SLX75	4.32	N/A	4.77	N/A	ns
		XA6SLX75T	4.32	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.41	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	7.15	ns
XQ6SLX75T	4.32	N/A	4.77	N/A	ns		
XQ6SLX150	N/A	N/A	4.60	6.94	ns		
XQ6SLX150T	4.35	N/A	4.60	N/A	ns		

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

## Spartan-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 70 through Table 77. Values are expressed in nanoseconds unless otherwise noted.

Table 70: Global Clock Setup and Hold Without DCM or PLL (No Delay)

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
<b>Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.<sup>(1)</sup></b>							
T <sub>PSND</sub> / T <sub>PHND</sub>	No Delay Global Clock and IFF <sup>(3)</sup> without DCM or PLL	XC6SLX4	0.10/1.56	N/A	0.10/1.83	0.07/2.54	ns
		XC6SLX9	0.10/1.56	0.10/1.57	0.10/1.84	0.07/2.54	ns
		XC6SLX16	0.12/1.42	0.12/1.48	0.12/1.64	0.13/2.19	ns
		XC6SLX25	0.18/1.64	0.18/1.75	0.18/1.99	0.11/2.57	ns
		XC6SLX25T	0.18/1.64	0.18/1.75	0.18/1.99	N/A	ns
		XC6SLX45	-0.08/1.80	-0.08/1.95	-0.08/2.27	-0.17/2.74	ns
		XC6SLX45T	-0.08/1.80	-0.08/1.95	-0.08/2.27	N/A	ns
		XC6SLX75	0.13/1.81	0.13/2.06	0.13/2.27	-0.12/3.30	ns
		XC6SLX75T	0.13/1.81	0.13/2.06	0.13/2.27	N/A	ns
		XC6SLX100	-0.14/2.03	-0.14/2.24	-0.14/2.56	-0.17/3.44	ns
		XC6SLX100T	-0.14/2.03	-0.14/2.24	-0.14/2.56	N/A	ns
		XC6SLX150	-0.24/2.42	-0.24/2.74	-0.24/2.95	-0.60/3.75	ns
		XC6SLX150T	-0.24/2.42	-0.24/2.74	-0.24/2.95	N/A	ns
		XA6SLX4	0.10/1.57	N/A	0.10/1.84	N/A	ns
		XA6SLX9	0.10/1.57	N/A	0.10/1.84	N/A	ns
		XA6SLX16	0.12/1.43	N/A	0.12/1.64	N/A	ns
		XA6SLX25	0.18/1.65	N/A	0.18/1.99	N/A	ns
		XA6SLX25T	0.18/1.65	N/A	0.18/1.99	N/A	ns
		XA6SLX45	-0.08/1.82	N/A	-0.08/2.27	N/A	ns
		XA6SLX45T	-0.08/1.82	N/A	-0.08/2.27	N/A	ns
		XA6SLX75	0.13/2.02	N/A	0.13/2.32	N/A	ns
		XA6SLX75T	0.13/2.02	N/A	0.13/2.32	N/A	ns
		XA6SLX100	N/A	N/A	0.10/2.51	N/A	ns
		XQ6SLX75	N/A	N/A	0.13/2.32	-0.12/3.30	ns
XQ6SLX75T	0.13/2.02	N/A	0.13/2.32	N/A	ns		
XQ6SLX150	N/A	N/A	-0.24/2.95	-0.60/3.75	ns		
XQ6SLX150T	-0.24/2.74	N/A	-0.24/2.95	N/A	ns		

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.

Table 74: Global Clock Setup and Hold With PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
<b>Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.<sup>(1)</sup></b>							
T <sub>PSPLL</sub> / T <sub>PHPLL</sub>	No Delay Global Clock and IFF <sup>(2)</sup> with PLL in System-Synchronous Mode	XC6SLX4	1.37/0.25	N/A	1.52/0.41	2.07/0.69	ns
		XC6SLX9	1.37/0.21	1.48/0.21	1.52/0.26	2.07/0.69	ns
		XC6SLX16	1.33/-0.03	1.53/-0.02	1.60/-0.02	1.57/0.48	ns
		XC6SLX25	1.65/0.28	1.71/0.28	1.91/0.28	2.44/0.76	ns
		XC6SLX25T	1.65/0.28	1.71/0.28	1.91/0.28	N/A	ns
		XC6SLX45	1.55/0.18	1.64/0.18	1.75/0.18	2.02/0.90	ns
		XC6SLX45T	1.55/0.18	1.64/0.18	1.75/0.18	N/A	ns
		XC6SLX75	1.77/0.21	1.89/0.21	2.13/0.21	2.46/0.53	ns
		XC6SLX75T	1.77/0.21	1.89/0.21	2.13/0.21	N/A	ns
		XC6SLX100	1.44/0.32	1.52/0.32	1.70/0.32	1.78/0.86	ns
		XC6SLX100T	1.44/0.32	1.52/0.32	1.70/0.32	N/A	ns
		XC6SLX150	1.39/0.49	1.48/0.49	1.67/0.49	1.94/0.94	ns
		XC6SLX150T	1.39/0.49	1.48/0.49	1.67/0.49	N/A	ns
		XA6SLX4	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX9	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX16	1.89/-0.08	N/A	1.72/-0.08	N/A	ns
		XA6SLX25	1.85/0.16	N/A	2.08/0.16	N/A	ns
		XA6SLX25T	1.85/0.16	N/A	2.17/0.16	N/A	ns
		XA6SLX45	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX45T	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX75	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX100	N/A	N/A	2.34/0.14	N/A	ns
		XQ6SLX75	N/A	N/A	2.25/0.06	2.46/0.53	ns
		XQ6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XQ6SLX150	N/A	N/A	1.79/0.37	1.94/0.94	ns
XQ6SLX150T	1.43/0.37	N/A	1.79/0.37	N/A	ns		

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 76: Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
<b>Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.<sup>(1)</sup></b>							
T <sub>PSDCMPLL</sub> / T <sub>PHDCMPLL</sub>	No Delay Global Clock and IFF <sup>(2)</sup> with DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.	XC6SLX4	1.16/0.49	N/A	1.39/0.49	2.36/0.59	ns
		XC6SLX9	1.16/0.44	1.37/0.44	1.39/0.44	2.36/0.59	ns
		XC6SLX16	1.44/-0.08	1.49/-0.04	1.62/-0.04	2.06/0.55	ns
		XC6SLX25	1.52/0.42	1.65/0.42	1.83/0.42	2.52/0.43	ns
		XC6SLX25T	1.52/0.42	1.65/0.42	1.83/0.42	N/A	ns
		XC6SLX45	1.54/0.39	1.59/0.39	1.75/0.39	2.48/0.76	ns
		XC6SLX45T	1.54/0.39	1.59/0.39	1.75/0.39	N/A	ns
		XC6SLX75	1.72/0.41	1.80/0.41	1.99/0.41	2.60/0.75	ns
		XC6SLX75T	1.72/0.41	1.80/0.41	1.99/0.41	N/A	ns
		XC6SLX100	1.34/0.51	1.46/0.51	1.64/0.51	2.12/0.90	ns
		XC6SLX100T	1.34/0.51	1.46/0.51	1.64/0.51	N/A	ns
		XC6SLX150	1.30/0.60	1.40/0.60	1.55/0.60	2.57/0.97	ns
		XC6SLX150T	1.30/0.60	1.40/0.60	1.55/0.60	N/A	ns
		XA6SLX4	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX9	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX16	2.67/0.35	N/A	2.67/0.17	N/A	ns
		XA6SLX25	1.74/0.27	N/A	1.95/0.27	N/A	ns
		XA6SLX25T	1.74/0.27	N/A	2.03/0.27	N/A	ns
		XA6SLX45	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX45T	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX75	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX100	N/A	N/A	2.64/0.82	N/A	ns
		XQ6SLX75	N/A	N/A	2.11/0.24	2.60/0.75	ns
		XQ6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XQ6SLX150	N/A	N/A	1.67/0.70	2.57/0.97	ns
		XQ6SLX150T	1.50/0.70	N/A	1.67/0.70	N/A	ns

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Date	Version	Description of Revisions
06/14/10	1.5	<p>In <a href="#">Table 2</a>, added note 5 and added temperature range to <math>V_{FS}</math> and <math>R_{FUSE}</math>. Removed speed grade delineation, revised <math>I_{RPD}</math> description, and updated note 2 in <a href="#">Table 4</a>. Added note 2 to <a href="#">Table 7</a>. Added DIFF_MOBILE_DDR to <a href="#">Table 8</a> and <a href="#">Table 10</a>. Added note 4 to <a href="#">Table 15</a>. Changed minimum <math>DV_{PPIN}</math> in <a href="#">Table 16</a>. Updated <math>F_{GTPDRPCLK}</math> in <a href="#">Table 19</a>. Increased maximum <math>T_{LLSKEW}</math> in <a href="#">Table 22</a>. Updated descriptions and added data to <a href="#">Table 23</a>. Removed note 1 and added new data to the Networking Applications section in <a href="#">Table 25</a>. Updated <a href="#">Table 26</a> and <a href="#">Table 27</a> to the data in ISE v12.1 software with speed specification v1.08. In <a href="#">Table 28</a>, added DIFF_MOBILE_DDR and updated -4 speed grade data. Updated the maximum I/O pairs per bank in <a href="#">Table 33</a>. Updated note 2 on <a href="#">Table 39</a>. Revised the <math>F_{MAX}</math> in <a href="#">Table 44</a>. In <a href="#">Table 47</a>, updated description for <math>T_{SMCKCSO}</math>, revised values for <math>T_{POR}</math> and added Min value, added <math>T_{BPIICCK}</math> and <math>T_{SPIICCK}</math>. Also in <a href="#">Table 47</a>, added device dependencies to <math>F_{SMCCK}</math> and <math>F_{RBCKK}</math>. Updated and added data to <a href="#">Table 63</a> through <a href="#">Table 78</a>, and <a href="#">Table 81</a>. In <a href="#">Table 79</a>, added data on the XC6SLX45-FG(G)676 and revised the XC6SLX45T and XC6SLX150T values.</p> <p>The following changes to this specification are addressed in the product change notice <a href="#">XCN10024</a>, <i>MCB Performance and JTAG Revision Code for Spartan-6 LX16 and LX45 FPGAs</i>. In <a href="#">Table 2</a>, revised the <math>V_{CCINT}</math> to add the memory controller block extended performance specifications. In <a href="#">Table 25</a>, changed the standard specifications and added extended performance specifications for the memory controller block and note 2. Added note 4 and updated values in <a href="#">Table 34</a>.</p>
06/24/10	1.6	<p>Production release of XC6SLX45T (-2 and -3 speed grades), XC6SLX16 and XC6SLX45 (-3 speed grade) devices which includes changes to <a href="#">Table 26</a> and <a href="#">Table 27</a> (ISE v12.1 software with speed specification v1.08).</p> <p>Added the -3N speed grade, which designates Spartan-6 devices that do not support MCB functionality. This includes changes to <a href="#">Table 2</a> (note 2), <a href="#">Table 25</a> (note 4), and <a href="#">Switching Characteristics</a> (<a href="#">Table 26</a>).</p> <p>Updated <a href="#">Simultaneously Switching Outputs</a> discussion. Added -3 speed grade values for <math>T_{TAP}</math> and <math>F_{MINCAL}</math> values in <a href="#">Table 39</a>. In <a href="#">Table 40</a>, updated <math>T_{RPW}</math> (-2 and -3 speed grade) values and <math>F_{TOG}</math> (-3 speed grade) values. In <a href="#">Table 48</a>, updated <math>T_{GIO}</math> (-2 and -3 speed grade) values. Updated -3 values in spread spectrum section of <a href="#">Table 57</a>.</p>
07/16/10	1.7	<p>Production release of specific devices listed in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v12.2 software with speed specification v1.11. Added note 4 advising designers of the patch which contains v1.11. Also updated the -1L speed specification to v1.04. Updated numerous -4 and -1L values. Added -4 <math>T_{TAP}</math> values and <math>F_{MINCAL}</math> to <a href="#">Table 39</a>. Revised <math>T_{CINCK}/T_{CKCIN}</math> in <a href="#">Table 40</a>. In <a href="#">Table 41</a>, revised <math>T_{SHCKO}</math>. In <a href="#">Table 42</a>, revised <math>T_{REG}</math>. Added new -1L values to <a href="#">Table 47</a>. Added and updated values in <a href="#">Table 79</a>.</p>
07/26/10	1.8	<p>Production release of XC6SLX25, XC6SLX25T, XC6SLX100 and XC6SLX100T in the specific speed grades listed in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v12.2 software with speed specification v1.11. Added note 7 to <a href="#">Table 2</a> and moved <math>V_{FS}</math> and <math>R_{FUSE}</math> to a new <a href="#">Table 3</a>. Added <math>I_{HS}</math> and note 4 to <a href="#">Table 4</a>. Added note 1 to <a href="#">Table 28</a>. Added and updated SSO limits per <math>V_{CC0}/GND</math> pairs in <a href="#">Table 34</a>. Added note 3 to <a href="#">Table 47</a>. In <a href="#">Table 54</a>, removed -1L specifications for CLKOUT_PER_JITT_DV1/2 and revised CLKIN_CLKFB_PHASE and CLKOUT_PHASE_DLL values. Updated note 3 in both <a href="#">Table 56</a> and <a href="#">Table 57</a>.</p>
08/23/10	1.9	<p>Updated values for <math>F_{GTPRANGE1}</math>, <math>F_{GTPRANGE2}</math>, and <math>F_{GPLLMIN}</math> in <a href="#">Table 18</a>. Revised -3 and -4 values in <a href="#">Table 21</a>. Removed the -1L speed grade readback support restriction and note 3 in <a href="#">Table 47</a>.</p>
11/05/10	1.10	<p>Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v12.3 software with speed specification v1.12 for the -2 speed grade available in the 12.3 <i>Speed Files Patch</i>. Added note 3 advising designers of the patch which contains v1.12.</p> <p>In <a href="#">Table 2</a>, added note 4. In <a href="#">Table 4</a>, added note 2. In <a href="#">Table 10</a>, added notes 2 and 3. In <a href="#">Table 44</a>, added note 2. In <a href="#">Table 47</a>, updated symbol for <math>T_{SMWCKK}/T_{SMCKKW}</math>, changed -1L values for <math>T_{USERCCLKH}</math> and <math>T_{USERCCLKL}</math>, and added and revised the modes for <math>F_{MCKK}</math> and <math>F_{SMCKK}</math>. In <a href="#">Table 53</a>, redefined and expanded description for CLKIN_FREQ_DLL and rewrote note 3. Updated title of <a href="#">Table 58</a>. Also in <a href="#">Table 78</a>, revised <math>T_{DCD\_CLK}</math> for XC6SLX150 and XC6SLX150T. Changed description of <math>T_{PSFD}/T_{PHFD}</math> in <a href="#">Table 71</a>.</p> <p>For the -1L speed grade, updated data sheet to ISE 12.3 software with speed specification v1.05 which revised the values in the following tables: <a href="#">Table 25</a>, <a href="#">Table 28</a>, <a href="#">Table 35</a>, <a href="#">Table 36</a>, <a href="#">Table 37</a>, <a href="#">Table 40</a> through <a href="#">Table 43</a>, <a href="#">Table 48</a> through <a href="#">Table 56</a>, <a href="#">Table 62</a> through <a href="#">Table 78</a>, <a href="#">Table 80</a>, and <a href="#">Table 81</a>. Updated <a href="#">Notice of Disclaimer</a>.</p>