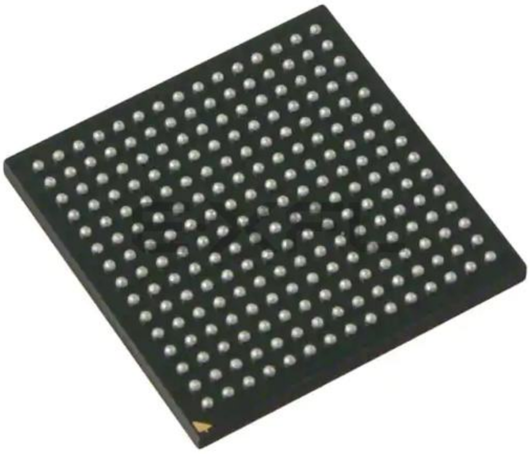
AMD Xilinx - XA6SLX4-2CSG225I Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	300
Number of Logic Elements/Cells	3840
Total RAM Bits	221184
Number of I/O	132
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	225-LFBGA, CSPBGA
Supplier Device Package	225-CSPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xa6slx4-2csg225i

Table 5: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	LX4	2.5	2.5	2.5	2.5	mA
		LX9	2.5	2.5	2.5	2.5	mA
		LX16	3.0	3.0	3.0	3.0	mA
		LX25	4.0	4.0	4.0	4.0	mA
		LX25T	4.0	4.0	4.0	N/A	mA
		LX45	5.0	5.0	5.0	5.0	mA
		LX45T	5.0	5.0	5.0	N/A	mA
		LX75	7.0	7.0	7.0	7.0	mA
		LX75T	7.0	7.0	7.0	N/A	mA
		LX100	9.0	9.0	9.0	9.0	mA
		LX100T	9.0	9.0	9.0	N/A	mA
		LX150	12.0	12.0	12.0	12.0	mA
		LX150T	12.0	12.0	12.0	N/A	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C junction temperatures (Tj). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 25°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. Nominal V_{CCINT} is 1.20V; use the XPE tool to calculate 1.23V values for the nominal V_{CCINT} of the extended performance range.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 6: **Power Supply Ramp Time**

Symbol	Description	Speed Grade	Ramp Time	Units
V_{CCINTR}	Internal supply voltage ramp time	-3, -3N, -2	0.20 to 50.0	ms
		-1L	0.20 to 40.0	ms
V_{CCO2}[(1)]	Output drivers bank 2 supply voltage ramp time	All	0.20 to 50.0	ms
V_{CCAUXR}	Auxiliary supply voltage ramp time	All	0.20 to 50.0	ms

Notes:

1. The minimum V_{CCO2} for power-on reset and configuration is 1.65V.
2. Spartan-6 FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply. Use the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools to estimate current drain on these supplies. Spartan-6 devices do not have a required power-on sequence.

Table 8: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

I/O Standard	V_{CCO} for Drivers		
	V, Min	V, Nom	V, Max
LVDS_33	3.0	3.3	3.45
LVDS_25	2.25	2.5	2.75
BLVDS_25	2.25	2.5	2.75
MINI_LVDS_33	3.0	3.3	3.45
MINI_LVDS_25	2.25	2.5	2.75
LVPECL_33(1)	N/A–Inputs Only		
LVPECL_25	N/A–Inputs Only		
RSDS_33	3.0	3.3	3.45
RSDS_25	2.25	2.5	2.75
TMDS_33(1)	3.14	3.3	3.45
PPDS_33	3.0	3.3	3.45
PPDS_25	2.25	2.5	2.75
DISPLAY_PORT	2.3	2.5	2.7
DIFF_MOBILE_DDR	1.7	1.8	1.9
DIFF_HSTL_I	1.4	1.5	1.6
DIFF_HSTL_II	1.4	1.5	1.6
DIFF_HSTL_III	1.4	1.5	1.6
DIFF_HSTL_I_18	1.7	1.8	1.9
DIFF_HSTL_II_18	1.7	1.8	1.9
DIFF_HSTL_III_18	1.7	1.8	1.9
DIFF_SSTL3_I	3.0	3.3	3.45
DIFF_SSTL3_II	3.0	3.3	3.45
DIFF_SSTL2_I	2.3	2.5	2.7
DIFF_SSTL2_II	2.3	2.5	2.7
DIFF_SSTL18_I	1.7	1.8	1.9
DIFF_SSTL18_II	1.7	1.8	1.9
DIFF_SSTL15_II	1.425	1.5	1.575

Notes:

1. LVPECL_33 and TMDS_33 inputs require V_{CCAUX} = 3.3V nominal.

Table 10: **Differential I/O Standard DC Input and Output Levels**

I/O Standard	V_{ID}		V_{ICM}		V_{OD}		V_{OCM}		V_{OH}	V_{OL}
	mV, Min	mV, Max	V, Min	V, Max	mV, Min	mV, Max	V, Min	V, Max	V, Min	V, Max
LVDS_33[(2)(3)]	100	600	0.3	2.35	247	454	1.125	1.375	–	–
LVDS_25[(2)(3)]	100	600	0.3	2.35	247	454	1.125	1.375	–	–
BLVDS_25[(2)(3)]	100	–	0.3	2.35	240	460	Typical 50% V_{CCO}		–	–
MINI_LVDS_33	200	600	0.3	1.95	300	600	1.0	1.4	–	–
MINI_LVDS_25	200	600	0.3	1.95	300	600	1.0	1.4	–	–
LVPECL_33[(2)(3)]	100	1000	0.3	2.8[(1)]	Inputs only					
LVPECL_25[(2)(3)]	100	1000	0.3	1.95	Inputs only					
RSDS_33[(2)(3)]	100	–	0.3	1.5	100	400	1.0	1.4	–	–
RSDS_25[(2)(3)]	100	–	0.3	1.5	100	400	1.0	1.4	–	–
TMDS_33	150	1200	2.7	3.23[(1)]	400	800	V_{CCO} – 0.405	V_{CCO} – 0.190	–	–
PPDS_33[(2)(3)]	100	400	0.2	2.3	100	400	0.5	1.4	–	–
PPDS_25[(2)(3)]	100	400	0.2	2.3	100	400	0.5	1.4	–	–
DISPLAY_PORT	190	1260	0.3	2.35	–	–	Typical 50% V_{CCO}		–	–
DIFF_MOBILE_DDR	100	–	0.78	1.02	–	–	–	–	90% V_{CCO}	10% V_{CCO}
DIFF_HSTL_I	100	–	0.68	0.9	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II	100	–	0.68	0.9	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III	100	–	0.68	0.9	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_I_18	100	–	0.8	1.1	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II_18	100	–	0.8	1.1	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	100	–	0.8	1.1	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL3_I	100	–	1.0	1.9	–	–	–	–	V_{TT} + 0.6	V_{TT} – 0.6
DIFF_SSTL3_II	100	–	1.0	1.9	–	–	–	–	V_{TT} + 0.8	V_{TT} – 0.8
DIFF_SSTL2_I	100	–	1.0	1.5	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61
DIFF_SSTL2_II	100	–	1.0	1.5	–	–	–	–	V_{TT} + 0.81	V_{TT} – 0.81
DIFF_SSTL18_I	100	–	0.7	1.1	–	–	–	–	V_{TT} + 0.47	V_{TT} – 0.47
DIFF_SSTL18_II	100	–	0.7	1.1	–	–	–	–	V_{TT} + 0.6	V_{TT} – 0.6
DIFF_SSTL15_II	100	–	0.55	0.95	–	–	–	–	V_{TT} + 0.4	V_{TT} – 0.4

Notes:

1. LVPECL_33 and TMDS_33 maximum V_{ICM} is the lower of V (maximum) or V_{CCAUX} – (V_{ID}/2)
2. When V_{CCAUX} = 3.3V, the DCD can be higher than 5% for V_{ICM} < 0.7V when using these I/O standards: LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, LVPECL_33, RSDS_25, RSDS_33, PPDS_25, and PPDS_33.
3. The -1L devices require V_{CCAUX} = 2.5V when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.

Table 17: **GTP Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	200	800	2000	mV
R_{IN}	Differential input resistance	80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult UG386: *Spartan-6 FPGA GTP Transceivers User Guide* for further information.

Table 18: **GTP Transceiver Performance**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
F_{GTPMAX}	Maximum GTP transceiver data rate	3.2	3.2	2.7	N/A	Gb/s
$F_{GTPRANGE1}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 1	1.88 to 3.2	1.88 to 3.2	1.88 to 2.7	N/A	Gb/s
$F_{GTPRANGE2}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 2	0.94 to 1.62	0.94 to 1.62	0.94 to 1.62	N/A	Gb/s
$F_{GTPRANGE3}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 4	0.6 to 0.81	0.6 to 0.81	0.6 to 0.81	N/A	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	1.62	1.62	1.62	N/A	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	0.94	0.94	0.94	N/A	GHz

Table 19: **GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
$F_{GTPDRPCLK}$	GTP transceiver DCLK (DRP clock) maximum frequency	125	125	100	N/A	MHz

Table 20: **GTP Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All LXT Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	160	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	µs

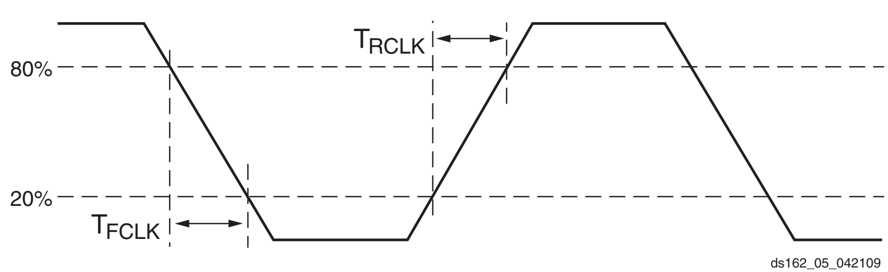

Figure 3: **Reference Clock Timing Parameters**

Table 21: **GTP Transceiver User Clock Switching Characteristics[1]**

Symbol	Description	Conditions	Speed Grade				Units
			-3	-3N	-2	-1L	
F_{TXOUT}	TXOUTCLK maximum frequency		320	320	270	N/A	MHz
F_{RXREC}	RXRECCLK maximum frequency		320	320	270	N/A	MHz
T_{RX}	RXUSRCLK maximum frequency		320	320	270	N/A	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz
T_{TX}	TXUSRCLK maximum frequency		320	320	270	N/A	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz

Notes:
1. Clocking must be implemented as described in UG386: *Spartan-6 FPGA GTP Transceivers User Guide*.

Table 22: **GTP Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
T_{RTX}	TX Rise time	20%–80%	–	140	–	ps
T_{FTX}	TX Fall time	80%–20%	–	120	–	ps
T_{LLSKEW}	TX lane-to-lane skew[1]		–	–	400	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	20	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	50	ns
$T_{J3.125}$	Total Jitter[2]	3.125 Gb/s	–	–	0.35	UI
$D_{J3.125}$	Deterministic Jitter[2]		–	–	0.15	UI
$T_{J2.5}$	Total Jitter[2]	2.5 Gb/s	–	–	0.33	UI
$D_{J2.5}$	Deterministic Jitter[2]		–	–	0.15	UI
$T_{J1.62}$	Total Jitter[2]	1.62 Gb/s	–	–	0.20	UI
$D_{J1.62}$	Deterministic Jitter[2]		–	–	0.10	UI
$T_{J1.25}$	Total Jitter[2]	1.25 Gb/s	–	–	0.20	UI
$D_{J1.25}$	Deterministic Jitter[2]		–	–	0.10	UI
T_{J614}	Total Jitter[2]	614 Mb/s	–	–	0.10	UI
D_{J614}	Deterministic Jitter[2]		–	–	0.05	UI

Notes:
1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP transceiver sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics, page 19.

Table 25: **Interface Performances**

Description	I/O Resource	Clock Buffer	Data Width	Speed Grade				Units
				-3	-3N	-2	-1L	
Networking Applications[1]								
SDR LVDS transmitter or receiver	IOB SDR register	BUFG	–	400	400	375	250	Mb/s
DDR LVDS transmitter or receiver	ODDR2/IDDR2 register	2 BUFGs	–	800	800	750	500	Mb/s
SDR LVDS transmitter	OSERDES2	BUFPLL	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
DDR LVDS transmitter	OSERDES2	2 BUFIO2s	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
SDR LVDS receiver	ISERDES2 in RETIMED mode	BUFPLL	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
DDR LVDS receiver	ISERDES2 in RETIMED mode	2 BUFIO2s	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
Memory Interfaces (Implemented using the Spartan-6 FPGA Memory Controller Block)[2]								
Standard Performance (Standard V_{CCINT})								
DDR				400	Note 4	400	350	Mb/s
DDR2				667	Note 4	625	400	Mb/s
DDR3				800	Note 4	667	—	Mb/s
LPDDR (Mobile_DDR)				400	Note 4	400	350	Mb/s
Extended Performance (Requires Extended Performance V_{CCINT})[3]								
DDR2				800	Note 4	667	—	Mb/s

Notes:
1. Refer to XAPP1064, *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)* and UG381, *Spartan-6 FPGA SelectIO Resources User Guide.*
2. Refer to UG388, *Spartan-6 FPGA Memory Controller User Guide*.
3. Extended Memory Controller block performance for DDR2 can be achieved using the extended performance V_{CCINT} range from Table 2.
4. The LX4 device, all devices in the TQG144 and CPG196 packages, and the -3N speed grade do not support a Memory Controller Block.

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L[(1)]	-3	-3N	-2	-1L[(1)]	-3	-3N	-2	-1L[(1)]	
LVCMOS18, Slow, 24 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18, Fast, 2 mA	1.18	1.30	1.43	2.04	3.59	3.73	3.93	4.53	3.59	3.73	3.93	4.53	ns
LVCMOS18, Fast, 4 mA	1.18	1.30	1.43	2.04	2.39	2.53	2.73	3.35	2.39	2.53	2.73	3.35	ns
LVCMOS18, Fast, 6 mA	1.18	1.30	1.43	2.04	1.88	2.02	2.22	2.84	1.88	2.02	2.22	2.84	ns
LVCMOS18, Fast, 8 mA	1.18	1.30	1.43	2.04	1.81	1.95	2.15	2.77	1.81	1.95	2.15	2.77	ns
LVCMOS18, Fast, 12 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVCMOS18, Fast, 16 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVCMOS18, Fast, 24 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVCMOS18_JEDEC, QUIETIO, 2 mA	0.94	1.06	1.19	1.41	5.91	6.05	6.25	6.79	5.91	6.05	6.25	6.79	ns
LVCMOS18_JEDEC, QUIETIO, 4 mA	0.94	1.06	1.19	1.41	4.75	4.89	5.09	5.64	4.75	4.89	5.09	5.64	ns
LVCMOS18_JEDEC, QUIETIO, 6 mA	0.94	1.06	1.19	1.41	4.04	4.18	4.38	4.96	4.04	4.18	4.38	4.96	ns
LVCMOS18_JEDEC, QUIETIO, 8 mA	0.94	1.06	1.19	1.41	3.71	3.85	4.05	4.62	3.71	3.85	4.05	4.62	ns
LVCMOS18_JEDEC, QUIETIO, 12 mA	0.94	1.06	1.19	1.41	3.35	3.49	3.69	4.28	3.35	3.49	3.69	4.28	ns
LVCMOS18_JEDEC, QUIETIO, 16 mA	0.94	1.06	1.19	1.41	3.20	3.34	3.54	4.13	3.20	3.34	3.54	4.13	ns
LVCMOS18_JEDEC, QUIETIO, 24 mA	0.94	1.06	1.19	1.41	2.96	3.10	3.30	3.98	2.96	3.10	3.30	3.98	ns
LVCMOS18_JEDEC, Slow, 2 mA	0.94	1.06	1.19	1.41	4.59	4.73	4.93	5.54	4.59	4.73	4.93	5.54	ns
LVCMOS18_JEDEC, Slow, 4 mA	0.94	1.06	1.19	1.41	3.69	3.83	4.03	4.60	3.69	3.83	4.03	4.60	ns
LVCMOS18_JEDEC, Slow, 6 mA	0.94	1.06	1.19	1.41	3.00	3.14	3.34	3.94	3.00	3.14	3.34	3.94	ns
LVCMOS18_JEDEC, Slow, 8 mA	0.94	1.06	1.19	1.41	2.19	2.33	2.53	3.18	2.19	2.33	2.53	3.18	ns
LVCMOS18_JEDEC, Slow, 12 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18_JEDEC, Slow, 16 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18_JEDEC, Slow, 24 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18_JEDEC, Fast, 2 mA	0.94	1.06	1.19	1.41	3.57	3.71	3.91	4.52	3.57	3.71	3.91	4.52	ns
LVCMOS18_JEDEC, Fast, 4 mA	0.94	1.06	1.19	1.41	2.39	2.53	2.73	3.35	2.39	2.53	2.73	3.35	ns
LVCMOS18_JEDEC, Fast, 6 mA	0.94	1.06	1.19	1.41	1.88	2.02	2.22	2.84	1.88	2.02	2.22	2.84	ns
LVCMOS18_JEDEC, Fast, 8 mA	0.94	1.06	1.19	1.41	1.80	1.94	2.14	2.76	1.80	1.94	2.14	2.76	ns
LVCMOS18_JEDEC, Fast, 12 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVCMOS18_JEDEC, Fast, 16 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVCMOS18_JEDEC, Fast, 24 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVCMOS15, QUIETIO, 2 mA	0.98	1.10	1.23	1.79	5.47	5.61	5.81	6.38	5.47	5.61	5.81	6.38	ns
LVCMOS15, QUIETIO, 4 mA	0.98	1.10	1.23	1.79	4.61	4.75	4.95	5.51	4.61	4.75	4.95	5.51	ns
LVCMOS15, QUIETIO, 6 mA	0.98	1.10	1.23	1.79	4.07	4.21	4.41	4.97	4.07	4.21	4.41	4.97	ns
LVCMOS15, QUIETIO, 8 mA	0.98	1.10	1.23	1.79	3.91	4.05	4.25	4.81	3.91	4.05	4.25	4.81	ns
LVCMOS15, QUIETIO, 12 mA	0.98	1.10	1.23	1.79	3.53	3.67	3.87	4.51	3.53	3.67	3.87	4.51	ns
LVCMOS15, QUIETIO, 16 mA	0.98	1.10	1.23	1.79	3.32	3.46	3.66	4.31	3.32	3.46	3.66	4.31	ns
LVCMOS15, Slow, 2 mA	0.98	1.10	1.23	1.79	4.18	4.32	4.52	5.11	4.18	4.32	4.52	5.11	ns
LVCMOS15, Slow, 4 mA	0.98	1.10	1.23	1.79	3.42	3.56	3.76	4.34	3.42	3.56	3.76	4.34	ns
LVCMOS15, Slow, 6 mA	0.98	1.10	1.23	1.79	2.29	2.43	2.63	3.24	2.29	2.43	2.63	3.24	ns

Table 29: **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices[1] *(Cont'd)***

I/O Standard	T_{IOPI} Speed Grade		T_{IOOP} Speed Grade		T_{IOTP} Speed Grade		Units
	-3	-2	-3	-2	-3	-2	
LVCMOS12, QUIETIO, 6 mA	0.98	1.16	4.79	4.99	4.79	4.99	ns
LVCMOS12, QUIETIO, 8 mA	0.98	1.16	4.43	4.63	4.43	4.63	ns
LVCMOS12, QUIETIO, 12 mA	0.98	1.16	4.18	4.38	4.18	4.38	ns
LVCMOS12, Slow, 2 mA	0.98	1.16	5.12	5.32	5.12	5.32	ns
LVCMOS12, Slow, 4 mA	0.98	1.16	3.00	3.20	3.00	3.20	ns
LVCMOS12, Slow, 6 mA	0.98	1.16	2.91	3.11	2.91	3.11	ns
LVCMOS12, Slow, 8 mA	0.98	1.16	2.51	2.71	2.51	2.71	ns
LVCMOS12, Slow, 12 mA	0.98	1.16	2.25	2.45	2.25	2.45	ns
LVCMOS12, Fast, 2 mA	0.98	1.16	3.60	3.80	3.60	3.80	ns
LVCMOS12, Fast, 4 mA	0.98	1.16	2.49	2.69	2.49	2.69	ns
LVCMOS12, Fast, 6 mA	0.98	1.16	1.94	2.14	1.94	2.14	ns
LVCMOS12, Fast, 8 mA	0.98	1.16	1.82	2.02	1.82	2.02	ns
LVCMOS12, Fast, 12 mA	0.98	1.16	1.80	2.00	1.80	2.00	ns
LVCMOS12_JEDEC, QUIETIO, 2 mA	1.57	1.75	6.53	6.73	6.53	6.73	ns
LVCMOS12_JEDEC, QUIETIO, 4 mA	1.57	1.75	5.12	5.32	5.12	5.32	ns
LVCMOS12_JEDEC, QUIETIO, 6 mA	1.57	1.75	4.81	5.01	4.81	5.01	ns
LVCMOS12_JEDEC, QUIETIO, 8 mA	1.57	1.75	4.44	4.64	4.44	4.64	ns
LVCMOS12_JEDEC, QUIETIO, 12 mA	1.57	1.75	4.20	4.40	4.20	4.40	ns
LVCMOS12_JEDEC, Slow, 2 mA	1.57	1.75	5.14	5.34	5.14	5.34	ns
LVCMOS12_JEDEC, Slow, 4 mA	1.57	1.75	2.99	3.19	2.99	3.19	ns
LVCMOS12_JEDEC, Slow, 6 mA	1.57	1.75	2.90	3.10	2.90	3.10	ns
LVCMOS12_JEDEC, Slow, 8 mA	1.57	1.75	2.50	2.70	2.50	2.70	ns
LVCMOS12_JEDEC, Slow, 12 mA	1.57	1.75	2.26	2.46	2.26	2.46	ns
LVCMOS12_JEDEC, Fast, 2 mA	1.57	1.75	3.60	3.80	3.60	3.80	ns
LVCMOS12_JEDEC, Fast, 4 mA	1.57	1.75	2.49	2.69	2.49	2.69	ns
LVCMOS12_JEDEC, Fast, 6 mA	1.57	1.75	1.94	2.14	1.94	2.14	ns
LVCMOS12_JEDEC, Fast, 8 mA	1.57	1.75	1.83	2.03	1.83	2.03	ns
LVCMOS12_JEDEC, Fast, 12 mA	1.57	1.75	1.80	2.00	1.80	2.00	ns

Notes:

1. The Spartan-6Q FPGA -1L values are listed in Table 28.

Table 30 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). These delays are measured using LVCMOS25, Fast, 12 mA.

Table 30: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T_{IOTPHZ}	T input to Pad high-impedance	1.39	1.59	1.59	1.91	ns

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 4 and Figure 5.

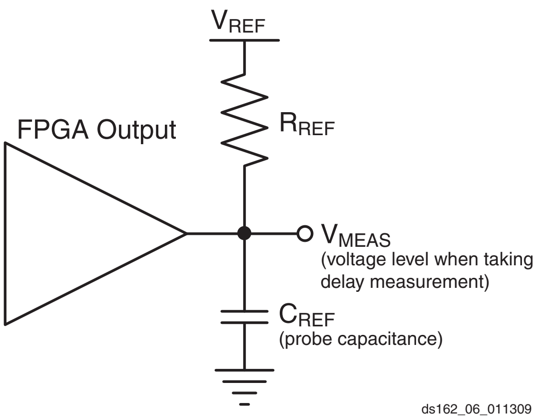

Figure 4: **Single-Ended Test Setup**

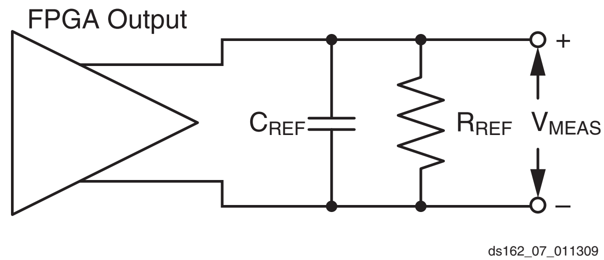

Figure 5: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 32.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 32: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.4	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
PCI (Peripheral Component Interface) 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3 (rising edge)	25	10[2]	0.94	0
	PCI33_3, PCI66_3 (falling edge)	25	10[2]	2.03	3.3
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25

Table 33: **Spartan-6 FPGA V_{CCO}/GND Pairs per Bank**

Package	Devices	Description	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5
TQG144	LX	V_{CCO}/GND Pairs	3	3	2	3	N/A	N/A
		Maximum I/O per Pair	8	8	13	8	N/A	N/A
CPG196	LX	VCCO/GND Pairs	4	6	4	6	N/A	N/A
		Maximum I/O per Pair	6	4	7	4	N/A	N/A
CSG225	LX	V_{CCO}/GND Pairs	4	4	4	4	N/A	N/A
		Maximum I/O per Pair	10	10	9	10	N/A	N/A
FT(G)256	LX	V_{CCO}/GND Pairs	5	6	4	5	N/A	N/A
		Maximum I/O per Pair	8	9	9	10	N/A	N/A
CSG324	LX	V_{CCO}/GND Pairs	6	6	6	6	N/A	N/A
		Maximum I/O per Pair	10	9	10	9	N/A	N/A
	LXT	V_{CCO}/GND Pairs	4	6	6	6	N/A	N/A
		Maximum I/O per Pair	4	9	10	9	N/A	N/A
CS(G)484	LX	V_{CCO}/GND Pairs	8	13	8	13	N/A	N/A
		Maximum I/O per Pair	7	8	7	8	N/A	N/A
	LXT	V_{CCO}/GND Pairs	7	12	8	13	N/A	N/A
		Maximum I/O per Pair	5	8	6	8	N/A	N/A
FG(G)484	LX	V_{CCO}/GND Pairs	10	10	11	11	N/A	N/A
		Maximum I/O per Pair	6	8	9	8	N/A	N/A
	LXT	V_{CCO}/GND Pairs	6	10	11	10	N/A	N/A
		Maximum I/O per Pair	7	8	7	8	N/A	N/A
FG(G)676	LX45	V_{CCO}/GND Pairs	12	15	10	16	N/A	N/A
		Maximum I/O per Pair	3	7	8	7	N/A	N/A
	LX75, LX100, LX150	V_{CCO}/GND Pairs	12	9	10	10	6	6
		Maximum I/O per Pair	9	10	9	9	8	9
	LXT	V_{CCO}/GND Pairs	10	8	10	8	7	7
		Maximum I/O per Pair	8	7	8	8	7	7
FG(G)900	LX	V_{CCO}/GND Pairs	17	14	17	14	7	8
		Maximum I/O per Pair	7	6	7	8	7	6
	LXT	V_{CCO}/GND Pairs	15	14	13	14	7	8
		Maximum I/O per Pair	7	6	8	8	7	6

Table 34: **SSO Limit per V_{CCO}/GND Pair *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
2.5V	LVCMOS25	2	Fast	38	43	38	43
			Slow	46	52	46	48
			QuietIO	57	64	57	59
		4	Fast	21	24	21	23
			Slow	26	31	26	27
			QuietIO	33	32	33	30
		6	Fast	15	17	15	16
			Slow	19	22	19	19
			QuietIO	25	23	25	19
		8	Fast	12	15	12	14
			Slow	15	18	15	16
			QuietIO	21	19	21	16
		12	Fast	1	3	1	1
			Slow	2	7	2	4
			QuietIO	3	8	3	8
		16	Fast	1	3	1	1
			Slow	3	7	3	3
			QuietIO	4	9	4	8
		24	Fast	N/A	3	N/A	1
			Slow	N/A	5	N/A	2
			QuietIO	N/A	8	N/A	6
	SSTL_2_I [3]			10	11	10	11
	SSTL_2_II [3]			N/A	7	N/A	7
	DIFF_SSTL_2_I [3]			30	33	30	33
	DIFF_SSTL_2_II [3]			N/A	21	N/A	24

Input/Output Logic Switching Characteristics

Table 35: **ILOGIC2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T_{ICE0CK}/T_{ICKCE0}	CE0 pin Setup/Hold with respect to CLK	0.56/ –0.30	0.56/ –0.25	0.79/ –0.22	1.21/ –0.52	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.74/ –0.23	0.74/ –0.22	0.98/ –0.20	1.31/ –0.45	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	1.19/ –0.83	1.36/ –0.83	1.73/ –0.83	2.18/ –1.77	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	0.31/ 0.00	0.47/ 0.00	0.54/ 0.00	0.63/ –0.39	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.95	1.28	1.53	2.25	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY2)	0.23	0.39	0.44	0.74	ns
Sequential Delays						
T_{IDLO}	D pin to Q pin using flip-flop as a latch without Delay	1.56	1.86	2.39	3.49	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY2)	0.68	0.97	1.20	1.94	ns
T_{ICKQ}	CLK to Q outputs for XC devices	1.03	1.24	1.43	2.11	ns
	CLK to Q outputs for XA and XQ devices	1.38	N/A	1.78	2.11	ns
$T_{RQ\_ILOGIC2}$	SR pin to Q outputs	1.81	1.81	2.50	3.05	ns

Table 36: **OLOGIC2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.81/ –0.05	0.86/ –0.05	1.18/ 0.00	1.73/ –0.27	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.75/ –0.10	0.75/ –0.10	1.01/ –0.05	1.66/ –0.23	ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.70/ –0.28	0.79/ –0.28	1.03/ –0.23	1.39/ –0.47	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.24/ –0.08	0.56/ –0.06	0.83/ –0.01	0.99/ –0.19	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.58/ –0.06	0.72/ –0.06	1.18/ –0.01	1.51/ –0.13	ns
Sequential Delays						
T_{OCKQ}	CLK to OQ/TQ out for XC devices	0.48	0.51	0.74	0.74	ns
	CLK to OQ/TQ out for XA and XQ devices	0.85	N/A	1.16	0.74	ns
$T_{RQ\_OLOGIC2}$	SR pin to OQ/TQ out	1.81	1.81	2.50	3.05	ns

Block RAM Switching Characteristics

Table 43: **Block RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Block RAM Clock to Out Delays						
T_{RCKO_DO}	Clock CLK to DOUT output (without output register)(1)	1.85	2.10	2.10	3.50	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register)(2)	1.60	1.75	1.75	2.30	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs for XC devices(3)	0.35/ 0.10	0.40/ 0.12	0.40/ 0.12	0.50/ 0.15	ns, Min
	ADDR inputs for XA and XQ devices(3)	0.35/ 0.17	N/A	0.40/ 0.17	0.50/ 0.15	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs(4)	0.30/ 0.10	0.30/ 0.10	0.30/ 0.10	0.40/ 0.15	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.22/ 0.05	0.25/ 0.06	0.25/ 0.06	0.44/ 0.10	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.20/ 0.10	0.20/ 0.10	0.20/ 0.10	0.28/ 0.15	ns, Min
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input	0.25/ 0.10	0.33/ 0.10	0.33/ 0.10	0.28/ 0.15	ns, Min
Maximum Frequency						
F_{MAX}	Block RAM in all modes	320	280	280	150	MHz

Notes:

1. T_{RCKO_DO} includes T_{RCKO_DOA} and T_{RCKO_DOPA} as well as the B port equivalent timing parameters.
2. $T_{RCKO\_DO\_REG}$ includes $T_{RCKO\_DOA\_REG}$ and $T_{RCKO\_DOPA\_REG}$ as well as the B port equivalent timing parameters.
3. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
4. T_{RDCK_DI} includes both A and B inputs as well as the parity inputs of A and B.

Table 56: **Switching Characteristics for the Digital Frequency Synthesizer (DFS) for DCM_SP[(1)]**

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz
Output Clock Jitter[(2)(3)]										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN < 20 MHz	Use the Clocking Wizard								ps
	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN > 20 MHz	Typical = ±(1% of CLKFX period + 100)								ps
Duty Cycle[(4)(5)]										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±(1% of CLKFX period + 350)								ps
Phase Alignment[(5)]										
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used	–	±200	–	±200	–	±200	–	±250	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used	Maximum = ±(1% of CLKFX period + 200)								ps
LOCKED Time										
LOCK_FX[(2)]	When FCLKIN < 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	–	5	–	5	–	5	–	5	ms
	When FCLKIN > 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	–	0.45	–	0.45	–	0.45	–	0.60	ms

Notes:
1. The values in this table are based on the operating conditions described in Table 2 and Table 55.
2. For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
3. Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
5. Some duty cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.

Table 57: **Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)[(1)]**

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges (DCM_CLKGEN)										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz
CLKOUT_FREQ_FXDV	Frequency for the CLKFXDV output	0.15625	187.5	0.15625	187.5	0.15625	166.5	0.15625	100	MHz
Output Clock Jitter[(2)(3)]										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKOUT_PER_JITT_FXDV	Period jitter at the CLKFXDV output.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKFX_FREEZE_VAR	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX > 50 MHz	Maximum = ±3% of CLKFX period								ps
	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX < 50 MHz	Maximum = ±5% of CLKFX period								ps
CLKFX_FREEZE_TEMP_SLOPE	CLKFX period will change in free_oscillator mode over temperature. Add to CLKFX_FREEZE_VAR to determine total CLKFX period change. Percentage change for CLKFX period over 1°C.	Maximum = 0.1								%/°C
Duty Cycle[(4)(5)]										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
CLKOUT_DUTY_CYCLE_FXDV	Duty cycle precision for the CLKFXDV outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
Lock Time										
LOCK_FX[(2)]	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX, CLKFX180, and CLKFXDV signals are valid. Lock time requires CLKFX_DIVIDE < F_{IN}/(0.50 MHz) when: F_{CLKIN} < 50 MHz	–	50	–	50	–	50	–	50	ms
	when: F_{CLKIN} > 50 MHz	–	5	–	5	–	5	–	5	ms

Table 57: **Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)[(1)] *(Cont'd)***

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Spread Spectrum										
$F_{CLKIN\_FIXED\_SPREAD\_SPECTRUM}$	Frequency of the CLKIN input for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD/ CENTER_HIGH_SPREAD)	30	200	30	200	30	200	30	200	MHz
$T_{CENTER\_LOW\_SPREAD}$[(6)]	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD)	Typical = $\frac{100}{CLKFX\_DIVIDE}$ Maximum = 250								ps
$T_{CENTER\_HIGH\_SPREAD}$[(6)]	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM= CENTER_HIGH_SPREAD)	Typical = $\frac{240}{CLKFX\_DIVIDE}$ Maximum = 400								ps
$F_{MOD\_FIXED\_SPREAD\_SPECTRUM}$[(6)]	Average modulation frequency when using fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD / CENTER_HIGH_SPREAD)	Typical = F_{IN}/1024								MHz

Notes:
1. The values in this table are based on the operating conditions described in Table 2 and Table 55.
2. For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
3. Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
5. Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.
6. When using CENTER_LOW_SPREAD, CENTER_HIGH_SPREAD, the valid values for CLKFX_MULTIPLY are limited to 2 through 32, and the valid values for CLKFX_DIVIDE are limited to 1 through 4.

Table 58: **Recommended Operating Conditions for the Phase-Shift Clock in Variable Phase Mode (DCM_SP) or Dynamic Frequency Synthesis (DCM_CLKGEN)**

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Operating Frequency Ranges										
PSCLK_FREQ	Frequency for the PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) input.	1	167	1	167	1	167	1	100	MHz
Input Pulse Requirements										
PSCLK_PULSE	PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) pulse width as a percentage of the clock period.	40	60	40	60	40	60	40	60	%

Table 65: **Global Clock Input to Output Delay With DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in Source-Synchronous Mode.							
$T_{ICKOFDCM\_0}$	Global Clock and OUTFF *with* DCM	XC6SLX4	5.03	N/A	7.21	8.05	ns
		XC6SLX9	5.03	6.13	7.21	8.05	ns
		XC6SLX16	5.08	5.51	6.44	7.96	ns
		XC6SLX25	4.81	5.13	5.69	7.94	ns
		XC6SLX25T	4.81	5.13	5.69	N/A	ns
		XC6SLX45	5.26	5.69	6.63	7.92	ns
		XC6SLX45T	5.26	5.69	6.63	N/A	ns
		XC6SLX75	4.77	5.18	5.88	7.95	ns
		XC6SLX75T	4.77	5.18	5.88	N/A	ns
		XC6SLX100	4.72	5.11	5.76	8.59	ns
		XC6SLX100T	4.76	5.11	5.76	N/A	ns
		XC6SLX150	4.90	5.30	5.93	7.93	ns
		XC6SLX150T	4.90	5.30	5.93	N/A	ns
		XA6SLX4	5.35	N/A	7.21	N/A	ns
		XA6SLX9	5.35	N/A	7.21	N/A	ns
		XA6SLX16	5.42	N/A	6.44	N/A	ns
		XA6SLX25	5.13	N/A	5.69	N/A	ns
		XA6SLX25T	5.13	N/A	5.79	N/A	ns
		XA6SLX45	5.58	N/A	6.63	N/A	ns
		XA6SLX45T	5.58	N/A	6.63	N/A	ns
		XA6SLX75	5.09	N/A	5.87	N/A	ns
		XA6SLX75T	5.09	N/A	5.87	N/A	ns
		XA6SLX100	N/A	N/A	6.44	N/A	ns
		XQ6SLX75	N/A	N/A	5.87	7.95	ns
		XQ6SLX75T	5.09	N/A	5.87	N/A	ns
		XQ6SLX150	N/A	N/A	6.06	7.93	ns
		XQ6SLX150T	5.50	N/A	6.06	N/A	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 68: **Global Clock Input to Output Delay With DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.							
$T_{ICKOFDCM\_PLL}$	Global Clock and OUTFF with DCM and PLL	XC6SLX4	4.78	N/A	6.32	7.09	ns
		XC6SLX9	4.78	5.24	6.32	7.09	ns
		XC6SLX16	4.70	5.12	5.94	6.63	ns
		XC6SLX25	4.70	5.09	5.92	7.30	ns
		XC6SLX25T	4.70	5.09	5.92	N/A	ns
		XC6SLX45	4.63	4.98	5.83	7.26	ns
		XC6SLX45T	4.63	4.98	5.83	N/A	ns
		XC6SLX75	4.68	5.04	5.88	6.90	ns
		XC6SLX75T	4.68	5.04	5.88	N/A	ns
		XC6SLX100	4.72	5.07	5.92	7.77	ns
		XC6SLX100T	4.76	5.07	5.92	N/A	ns
		XC6SLX150	4.44	4.73	5.31	6.96	ns
		XC6SLX150T	4.44	4.73	5.31	N/A	ns
		XA6SLX4	5.07	N/A	6.18	N/A	ns
		XA6SLX9	5.07	N/A	6.18	N/A	ns
		XA6SLX16	5.22	N/A	5.77	N/A	ns
		XA6SLX25	5.01	N/A	5.80	N/A	ns
		XA6SLX25T	5.01	N/A	5.90	N/A	ns
		XA6SLX45	4.93	N/A	5.67	N/A	ns
		XA6SLX45T	4.93	N/A	5.67	N/A	ns
		XA6SLX75	4.94	N/A	5.70	N/A	ns
		XA6SLX75T	4.94	N/A	5.70	N/A	ns
		XA6SLX100	N/A	N/A	5.77	N/A	ns
		XQ6SLX75	N/A	N/A	5.70	6.90	ns
		XQ6SLX75T	4.94	N/A	5.70	N/A	ns
		XQ6SLX150	N/A	N/A	5.31	6.96	ns
		XQ6SLX150T	5.02	N/A	5.31	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Spartan-6 FPGA source-synchronous transmitter and receiver data-valid windows.

Table 78: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device[1]	Speed Grade				Units
			-3	-3N	-2	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion[2]	LX4	0.20	N/A	0.20	0.35	ns
		LX9	0.20	0.20	0.20	0.35	ns
		LX16	0.20	0.20	0.20	0.35	ns
		LX25	0.20	0.20	0.20	0.35	ns
		LX25T	0.20	0.20	0.20	N/A	ns
		LX45	0.20	0.20	0.20	0.35	ns
		LX45T	0.20	0.20	0.20	N/A	ns
		LX75	0.20	0.20	0.20	0.35	ns
		LX75T	0.20	0.20	0.20	N/A	ns
		LX100	0.20	0.20	0.20	0.35	ns
		LX100T	0.20	0.20	0.20	N/A	ns
		LX150	0.35	0.35	0.35	0.35	ns
		LX150T	0.35	0.35	0.35	N/A	ns
T_{CKSKEW}	Global Clock Tree Skew[3]	LX4	0.25	N/A	0.25	0.29	ns
		LX9	0.25	0.25	0.25	0.29	ns
		LX16	0.15	0.15	0.15	0.22	ns
		LX25	0.26	0.26	0.26	0.41	ns
		LX25T	0.26	0.26	0.26	N/A	ns
		LX45	0.20	0.20	0.20	0.28	ns
		LX45T	0.20	0.20	0.20	N/A	ns
		LX75	0.56	0.56	0.56	0.50	ns
		LX75T	0.56	0.56	0.56	N/A	ns
		XC6SLX100[4]	0.22	0.22	0.22	0.21	ns
		XA6SLX100[4]	N/A	N/A	0.43	N/A	ns
		LX100T	0.22	0.22	0.22	N/A	ns
		LX150	0.48	0.48	0.48	0.35	ns
		LX150T	0.48	0.48	0.48	N/A	ns
T_{DCD_BUFIO2}	I/O clock tree duty cycle distortion	LX devices	0.25	0.25	0.25	0.50	ns
		LXT devices	0.25	0.25	0.25	N/A	ns

Date	Version	Description of Revisions
09/14/11	2.4	Production release of the XA6SLX4 and XA6SLX9 devices in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added production released version of the XA6SLX100 to Table 26 and Table 27 using ISE v13.3 software with -2 speed specification v1.20. Updated R_{OUT_TERM} description in Table 4. Fixed the LVPECL V_H error in Table 31. Updated introduction in Simultaneously Switching Outputs. Added the XA6SLX100 to Table 63 through Table 78, and Table 81. Added Note 4 to Table 78 because the T_{CKSKEW} for the XC6SLX100 is not the same as the T_{CKSKEW} for the XA6SLX100. Revised the revision history for version 1.6 dated 06/24/10. Removed the parenthetical statement about the -3N speed grade: (specifications are identical to the -3 speed grade).
10/17/11	3.0	Changed the data sheet from Preliminary Product Specification to Product Specification. Updated the Switching Characteristics, page 19 speed specification version ISE v13.3 software to -2 and -3 speed specification v1.20 and -1L speed specification of v1.08. Also updated Note 1 in Table 27. In Table 43, *Block RAM Switching Characteristics*, the F_{MAX} value for the -2 speed grade has been changed from 260 MHz to 280 MHz. In Table 54, *Switching Characteristics for the DLL*, a Note 6 was added and linked to CLKIN_CLKFB_PHASE.