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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	7911
Number of Logic Elements/Cells	101261
Total RAM Bits	4939776
Number of I/O	338
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA, CSPBGA
Supplier Device Package	484-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx100-2csg484c

Table 2: Recommended Operating Conditions⁽¹⁾

Symbol	Description			Min	Typ	Max	Units
V _{CCINT}	Internal supply voltage relative to GND	-3, -3N, -2	Standard performance ⁽²⁾	1.14	1.2	1.26	V
		-3, -2	Extended performance ⁽²⁾	1.2	1.23	1.26	V
		-1L	Standard performance ⁽²⁾	0.95	1.0	1.05	V
V _{CCAUX} ⁽³⁾⁽⁴⁾	Auxiliary supply voltage relative to GND	V _{CCAUX} = 2.5V ⁽⁵⁾		2.375	2.5	2.625	V
		V _{CCAUX} = 3.3V		3.15	3.3	3.45	V
V _{CCO} ⁽⁶⁾⁽⁷⁾⁽⁸⁾	Output supply voltage relative to GND			1.1	–	3.45	V
V _{IN}	Input voltage relative to GND	All I/O standards (except PCI)	Commercial temperature (C)	–0.5	–	4.0	V
			Industrial temperature (I)	–0.5	–	3.95	V
			Expanded (Q) temperature	–0.5	–	3.95	V
		PCI I/O standard ⁽⁹⁾		–0.5	–	V _{CCO} + 0.5	V
I _{IN} ⁽¹⁰⁾	Maximum current through pin using PCI I/O standard when forward biasing the clamp diode. ⁽⁹⁾	Commercial (C) and Industrial temperature (I)		–	–	10	mA
		Expanded (Q) temperature		–	–	7	mA
V _{BATT} ⁽¹¹⁾	Battery voltage relative to GND, T _j = 0°C to +85°C (LX75, LX75T, LX100, LX100T, LX150, and LX150T only)			1.0	–	3.6	V
T _j	Junction temperature operating range	Commercial (C) range		0	–	85	°C
		Industrial temperature (I) range		–40	–	100	°C
		Expanded (Q) temperature range		–40	–	125	°C

Notes:

- All voltages are relative to ground.
- See *Interface Performances for Memory Interfaces* in Table 25. The extended performance range is specified for designs not using the standard V_{CCINT} voltage range. The standard V_{CCINT} voltage range is used for:
 - Designs that do not use an MCB
 - LX4 devices
 - Devices in the TQG144 or CPG196 packages
 - Devices with the -3N speed grade
- Recommended maximum voltage droop for V_{CCAUX} is 10 mV/ms.
- During configuration, if V_{CCO_2} is 1.8V, then V_{CCAUX} must be 2.5V.
- The -1L devices require $V_{CCAUX} = 2.5V$ when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.
- Configuration data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
- For PCI systems, the transmitter and receiver should have common supplies for V_{CCO} .
- Devices with a -1L speed grade do not support Xilinx PCI IP.
- Do not exceed a total of 100 mA per bank.
- V_{BATT} is required to maintain the battery backed RAM (BBR) AES key when V_{CCAUX} is not applied. Once V_{CCAUX} is applied, V_{BATT} can be unconnected. When BBR is not used, Xilinx recommends connecting to V_{CCAUX} or GND. However, V_{BATT} can be unconnected.

Table 5: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	LX4	2.5	2.5	2.5	2.5	mA
		LX9	2.5	2.5	2.5	2.5	mA
		LX16	3.0	3.0	3.0	3.0	mA
		LX25	4.0	4.0	4.0	4.0	mA
		LX25T	4.0	4.0	4.0	N/A	mA
		LX45	5.0	5.0	5.0	5.0	mA
		LX45T	5.0	5.0	5.0	N/A	mA
		LX75	7.0	7.0	7.0	7.0	mA
		LX75T	7.0	7.0	7.0	N/A	mA
		LX100	9.0	9.0	9.0	9.0	mA
		LX100T	9.0	9.0	9.0	N/A	mA
		LX150	12.0	12.0	12.0	12.0	mA
		LX150T	12.0	12.0	12.0	N/A	mA

Notes:

- Typical values are specified at nominal voltage, 25°C junction temperatures (T_j). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 25°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. Nominal V_{CCINT} is 1.20V; use the XPE tool to calculate 1.23V values for the nominal V_{CCINT} of the extended performance range.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- If differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 6: Power Supply Ramp Time

Symbol	Description	Speed Grade	Ramp Time	Units
V _{CCINTR}	Internal supply voltage ramp time	-3, -3N, -2	0.20 to 50.0	ms
		-1L	0.20 to 40.0	ms
V _{CCO2} ⁽¹⁾	Output drivers bank 2 supply voltage ramp time	All	0.20 to 50.0	ms
V _{CCAUXR}	Auxiliary supply voltage ramp time	All	0.20 to 50.0	ms

Notes:

- The minimum V_{CCO2} for power-on reset and configuration is 1.65V.
- Spartan-6 FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply. Use the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools to estimate current drain on these supplies. Spartan-6 devices do not have a required power-on sequence.

Table 10: Differential I/O Standard DC Input and Output Levels

I/O Standard	V _{ID}		V _{ICM}		V _{OD}		V _{OCM}		V _{OH}	V _{OL}
	mV, Min	mV, Max	V, Min	V, Max	mV, Min	mV, Max	V, Min	V, Max	V, Min	V, Max
LVDS_33 ⁽²⁾⁽³⁾	100	600	0.3	2.35	247	454	1.125	1.375	–	–
LVDS_25 ⁽²⁾⁽³⁾	100	600	0.3	2.35	247	454	1.125	1.375	–	–
BLVDS_25 ⁽²⁾⁽³⁾	100	–	0.3	2.35	240	460	Typical 50% V _{CCO}		–	–
MINI_LVDS_33	200	600	0.3	1.95	300	600	1.0	1.4	–	–
MINI_LVDS_25	200	600	0.3	1.95	300	600	1.0	1.4	–	–
LVPECL_33 ⁽²⁾⁽³⁾	100	1000	0.3	2.8 ⁽¹⁾	Inputs only					
LVPECL_25 ⁽²⁾⁽³⁾	100	1000	0.3	1.95	Inputs only					
RSDS_33 ⁽²⁾⁽³⁾	100	–	0.3	1.5	100	400	1.0	1.4	–	–
RSDS_25 ⁽²⁾⁽³⁾	100	–	0.3	1.5	100	400	1.0	1.4	–	–
TMDS_33	150	1200	2.7	3.23 ⁽¹⁾	400	800	V _{CCO} – 0.405	V _{CCO} – 0.190	–	–
PPDS_33 ⁽²⁾⁽³⁾	100	400	0.2	2.3	100	400	0.5	1.4	–	–
PPDS_25 ⁽²⁾⁽³⁾	100	400	0.2	2.3	100	400	0.5	1.4	–	–
DISPLAY_PORT	190	1260	0.3	2.35	–	–	Typical 50% V _{CCO}		–	–
DIFF_MOBILE_DDR	100	–	0.78	1.02	–	–	–	–	90% V _{CCO}	10% V _{CCO}
DIFF_HSTL_I	100	–	0.68	0.9	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_HSTL_II	100	–	0.68	0.9	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_HSTL_III	100	–	0.68	0.9	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_HSTL_I_18	100	–	0.8	1.1	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_HSTL_II_18	100	–	0.8	1.1	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_HSTL_III_18	100	–	0.8	1.1	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_SSTL3_I	100	–	1.0	1.9	–	–	–	–	V _{TT} + 0.6	V _{TT} – 0.6
DIFF_SSTL3_II	100	–	1.0	1.9	–	–	–	–	V _{TT} + 0.8	V _{TT} – 0.8
DIFF_SSTL2_I	100	–	1.0	1.5	–	–	–	–	V _{TT} + 0.61	V _{TT} – 0.61
DIFF_SSTL2_II	100	–	1.0	1.5	–	–	–	–	V _{TT} + 0.81	V _{TT} – 0.81
DIFF_SSTL18_I	100	–	0.7	1.1	–	–	–	–	V _{TT} + 0.47	V _{TT} – 0.47
DIFF_SSTL18_II	100	–	0.7	1.1	–	–	–	–	V _{TT} + 0.6	V _{TT} – 0.6
DIFF_SSTL15_II	100	–	0.55	0.95	–	–	–	–	V _{TT} + 0.4	V _{TT} – 0.4

Notes:

1. LVPECL_33 and TMDS_33 maximum V_{ICM} is the lower of V (maximum) or V_{CCAUX} – (V_{ID}/2)
2. When V_{CCAUX} = 3.3V, the DCD can be higher than 5% for V_{ICM} < 0.7V when using these I/O standards: LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, LVPECL_33, RSDS_25, RSDS_33, PPDS_25, and PPDS_33.
3. The -1L devices require V_{CCAUX} = 2.5V when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.

Table 17: GTP Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	200	800	2000	mV
R_{IN}	Differential input resistance	80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult [UG386](#): *Spartan-6 FPGA GTP Transceivers User Guide* for further information.

Table 18: GTP Transceiver Performance

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
F_{GTPMAX}	Maximum GTP transceiver data rate	3.2	3.2	2.7	N/A	Gb/s
$F_{GTPRANGE1}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 1	1.88 to 3.2	1.88 to 3.2	1.88 to 2.7	N/A	Gb/s
$F_{GTPRANGE2}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 2	0.94 to 1.62	0.94 to 1.62	0.94 to 1.62	N/A	Gb/s
$F_{GTPRANGE3}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 4	0.6 to 0.81	0.6 to 0.81	0.6 to 0.81	N/A	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	1.62	1.62	1.62	N/A	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	0.94	0.94	0.94	N/A	GHz

Table 19: GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
$F_{GTPDRCLK}$	GTP transceiver DCLK (DRP clock) maximum frequency	125	125	100	N/A	MHz

Table 20: GTP Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All LXT Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	160	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	μ s

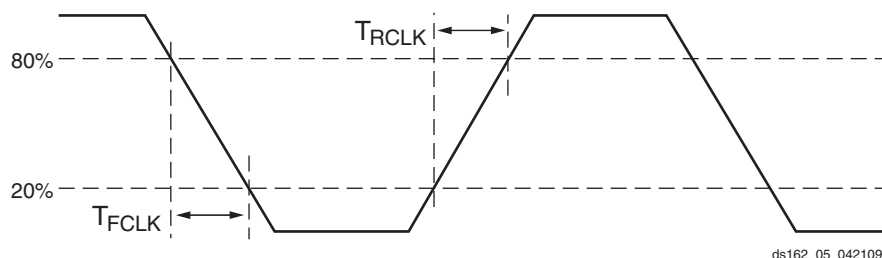


Figure 3: Reference Clock Timing Parameters

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVDS_33	1.24	1.42	1.69	1.89	3000	3000	ns
LVDS_25	1.08	1.26	1.79	1.99	3000	3000	ns
BLVDS_25	1.09	1.27	1.86	2.06	1.86	2.06	ns
MINI_LVDS_33	1.25	1.43	1.71	1.91	3000	3000	ns
MINI_LVDS_25	1.08	1.26	1.79	1.99	3000	3000	ns
LVPECL_33	1.25	1.43	N/A	N/A	N/A	N/A	ns
LVPECL_25	1.09	1.27	N/A	N/A	N/A	N/A	ns
RSDS_33 (point to point)	1.24	1.42	1.71	1.91	3000	3000	ns
RSDS_25 (point to point)	1.08	1.26	1.79	1.99	3000	3000	ns
TMDS_33	1.29	1.47	1.68	1.88	3000	3000	ns
PPDS_33	1.25	1.43	1.71	1.91	3000	3000	ns
PPDS_25	1.08	1.26	1.82	2.02	3000	3000	ns
PCI33_3	1.14	1.32	3.81	4.01	3.81	4.01	ns
PCI66_3	1.14	1.32	3.81	4.01	3.81	4.01	ns
DISPLAY_PORT	1.09	1.27	3.29	3.49	3.29	3.49	ns
I2C	1.40	1.58	11.70	11.90	11.70	11.90	ns
SMBUS	1.40	1.58	11.70	11.90	11.70	11.90	ns
SDIO	1.43	1.61	2.78	2.98	2.78	2.98	ns
MOBILE_DDR	1.01	1.19	2.50	2.70	2.50	2.70	ns
HSTL_I	1.01	1.19	1.80	2.00	1.80	2.00	ns
HSTL_II	1.01	1.19	1.86	2.06	1.86	2.06	ns
HSTL_III	1.07	1.25	1.81	2.01	1.81	2.01	ns
HSTL_I_18	1.05	1.23	1.91	2.11	1.91	2.11	ns
HSTL_II_18	1.05	1.23	1.99	2.19	1.99	2.19	ns
HSTL_III_18	1.13	1.31	1.93	2.13	1.93	2.13	ns
SSTL3_I	1.65	1.83	1.97	2.17	1.97	2.17	ns
SSTL3_II	1.65	1.83	2.15	2.35	2.15	2.35	ns
SSTL2_I	1.37	1.55	1.91	2.11	1.91	2.11	ns
SSTL2_II	1.37	1.55	2.00	2.20	2.00	2.20	ns
SSTL18_I	0.99	1.17	1.77	1.97	1.77	1.97	ns
SSTL18_II	1.00	1.18	1.80	2.00	1.80	2.00	ns
SSTL15_II	1.00	1.18	1.81	2.01	1.81	2.01	ns
DIFF_HSTL_I	1.01	1.19	1.91	2.11	1.91	2.11	ns
DIFF_HSTL_II	1.00	1.18	1.86	2.06	1.86	2.06	ns
DIFF_HSTL_III	1.00	1.18	1.83	2.03	1.83	2.03	ns
DIFF_HSTL_I_18	1.04	1.22	1.93	2.13	1.93	2.13	ns
DIFF_HSTL_II_18	1.04	1.22	1.83	2.03	1.83	2.03	ns
DIFF_HSTL_III_18	1.04	1.22	1.83	2.03	1.83	2.03	ns

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS33, Slow, 6 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVC MOS33, Slow, 8 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVC MOS33, Slow, 12 mA	1.41	1.59	2.53	2.73	2.53	2.73	ns
LVC MOS33, Slow, 16 mA	1.41	1.59	2.45	2.65	2.45	2.65	ns
LVC MOS33, Slow, 24 mA	1.41	1.59	2.42	2.62	2.42	2.62	ns
LVC MOS33, Fast, 2 mA	1.41	1.59	4.05	4.25	4.05	4.25	ns
LVC MOS33, Fast, 4 mA	1.41	1.59	2.66	2.86	2.66	2.86	ns
LVC MOS33, Fast, 6 mA	1.41	1.59	2.46	2.66	2.46	2.66	ns
LVC MOS33, Fast, 8 mA	1.41	1.59	2.21	2.41	2.21	2.41	ns
LVC MOS33, Fast, 12 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVC MOS33, Fast, 16 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVC MOS33, Fast, 24 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVC MOS25, QUIETIO, 2 mA	0.89	1.07	5.00	5.20	5.00	5.20	ns
LVC MOS25, QUIETIO, 4 mA	0.89	1.07	3.85	4.05	3.85	4.05	ns
LVC MOS25, QUIETIO, 6 mA	0.89	1.07	3.60	3.80	3.60	3.80	ns
LVC MOS25, QUIETIO, 8 mA	0.89	1.07	3.34	3.54	3.34	3.54	ns
LVC MOS25, QUIETIO, 12 mA	0.89	1.07	2.98	3.18	2.98	3.18	ns
LVC MOS25, QUIETIO, 16 mA	0.89	1.07	2.79	2.99	2.79	2.99	ns
LVC MOS25, QUIETIO, 24 mA	0.89	1.07	2.64	2.84	2.64	2.84	ns
LVC MOS25, Slow, 2 mA	0.89	1.07	3.96	4.16	3.96	4.16	ns
LVC MOS25, Slow, 4 mA	0.89	1.07	2.96	3.16	2.96	3.16	ns
LVC MOS25, Slow, 6 mA	0.89	1.07	2.88	3.08	2.88	3.08	ns
LVC MOS25, Slow, 8 mA	0.89	1.07	2.63	2.83	2.63	2.83	ns
LVC MOS25, Slow, 12 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVC MOS25, Slow, 16 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVC MOS25, Slow, 24 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVC MOS25, Fast, 2 mA	0.89	1.07	3.52	3.72	3.52	3.72	ns
LVC MOS25, Fast, 4 mA	0.89	1.07	2.43	2.63	2.43	2.63	ns
LVC MOS25, Fast, 6 mA	0.89	1.07	2.23	2.43	2.23	2.43	ns
LVC MOS25, Fast, 8 mA	0.89	1.07	2.16	2.36	2.16	2.36	ns
LVC MOS25, Fast, 12 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVC MOS25, Fast, 16 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVC MOS25, Fast, 24 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVC MOS18, QUIETIO, 2 mA	1.25	1.43	6.11	6.31	6.11	6.31	ns
LVC MOS18, QUIETIO, 4 mA	1.25	1.43	4.88	5.08	4.88	5.08	ns
LVC MOS18, QUIETIO, 6 mA	1.25	1.43	4.20	4.40	4.20	4.40	ns
LVC MOS18, QUIETIO, 8 mA	1.25	1.43	3.86	4.06	3.86	4.06	ns
LVC MOS18, QUIETIO, 12 mA	1.25	1.43	3.49	3.69	3.49	3.69	ns

I/O Standard Measurement Methodology

Input Delay Measurements

Table 31 shows the test setup parameters used for measuring input delay.

Table 31: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)}$	$V_H^{(1)}$	$V_{MEAS}^{(3)(4)}$	$V_{REF}^{(2)(4)}$
LVTTTL (Low-Voltage Transistor-Transistor Logic)	LVTTTL	0	3.0	1.4	—
LVC MOS (Low-Voltage CMOS), 3.3V	LVC MOS33	0	3.3	1.65	—
LVC MOS, 2.5V	LVC MOS25	0	2.5	1.25	—
LVC MOS, 1.8V	LVC MOS18	0	1.8	0.9	—
LVC MOS, 1.5V	LVC MOS15	0	1.5	0.75	—
LVC MOS, 1.2V	LVC MOS12	0	1.2	0.6	—
PCI (Peripheral Component Interface), 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3	Per PCI Specification			—
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III	HSTL_III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	1.1
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
SSTL, Class II, 1.5V	SSTL15_II	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	$1.25 - 0.125$	$1.25 + 0.125$	0 ⁽⁵⁾	—
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V & 3.3V	LVPECL_25, LVPECL_33	$1.2 - 0.3$	$1.2 + 0.3$	0 ⁽⁵⁾	—
BLVDS (Bus LVDS), 2.5V	BLVDS_25	$1.3 - 0.125$	$1.3 + 0.125$	0 ⁽⁵⁾	—
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	$1.2 - 0.125$	$1.2 + 0.125$	0 ⁽⁵⁾	—
RS DS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RS DS_25, RS DS_33	$1.2 - 0.1$	$1.2 + 0.1$	0 ⁽⁵⁾	—
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	$3.0 - 0.1$	$3.0 + 0.1$	0 ⁽⁵⁾	—
PPDS (Point-to-Point Differential Signaling), 2.5V & 3.3V	PPDS_25, PPDS_33	$1.25 - 0.1$	$1.25 + 0.1$	0 ⁽⁵⁾	—

Notes:

1. Input waveform switches between V_L and V_H .
2. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 4.
5. The value given is the differential input voltage.

Table 33: Spartan-6 FPGA V_{CCO}/GND Pairs per Bank

Package	Devices	Description	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5
TQG144	LX	V _{CCO} /GND Pairs	3	3	2	3	N/A	N/A
		Maximum I/O per Pair	8	8	13	8	N/A	N/A
CPG196	LX	V _{CCO} /GND Pairs	4	6	4	6	N/A	N/A
		Maximum I/O per Pair	6	4	7	4	N/A	N/A
CSG225	LX	V _{CCO} /GND Pairs	4	4	4	4	N/A	N/A
		Maximum I/O per Pair	10	10	9	10	N/A	N/A
FT(G)256	LX	V _{CCO} /GND Pairs	5	6	4	5	N/A	N/A
		Maximum I/O per Pair	8	9	9	10	N/A	N/A
CSG324	LX	V _{CCO} /GND Pairs	6	6	6	6	N/A	N/A
		Maximum I/O per Pair	10	9	10	9	N/A	N/A
	LXT	V _{CCO} /GND Pairs	4	6	6	6	N/A	N/A
		Maximum I/O per Pair	4	9	10	9	N/A	N/A
CS(G)484	LX	V _{CCO} /GND Pairs	8	13	8	13	N/A	N/A
		Maximum I/O per Pair	7	8	7	8	N/A	N/A
	LXT	V _{CCO} /GND Pairs	7	12	8	13	N/A	N/A
		Maximum I/O per Pair	5	8	6	8	N/A	N/A
FG(G)484	LX	V _{CCO} /GND Pairs	10	10	11	11	N/A	N/A
		Maximum I/O per Pair	6	8	9	8	N/A	N/A
	LXT	V _{CCO} /GND Pairs	6	10	11	10	N/A	N/A
		Maximum I/O per Pair	7	8	7	8	N/A	N/A
FG(G)676	LX45	V _{CCO} /GND Pairs	12	15	10	16	N/A	N/A
		Maximum I/O per Pair	3	7	8	7	N/A	N/A
	LX75, LX100, LX150	V _{CCO} /GND Pairs	12	9	10	10	6	6
		Maximum I/O per Pair	9	10	9	9	8	9
	LXT	V _{CCO} /GND Pairs	10	8	10	8	7	7
		Maximum I/O per Pair	8	7	8	8	7	7
FG(G)900	LX	V _{CCO} /GND Pairs	17	14	17	14	7	8
		Maximum I/O per Pair	7	6	7	8	7	6
	LXT	V _{CCO} /GND Pairs	15	14	13	14	7	8
		Maximum I/O per Pair	7	6	8	8	7	6

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

V _{CCO}	I/O Standard	Drive	Slew	SSO Limit per V _{CCO} /GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
3.3V	LVCMOS33	2	Fast	42	46	42	44
			Slow	50	55	50	49
			QuietIO	60	68	60	60
		4	Fast	21	27	21	25
			Slow	32	37	32	32
			QuietIO	39	42	39	37
		6	Fast	14	19	14	17
			Slow	19	25	19	22
			QuietIO	29	30	29	25
		8	Fast	11	15	11	14
			Slow	15	20	15	18
			QuietIO	25	24	25	20
		12	Fast	1	3	1	1
			Slow	2	5	2	2
			QuietIO	4	9	4	7
		16	Fast	1	2	1	1
			Slow	1	5	1	1
			QuietIO	3	10	3	8
		24	Fast	1	2	1	1
			Slow	2	5	2	1
			QuietIO	7	9	7	7

Input/Output Logic Switching Characteristics

Table 35: ILOGIC2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T _{ICE0CK} /T _{ICKCE0}	CE0 pin Setup/Hold with respect to CLK	0.56/ −0.30	0.56/ −0.25	0.79/ −0.22	1.21/ −0.52	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.74/ −0.23	0.74/ −0.22	0.98/ −0.20	1.31/ −0.45	ns
T _{IDOCK} /T _{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	1.19/ −0.83	1.36/ −0.83	1.73/ −0.83	2.18/ −1.77	ns
T _{IDOCKD} /T _{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	0.31/ 0.00	0.47/ 0.00	0.54/ 0.00	0.63/ −0.39	ns
Combinatorial						
T _{IDI}	D pin to O pin propagation delay, no Delay	0.95	1.28	1.53	2.25	ns
T _{IDID}	DDLY pin to O pin propagation delay (using IODELAY2)	0.23	0.39	0.44	0.74	ns
Sequential Delays						
T _{IDLO}	D pin to Q pin using flip-flop as a latch without Delay	1.56	1.86	2.39	3.49	ns
T _{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY2)	0.68	0.97	1.20	1.94	ns
T _{ICKQ}	CLK to Q outputs for XC devices	1.03	1.24	1.43	2.11	ns
	CLK to Q outputs for XA and XQ devices	1.38	N/A	1.78	2.11	ns
T _{RQ_ILOGIC2}	SR pin to Q outputs	1.81	1.81	2.50	3.05	ns

Table 36: OLOGIC2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T _{ODCK} /T _{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.81/ −0.05	0.86/ −0.05	1.18/ 0.00	1.73/ −0.27	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.75/ −0.10	0.75/ −0.10	1.01/ −0.05	1.66/ −0.23	ns
T _{OSRCK} /T _{OCKSR}	SR pin Setup/Hold with respect to CLK	0.70/ −0.28	0.79/ −0.28	1.03/ −0.23	1.39/ −0.47	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.24/ −0.08	0.56/ −0.06	0.83/ −0.01	0.99/ −0.19	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.58/ −0.06	0.72/ −0.06	1.18/ −0.01	1.51/ −0.13	ns
Sequential Delays						
T _{OCKQ}	CLK to OQ/TQ out for XC devices	0.48	0.51	0.74	0.74	ns
	CLK to OQ/TQ out for XA and XQ devices	0.85	N/A	1.16	0.74	ns
T _{RQ_OLOGIC2}	SR pin to OQ/TQ out	1.81	1.81	2.50	3.05	ns

Input Serializer/Deserializer Switching Characteristics

Table 37: ISERDES2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold for Control Lines						
T _{ISCKC_BITSIP} / T _{ISCKC_BITSIP}	BITSIP pin Setup/Hold with respect to CLKDIV	0.16/ −0.09	0.20/ −0.09	0.31/ −0.09	0.34/ −0.14	ns
T _{ISCKC_CE} / T _{ISCKC_CE}	CE pin Setup/Hold with respect to CLK	0.71/ −0.47	0.71/ −0.42	0.97/ −0.42	1.39/ −0.71	ns
Setup/Hold for Data Lines						
T _{ISDCK_D} / T _{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.24/ −0.15	0.25/ −0.05	0.29/ −0.05	0.09/ −0.05	ns
T _{ISDCK_DDLY} / T _{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	−0.25/ 0.30	−0.25/ 0.42	−0.25/ 0.56	−0.54/ 0.67	ns
T _{ISDCK_D_DDR} / T _{ISCKD_D_DDR}	D pin Setup/Hold with respect to CLK at DDR mode	−0.03/ 0.04	−0.03/ 0.16	−0.03/ 0.18	−0.05/ 0.12	ns
T _{ISDCK_DDLY_DDR} / T _{ISCKD_DDLY_DDR}	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY2)	−0.40/ 0.48	−0.40/ 0.53	−0.40/ 0.71	−0.71/ 0.86	ns
Sequential Delays						
T _{ISCKO_Q}	CLKDIV to out at Q pin	1.30	1.44	2.02	2.22	ns
F _{CLKDIV}	CLKDIV maximum frequency	270	262.5	250	125	MHz

Output Serializer/Deserializer Switching Characteristics

Table 38: OSERDES2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T _{OSDCK_D} /T _{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	−0.03/ 1.02	−0.03/ 1.17	−0.03/ 1.27	−0.02/ 0.23	ns
T _{OSDCK_T} /T _{OSCKD_T} ⁽¹⁾	T input Setup/Hold with respect to CLK	−0.05/ 1.03	−0.05/ 1.13	−0.05/ 1.23	−0.05/ 0.24	ns
T _{OSCCK_OCE} /T _{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.12/ −0.03	0.15/ −0.03	0.24/ −0.03	0.28/ −0.17	ns
T _{OSCCK_TCE} /T _{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.14/ −0.08	0.17/ −0.08	0.27/ −0.08	0.31/ −0.16	ns
Sequential Delays						
T _{OSCKO_OQ}	Clock to out from CLK to OQ	0.94	1.11	1.51	1.89	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ	0.94	1.11	1.51	1.91	ns
F _{CLKDIV}	CLKDIV maximum frequency	270	262.5	250	125	MHz

Notes:

- $T_{OSDCK_T2} / T_{OSCKD_T2}$ (T input setup/hold with respect to CLKDIV) are reported as $T_{OSDCK_T} / T_{OSCKD_T}$ in TRACE report.

Configuration Switching Characteristics

Table 47: Configuration Switching Characteristics⁽¹⁾

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Power-up Timing Characteristics						
T _{PL} ⁽²⁾	PROGRAM_B Latency	4	4	4	5	ms, Max
T _{POR} ⁽²⁾	Power-on reset (50 ms ramp time) ⁽³⁾	5/30	5/34	5/40	5/40	ms, Min/Max
	Power-on reset (10 ms ramp time)	5/25	5/29	5/35	5/40	ms, Min/Max
T _{PROGRAM}	PROGRAM_B Pulse Width	500	500	500	500	ns, Min
Slave Serial Mode Programming Switching						
T _{DCCK} /T _{CCKD}	DIN Setup/Hold, slave mode	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T _{CCO}	CCLK to DOUT	12	12	12	17	ns, Max
F _{SCCK}	Slave mode external CCLK	80	80	80	50	MHz, Max
Slave SelectMAP Mode Programming Switching						
T _{SMDCK} /T _{SMCKD}	SelectMAP Data Setup/Hold	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T _{SMCSCCK} /T _{SMCKCS}	CSI_B Setup/Hold	7.0/0.0	7.0/0.0	7.0/0.0	9.0/2.0	ns, Min
T _{SMWCCK} /T _{SMCKW}	RDWR_B Setup/Hold	17.0/1.0	17.0/1.0	17.0/1.0	27.0/2.0	ns, Min
T _{SMCKCSO}	CSO_B clock to out	16	16	16	26	ns, Max
T _{SMCO}	CCLK to DATA out in readback	13	13	13	25	ns, Max
T _{SMCKBY}	CCLK to BUSY out in readback	12	12	12	17	ns, Max
F _{SMCK}	Maximum CCLK frequency (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	25	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x8 mode, LX150, and LX150T only)	40	40	40	20	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x16 mode only)	35	35	35	20	MHz, Max
F _{RBCK}	Maximum Readback CCLK frequency, including block RAM (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	20	20	20	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	30	MHz, Max
	Maximum Readback CCLK frequency, including block RAM (LX100, LX100T, LX150, and LX150T only)	12	12	12	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX100, LX100T, LX150, and LX150T only)	35	35	35	20	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK}	TMS and TDI Setup time before TCK	10	10	10	17	ns, Min
T _{TCKTAP}	TMS and TDI Hold time after TCK	5.5	5.5	5.5	5.5	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output valid	6.5	6.5	6.5	8	ns, Max
T _{TCKH}	TCK clock minimum High time	12	12	12	21	ns, Min
T _{TCKL}	TCK clock minimum Low time	12	12	12	21	ns, Min
F _{TCK}	Maximum configuration TCK clock frequency	33	33	33	18	MHz, Max
F _{TCKB}	Maximum boundary-scan TCK clock frequency	33	33	33	18	MHz, Max
F _{TCKAES}	Maximum AES key TCK clock frequency	2	2	2	2	MHz, Max

Table 47: Configuration Switching Characteristics⁽¹⁾ (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
BPI Master Flash Mode Programming Switching ⁽⁴⁾						
T _{BPICCO} ⁽⁵⁾	A[25:0], FCS_B, FOE_B, FWE_B, LDC outputs valid after CCLK falling edge	15	15	15	20	ns, Max
T _{BPIICCK}	Master BPI CCLK (output) delay	10/100	10/100	10/100	10/130	μs, Min/Max
T _{BPIDCC} /T _{BPICCD}	Setup/Hold on D[15:0] data input pins	5.0/1.0	5.0/1.0	5.0/1.0	6.0/2.0	ns, Min
SPI Master Flash Mode Programming Switching ⁽⁶⁾						
T _{SPIDCC} /T _{SPIDCCD}	DIN, MISO0, MISO1, MISO2, MISO3, Setup/Hold before/after the rising CCLK edge	5.0/1.0	5.0/1.0	5.0/1.0	7.0/1.0	ns, Min
T _{SPIICCK}	Master SPI CCLK (output) delay	0.4/7.0	0.4/7.0	0.4/7.0	0.4/10.0	μs, Min/Max
T _{SPICCM}	MOSI clock to out	13	13	13	19	ns, Max
T _{SPICCF}	CSO_B clock to out	16	16	16	26	ns, Max
CCLK Output (Master Modes)						
T _{MCCKL}	Master CCLK clock duty cycle Low	40/60				%, Min/Max
T _{MCCKH}	Master CCLK clock duty cycle High	40/60				%, Min/Max
F _{MCCK}	Maximum frequency, serial mode (Master Serial/SPI) All devices	40	40	40	30	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T	40	40	40	25	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x8 mode, LX150, and LX150T	40	40	40	20	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x16 mode	35	35	35	20	MHz, Max
F _{MCCKTOL}	Frequency Tolerance, master mode	±50	±50	±50	±50	%
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time	5	5	5	8	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time	5	5	5	8	ns, Min
USERCCLK Input						
T _{USERCCLKL}	USERCCLK clock minimum Low time	12	12	12	16	ns, Min
T _{USERCCLKH}	USERCCLK clock minimum High time	12	12	12	16	ns, Min
F _{USERCCLK}	Maximum USERCCLK frequency	40	40	40	30	MHz, Max

Notes:

- Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
- To support longer delays in configuration, use the design solutions described in [UG380: Spartan-6 FPGA Configuration User Guide](#).
- [Table 6](#) specifies the power supply ramp time.
- BPI mode is not supported in:
 - LX4, LX25, or LX25T devices
 - LX9 devices in the TQG144 package
 - LX9 or LX16 devices in the CPG196 package.
- Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
- Defense-grade Spartan-6Q -2Q devices configure in single default SPI Master (x1) mode at T_j = -55°C. During operation and when using all other configuration functions, the minimum operating temperature is -40°C.

Table 57: Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)⁽¹⁾ (Cont'd)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Spread Spectrum										
F _{CLKIN_FIXED_SPREAD_SPECTRUM}	Frequency of the CLKIN input for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD/ CENTER_HIGH_SPREAD)	30	200	30	200	30	200	30	200	MHz
T _{CENTER_LOW_SPREAD} ⁽⁶⁾	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD)	Typical = $\frac{100}{\text{CLKFX_DIVIDE}}$ Maximum = 250								ps
T _{CENTER_HIGH_SPREAD} ⁽⁶⁾	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM= CENTER_HIGH_SPREAD)	Typical = $\frac{240}{\text{CLKFX_DIVIDE}}$ Maximum = 400								ps
F _{MOD_FIXED_SPREAD_SPECTRUM} ⁽⁶⁾	Average modulation frequency when using fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD / CENTER_HIGH_SPREAD)	Typical = F _{IN} /1024								MHz

Notes:

- The values in this table are based on the operating conditions described in Table 2 and Table 55.
- For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
- Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
- The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
- Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of $\pm(1\% \text{ of CLKFX period} + 200 \text{ ps})$. Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is $\pm(100 \text{ ps} + 200 \text{ ps}) = \pm 300 \text{ ps}$.
- When using CENTER_LOW_SPREAD, CENTER_HIGH_SPREAD, the valid values for CLKFX_MULTIPLY are limited to 2 through 32, and the valid values for CLKFX_DIVIDE are limited to 1 through 4.

Table 58: Recommended Operating Conditions for the Phase-Shift Clock in Variable Phase Mode (DCM_SP) or Dynamic Frequency Synthesis (DCM_CLKGEN)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Operating Frequency Ranges										
PSCLK_FREQ	Frequency for the PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) input.	1	167	1	167	1	167	1	100	MHz
Input Pulse Requirements										
PSCLK_PULSE	PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) pulse width as a percentage of the clock period.	40	60	40	60	40	60	40	60	%

Table 64: Global Clock Input to Output Delay With DCM in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in System-Synchronous Mode.							
T _{ICKOFDCM}	Global Clock and OUTFF <i>with</i> DCM	XC6SLX4	4.23	N/A	6.11	6.60	ns
		XC6SLX9	4.23	5.17	6.11	6.60	ns
		XC6SLX16	4.28	4.57	5.34	6.36	ns
		XC6SLX25	3.95	4.18	4.59	6.91	ns
		XC6SLX25T	3.95	4.18	4.59	N/A	ns
		XC6SLX45	4.37	4.70	5.50	6.85	ns
		XC6SLX45T	4.37	4.70	5.50	N/A	ns
		XC6SLX75	3.90	4.23	4.77	6.31	ns
		XC6SLX75T	3.90	4.23	4.77	N/A	ns
		XC6SLX100	3.86	4.16	4.66	7.25	ns
		XC6SLX100T	3.90	4.16	4.66	N/A	ns
		XC6SLX150	4.03	4.33	4.83	6.63	ns
		XC6SLX150T	4.03	4.33	4.83	N/A	ns
		XA6SLX4	4.55	N/A	6.11	N/A	ns
		XA6SLX9	4.55	N/A	6.11	N/A	ns
		XA6SLX16	4.62	N/A	5.33	N/A	ns
		XA6SLX25	4.27	N/A	4.59	N/A	ns
		XA6SLX25T	4.27	N/A	4.69	N/A	ns
		XA6SLX45	4.69	N/A	5.50	N/A	ns
		XA6SLX45T	4.69	N/A	5.50	N/A	ns
		XA6SLX75	4.22	N/A	4.77	N/A	ns
		XA6SLX75T	4.22	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.34	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	6.31	ns
		XQ6SLX75T	4.22	N/A	4.77	N/A	ns
		XQ6SLX150	N/A	N/A	4.96	6.63	ns
		XQ6SLX150T	4.62	N/A	4.96	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Spartan-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 70 through Table 77. Values are expressed in nanoseconds unless otherwise noted.

Table 70: Global Clock Setup and Hold Without DCM or PLL (No Delay)

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.(1)							
T _{PSND} / T _{PHND}	No Delay Global Clock and IFF(3) without DCM or PLL	XC6SLX4	0.10/1.56	N/A	0.10/1.83	0.07/2.54	ns
		XC6SLX9	0.10/1.56	0.10/1.57	0.10/1.84	0.07/2.54	ns
		XC6SLX16	0.12/1.42	0.12/1.48	0.12/1.64	0.13/2.19	ns
		XC6SLX25	0.18/1.64	0.18/1.75	0.18/1.99	0.11/2.57	ns
		XC6SLX25T	0.18/1.64	0.18/1.75	0.18/1.99	N/A	ns
		XC6SLX45	−0.08/1.80	−0.08/1.95	−0.08/2.27	−0.17/2.74	ns
		XC6SLX45T	−0.08/1.80	−0.08/1.95	−0.08/2.27	N/A	ns
		XC6SLX75	0.13/1.81	0.13/2.06	0.13/2.27	−0.12/3.30	ns
		XC6SLX75T	0.13/1.81	0.13/2.06	0.13/2.27	N/A	ns
		XC6SLX100	−0.14/2.03	−0.14/2.24	−0.14/2.56	−0.17/3.44	ns
		XC6SLX100T	−0.14/2.03	−0.14/2.24	−0.14/2.56	N/A	ns
		XC6SLX150	−0.24/2.42	−0.24/2.74	−0.24/2.95	−0.60/3.75	ns
		XC6SLX150T	−0.24/2.42	−0.24/2.74	−0.24/2.95	N/A	ns
		XA6SLX4	0.10/1.57	N/A	0.10/1.84	N/A	ns
		XA6SLX9	0.10/1.57	N/A	0.10/1.84	N/A	ns
		XA6SLX16	0.12/1.43	N/A	0.12/1.64	N/A	ns
		XA6SLX25	0.18/1.65	N/A	0.18/1.99	N/A	ns
		XA6SLX25T	0.18/1.65	N/A	0.18/1.99	N/A	ns
		XA6SLX45	−0.08/1.82	N/A	−0.08/2.27	N/A	ns
		XA6SLX45T	−0.08/1.82	N/A	−0.08/2.27	N/A	ns
		XA6SLX75	0.13/2.02	N/A	0.13/2.32	N/A	ns
		XA6SLX75T	0.13/2.02	N/A	0.13/2.32	N/A	ns
		XA6SLX100	N/A	N/A	0.10/2.51	N/A	ns
		XQ6SLX75	N/A	N/A	0.13/2.32	−0.12/3.30	ns
		XQ6SLX75T	0.13/2.02	N/A	0.13/2.32	N/A	ns
		XQ6SLX150	N/A	N/A	−0.24/2.95	−0.60/3.75	ns
		XQ6SLX150T	−0.24/2.74	N/A	−0.24/2.95	N/A	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch.

Table 76: Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾							
T _{PSDCMPLL} / T _{PHDCMPLL}	No Delay Global Clock and IFF ⁽²⁾ with DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.	XC6SLX4	1.16/0.49	N/A	1.39/0.49	2.36/0.59	ns
		XC6SLX9	1.16/0.44	1.37/0.44	1.39/0.44	2.36/0.59	ns
		XC6SLX16	1.44/−0.08	1.49/−0.04	1.62/−0.04	2.06/0.55	ns
		XC6SLX25	1.52/0.42	1.65/0.42	1.83/0.42	2.52/0.43	ns
		XC6SLX25T	1.52/0.42	1.65/0.42	1.83/0.42	N/A	ns
		XC6SLX45	1.54/0.39	1.59/0.39	1.75/0.39	2.48/0.76	ns
		XC6SLX45T	1.54/0.39	1.59/0.39	1.75/0.39	N/A	ns
		XC6SLX75	1.72/0.41	1.80/0.41	1.99/0.41	2.60/0.75	ns
		XC6SLX75T	1.72/0.41	1.80/0.41	1.99/0.41	N/A	ns
		XC6SLX100	1.34/0.51	1.46/0.51	1.64/0.51	2.12/0.90	ns
		XC6SLX100T	1.34/0.51	1.46/0.51	1.64/0.51	N/A	ns
		XC6SLX150	1.30/0.60	1.40/0.60	1.55/0.60	2.57/0.97	ns
		XC6SLX150T	1.30/0.60	1.40/0.60	1.55/0.60	N/A	ns
		XA6SLX4	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX9	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX16	2.67/0.35	N/A	2.67/0.17	N/A	ns
		XA6SLX25	1.74/0.27	N/A	1.95/0.27	N/A	ns
		XA6SLX25T	1.74/0.27	N/A	2.03/0.27	N/A	ns
		XA6SLX45	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX45T	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX75	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX100	N/A	N/A	2.64/0.82	N/A	ns
		XQ6SLX75	N/A	N/A	2.11/0.24	2.60/0.75	ns
		XQ6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XQ6SLX150	N/A	N/A	1.67/0.70	2.57/0.97	ns
		XQ6SLX150T	1.50/0.70	N/A	1.67/0.70	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 78: Duty Cycle Distortion and Clock-Tree Skew (Cont'd)

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{BUFIOSKEW}	I/O clock tree skew across one clock region	LX4	0.06	N/A	0.06	0.07	ns
		LX9	0.06	0.06	0.06	0.07	ns
		LX16	0.06	0.06	0.06	0.07	ns
		LX25	0.06	0.06	0.06	0.07	ns
		LX25T	0.06	0.06	0.06	N/A	ns
		LX45	0.06	0.06	0.06	0.07	ns
		LX45T	0.06	0.06	0.06	N/A	ns
		LX75	0.06	0.06	0.06	0.07	ns
		LX75T	0.06	0.06	0.06	N/A	ns
		LX100	0.06	0.06	0.06	0.07	ns
		LX100T	0.06	0.06	0.06	N/A	ns
		LX150	0.06	0.06	0.06	0.07	ns
		LX150T	0.06	0.06	0.06	N/A	ns

Notes:

1. LXT devices are not available with a -1L speed grade. The LX4 is not available in -3N speed grade.
2. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
3. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
4. The T_{CKSKEW} is 0.43 ns for the XA6SLX100 device using a -2 speed grade and 0.22 ns for the XC6SLX100 devices using the -2 speed grade.

Table 79: Package Skew

Symbol	Description	Device	Package ⁽²⁾	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	LX4	TQG144	N/A	ps
			CPG196	23	ps
			CSG225	58	ps
		LX9	TQG144	N/A	ps
			CPG196	23	ps
			CSG225	58	ps
			FT(G)256	88	ps
			CSG324	64	ps
		LX16	CPG196	19	ps
			CSG225	70	ps
			FT(G)256	71	ps
			CSG324	54	ps
		LX25	FT(G)256	90	ps
			CSG324	61	ps
			FG(G)484	84	ps
		LX25T	CSG324	48	ps
			FG(G)484	112	ps

Date	Version	Description of Revisions
01/10/11	1.11	Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.4 software with speed specification v1.15 for the -4, -3, -3N, and -2 speed grades. Added note 3 to Table 27. Also updated the -1L speed grade requirements to ISE v12.4 software with speed specification v1.06. Revised -3N definition throughout the document. Added note 4 to Table 2 and updated note 5. Added information on V_{CCINT} to note 1 in Table 5. Updated Networking Applications -3 values in Table 25 to match improvements made in ISE v12.4. In Table 28, added note 1 and revised the T_{IOTP} values for LVDS_33, LVDS_25, MINI_LVDS_33, MINI_LVDS_25, RSDS_33, RSDS_25, TMDS_33, PPDS_33, and PPDS_25. Added note 3 to Table 55.
02/11/11	1.12	As described in XCEN11008: Product Discontinuation Notice For Spartan-6 LXT -4 Devices, the -4 speed specifications have been discontinued. As outlined in page 2 of the XCN, designers currently using -4 speed specifications should rerun timing analysis using the new -3 speed specifications before moving to a replacement device. Updated the networking applications section of Table 25. Updated -2 speed specifications throughout document and added note 3 to Table 27 advising designers to use the -2 speed specification update (v1.17) with the ISE 12.4 software patch. Added F_{CLKDIV} to Table 37 and Table 38. Updated note 2 in Table 39. Updated units for $T_{SMCKCSO}$ and T_{BPICCO} in Table 47. Updated -1L in Table 71. Removed Note 2: <i>Package delay information is available for these device/package combinations. This information can be used to deskew the package</i> from Table 79.
03/31/11	2.0	Production release of XC6SLX45 in the -1L speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. In Table 39, removed values in the -1L column and added note 3 as IODELAY2 only supports Tap0 for lower-power devices. Updated copyright page 1 and Notice of Disclaimer.
05/20/11	2.1	Production release of XC6SLX100 and XC6SLX150 in the specific speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. Updated Table 27 and Note 7 with changes per XCEN11012: Speed File Change for -3N Devices. Revised Switching Characteristics section for speed specifications: v1.18 for -3, -3N, and -2; including improvements in Table 73 through Table 77 and Table 81. Removed <i>Memory Controller Block</i> from the performance heading in Table 2 and revised Note 2. In Table 4, added Note 1 to C_{IN} and updated the description of R_{IN_TERM}. Updated Note 1 in Table 5. Updated Note 1 of Table 7. In Table 25, added and removed -1L specifications, increased the standard performance DDR3 specifications, removed the extended performance DDR3 row and updated Note 3 and Note 4. Clarified the introductory information for Table 28 and Table 30. In Table 32: Revised V_{MEAS} value for LVCMOS12; revised V_{REF} for LVDS_25, LVDS_33, BLVDS_25, MINI_LVDS_25, MINI_LVDS_33, RSDS_25, and RSDS_33; revised R_{REF} for BLVDS_25 and TMDS_33; and added Note 4 and Note 5. Updated Note 2 and Note 3 in Table 39. In Table 47, revised the values and description of T_{POR} including adding Note 3. Also in Table 47, augmented the description and added specifications for F_{RBCK} and removed XC6SLX4 from F_{MCCK} (maximum frequency, parallel mode (Master SelectMAP/BPI)). Added BUFGMUX to Table 48 title. Added Table 50. In Table 52, revised specifications for $T_{EXTFVAR}$ and $F_{INJITTER}$. In Table 54 removed the 5 MHz < CLKIN_FREQ_DLL parameter in the LOCK_DLL description. In both Table 56 and Table 57, removed the 5 MHz < F_{CLKIN} parameter in the LOCK_FX description. In Table 58, updated description for PSCLK_FREQ and PSCLK_PULSE. Revised title and symbol of Table 70, added new speed specifications for -1L, and added Note 2. Added Table 71.
07/11/11	2.2	Added the Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices to all appropriate tables while sometimes removing the XC6S nomenclature. Added expanded temperature range (Q) to all appropriate tables. Updated T_{SOL} packages in Table 1. Added R_{OUT_TERM} to Table 4. Updated Note 2 on Table 13. Production release of the XC6SLX4, XC6SLX9, XC6SLX16, XC6SLX25, XC6SLX75, XQ6SLX75, and XQ6SLX150 in Table 26 and Table 27 using ISE v13.2 software with -1L speed specification v1.07. Production release of the XA6SLX16, XA6SLX25T, XA6SLX45, XA6SLX45T, XQ6SLX75, XQ6SLX75T, XQ6SLX150, and XQ6SLX150T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices(1). Updated CS(G)484 from CSG484 throughout data sheet. Clarified Note 3 in Table 39.
08/08/11	2.3	Production release of the XA6SLX25, XA6SLX75, and XA6SLX75T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19.

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