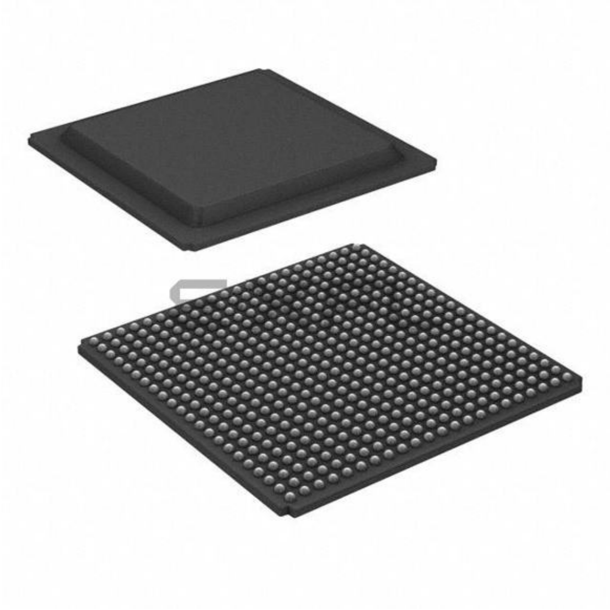
# AMD Xilinx - XC6SLX100-2FGG484C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 7911 |
| Number of Logic Elements/Cells | 101261 |
| Total RAM Bits | 4939776 |
| Number of I/O | 326 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc6slx100-2fgg484c |

*Table 3:* **eFUSE Programming Conditions**[1]

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{FS}$[2] | External voltage supply | 3.2 | 3.3 | 3.4 | V |
| $I_{FS}$ | $V_{FS}$ supply current | – | – | 40 | mA |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND | 3.2 | 3.3 | 3.45 | V |
| $R_{FUSE}$[3] | External resistor from $R_{FUSE}$ pin to GND | 1129 | 1140 | 1151 | Ω |
| $V_{CCINT}$ | Internal supply voltage relative to GND | 1.14 | 1.2 | 1.26 | V |
| $t_j$ | Temperature range | 15 | – | 85 | °C |

**Notes:**

1. These specifications apply during programming of the eFUSE AES key. Programming is only supported through JTAG.The AES key is only supported in the following devices: LX75, LX75T, LX100, LX100T, LX150, and LX150T.
2. When programming eFUSE, $V_{FS}$ must be less than or equal to $V_{CCAUX}$. When not programming or when eFUSE is not used, Xilinx recommends connecting $V_{FS}$ to GND. However, $V_{FS}$ can be between GND and 3.45 V.
3. An $R_{FUSE}$ resistor is required when programming the eFUSE AES key. When not programming or when eFUSE is not used, Xilinx recommends connecting the $R_{FUSE}$ pin to $V_{CCAUX}$ or GND. However, $R_{FUSE}$ can be unconnected.

## Quiescent Current

Typical values for quiescent supply current are specified at nominal voltage, 25°C junction temperatures ($T_j$). Quiescent supply current is specified by speed grade for Spartan-6 devices. Xilinx recommends analyzing static power consumption using the XPOWER™ Estimator (XPE) tool (download at http://www.xilinx.com/power) for conditions other than those specified in Table 5.

*Table 5:* **Typical Quiescent Supply Current**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current | LX4 | 4.0 | 4.0 | 4.0 | 2.4 | mA |
| | | LX9 | 4.0 | 4.0 | 4.0 | 2.4 | mA |
| | | LX16 | 6.0 | 6.0 | 6.0 | 4.0 | mA |
| | | LX25 | 11.0 | 11.0 | 11.0 | 6.6 | mA |
| | | LX25T | 11.0 | 11.0 | 11.0 | N/A | mA |
| | | LX45 | 15.0 | 15.0 | 15.0 | 9.0 | mA |
| | | LX45T | 15.0 | 15.0 | 15.0 | N/A | mA |
| | | LX75 | 29.0 | 29.0 | 29.0 | 17.4 | mA |
| | | LX75T | 29.0 | 29.0 | 29.0 | N/A | mA |
| | | LX100 | 36.0 | 36.0 | 36.0 | 21.6 | mA |
| | | LX100T | 36.0 | 36.0 | 36.0 | N/A | mA |
| | | LX150 | 51.0 | 51.0 | 51.0 | 31.0 | mA |
| | | LX150T | 51.0 | 51.0 | 51.0 | N/A | mA |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current | LX4 | 1.0 | 1.0 | 1.0 | 1.0 | mA |
| | | LX9 | 1.0 | 1.0 | 1.0 | 1.0 | mA |
| | | LX16 | 2.0 | 2.0 | 2.0 | 2.0 | mA |
| | | LX25 | 2.0 | 2.0 | 2.0 | 2.0 | mA |
| | | LX25T | 2.0 | 2.0 | 2.0 | N/A | mA |
| | | LX45 | 3.0 | 3.0 | 3.0 | 3.0 | mA |
| | | LX45T | 3.0 | 3.0 | 3.0 | N/A | mA |
| | | LX75 | 4.0 | 4.0 | 4.0 | 4.0 | mA |
| | | LX75T | 4.0 | 4.0 | 4.0 | N/A | mA |
| | | LX100 | 5.0 | 5.0 | 5.0 | 5.0 | mA |
| | | LX100T | 5.0 | 5.0 | 5.0 | N/A | mA |
| | | LX150 | 7.0 | 7.0 | 7.0 | 7.0 | mA |
| | | LX150T | 7.0 | 7.0 | 7.0 | N/A | mA |

## SelectIO™ Interface DC Input and Output Levels

*Table 7:* **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

| I/O Standard | $V_{CCO}$ for Drivers(1) | | | $V_{REF}$ for Inputs | | |
|---|---|---|---|---|---|---|
| | V, Min | V, Nom | V, Max | V, Min | V, Nom | V, Max |
| LVTTL | 3.0 | 3.3 | 3.45 | $V_{REF}$ is not used for these I/O standards | | |
| LVCMOS33 | 3.0 | 3.3 | 3.45 | | | |
| LVCMOS25 | 2.3 | 2.5 | 2.7 | | | |
| LVCMOS18 | 1.65 | 1.8 | 1.95 | | | |
| LVCMOS18_JEDEC | 1.65 | 1.8 | 1.95 | | | |
| LVCMOS15 | 1.4 | 1.5 | 1.6 | | | |
| LVCMOS15_JEDEC | 1.4 | 1.5 | 1.6 | | | |
| LVCMOS12 | 1.1 | 1.2 | 1.3 | | | |
| LVCMOS12_JEDEC | 1.1 | 1.2 | 1.3 | | | |
| PCI33_3(2) | 3.0 | 3.3 | 3.45 | | | |
| PCI66_3(2) | 3.0 | 3.3 | 3.45 | | | |
| I2C | 2.7 | 3.0 | 3.45 | | | |
| SMBUS | 2.7 | 3.0 | 3.45 | | | |
| SDIO | 3.0 | 3.3 | 3.45 | | | |
| MOBILE_DDR | 1.7 | 1.8 | 1.9 | | | |
| HSTL_I | 1.4 | 1.5 | 1.6 | 0.68 | 0.75 | 0.9 |
| HSTL_II | 1.4 | 1.5 | 1.6 | 0.68 | 0.75 | 0.9 |
| HSTL_III | 1.4 | 1.5 | 1.6 | – | 0.9 | – |
| HSTL_I_18 | 1.7 | 1.8 | 1.9 | 0.8 | 0.9 | 1.1 |
| HSTL_II_18 | 1.7 | 1.8 | 1.9 | – | 0.9 | – |
| HSTL_III_18 | 1.7 | 1.8 | 1.9 | – | 1.1 | – |
| SSTL3_I | 3.0 | 3.3 | 3.45 | 1.3 | 1.5 | 1.7 |
| SSTL3_II | 3.0 | 3.3 | 3.45 | 1.3 | 1.5 | 1.7 |
| SSTL2_I | 2.3 | 2.5 | 2.7 | 1.13 | 1.25 | 1.38 |
| SSTL2_II | 2.3 | 2.5 | 2.7 | 1.13 | 1.25 | 1.38 |
| SSTL18_I | 1.7 | 1.8 | 1.9 | 0.833 | 0.9 | 0.969 |
| SSTL18_II | 1.7 | 1.8 | 1.9 | 0.833 | 0.9 | 0.969 |
| SSTL15_II | 1.425 | 1.5 | 1.575 | 0.69 | 0.75 | 0.81 |

**Notes:**

1. $V_{CCO}$ range required when using I/O standard for an output. Also required for MOBILE_DDR, PCI33_3, LVCMOS18_JEDEC, LVCMOS15_JEDEC, and LVCMOS12_JEDEC inputs, and for LVCMOS25 inputs when $V_{CCAUX} = 3.3V$.
2. For PCI systems, the transmitter and receiver should have common supplies for $V_{CCO}$.

### *Table 14:* GTP Transceiver Current Supply (per Lane)

| Symbol | Description | Typ[(1)] | Max | Units |
|---|---|---|---|---|
| $I_{MGTAVCC}$ | GTP transceiver internal analog supply current | 40.4 | Note 2 | mA |
| $I_{MGTAVTTTX}$ | GTP transmitter termination supply current | 27.4 | | mA |
| $I_{MGTAVTTRX}$ | GTP receiver termination supply current | 13.6 | | mA |
| $I_{MGTAVCCPLL}$ | GTP transmitter and receiver PLL supply current | 28.7 | | mA |
| $R_{MGTRREF}$ | Precision reference resistor for internal calibration termination | 50.0 ± 1% tolerance | | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C, with a 2.5 Gb/s line rate, with a shared PLL use mode.
2. Values for currents of other transceiver configurations and conditions can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

### *Table 15:* GTP Transceiver Quiescent Supply Current (per Lane)(1)(2)(3)(4)

| Symbol | Description | Typ[(5)] | Max | Units |
|---|---|---|---|---|
| $I_{MGTAVCCQ}$ | Quiescent MGTAVCC supply current | 1.7 | Note 2 | mA |
| $I_{MGTAVTTTXQ}$ | Quiescent MGTAVTTTX supply current | 0.1 | | mA |
| $I_{MGTAVTTRXQ}$ | Quiescent MGTAVTTRX supply current | 1.2 | | mA |
| $I_{MGTAVCCPLLQ}$ | Quiescent MGTAVCCPLL supply current | 1.0 | | mA |

**Notes:**

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
3. GTP transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTP transceivers.
4. Does not include power-up MGTAVTTRCAL supply current during device configuration.
5. Typical values are specified at nominal voltage, 25°C.

*Table 23:* **GTP Transceiver Receiver Switching Characteristics**

| Symbol | Description | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $T_{RXELECIDLE}$ | Time for RXELECIDLE to respond to loss or restoration of data | | | – | 75 | – | ns |
| $R_{XOOBVDPP}$ | OOB detect threshold peak-to-peak | | | 60 | – | 150 | mV |
| $R_{XSST}$ | Receiver spread-spectrum tracking(1) | | Modulated @ 33 KHz | –5000 | – | 0 | ppm |
| $R_{XRL}$ | Run length (CID) | Internal AC capacitor bypassed | | – | – | 150 | UI |
| $R_{XPPMTOL}$ | Data/REFCLK PPM offset tolerance | CDR 2nd-order loop disabled | | –200 | – | 200 | ppm |
| | | CDR 2nd-order loop enabled | PLL_RXDIVSEL_OUT = 1 | –2000 | – | 2000 | ppm |
| | | | PLL_RXDIVSEL_OUT = 2 | –2000 | – | 2000 | ppm |
| | | | PLL_RXDIVSEL_OUT = 4 | –1000 | – | 1000 | ppm |
| **SJ Jitter Tolerance(2)** | | | | | | | |
| $JT\_SJ_{3.125}$ | Sinusoidal Jitter(3) | | 3.125 Gb/s | 0.4 | – | – | UI |
| $JT\_SJ_{2.5}$ | Sinusoidal Jitter(3) | | 2.5 Gb/s | 0.4 | – | – | UI |
| $JT\_SJ_{1.62}$ | Sinusoidal Jitter(3) | | 1.62 Gb/s | 0.5 | – | – | UI |
| $JT\_SJ_{1.25}$ | Sinusoidal Jitter(3) | | 1.25 Gb/s | 0.5 | – | – | UI |
| $JT\_SJ_{614}$ | Sinusoidal Jitter(3) | | 614 Mb/s | 0.5 | – | – | UI |
| **SJ Jitter Tolerance with Stressed Eye(2)(5)** | | | | | | | |
| $JT\_TJSE_{3.125}$ | Total Jitter with stressed eye(4) | | 3.125 Gb/s | 0.65 | – | – | UI |
| $JT\_SJSE_{3.125}$ | Sinusoidal Jitter with stressed eye | | 3.125 Gb/s | 0.1 | – | – | UI |
| $JT\_TJSE_{2.7}$ | Total Jitter with stressed eye(4) | | 2.7 Gb/s | 0.65 | – | – | UI |
| $JT\_SJSE_{2.7}$ | Sinusoidal Jitter with stressed eye | | 2.7 Gb/s | 0.1 | – | – | UI |

**Notes:**

1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a Bit Error Ratio of $1e^{-12}$.
3. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
4. Composed of 0.37 UI DJ in the form of ISI and 0.18 UI RJ.
5. Measured using PRBS7 data pattern.

## Endpoint Block for PCI Express Designs Switching Characteristics

The Endpoint block for PCI Express is available in the Spartan-6 LXT devices. Consult the Spartan-6 FPGA Integrated Endpoint Block for PCI Express for further information.

*Table 24:* **Maximum Performance for PCI Express Designs**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| $F_{PCIEUSER}$ | User clock maximum frequency | 62.5 | 62.5 | 62.5 | N/A | MHz |

*Table 28:* **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -3N | -2 | -1L(1) | -3 | -3N | -2 | -1L(1) | -3 | -3N | -2 | -1L(1) | |
| LVTTL, QUIETIO, 2 mA | 1.35 | 1.47 | 1.60 | 1.82 | 5.39 | 5.53 | 5.73 | 6.37 | 5.39 | 5.53 | 5.73 | 6.37 | ns |
| LVTTL, QUIETIO, 4 mA | 1.35 | 1.47 | 1.60 | 1.82 | 4.29 | 4.43 | 4.63 | 5.22 | 4.29 | 4.43 | 4.63 | 5.22 | ns |
| LVTTL, QUIETIO, 6 mA | 1.35 | 1.47 | 1.60 | 1.82 | 3.75 | 3.89 | 4.09 | 4.69 | 3.75 | 3.89 | 4.09 | 4.69 | ns |
| LVTTL, QUIETIO, 8 mA | 1.35 | 1.47 | 1.60 | 1.82 | 3.23 | 3.37 | 3.57 | 4.20 | 3.23 | 3.37 | 3.57 | 4.20 | ns |
| LVTTL, QUIETIO, 12 mA | 1.35 | 1.47 | 1.60 | 1.82 | 3.28 | 3.42 | 3.62 | 4.22 | 3.28 | 3.42 | 3.62 | 4.22 | ns |
| LVTTL, QUIETIO, 16 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.94 | 3.08 | 3.28 | 3.92 | 2.94 | 3.08 | 3.28 | 3.92 | ns |
| LVTTL, QUIETIO, 24 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.69 | 2.83 | 3.03 | 3.67 | 2.69 | 2.83 | 3.03 | 3.67 | ns |
| LVTTL, Slow, 2 mA | 1.35 | 1.47 | 1.60 | 1.82 | 4.36 | 4.50 | 4.70 | 5.30 | 4.36 | 4.50 | 4.70 | 5.30 | ns |
| LVTTL, Slow, 4 mA | 1.35 | 1.47 | 1.60 | 1.82 | 3.17 | 3.31 | 3.51 | 4.16 | 3.17 | 3.31 | 3.51 | 4.16 | ns |
| LVTTL, Slow, 6 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.76 | 2.90 | 3.10 | 3.75 | 2.76 | 2.90 | 3.10 | 3.75 | ns |
| LVTTL, Slow, 8 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.59 | 2.73 | 2.93 | 3.55 | 2.59 | 2.73 | 2.93 | 3.55 | ns |
| LVTTL, Slow, 12 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.58 | 2.72 | 2.92 | 3.54 | 2.58 | 2.72 | 2.92 | 3.54 | ns |
| LVTTL, Slow, 16 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.39 | 2.53 | 2.73 | 3.40 | 2.39 | 2.53 | 2.73 | 3.40 | ns |
| LVTTL, Slow, 24 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.28 | 2.42 | 2.62 | 3.24 | 2.28 | 2.42 | 2.62 | 3.24 | ns |
| LVTTL, Fast, 2 mA | 1.35 | 1.47 | 1.60 | 1.82 | 3.78 | 3.92 | 4.12 | 4.74 | 3.78 | 3.92 | 4.12 | 4.74 | ns |
| LVTTL, Fast, 4 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.49 | 2.63 | 2.83 | 3.45 | 2.49 | 2.63 | 2.83 | 3.45 | ns |
| LVTTL, Fast, 6 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.44 | 2.58 | 2.78 | 3.40 | 2.44 | 2.58 | 2.78 | 3.40 | ns |
| LVTTL, Fast, 8 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.32 | 2.46 | 2.66 | 3.28 | 2.32 | 2.46 | 2.66 | 3.28 | ns |
| LVTTL, Fast, 12 mA | 1.35 | 1.47 | 1.60 | 1.82 | 1.83 | 1.97 | 2.17 | 2.79 | 1.83 | 1.97 | 2.17 | 2.79 | ns |
| LVTTL, Fast, 16 mA | 1.35 | 1.47 | 1.60 | 1.82 | 1.83 | 1.97 | 2.17 | 2.79 | 1.83 | 1.97 | 2.17 | 2.79 | ns |
| LVTTL, Fast, 24 mA | 1.35 | 1.47 | 1.60 | 1.82 | 1.83 | 1.97 | 2.17 | 2.79 | 1.83 | 1.97 | 2.17 | 2.79 | ns |
| LVCMOS33, QUIETIO, 2 mA | 1.34 | 1.46 | 1.59 | 1.82 | 5.40 | 5.54 | 5.74 | 6.37 | 5.40 | 5.54 | 5.74 | 6.37 | ns |
| LVCMOS33, QUIETIO, 4 mA | 1.34 | 1.46 | 1.59 | 1.82 | 4.03 | 4.17 | 4.37 | 5.01 | 4.03 | 4.17 | 4.37 | 5.01 | ns |
| LVCMOS33, QUIETIO, 6 mA | 1.34 | 1.46 | 1.59 | 1.82 | 3.51 | 3.65 | 3.85 | 4.47 | 3.51 | 3.65 | 3.85 | 4.47 | ns |
| LVCMOS33, QUIETIO, 8 mA | 1.34 | 1.46 | 1.59 | 1.82 | 3.37 | 3.51 | 3.71 | 4.33 | 3.37 | 3.51 | 3.71 | 4.33 | ns |
| LVCMOS33, QUIETIO, 12 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.94 | 3.08 | 3.28 | 3.93 | 2.94 | 3.08 | 3.28 | 3.93 | ns |
| LVCMOS33, QUIETIO, 16 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.77 | 2.91 | 3.11 | 3.78 | 2.77 | 2.91 | 3.11 | 3.78 | ns |
| LVCMOS33, QUIETIO, 24 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.59 | 2.73 | 2.93 | 3.58 | 2.59 | 2.73 | 2.93 | 3.58 | ns |
| LVCMOS33, Slow, 2 mA | 1.34 | 1.46 | 1.59 | 1.82 | 4.37 | 4.51 | 4.71 | 5.28 | 4.37 | 4.51 | 4.71 | 5.28 | ns |
| LVCMOS33, Slow, 4 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.98 | 3.12 | 3.32 | 3.94 | 2.98 | 3.12 | 3.32 | 3.94 | ns |
| LVCMOS33, Slow, 6 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.58 | 2.72 | 2.92 | 3.61 | 2.58 | 2.72 | 2.92 | 3.61 | ns |
| LVCMOS33, Slow, 8 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.65 | 2.79 | 2.99 | 3.61 | 2.65 | 2.79 | 2.99 | 3.61 | ns |
| LVCMOS33, Slow, 12 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.39 | 2.53 | 2.73 | 3.31 | 2.39 | 2.53 | 2.73 | 3.31 | ns |
| LVCMOS33, Slow, 16 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.31 | 2.45 | 2.65 | 3.27 | 2.31 | 2.45 | 2.65 | 3.27 | ns |
| LVCMOS33, Slow, 24 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.28 | 2.42 | 2.62 | 3.24 | 2.28 | 2.42 | 2.62 | 3.24 | ns |
| LVCMOS33, Fast, 2 mA | 1.34 | 1.46 | 1.59 | 1.82 | 3.76 | 3.90 | 4.10 | 4.70 | 3.76 | 3.90 | 4.10 | 4.70 | ns |
| LVCMOS33, Fast, 4 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.48 | 2.62 | 2.82 | 3.44 | 2.48 | 2.62 | 2.82 | 3.44 | ns |
| LVCMOS33, Fast, 6 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.32 | 2.46 | 2.66 | 3.28 | 2.32 | 2.46 | 2.66 | 3.28 | ns |

*Table 28:* **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -3N | -2 | -1L(1) | -3 | -3N | -2 | -1L(1) | -3 | -3N | -2 | -1L(1) | |
| LVCMOS15, Slow, 8 mA | 0.98 | 1.10 | 1.23 | 1.79 | 2.30 | 2.44 | 2.64 | 3.25 | 2.30 | 2.44 | 2.64 | 3.25 | ns |
| LVCMOS15, Slow, 12 mA | 0.98 | 1.10 | 1.23 | 1.79 | 2.03 | 2.17 | 2.37 | 2.99 | 2.03 | 2.17 | 2.37 | 2.99 | ns |
| LVCMOS15, Slow, 16 mA | 0.98 | 1.10 | 1.23 | 1.79 | 2.01 | 2.15 | 2.35 | 2.97 | 2.01 | 2.15 | 2.35 | 2.97 | ns |
| LVCMOS15, Fast, 2 mA | 0.98 | 1.10 | 1.23 | 1.79 | 3.29 | 3.43 | 3.63 | 4.24 | 3.29 | 3.43 | 3.63 | 4.24 | ns |
| LVCMOS15, Fast, 4 mA | 0.98 | 1.10 | 1.23 | 1.79 | 2.27 | 2.41 | 2.61 | 3.22 | 2.27 | 2.41 | 2.61 | 3.22 | ns |
| LVCMOS15, Fast, 6 mA | 0.98 | 1.10 | 1.23 | 1.79 | 1.78 | 1.92 | 2.12 | 2.74 | 1.78 | 1.92 | 2.12 | 2.74 | ns |
| LVCMOS15, Fast, 8 mA | 0.98 | 1.10 | 1.23 | 1.79 | 1.73 | 1.87 | 2.07 | 2.69 | 1.73 | 1.87 | 2.07 | 2.69 | ns |
| LVCMOS15, Fast, 12 mA | 0.98 | 1.10 | 1.23 | 1.79 | 1.73 | 1.87 | 2.07 | 2.64 | 1.73 | 1.87 | 2.07 | 2.64 | ns |
| LVCMOS15, Fast, 16 mA | 0.98 | 1.10 | 1.23 | 1.79 | 1.73 | 1.87 | 2.07 | 2.64 | 1.73 | 1.87 | 2.07 | 2.64 | ns |
| LVCMOS15_JEDEC, QUIETIO, 2 mA | 1.03 | 1.15 | 1.28 | 1.49 | 5.49 | 5.63 | 5.83 | 6.37 | 5.49 | 5.63 | 5.83 | 6.37 | ns |
| LVCMOS15_JEDEC, QUIETIO, 4 mA | 1.03 | 1.15 | 1.28 | 1.49 | 4.61 | 4.75 | 4.95 | 5.51 | 4.61 | 4.75 | 4.95 | 5.51 | ns |
| LVCMOS15_JEDEC, QUIETIO, 6 mA | 1.03 | 1.15 | 1.28 | 1.49 | 4.07 | 4.21 | 4.41 | 4.97 | 4.07 | 4.21 | 4.41 | 4.97 | ns |
| LVCMOS15_JEDEC, QUIETIO, 8 mA | 1.03 | 1.15 | 1.28 | 1.49 | 3.92 | 4.06 | 4.26 | 4.81 | 3.92 | 4.06 | 4.26 | 4.81 | ns |
| LVCMOS15_JEDEC, QUIETIO, 12 mA | 1.03 | 1.15 | 1.28 | 1.49 | 3.54 | 3.68 | 3.88 | 4.51 | 3.54 | 3.68 | 3.88 | 4.51 | ns |
| LVCMOS15_JEDEC, QUIETIO, 16 mA | 1.03 | 1.15 | 1.28 | 1.49 | 3.33 | 3.47 | 3.67 | 4.31 | 3.33 | 3.47 | 3.67 | 4.31 | ns |
| LVCMOS15_JEDEC, Slow, 2 mA | 1.03 | 1.15 | 1.28 | 1.49 | 4.18 | 4.32 | 4.52 | 5.13 | 4.18 | 4.32 | 4.52 | 5.13 | ns |
| LVCMOS15_JEDEC, Slow, 4 mA | 1.03 | 1.15 | 1.28 | 1.49 | 3.42 | 3.56 | 3.76 | 4.35 | 3.42 | 3.56 | 3.76 | 4.35 | ns |
| LVCMOS15_JEDEC, Slow, 6 mA | 1.03 | 1.15 | 1.28 | 1.49 | 2.29 | 2.43 | 2.63 | 3.25 | 2.29 | 2.43 | 2.63 | 3.25 | ns |
| LVCMOS15_JEDEC, Slow, 8 mA | 1.03 | 1.15 | 1.28 | 1.49 | 2.30 | 2.44 | 2.64 | 3.26 | 2.30 | 2.44 | 2.64 | 3.26 | ns |
| LVCMOS15_JEDEC, Slow, 12 mA | 1.03 | 1.15 | 1.28 | 1.49 | 2.01 | 2.15 | 2.35 | 2.97 | 2.01 | 2.15 | 2.35 | 2.97 | ns |
| LVCMOS15_JEDEC, Slow, 16 mA | 1.03 | 1.15 | 1.28 | 1.49 | 2.01 | 2.15 | 2.35 | 2.97 | 2.01 | 2.15 | 2.35 | 2.97 | ns |
| LVCMOS15_JEDEC, Fast, 2 mA | 1.03 | 1.15 | 1.28 | 1.49 | 3.28 | 3.42 | 3.62 | 4.22 | 3.28 | 3.42 | 3.62 | 4.22 | ns |
| LVCMOS15_JEDEC, Fast, 4 mA | 1.03 | 1.15 | 1.28 | 1.49 | 2.27 | 2.41 | 2.61 | 3.23 | 2.27 | 2.41 | 2.61 | 3.23 | ns |
| LVCMOS15_JEDEC, Fast, 6 mA | 1.03 | 1.15 | 1.28 | 1.49 | 1.78 | 1.92 | 2.12 | 2.74 | 1.78 | 1.92 | 2.12 | 2.74 | ns |
| LVCMOS15_JEDEC, Fast, 8 mA | 1.03 | 1.15 | 1.28 | 1.49 | 1.73 | 1.87 | 2.07 | 2.69 | 1.73 | 1.87 | 2.07 | 2.69 | ns |
| LVCMOS15_JEDEC, Fast, 12 mA | 1.03 | 1.15 | 1.28 | 1.49 | 1.73 | 1.87 | 2.07 | 2.63 | 1.73 | 1.87 | 2.07 | 2.63 | ns |
| LVCMOS15_JEDEC, Fast, 16 mA | 1.03 | 1.15 | 1.28 | 1.49 | 1.73 | 1.87 | 2.07 | 2.63 | 1.73 | 1.87 | 2.07 | 2.63 | ns |
| LVCMOS12, QUIETIO, 2 mA | 0.91 | 1.03 | 1.16 | 1.51 | 6.40 | 6.54 | 6.74 | 7.30 | 6.40 | 6.54 | 6.74 | 7.30 | ns |
| LVCMOS12, QUIETIO, 4 mA | 0.91 | 1.03 | 1.16 | 1.51 | 4.98 | 5.12 | 5.32 | 5.90 | 4.98 | 5.12 | 5.32 | 5.90 | ns |
| LVCMOS12, QUIETIO, 6 mA | 0.91 | 1.03 | 1.16 | 1.51 | 4.65 | 4.79 | 4.99 | 5.55 | 4.65 | 4.79 | 4.99 | 5.55 | ns |
| LVCMOS12, QUIETIO, 8 mA | 0.91 | 1.03 | 1.16 | 1.51 | 4.23 | 4.37 | 4.57 | 5.21 | 4.23 | 4.37 | 4.57 | 5.21 | ns |
| LVCMOS12, QUIETIO, 12 mA | 0.91 | 1.03 | 1.16 | 1.51 | 3.98 | 4.12 | 4.32 | 4.94 | 3.98 | 4.12 | 4.32 | 4.94 | ns |
| LVCMOS12, Slow, 2 mA | 0.91 | 1.03 | 1.16 | 1.51 | 4.98 | 5.12 | 5.32 | 5.91 | 4.98 | 5.12 | 5.32 | 5.91 | ns |
| LVCMOS12, Slow, 4 mA | 0.91 | 1.03 | 1.16 | 1.51 | 2.84 | 2.98 | 3.18 | 3.81 | 2.84 | 2.98 | 3.18 | 3.81 | ns |
| LVCMOS12, Slow, 6 mA | 0.91 | 1.03 | 1.16 | 1.51 | 2.77 | 2.91 | 3.11 | 3.72 | 2.77 | 2.91 | 3.11 | 3.72 | ns |
| LVCMOS12, Slow, 8 mA | 0.91 | 1.03 | 1.16 | 1.51 | 2.34 | 2.48 | 2.68 | 3.31 | 2.34 | 2.48 | 2.68 | 3.31 | ns |
| LVCMOS12, Slow, 12 mA | 0.91 | 1.03 | 1.16 | 1.51 | 2.08 | 2.22 | 2.42 | 3.06 | 2.08 | 2.22 | 2.42 | 3.06 | ns |

*Table 29:* **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices**[(1)] ***(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | $T_{IOOP}$ | | $T_{IOTP}$ | | Units |
|---|---|---|---|---|---|---|---|
| | Speed Grade | | Speed Grade | | Speed Grade | | |
| | -3 | -2 | -3 | -2 | -3 | -2 | |
| LVCMOS18, QUIETIO, 16 mA | 1.25 | 1.43 | 3.34 | 3.54 | 3.34 | 3.54 | ns |
| LVCMOS18, QUIETIO, 24 mA | 1.25 | 1.43 | 3.18 | 3.38 | 3.18 | 3.38 | ns |
| LVCMOS18, Slow, 2 mA | 1.25 | 1.43 | 4.79 | 4.99 | 4.79 | 4.99 | ns |
| LVCMOS18, Slow, 4 mA | 1.25 | 1.43 | 3.84 | 4.04 | 3.84 | 4.04 | ns |
| LVCMOS18, Slow, 6 mA | 1.25 | 1.43 | 3.17 | 3.37 | 3.17 | 3.37 | ns |
| LVCMOS18, Slow, 8 mA | 1.25 | 1.43 | 2.37 | 2.57 | 2.37 | 2.57 | ns |
| LVCMOS18, Slow, 12 mA | 1.25 | 1.43 | 2.13 | 2.33 | 2.13 | 2.33 | ns |
| LVCMOS18, Slow, 16 mA | 1.25 | 1.43 | 2.13 | 2.33 | 2.13 | 2.33 | ns |
| LVCMOS18, Slow, 24 mA | 1.25 | 1.43 | 2.13 | 2.33 | 2.13 | 2.33 | ns |
| LVCMOS18, Fast, 2 mA | 1.25 | 1.43 | 3.78 | 3.98 | 3.78 | 3.98 | ns |
| LVCMOS18, Fast, 4 mA | 1.25 | 1.43 | 2.54 | 2.74 | 2.54 | 2.74 | ns |
| LVCMOS18, Fast, 6 mA | 1.25 | 1.43 | 2.02 | 2.22 | 2.02 | 2.22 | ns |
| LVCMOS18, Fast, 8 mA | 1.25 | 1.43 | 1.95 | 2.15 | 1.95 | 2.15 | ns |
| LVCMOS18, Fast, 12 mA | 1.25 | 1.43 | 1.85 | 2.05 | 1.85 | 2.05 | ns |
| LVCMOS18, Fast, 16 mA | 1.25 | 1.43 | 1.85 | 2.05 | 1.85 | 2.05 | ns |
| LVCMOS18, Fast, 24 mA | 1.25 | 1.43 | 1.85 | 2.05 | 1.85 | 2.05 | ns |
| LVCMOS18_JEDEC, QUIETIO, 2 mA | 1.01 | 1.19 | 6.09 | 6.29 | 6.09 | 6.29 | ns |
| LVCMOS18_JEDEC, QUIETIO, 4 mA | 1.01 | 1.19 | 4.89 | 5.09 | 4.89 | 5.09 | ns |
| LVCMOS18_JEDEC, QUIETIO, 6 mA | 1.01 | 1.19 | 4.20 | 4.40 | 4.20 | 4.40 | ns |
| LVCMOS18_JEDEC, QUIETIO, 8 mA | 1.01 | 1.19 | 3.87 | 4.07 | 3.87 | 4.07 | ns |
| LVCMOS18_JEDEC, QUIETIO, 12 mA | 1.01 | 1.19 | 3.49 | 3.69 | 3.49 | 3.69 | ns |
| LVCMOS18_JEDEC, QUIETIO, 16 mA | 1.01 | 1.19 | 3.34 | 3.54 | 3.34 | 3.54 | ns |
| LVCMOS18_JEDEC, QUIETIO, 24 mA | 1.01 | 1.19 | 3.17 | 3.37 | 3.17 | 3.37 | ns |
| LVCMOS18_JEDEC, Slow, 2 mA | 1.01 | 1.19 | 4.79 | 4.99 | 4.79 | 4.99 | ns |
| LVCMOS18_JEDEC, Slow, 4 mA | 1.01 | 1.19 | 3.84 | 4.04 | 3.84 | 4.04 | ns |
| LVCMOS18_JEDEC, Slow, 6 mA | 1.01 | 1.19 | 3.18 | 3.38 | 3.18 | 3.38 | ns |
| LVCMOS18_JEDEC, Slow, 8 mA | 1.01 | 1.19 | 2.37 | 2.57 | 2.37 | 2.57 | ns |
| LVCMOS18_JEDEC, Slow, 12 mA | 1.01 | 1.19 | 2.13 | 2.33 | 2.13 | 2.33 | ns |
| LVCMOS18_JEDEC, Slow, 16 mA | 1.01 | 1.19 | 2.13 | 2.33 | 2.13 | 2.33 | ns |
| LVCMOS18_JEDEC, Slow, 24 mA | 1.01 | 1.19 | 2.13 | 2.33 | 2.13 | 2.33 | ns |
| LVCMOS18_JEDEC, Fast, 2 mA | 1.01 | 1.19 | 3.75 | 3.95 | 3.75 | 3.95 | ns |
| LVCMOS18_JEDEC, Fast, 4 mA | 1.01 | 1.19 | 2.54 | 2.74 | 2.54 | 2.74 | ns |
| LVCMOS18_JEDEC, Fast, 6 mA | 1.01 | 1.19 | 2.02 | 2.22 | 2.02 | 2.22 | ns |
| LVCMOS18_JEDEC, Fast, 8 mA | 1.01 | 1.19 | 1.94 | 2.14 | 1.94 | 2.14 | ns |
| LVCMOS18_JEDEC, Fast, 12 mA | 1.01 | 1.19 | 1.86 | 2.06 | 1.86 | 2.06 | ns |
| LVCMOS18_JEDEC, Fast, 16 mA | 1.01 | 1.19 | 1.86 | 2.06 | 1.86 | 2.06 | ns |
| LVCMOS18_JEDEC, Fast, 24 mA | 1.01 | 1.19 | 1.86 | 2.06 | 1.86 | 2.06 | ns |

*Table 29:* **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices[1] *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | $T_{IOOP}$ | | $T_{IOTP}$ | | Units |
|---|---|---|---|---|---|---|---|
| | Speed Grade | | Speed Grade | | Speed Grade | | |
| | -3 | -2 | -3 | -2 | -3 | -2 | |
| LVCMOS12, QUIETIO, 6 mA | 0.98 | 1.16 | 4.79 | 4.99 | 4.79 | 4.99 | ns |
| LVCMOS12, QUIETIO, 8 mA | 0.98 | 1.16 | 4.43 | 4.63 | 4.43 | 4.63 | ns |
| LVCMOS12, QUIETIO, 12 mA | 0.98 | 1.16 | 4.18 | 4.38 | 4.18 | 4.38 | ns |
| LVCMOS12, Slow, 2 mA | 0.98 | 1.16 | 5.12 | 5.32 | 5.12 | 5.32 | ns |
| LVCMOS12, Slow, 4 mA | 0.98 | 1.16 | 3.00 | 3.20 | 3.00 | 3.20 | ns |
| LVCMOS12, Slow, 6 mA | 0.98 | 1.16 | 2.91 | 3.11 | 2.91 | 3.11 | ns |
| LVCMOS12, Slow, 8 mA | 0.98 | 1.16 | 2.51 | 2.71 | 2.51 | 2.71 | ns |
| LVCMOS12, Slow, 12 mA | 0.98 | 1.16 | 2.25 | 2.45 | 2.25 | 2.45 | ns |
| LVCMOS12, Fast, 2 mA | 0.98 | 1.16 | 3.60 | 3.80 | 3.60 | 3.80 | ns |
| LVCMOS12, Fast, 4 mA | 0.98 | 1.16 | 2.49 | 2.69 | 2.49 | 2.69 | ns |
| LVCMOS12, Fast, 6 mA | 0.98 | 1.16 | 1.94 | 2.14 | 1.94 | 2.14 | ns |
| LVCMOS12, Fast, 8 mA | 0.98 | 1.16 | 1.82 | 2.02 | 1.82 | 2.02 | ns |
| LVCMOS12, Fast, 12 mA | 0.98 | 1.16 | 1.80 | 2.00 | 1.80 | 2.00 | ns |
| LVCMOS12_JEDEC, QUIETIO, 2 mA | 1.57 | 1.75 | 6.53 | 6.73 | 6.53 | 6.73 | ns |
| LVCMOS12_JEDEC, QUIETIO, 4 mA | 1.57 | 1.75 | 5.12 | 5.32 | 5.12 | 5.32 | ns |
| LVCMOS12_JEDEC, QUIETIO, 6 mA | 1.57 | 1.75 | 4.81 | 5.01 | 4.81 | 5.01 | ns |
| LVCMOS12_JEDEC, QUIETIO, 8 mA | 1.57 | 1.75 | 4.44 | 4.64 | 4.44 | 4.64 | ns |
| LVCMOS12_JEDEC, QUIETIO, 12 mA | 1.57 | 1.75 | 4.20 | 4.40 | 4.20 | 4.40 | ns |
| LVCMOS12_JEDEC, Slow, 2 mA | 1.57 | 1.75 | 5.14 | 5.34 | 5.14 | 5.34 | ns |
| LVCMOS12_JEDEC, Slow, 4 mA | 1.57 | 1.75 | 2.99 | 3.19 | 2.99 | 3.19 | ns |
| LVCMOS12_JEDEC, Slow, 6 mA | 1.57 | 1.75 | 2.90 | 3.10 | 2.90 | 3.10 | ns |
| LVCMOS12_JEDEC, Slow, 8 mA | 1.57 | 1.75 | 2.50 | 2.70 | 2.50 | 2.70 | ns |
| LVCMOS12_JEDEC, Slow, 12 mA | 1.57 | 1.75 | 2.26 | 2.46 | 2.26 | 2.46 | ns |
| LVCMOS12_JEDEC, Fast, 2 mA | 1.57 | 1.75 | 3.60 | 3.80 | 3.60 | 3.80 | ns |
| LVCMOS12_JEDEC, Fast, 4 mA | 1.57 | 1.75 | 2.49 | 2.69 | 2.49 | 2.69 | ns |
| LVCMOS12_JEDEC, Fast, 6 mA | 1.57 | 1.75 | 1.94 | 2.14 | 1.94 | 2.14 | ns |
| LVCMOS12_JEDEC, Fast, 8 mA | 1.57 | 1.75 | 1.83 | 2.03 | 1.83 | 2.03 | ns |
| LVCMOS12_JEDEC, Fast, 12 mA | 1.57 | 1.75 | 1.80 | 2.00 | 1.80 | 2.00 | ns |

**Notes:**

1. The Spartan-6Q FPGA -1L values are listed in Table 28.

Table 30 summarizes the value of $T_{IOTPHZ}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). These delays are measured using LVCMOS25, Fast, 12 mA.

*Table 30:* **IOB 3-state ON Output Switching Characteristics ($T_{IOTPHZ}$)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| $T_{IOTPHZ}$ | T input to Pad high-impedance | 1.39 | 1.59 | 1.59 | 1.91 | ns |

# I/O Standard Measurement Methodology

## Input Delay Measurements

Table 31 shows the test setup parameters used for measuring input delay.

*Table 31:* **Input Delay Measurement Methodology**

| Description | I/O Standard Attribute | $V_L$[1] | $V_H$[1] | $V_{MEAS}$[3][4] | $V_{REF}$[2][4] |
|---|---|---|---|---|---|
| LVTTL (Low-Voltage Transistor-Transistor Logic) | LVTTL | 0 | 3.0 | 1.4 | – |
| LVCMOS (Low-Voltage CMOS), 3.3V | LVCMOS33 | 0 | 3.3 | 1.65 | – |
| LVCMOS, 2.5V | LVCMOS25 | 0 | 2.5 | 1.25 | – |
| LVCMOS, 1.8V | LVCMOS18 | 0 | 1.8 | 0.9 | – |
| LVCMOS, 1.5V | LVCMOS15 | 0 | 1.5 | 0.75 | – |
| LVCMOS, 1.2V | LVCMOS12 | 0 | 1.2 | 0.6 | – |
| PCI (Peripheral Component Interface), 33 MHz and 66 MHz, 3.3V | PCI33_3, PCI66_3 | Per PCI Specification | | | – |
| HSTL (High-Speed Transceiver Logic), Class I & II | HSTL_I, HSTL_II | $V_{REF} – 0.5$ | $V_{REF} + 0.5$ | $V_{REF}$ | 0.75 |
| HSTL, Class III | HSTL_III | $V_{REF} – 0.5$ | $V_{REF} + 0.5$ | $V_{REF}$ | 0.90 |
| HSTL, Class I & II, 1.8V | HSTL_I_18, HSTL_II_18 | $V_{REF} – 0.5$ | $V_{REF} + 0.5$ | $V_{REF}$ | 0.90 |
| HSTL, Class III 1.8V | HSTL_III_18 | $V_{REF} – 0.5$ | $V_{REF} + 0.5$ | $V_{REF}$ | 1.1 |
| SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V | SSTL3_I, SSTL3_II | $V_{REF} – 0.75$ | $V_{REF} + 0.75$ | $V_{REF}$ | 1.5 |
| SSTL, Class I & II, 2.5V | SSTL2_I, SSTL2_II | $V_{REF} – 0.75$ | $V_{REF} + 0.75$ | $V_{REF}$ | 1.25 |
| SSTL, Class I & II, 1.8V | SSTL18_I, SSTL18_II | $V_{REF} – 0.5$ | $V_{REF} + 0.5$ | $V_{REF}$ | 0.90 |
| SSTL, Class II, 1.5V | SSTL15_II | $V_{REF} – 0.2$ | $V_{REF} + 0.2$ | $V_{REF}$ | 0.75 |
| LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V | LVDS_25, LVDS_33 | 1.25 – 0.125 | 1.25 + 0.125 | 0[5] | – |
| LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V & 3.3V | LVPECL_25, LVPECL_33 | 1.2 – 0.3 | 1.2 + 0.3 | 0[5] | – |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | 1.3 – 0.125 | 1.3 + 0.125 | 0[5] | – |
| Mini-LVDS, 2.5V & 3.3V | MINI_LVDS_25,<br>MINI_LVDS_33 | 1.2 – 0.125 | 1.2 + 0.125 | 0[5] | – |
| RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V | RSDS_25, RSDS_33 | 1.2 – 0.1 | 1.2 + 0.1 | 0[5] | – |
| TMDS (Transition Minimized Differential Signaling), 3.3V | TMDS_33 | 3.0 – 0.1 | 3.0 + 0.1 | 0[5] | – |
| PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V | PPDS_25, PPDS_33 | 1.25 – 0.1 | 1.25 + 0.1 | 0[5] | – |

**Notes:**

1. Input waveform switches between $V_L$ and $V_H$.
2. Measurements are made at typical, minimum, and maximum $V_{REF}$ values. Reported delays reflect worst case of these measurements. $V_{REF}$ values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the $V_{REF}$ / $V_{MEAS}$ parameters found in IBIS models and/or noted in Figure 4.
5. The value given is the differential input voltage.

*Table 34:* **SSO Limit per $V_{CCO}$/GND Pair *(Cont'd)***

| $V_{CCO}$ | I/O Standard | Drive | Slew | SSO Limit per $V_{CCO}$/GND Pair | | | |
|---|---|---|---|---|---|---|---|
| | | | | All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324 | | All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324 | |
| | | | | Bank 0/2 | Bank 1/3 | Bank 0/2 | Bank 1/3/4/5 |
| 3.3V | LVTTL | 2 | Fast | 53 | 65 | 53 | 62 |
| | | | Slow | 70 | 80 | 70 | 73 |
| | | | QuietIO | 79 | 89 | 79 | 91 |
| | | 4 | Fast | 23 | 30 | 23 | 27 |
| | | | Slow | 34 | 41 | 34 | 37 |
| | | | QuietIO | 44 | 49 | 44 | 46 |
| | | 6 | Fast | 16 | 21 | 16 | 20 |
| | | | Slow | 21 | 28 | 21 | 25 |
| | | | QuietIO | 34 | 39 | 34 | 34 |
| | | 8 | Fast | 12 | 16 | 12 | 15 |
| | | | Slow | 16 | 22 | 16 | 19 |
| | | | QuietIO | 27 | 28 | 27 | 24 |
| | | 12 | Fast | 1 | 3 | 1 | 1 |
| | | | Slow | 2 | 5 | 2 | 4 |
| | | | QuietIO | 2 | 10 | 2 | 8 |
| | | 16 | Fast | 1 | 3 | 1 | 1 |
| | | | Slow | 1 | 7 | 1 | 2 |
| | | | QuietIO | 3 | 11 | 3 | 8 |
| | | 24 | Fast | 1 | 2 | 1 | 1 |
| | | | Slow | 2 | 5 | 2 | 2 |
| | | | QuietIO | 8 | 9 | 8 | 8 |
| | PCI33_3 | | | 18 | 19 | 18 | 19 |
| | PCI66_3 | | | 18 | 19 | 18 | 19 |
| | SSTL_3_I | | | 5 | 8 | 5 | 8 |
| | SSTL_3_II | | | 3 | 5 | 3 | 3 |
| | DIFF_SSTL_3_I | | | 15 | 24 | 15 | 24 |
| | DIFF_SSTL_3_II | | | 9 | 15 | 9 | 9 |
| | SDIO | | | 17 | 18 | 17 | 15 |

*Table 45:* **Device DNA Interface Port Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| $T_{DNASSU}$ | Setup time on SHIFT before the rising edge of CLK | 7 | | | | ns, Min |
| $T_{DNASH}$ | Hold time on SHIFT after the rising edge of CLK | 1 | | | | ns, Min |
| $T_{DNADSU}$ | Setup time on DIN before the rising edge of CLK | 7 | | | | ns, Min |
| $T_{DNADH}$ | Hold time on DIN after the rising edge of CLK | 1 | | | | ns, Min |
| $T_{DNARSU}$ | Setup time on READ before the rising edge of CLK | 7 | | | | ns, Min |
| | | 1,000 | | | | ns, Max |
| $T_{DNARH}$ | Hold time on READ after the rising edge of CLK | 1 | | | | ns, Min |
| $T_{DNADCKO}$ | Clock-to-output delay on DOUT after rising edge of CLK | 0.5 | | | | ns, Min |
| | | 6 | | | | ns, Max |
| $T_{DNACLKF}$(2) | CLK frequency | 2 | | | | MHz, Max |
| $T_{DNACLKL}$ | CLK Low time | 50 | | | | ns, Min |
| $T_{DNACLKH}$ | CLK High time | 50 | | | | ns, Min |

**Notes:**

1. The minimum READ pulse width is 8 ns, the maximum READ pulse width is 1 µs.
2. Also applies to TCK when reading DNA through the boundary-scan port.

*Table 46:* **Suspend Mode Switching Characteristics**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| **Entering Suspend Mode** | | | | |
| $T_{SUSPENDHIGH\_AWAKE}$ | Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter | 2.5 | 14 | ns |
| $T_{SUSPENDFILTER}$ | Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled | 31 | 430 | ns |
| $T_{SUSPEND\_GWE}$ | Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior (without glitch filter) | – | 15 | ns |
| $T_{SUSPEND\_GTS}$ | Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements (without glitch filter) | – | 15 | ns |
| $T_{SUSPEND\_DISABLE}$ | Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled (without glitch filter) | – | 1500 | ns |
| **Exiting Suspend Mode** | | | | |
| $T_{SUSPENDLOW\_AWAKE}$ | Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM or PLL lock time. | 7 | 75 | µs |
| $T_{SUSPEND\_ENABLE}$ | Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled | 7 | 41 | µs |
| $T_{AWAKE\_GWE1}$ | Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using **sw_clk:InternalClock** and **sw_gwe_cycle:1**. | – | 80 | ns |
| $T_{AWAKE\_GWE512}$ | Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using **sw_clk:InternalClock** and **sw_gwe_cycle:512**. | – | 20.5 | µs |
| $T_{AWAKE\_GTS1}$ | Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using **sw_clk:InternalClock** and **sw_gts_cycle:1**. | – | 80 | ns |
| $T_{AWAKE\_GTS512}$ | Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using **sw_clk:InternalClock** and **sw_gts_cycle:512**. | – | 20.5 | µs |
| $T_{SCP\_AWAKE}$ | Rising edge of SCP pins to rising edge of AWAKE pin | 7 | 75 | µs |

## Configuration Switching Characteristics

*Table 47:* **Configuration Switching Characteristics**[1]

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| **Power-up Timing Characteristics** | | | | | | |
| $T_{PL}$[2] | PROGRAM_B Latency | 4 | 4 | 4 | 5 | ms, Max |
| $T_{POR}$[2] | Power-on reset (50 ms ramp time)[3] | 5/30 | 5/34 | 5/40 | 5/40 | ms, Min/Max |
| | Power-on reset (10 ms ramp time) | 5/25 | 5/29 | 5/35 | 5/40 | ms, Min/Max |
| $T_{PROGRAM}$ | PROGRAM_B Pulse Width | 500 | 500 | 500 | 500 | ns, Min |
| **Slave Serial Mode Programming Switching** | | | | | | |
| $T_{DCCK}/T_{CCKD}$ | DIN Setup/Hold, slave mode | 6.0/1.0 | 6.0/1.0 | 6.0/1.0 | 8.0/2.0 | ns, Min |
| $T_{CCO}$ | CCLK to DOUT | 12 | 12 | 12 | 17 | ns, Max |
| $F_{SCCK}$ | Slave mode external CCLK | 80 | 80 | 80 | 50 | MHz, Max |
| **Slave SelectMAP Mode Programming Switching** | | | | | | |
| $T_{SMDCCK}/T_{SMCCKD}$ | SelectMAP Data Setup/Hold | 6.0/1.0 | 6.0/1.0 | 6.0/1.0 | 8.0/2.0 | ns, Min |
| $T_{SMCSCCK}/T_{SMCCKCS}$ | CSI_B Setup/Hold | 7.0/0.0 | 7.0/0.0 | 7.0/0.0 | 9.0/2.0 | ns, Min |
| $T_{SMWCCK}/T_{SMCCKW}$ | RDWR_B Setup/Hold | 17.0/1.0 | 17.0/1.0 | 17.0/1.0 | 27.0/2.0 | ns, Min |
| $T_{SMCKCSO}$ | CSO_B clock to out | 16 | 16 | 16 | 26 | ns, Max |
| $T_{SMCO}$ | CCLK to DATA out in readback | 13 | 13 | 13 | 25 | ns, Max |
| $T_{SMCKBY}$ | CCLK to BUSY out in readback | 12 | 12 | 12 | 17 | ns, Max |
| $F_{SMCCK}$ | Maximum CCLK frequency (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only) | 50 | 50 | 50 | 25 | MHz, Max |
| | Maximum CCLK frequency (LX100 and LX100T in x8 mode, LX150, and LX150T only) | 40 | 40 | 40 | 20 | MHz, Max |
| | Maximum CCLK frequency (LX100 and LX100T in x16 mode only) | 35 | 35 | 35 | 20 | MHz, Max |
| $F_{RBCCK}$ | Maximum Readback CCLK frequency, including block RAM (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only) | 20 | 20 | 20 | 4 | MHz, Max |
| | Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only) | 50 | 50 | 50 | 30 | MHz, Max |
| | Maximum Readback CCLK frequency, including block RAM (LX100, LX100T, LX150, and LX150T only) | 12 | 12 | 12 | 4 | MHz, Max |
| | Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX100, LX100T, LX150, and LX150T only) | 35 | 35 | 35 | 20 | MHz, Max |
| **Boundary-Scan Port Timing Specifications** | | | | | | |
| $T_{TAPTCK}$ | TMS and TDI Setup time before TCK | 10 | 10 | 10 | 17 | ns, Min |
| $T_{TCKTAP}$ | TMS and TDI Hold time after TCK | 5.5 | 5.5 | 5.5 | 5.5 | ns, Min |
| $T_{TCKTDO}$ | TCK falling edge to TDO output valid | 6.5 | 6.5 | 6.5 | 8 | ns, Max |
| $T_{TCKH}$ | TCK clock minimum High time | 12 | 12 | 12 | 21 | ns, Min |
| $T_{TCKL}$ | TCK clock minimum Low time | 12 | 12 | 12 | 21 | ns, Min |
| $F_{TCK}$ | Maximum configuration TCK clock frequency | 33 | 33 | 33 | 18 | MHz, Max |
| $F_{TCKB}$ | Maximum boundary-scan TCK clock frequency | 33 | 33 | 33 | 18 | MHz, Max |
| $F_{TCKAES}$ | Maximum AES key TCK clock frequency | 2 | 2 | 2 | 2 | MHz, Max |

## DCM Switching Characteristics

*Table 53:* **Operating Frequency Ranges and Conditions for the Delay-Locked Loop (DLL)(1)**

| Symbol | Description | Speed Grade | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| **Input Frequency Ranges** | | | | | | | | | | |
| CLKIN_FREQ_DLL | Frequency of the CLKIN clock input when the CLKDV output is not used. | 5(2) | 280(3) | 5(2) | 280(3) | 5(2) | 250(3) | 5(2) | 175(3) | MHz |
| | Frequency of the CLKIN clock input when using the CLKDV output. | 5(2) | 280(3) | 5(2) | 280(3) | 5(2) | 250(3) | 5(2) | 133(3) | MHz |
| **Input Pulse Requirements** | | | | | | | | | | |
| CLKIN_PULSE | CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL < 150 MHz | 40 | 60 | 40 | 60 | 40 | 60 | 40 | 60 | % |
| | CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL > 150 MHz | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |
| **Input Clock Jitter Tolerance and Delay Path Variation(4)** | | | | | | | | | | |
| CLKIN_CYC_JITT_DLL_LF | Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL < 150 MHz | – | ±300 | – | ±300 | – | ±300 | – | ±300 | ps |
| CLKIN_CYC_JITT_DLL_HF | Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL > 150 MHz. | – | ±150 | – | ±150 | – | ±150 | – | ±150 | ps |
| CLKIN_PER_JITT_DLL | Period jitter at the CLKIN input. | – | ±1 | – | ±1 | – | ±1 | – | ±1 | ns |
| CLKFB_DELAY_VAR_EXT | Allowable variation of the off-chip feedback delay from the DCM output to the CLKFB input. | – | ±1 | – | ±1 | – | ±1 | – | ±1 | ns |

**Notes:**

1. DLL specifications apply when using any of the DLL outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV.
2. When operating independently of the DLL, the DFS supports lower CLKIN_FREQ_DLL frequencies. See Table 55.
3. The CLKIN_DIVIDE_BY_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the $F_{MAX}$ (see Table 48 and Table 49 for BUFG and BUFIO2 limits). When used with CLK_FEEDBACK=2X, the input clock frequency matches the frequency for CLK2X, and is limited to CLKOUT_FREQ_2X.
4. CLKIN_FREQ_DLL input jitter beyond these limits can cause the DCM to lose LOCK, indicated by the LOCKED output deasserting. The user must then reset the DCM.
5. When using both DCMs in a CMT, both DCMs must be LOCKED.

*Table 54:* **Switching Characteristics for the Delay-Locked Loop (DLL)(1)**

| Symbol | Description | Speed Grade | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| **Output Frequency Ranges** | | | | | | | | | | |
| CLKOUT_FREQ_CLK0 | Frequency for the CLK0 and CLK180 outputs. | 5 | 280 | 5 | 280 | 5 | 250 | 5 | 175 | MHz |
| CLKOUT_FREQ_CLK90 | Frequency for the CLK90 and CLK270 outputs. | 5 | 200 | 5 | 200 | 5 | 200 | 5 | 175 | MHz |
| CLKOUT_FREQ_2X | Frequency for the CLK2X and CLK2X180 outputs. | 10 | 375 | 10 | 375 | 10 | 334 | 10 | 250 | MHz |
| CLKOUT_FREQ_DV | Frequency for the CLKDV output. | 0.3125 | 186 | 0.3125 | 186 | 0.3125 | 166 | 0.3125 | 88.6 | MHz |
| **Output Clock Jitter(2)(3)(4)** | | | | | | | | | | |
| CLKOUT_PER_JITT_0 | Period jitter at the CLK0 output. | – | ±100 | – | ±100 | – | ±100 | – | ±100 | ps |
| CLKOUT_PER_JITT_90 | Period jitter at the CLK90 output. | – | ±150 | – | ±150 | – | ±150 | – | ±150 | ps |
| CLKOUT_PER_JITT_180 | Period jitter at the CLK180 output. | – | ±150 | – | ±150 | – | ±150 | – | ±150 | ps |
| CLKOUT_PER_JITT_270 | Period jitter at the CLK270 output. | – | ±150 | – | ±150 | – | ±150 | – | ±150 | ps |
| CLKOUT_PER_JITT_2X | Period jitter at the CLK2X and CLK2X180 outputs. | Maximum = ±[0.5% of CLKIN period + 100] | | | | | | | | ps |
| CLKOUT_PER_JITT_DV1 | Period jitter at the CLKDV output when performing integer division. | – | ±150 | – | ±150 | – | ±150 | – | ±150 | ps |
| CLKOUT_PER_JITT_DV2 | Period jitter at the CLKDV output when performing non-integer division. | Maximum = ±[0.5% of CLKIN period + 100] | | | | | | | | ps |
| **Duty Cycle(4)** | | | | | | | | | | |
| CLKOUT_DUTY_CYCLE_DLL | Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion. | Typical = ±[1% of CLKIN period + 350] | | | | | | | | ps |
| **Phase Alignment(4)** | | | | | | | | | | |
| CLKIN_CLKFB_PHASE | Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 1X). | – | ±150 | – | ±150 | – | ±150 | – | ±250 | ps |
| | Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 2X).(6) | – | ±250 | – | ±250 | – | ±250 | – | ±350 | |
| CLKOUT_PHASE_DLL | Phase offset between DLL outputs for CLK0 to CLK2X (not CLK2X180). | Maximum = ±[1% of CLKIN period + 100] | | | | | | | | ps |
| | Phase offset between DLL outputs for all others. | Maximum = ±[1% of CLKIN period + 150] | | | | | | Maximum = ±[1% of CLKIN period + 200] | | ps |

### *Table 54:* Switching Characteristics for the Delay-Locked Loop (DLL)[(1)] *(Cont'd)*

| Symbol | Description | Speed Grade | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| LOCK_DLL[(3)] | When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.<br>CLKIN_FREQ_DLL < 50 MHz. | – | 5 | – | 5 | – | 5 | – | 5 | ms |
| | When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.<br>CLKIN_FREQ_DLL > 50 MHz | – | 0.60 | – | 0.60 | – | 0.60 | – | 0.60 | ms |
| **Delay Lines** | | | | | | | | | | |
| DCM_DELAY_STEP[(5)] | Finest delay resolution, averaged over all steps. | 10 | 40 | 10 | 40 | 10 | 40 | 10 | 40 | ps |

**Notes:**

1. The values in this table are based on the operating conditions described in Table 2 and Table 53.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster LOCK time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, this data sheet specifies a maximum jitter of ±(1% of CLKIN period + 150 ps). Assuming that the CLKIN frequency is 100 MHz, the equivalent CLKIN period is 10 ns. Since 1% of 10 ns is 0.1 ns or 100 ps, the maximum jitter is ±(100 ps + 150 ps) = ±250 ps.
5. A typical delay step size is 23 ps.
6. The timing analysis tools use the CLK_FEEDBACK = 1X condition for the CLKIN_CLKFB_PHASE value (reported as phase error). When using CLK_FEEDBACK = 2X, add 100 ps to the phase error for the CLKIN_CLKFB_PHASE value (as shown in this table).

### *Table 55:* Recommended Operating Conditions for the Digital Frequency Synthesizer (DFS)[(1)]

| Symbol | Description | Speed Grade | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| **Input Frequency Ranges[(2)]** | | | | | | | | | | |
| CLKIN_FREQ_FX | Frequency for the CLKIN input. Also described as $F_{CLKIN}$. | 0.5 | 375[(3)] | 0.5 | 375[(3)] | 0.5 | 333[(3)] | 0.5 | 200[(3)] | MHz |
| **Input Clock Jitter Tolerance[(4)]** | | | | | | | | | | |
| CLKIN_CYC_JITT_FX_LF | Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency:<br>FCLKFX < 150 MHz. | – | ±300 | – | ±300 | – | ±300 | – | ±300 | ps |
| CLKIN_CYC_JITT_FX_HF | Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency:<br>FCLKFX > 150 MHz. | – | ±150 | – | ±150 | – | ±150 | – | ±150 | ps |
| CLKIN_PER_JITT_FX | Period jitter at the CLKIN input. | – | ±1 | – | ±1 | – | ±1 | – | ±1 | ns |

**Notes:**

1. DFS specifications apply when using either of the DFS outputs (CLKFX or CLKFX180).
2. When using both DFS and DLL outputs on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 53.
3. The CLKIN_DIVIDE_BY_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the $F_{MAX}$ (see Table 48 and Table 49 for BUFG and BUFIO2 limits).
4. CLKIN input jitter beyond these limits can cause the DCM to lose LOCK.

## Spartan-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 70 through Table 77. Values are expressed in nanoseconds unless otherwise noted.

*Table 70:* **Global Clock Setup and Hold Without DCM or PLL (No Delay)**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.**[1] | | | | | | | |
| $T_{PSND}$/ $T_{PHND}$ | No Delay Global Clock and IFF[3] without DCM or PLL | XC6SLX4 | 0.10/1.56 | N/A | 0.10/1.83 | 0.07/2.54 | ns |
| | | XC6SLX9 | 0.10/1.56 | 0.10/1.57 | 0.10/1.84 | 0.07/2.54 | ns |
| | | XC6SLX16 | 0.12/1.42 | 0.12/1.48 | 0.12/1.64 | 0.13/2.19 | ns |
| | | XC6SLX25 | 0.18/1.64 | 0.18/1.75 | 0.18/1.99 | 0.11/2.57 | ns |
| | | XC6SLX25T | 0.18/1.64 | 0.18/1.75 | 0.18/1.99 | N/A | ns |
| | | XC6SLX45 | –0.08/1.80 | –0.08/1.95 | –0.08/2.27 | –0.17/2.74 | ns |
| | | XC6SLX45T | –0.08/1.80 | –0.08/1.95 | –0.08/2.27 | N/A | ns |
| | | XC6SLX75 | 0.13/1.81 | 0.13/2.06 | 0.13/2.27 | –0.12/3.30 | ns |
| | | XC6SLX75T | 0.13/1.81 | 0.13/2.06 | 0.13/2.27 | N/A | ns |
| | | XC6SLX100 | –0.14/2.03 | –0.14/2.24 | –0.14/2.56 | –0.17/3.44 | ns |
| | | XC6SLX100T | –0.14/2.03 | –0.14/2.24 | –0.14/2.56 | N/A | ns |
| | | XC6SLX150 | –0.24/2.42 | –0.24/2.74 | –0.24/2.95 | –0.60/3.75 | ns |
| | | XC6SLX150T | –0.24/2.42 | –0.24/2.74 | –0.24/2.95 | N/A | ns |
| | | XA6SLX4 | 0.10/1.57 | N/A | 0.10/1.84 | N/A | ns |
| | | XA6SLX9 | 0.10/1.57 | N/A | 0.10/1.84 | N/A | ns |
| | | XA6SLX16 | 0.12/1.43 | N/A | 0.12/1.64 | N/A | ns |
| | | XA6SLX25 | 0.18/1.65 | N/A | 0.18/1.99 | N/A | ns |
| | | XA6SLX25T | 0.18/1.65 | N/A | 0.18/1.99 | N/A | ns |
| | | XA6SLX45 | –0.08/1.82 | N/A | –0.08/2.27 | N/A | ns |
| | | XA6SLX45T | –0.08/1.82 | N/A | –0.08/2.27 | N/A | ns |
| | | XA6SLX75 | 0.13/2.02 | N/A | 0.13/2.32 | N/A | ns |
| | | XA6SLX75T | 0.13/2.02 | N/A | 0.13/2.32 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 0.10/2.51 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 0.13/2.32 | –0.12/3.30 | ns |
| | | XQ6SLX75T | 0.13/2.02 | N/A | 0.13/2.32 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | –0.24/2.95 | –0.60/3.75 | ns |
| | | XQ6SLX150T | –0.24/2.74 | N/A | –0.24/2.95 | N/A | ns |

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.

*Table 73:* **Global Clock Setup and Hold With DCM in Source-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.[1]** | | | | | | | |
| $T_{PSDCM0}$/ $T_{PHDCM0}$ | No Delay Global Clock and IFF[2] with DCM in Source-Synchronous Mode | XC6SLX4 | 0.71/0.65 | N/A | 0.72/1.22 | 1.58/1.18 | ns |
| | | XC6SLX9 | 0.71/0.69 | 0.71/1.19 | 0.72/1.36 | 1.58/1.18 | ns |
| | | XC6SLX16 | 0.86/0.52 | 0.92/0.57 | 1.04/0.60 | 1.02/1.06 | ns |
| | | XC6SLX25 | 0.84/0.58 | 0.90/0.59 | 1.01/0.59 | 1.58/1.07 | ns |
| | | XC6SLX25T | 0.84/0.58 | 0.90/0.59 | 1.01/0.59 | N/A | ns |
| | | XC6SLX45 | 0.85/0.70 | 0.90/0.76 | 0.98/0.79 | 1.34/1.34 | ns |
| | | XC6SLX45T | 0.85/0.70 | 0.90/0.76 | 0.98/0.79 | N/A | ns |
| | | XC6SLX75 | 1.00/0.62 | 1.06/0.63 | 1.15/0.63 | 1.65/1.46 | ns |
| | | XC6SLX75T | 1.00/0.71 | 1.06/0.72 | 1.15/0.72 | N/A | ns |
| | | XC6SLX100 | 0.81/0.68 | 0.81/0.69 | 0.94/0.69 | 1.42/2.07 | ns |
| | | XC6SLX100T | 0.81/0.68 | 0.81/0.69 | 0.94/0.69 | N/A | ns |
| | | XC6SLX150 | 0.68/0.98 | 0.69/0.99 | 0.79/0.99 | 1.45/1.60 | ns |
| | | XC6SLX150T | 0.68/0.98 | 0.69/0.99 | 0.79/0.99 | N/A | ns |
| | | XA6SLX4 | 0.81/0.74 | N/A | 0.72/1.36 | N/A | ns |
| | | XA6SLX9 | 0.81/0.74 | N/A | 0.72/1.36 | N/A | ns |
| | | XA6SLX16 | 1.01/0.56 | N/A | 1.04/0.60 | N/A | ns |
| | | XA6SLX25 | 0.94/0.76 | N/A | 1.06/0.77 | N/A | ns |
| | | XA6SLX25T | 0.94/0.76 | N/A | 1.14/0.77 | N/A | ns |
| | | XA6SLX45 | 0.86/0.74 | N/A | 0.98/0.78 | N/A | ns |
| | | XA6SLX45T | 0.86/0.74 | N/A | 0.98/0.78 | N/A | ns |
| | | XA6SLX75 | 1.02/0.71 | N/A | 1.15/0.72 | N/A | ns |
| | | XA6SLX75T | 1.02/0.71 | N/A | 1.15/0.72 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 1.37/0.75 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 1.15/0.72 | 1.65/1.46 | ns |
| | | XQ6SLX75T | 1.02/0.71 | N/A | 1.15/0.72 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | 0.79/1.15 | 1.45/1.60 | ns |
| | | XQ6SLX150T | 0.73/1.15 | N/A | 0.79/1.15 | N/A | ns |

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 79:* **Package Skew *(Cont'd)***

| Symbol | Description | Device | Package[2] | Value | Units |
|---|---|---|---|---|---|
| $T_{PKGSKEW}$ | Package Skew[1] | LX45 | CSG324 | 70 | ps |
| | | | CS(G)484 | 99 | ps |
| | | | FG(G)484 | 109 | ps |
| | | | FG(G)676 | 138 | ps |
| | | LX45T | CSG324 | 75 | ps |
| | | | CS(G)484 | 100 | ps |
| | | | FG(G)484 | 95 | ps |
| | | LX75 | CS(G)484 | 101 | ps |
| | | | FG(G)484 | 107 | ps |
| | | | FG(G)676 | 161 | ps |
| | | LX75T | CS(G)484 | 107 | ps |
| | | | FG(G)484 | 110 | ps |
| | | | FG(G)676 | 134 | ps |
| | | LX100 | CS(G)484 | 95 | ps |
| | | | FG(G)484 | 155 | ps |
| | | | FG(G)676 | 144 | ps |
| | | LX100T | CS(G)484 | 88 | ps |
| | | | FG(G)484 | 111 | ps |
| | | | FG(G)676 | 147 | ps |
| | | | FG(G)900 | 134 | ps |
| | | LX150 | CS(G)484 | 84 | ps |
| | | | FG(G)484 | 103 | ps |
| | | | FG(G)676 | 115 | ps |
| | | | FG(G)900 | 121 | ps |
| | | LX150T | CS(G)484 | 83 | ps |
| | | | FG(G)484 | 88 | ps |
| | | | FG(G)676 | 141 | ps |
| | | | FG(G)900 | 120 | ps |

**Notes:**

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from Pad to Ball.
2. Some of the devices are available in both Pb and Pb-free (additional G) packages as standard ordering options. See DS160: *Spartan-6 Family Overview* for more information.

*Table 80:* **Sample Window**

| Symbol | Description | Device[1] | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| $T_{SAMP}$ | Sampling Error at Receiver Pins[2] | All | 510 | 510 | 530 | 740 | ps |
| $T_{SAMP\_BUFIO2}$ | Sampling Error at Receiver Pins using BUFIO2[3] | All | 430 | 430 | 450 | 590 | ps |

**Notes:**

1. LXT devices are not available with a -1L speed grade.
2. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 DCM jitter
   - DCM accuracy (phase offset)
   - DCM phase shift resolution

   These measurements do not include package or clock tree skew.
3. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO2 clock network and IODELAY2 to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

| Date | Version | Description of Revisions |
|---|---|---|
| 06/14/10 | 1.5 | In Table 2, added note 5 and added temperature range to $V_{FS}$ and $R_{FUSE}$. Removed speed grade delineation, revised $I_{RPD}$ description, and updated note 2 in Table 4. Added note 2 to Table 7. Added DIFF_MOBILE_DDR to Table 8 and Table 10. Added note 4 to Table 15. Changed minimum $DV_{PPIN}$ in Table 16. Updated $F_{GTPDRPCLK}$ in Table 19. Increased maximum $T_{LLSKEW}$ in Table 22. Updated descriptions and added data to Table 23. Removed note 1 and added new data to the Networking Applications section in Table 25. Updated Table 26 and Table 27 to the data in ISE v12.1 software with speed specification v1.08. In Table 28, added DIFF_MOBILE_DDR and updated -4 speed grade data. Updated the maximum I/O pairs per bank in Table 33. Updated note 2 on Table 39. Revised the $F_{MAX}$ in Table 44. In Table 47, updated description for $T_{SMCKCSO}$, revised values for $T_{POR}$ and added Min value, added $T_{BPIICCK}$ and $T_{SPIICCK}$. Also in Table 47, added device dependencies to $F_{SMCCK}$ and $F_{RBCCK}$. Updated and added data to Table 63 through Table 78, and Table 81. In Table 79, added data on the XC6SLX45-FG(G)676 and revised the XC6SLX45T and XC6SLX150T values.<br>The following changes to this specification are addressed in the product change notice XCN10024, *MCB Performance and JTAG Revision Code for Spartan-6 LX16 and LX45 FPGAs*.<br>In Table 2, revised the $V_{CCINT}$ to add the memory controller block extended performance specifications. In Table 25, changed the standard specifications and added extended performance specifications for the memory controller block and note 2. Added note 4 and updated values in Table 34. |
| 06/24/10 | 1.6 | Production release of XC6SLX45T (-2 and -3 speed grades), XC6SLX16 and XC6SLX45 (-3 speed grade) devices which includes changes to Table 26 and Table 27 (ISE v12.1 software with speed specification v1.08).<br>Added the -3N speed grade, which designates Spartan-6 devices that do not support MCB functionality. This includes changes to Table 2 (note 2), Table 25 (note 4), and Switching Characteristics (Table 26).<br>Updated Simultaneously Switching Outputs discussion. Added -3 speed grade values for $T_{TAP}$ and $F_{MINCAL}$ values in Table 39. In Table 40, updated $T_{RPW}$ (-2 and -3 speed grade) values and $F_{TOG}$ (-3 speed grade) values. In Table 48, updated $T_{GIO}$ (-2 and -3 speed grade) values. Updated -3 values in spread spectrum section of Table 57. |
| 07/16/10 | 1.7 | Production release of specific devices listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 4 advising designers of the patch which contains v1.11. Also updated the -1L speed specification to v1.04. Updated numerous -4 and -1L values. Added -4 $T_{TAP}$ values and $F_{MINCAL}$ to Table 39. Revised $T_{CINCK}/T_{CKCIN}$ in Table 40. In Table 41, revised $T_{SHCKO}$. In Table 42, revised $T_{REG}$. Added new -1L values to Table 47. Added and updated values in Table 79. |
| 07/26/10 | 1.8 | Production release of XC6SLX25, XC6SLX25T, XC6SLX100 and XC6SLX100T in the specific speed grades listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 7 to Table 2 and moved $V_{FS}$ and $R_{FUSE}$ to a new Table 3. Added $I_{HS}$ and note 4 to Table 4. Added note 1 to Table 28. Added and updated SSO limits per $V_{CCO}$/GND pairs in Table 34. Added note 3 to Table 47. In Table 54, removed -1L specifications for CLKOUT_PER_JITT_DV1/2 and revised CLKIN_CLKFB_PHASE and CLKOUT_PHASE_DLL values. Updated note 3 in both Table 56 and Table 57. |
| 08/23/10 | 1.9 | Updated values for $F_{GTPRANGE1}$, $F_{GTPRANGE2}$, and $F_{GPLLMIN}$ in Table 18. Revised -3 and -4 values in Table 21. Removed the -1L speed grade readback support restriction and note 3 in Table 47. |
| 11/05/10 | 1.10 | Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.3 software with speed specification v1.12 for the -2 speed grade available in the 12.3 *Speed Files Patch*. Added note 3 advising designers of the patch which contains v1.12.<br>In Table 2, added note 4. In Table 4, added note 2. In Table 10, added notes 2 and 3. In Table 44, added note 2. In Table 47, updated symbol for $T_{SMWCCK}/T_{SMCCKW}$, changed -1L values for $T_{USERCCLKH}$ and $T_{USERCCLKL}$, and added and revised the modes for $F_{MCCK}$ and $F_{SMCCK}$. In Table 53, redefined and expanded description for CLKIN_FREQ_DLL and rewrote note 3. Updated title of Table 58. Also in Table 78, revised $T_{DCD\_CLK}$ for XC6SLX150 and XC6SLX150T. Changed description of $T_{PSFD}$/ $T_{PHFD}$ in Table 71.<br>For the -1L speed grade, updated data sheet to ISE 12.3 software with speed specification v1.05 which revised the values in the following tables: Table 25, Table 28, Table 35, Table 36, Table 37, Table 40 through Table 43, Table 48 through Table 56, Table 62 through Table 78, Table 80, and Table 81.<br>Updated Notice of Disclaimer. |