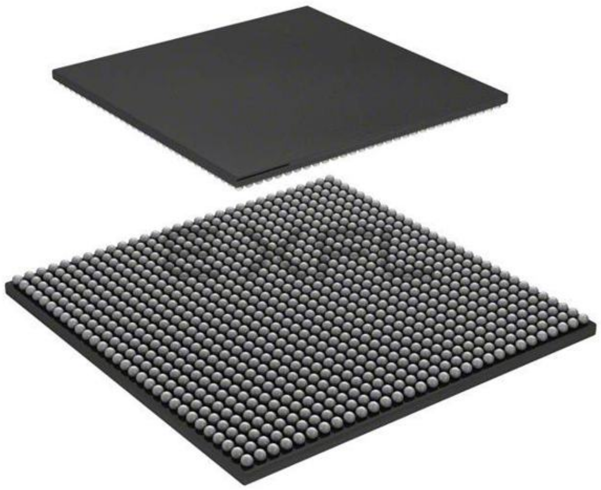
AMD Xilinx - XC6SLX100T-3FGG900C Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	7911
Number of Logic Elements/Cells	101261
Total RAM Bits	4939776
Number of I/O	498
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx100t-3fgg900c

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Table 1: **Absolute Maximum Ratings(1)** ***(Cont'd)***

Symbol	Description					Units
V_{IN} and V_{TS}(3)	I/O input voltage or voltage applied to 3-state output, relative to GND(4)	All user and dedicated I/Os	Commercial	DC	–0.60 to 4.10	V
				20% overshoot duration	–0.75 to 4.25	V
				8% overshoot duration(5)	–0.75 to 4.40	V
			Industrial	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration(5)	–0.75 to 4.40	V
			Expanded (Q)	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration(5)	–0.75 to 4.40	V
		Restricted to maximum of 100 user I/Os	Commercial	20% overshoot duration	–0.75 to 4.35	V
				15% overshoot duration(5)	–0.75 to 4.40	V
				10% overshoot duration	–0.75 to 4.45	V
			Industrial	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration(5)	–0.75 to 4.40	V
			Expanded (Q)	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration(5)	–0.75 to 4.40	V
T_{STG}	Storage temperature (ambient)				–65 to 150	°C
T_{SOL}	Maximum soldering temperature(6) (TQG144, CPG196, CSG225, CSG324, CSG484, and FTG256)				+260	°C
	Maximum soldering temperature(6) (Pb-free packages: FGG484, FGG676, and FGG900)				+250	°C
	Maximum soldering temperature(6) (Pb packages: CS484, FT256, FG484, FG676, and FG900)				+220	°C
T_j	Maximum junction temperature(6)				+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When programming eFUSE, $V_{FS} \leq V_{CCAUX}$. Requires up to 40 mA current. For read mode, V_{FS} can be between GND and 3.45 V.
3. I/O absolute maximum limit applied to DC and AC signals. Overshoot duration is the percentage of a data period that the I/O is stressed beyond 3.45V.
4. For I/O operation, refer to UG381: *Spartan-6 FPGA SelectIO Resources User Guide*.
5. Maximum percent overshoot duration to meet 4.40V maximum.
6. For soldering guidelines and thermal considerations, see UG385: *Spartan-6 FPGA Packaging and Pinout Specification*.

eFUSE Read Endurance

Table 11 lists the minimum guaranteed number of read cycle operations for Device DNA and for the AES eFUSE key. For more information, see UG380: *Spartan-6 FPGA Configuration User Guide*.

Table 11: **eFUSE Read Endurance**

Symbol	Description	Speed Grade				Units (Min)
		-3	-3N	-2	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTP Transceiver Specifications

GTP transceivers are available in the Spartan-6 LXT devices. See DS160: *Spartan-6 Family Overview* for more information.

GTP Transceiver DC Characteristics

Table 12: **Absolute Maximum Ratings for GTP Transceivers(1)**

Symbol	Description	MIn	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	–0.5	1.32	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	–0.5	1.32	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	–0.5	1.32	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 13: **Recommended Operating Conditions for GTP Transceivers(1)(2)(3)**

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	1.14	1.20	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in UG386: *Spartan-6 FPGA GTP Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +125°C.
3. The voltage level of MGTAVCCPLL must not exceed the voltage level of MGTAVCC +10mV. The voltage level of MGTAVCC must not exceed the voltage level of MGTAVCCPLL.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics, page 19.

Table 25: **Interface Performances**

Description	I/O Resource	Clock Buffer	Data Width	Speed Grade				Units
				-3	-3N	-2	-1L	
Networking Applications(1)								
SDR LVDS transmitter or receiver	IOB SDR register	BUFG	–	400	400	375	250	Mb/s
DDR LVDS transmitter or receiver	ODDR2/IDDR2 register	2 BUFGs	–	800	800	750	500	Mb/s
SDR LVDS transmitter	OSERDES2	BUFPLL	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
DDR LVDS transmitter	OSERDES2	2 BUFIO2s	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
SDR LVDS receiver	ISERDES2 in RETIMED mode	BUFPLL	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
DDR LVDS receiver	ISERDES2 in RETIMED mode	2 BUFIO2s	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
Memory Interfaces (Implemented using the Spartan-6 FPGA Memory Controller Block)(2)								
Standard Performance (Standard V_{CCINT})								
DDR				400	Note 4	400	350	Mb/s
DDR2				667	Note 4	625	400	Mb/s
DDR3				800	Note 4	667	—	Mb/s
LPDDR (Mobile_DDR)				400	Note 4	400	350	Mb/s
Extended Performance (Requires Extended Performance V_{CCINT})(3)								
DDR2				800	Note 4	667	—	Mb/s

Notes:

1. Refer to XAPP1064, *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)* and UG381, *Spartan-6 FPGA SelectIO Resources User Guide.*
2. Refer to UG388, *Spartan-6 FPGA Memory Controller User Guide*.
3. Extended Memory Controller block performance for DDR2 can be achieved using the extended performance V_{CCINT} range from Table 2.
4. The LX4 device, all devices in the TQG144 and CPG196 packages, and the -3N speed grade do not support a Memory Controller Block.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 27 lists the production released Spartan-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE® software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 27: **Spartan-6 Device Production Software and Speed Specification Release(1)**

Device	**Speed Grade Designations(2)**			
	-3(3)	**-3N**	**-2(4)**	**-1L**
XC6SLX4	ISE 12.4 v1.15	N/A	ISE 12.3 v1.12(5)	ISE 13.2 v1.07
XC6SLX9	ISE 12.4 v1.15	ISE 13.1 Update v1.18(7)	ISE 12.3 v1.12(5)	ISE 13.2 v1.07
XC6SLX16	ISE 12.1 v1.08	ISE 13.1 Update v1.18(7)	ISE 11.5 v1.06	ISE 13.2 v1.07
XC6SLX25	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	ISE 13.2 v1.07
XC6SLX25T	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	N/A
XC6SLX45	ISE 12.1 v1.08	ISE 13.1 Update v1.18(7)	ISE 11.5 v1.07	ISE 13.1 v1.06
XC6SLX45T	ISE 12.1 v1.08	ISE 13.1 Update v1.18(7)	ISE 12.1 v1.08	N/A
XC6SLX75	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	ISE 13.2 v1.07
XC6SLX75T	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	N/A
XC6SLX100	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	ISE 13.1 v1.06
XC6SLX100T	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	N/A
XC6SLX150	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	ISE 13.1 v1.06
XC6SLX150T	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	N/A
XA6SLX4	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX9	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX16	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX25	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX25T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX45	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX45T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX75	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX75T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX100	N/A	N/A	ISE 13.3 v1.20	N/A

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L(1)	-3	-3N	-2	-1L(1)	-3	-3N	-2	-1L(1)	
LVTTL, QUIETIO, 2 mA	1.35	1.47	1.60	1.82	5.39	5.53	5.73	6.37	5.39	5.53	5.73	6.37	ns
LVTTL, QUIETIO, 4 mA	1.35	1.47	1.60	1.82	4.29	4.43	4.63	5.22	4.29	4.43	4.63	5.22	ns
LVTTL, QUIETIO, 6 mA	1.35	1.47	1.60	1.82	3.75	3.89	4.09	4.69	3.75	3.89	4.09	4.69	ns
LVTTL, QUIETIO, 8 mA	1.35	1.47	1.60	1.82	3.23	3.37	3.57	4.20	3.23	3.37	3.57	4.20	ns
LVTTL, QUIETIO, 12 mA	1.35	1.47	1.60	1.82	3.28	3.42	3.62	4.22	3.28	3.42	3.62	4.22	ns
LVTTL, QUIETIO, 16 mA	1.35	1.47	1.60	1.82	2.94	3.08	3.28	3.92	2.94	3.08	3.28	3.92	ns
LVTTL, QUIETIO, 24 mA	1.35	1.47	1.60	1.82	2.69	2.83	3.03	3.67	2.69	2.83	3.03	3.67	ns
LVTTL, Slow, 2 mA	1.35	1.47	1.60	1.82	4.36	4.50	4.70	5.30	4.36	4.50	4.70	5.30	ns
LVTTL, Slow, 4 mA	1.35	1.47	1.60	1.82	3.17	3.31	3.51	4.16	3.17	3.31	3.51	4.16	ns
LVTTL, Slow, 6 mA	1.35	1.47	1.60	1.82	2.76	2.90	3.10	3.75	2.76	2.90	3.10	3.75	ns
LVTTL, Slow, 8 mA	1.35	1.47	1.60	1.82	2.59	2.73	2.93	3.55	2.59	2.73	2.93	3.55	ns
LVTTL, Slow, 12 mA	1.35	1.47	1.60	1.82	2.58	2.72	2.92	3.54	2.58	2.72	2.92	3.54	ns
LVTTL, Slow, 16 mA	1.35	1.47	1.60	1.82	2.39	2.53	2.73	3.40	2.39	2.53	2.73	3.40	ns
LVTTL, Slow, 24 mA	1.35	1.47	1.60	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVTTL, Fast, 2 mA	1.35	1.47	1.60	1.82	3.78	3.92	4.12	4.74	3.78	3.92	4.12	4.74	ns
LVTTL, Fast, 4 mA	1.35	1.47	1.60	1.82	2.49	2.63	2.83	3.45	2.49	2.63	2.83	3.45	ns
LVTTL, Fast, 6 mA	1.35	1.47	1.60	1.82	2.44	2.58	2.78	3.40	2.44	2.58	2.78	3.40	ns
LVTTL, Fast, 8 mA	1.35	1.47	1.60	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns
LVTTL, Fast, 12 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTL, Fast, 16 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTL, Fast, 24 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVCMOS33, QUIETIO, 2 mA	1.34	1.46	1.59	1.82	5.40	5.54	5.74	6.37	5.40	5.54	5.74	6.37	ns
LVCMOS33, QUIETIO, 4 mA	1.34	1.46	1.59	1.82	4.03	4.17	4.37	5.01	4.03	4.17	4.37	5.01	ns
LVCMOS33, QUIETIO, 6 mA	1.34	1.46	1.59	1.82	3.51	3.65	3.85	4.47	3.51	3.65	3.85	4.47	ns
LVCMOS33, QUIETIO, 8 mA	1.34	1.46	1.59	1.82	3.37	3.51	3.71	4.33	3.37	3.51	3.71	4.33	ns
LVCMOS33, QUIETIO, 12 mA	1.34	1.46	1.59	1.82	2.94	3.08	3.28	3.93	2.94	3.08	3.28	3.93	ns
LVCMOS33, QUIETIO, 16 mA	1.34	1.46	1.59	1.82	2.77	2.91	3.11	3.78	2.77	2.91	3.11	3.78	ns
LVCMOS33, QUIETIO, 24 mA	1.34	1.46	1.59	1.82	2.59	2.73	2.93	3.58	2.59	2.73	2.93	3.58	ns
LVCMOS33, Slow, 2 mA	1.34	1.46	1.59	1.82	4.37	4.51	4.71	5.28	4.37	4.51	4.71	5.28	ns
LVCMOS33, Slow, 4 mA	1.34	1.46	1.59	1.82	2.98	3.12	3.32	3.94	2.98	3.12	3.32	3.94	ns
LVCMOS33, Slow, 6 mA	1.34	1.46	1.59	1.82	2.58	2.72	2.92	3.61	2.58	2.72	2.92	3.61	ns
LVCMOS33, Slow, 8 mA	1.34	1.46	1.59	1.82	2.65	2.79	2.99	3.61	2.65	2.79	2.99	3.61	ns
LVCMOS33, Slow, 12 mA	1.34	1.46	1.59	1.82	2.39	2.53	2.73	3.31	2.39	2.53	2.73	3.31	ns
LVCMOS33, Slow, 16 mA	1.34	1.46	1.59	1.82	2.31	2.45	2.65	3.27	2.31	2.45	2.65	3.27	ns
LVCMOS33, Slow, 24 mA	1.34	1.46	1.59	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVCMOS33, Fast, 2 mA	1.34	1.46	1.59	1.82	3.76	3.90	4.10	4.70	3.76	3.90	4.10	4.70	ns
LVCMOS33, Fast, 4 mA	1.34	1.46	1.59	1.82	2.48	2.62	2.82	3.44	2.48	2.62	2.82	3.44	ns
LVCMOS33, Fast, 6 mA	1.34	1.46	1.59	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns

Table 34: **SSO Limit per V_{CCO}/GND Pair**

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
1.2V	LVCMOS12, LVCMOS12_JEDEC	2	Fast	30 (1)	35	30	35
			Slow	51	55	51	52
			QuietIO	71	58	71	70
		4	Fast	17	17	17	19
			Slow	23	25	23	22
			QuietIO	35	32	35	32
		6	Fast	13	15	13	14
			Slow	19	20	19	17
			QuietIO	26	24	26	24
		8	Fast	N/A	12	N/A	12
			Slow	N/A	15	N/A	13
			QuietIO	N/A	20	N/A	19
		12	Fast	N/A	5	N/A	4
			Slow	N/A	8	N/A	5
			QuietIO	N/A	11	N/A	10

Table 34: **SSO Limit per V_{CCO}/GND Pair *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
Various	LVDS_33			16	N/A	16	N/A
	LVDS_25			20	N/A	20	N/A
	BLVDS_25			20	48	20	20
	MINI_LVDS_33			13	N/A	13	N/A
	MINI_LVDS_25			18	N/A	18	N/A
	RSDS_33			12	N/A	12	N/A
	RSDS_25			15	N/A	15	N/A
	TMDS_33			83	N/A	83	N/A
	PPDS_33			12	N/A	12	N/A
	PPDS_25			16	N/A	16	N/A
	DISPLAY_PORT			42	40	42	30
	I2C			47	55	47	42
	SMBUS			44	52	44	40

Notes:

1. SSO limits greater than the number of I/O per V_{CCO}/GND pair (Table 33) indicate No Limit for the given I/O standard. They are provided in this table to calculate limits when using multiple I/O standards in a bank.
2. Not available (N/A) indicates that the I/O standard is not available in the given bank.
3. When used with the MCB, these signals are exempt from SSO analysis due to the known activity of the MCB switching patterns. SSO performance is validated for all MCB instances. MCB outputs can, in some cases, exceed the SSO limits.

Input Serializer/Deserializer Switching Characteristics

Table 37: **ISERDES2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold for Control Lines						
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.16/ –0.09	0.20/ –0.09	0.31/ –0.09	0.34/ –0.14	ns
T_{ISCCK_CE} / T_{ISCKC_CE}	CE pin Setup/Hold with respect to CLK	0.71/ –0.47	0.71/ –0.42	0.97/ –0.42	1.39/ –0.71	ns
Setup/Hold for Data Lines						
T_{ISDCK_D} /T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.24/ –0.15	0.25/ –0.05	0.29/ –0.05	0.09/ –0.05	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	–0.25/ 0.30	–0.25/ 0.42	–0.25/ 0.56	–0.54/ 0.67	ns
$T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	–0.03/ 0.04	–0.03/ 0.16	–0.03/ 0.18	–0.05/ 0.12	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY2)	–0.40/ 0.48	–0.40/ 0.53	–0.40/ 0.71	–0.71/ 0.86	ns
Sequential Delays						
T_{ISCKO_Q}	CLKDIV to out at Q pin	1.30	1.44	2.02	2.22	ns
F_{CLKDIV}	CLKDIV maximum frequency	270	262.5	250	125	MHz

Output Serializer/Deserializer Switching Characteristics

Table 38: **OSERDES2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	–0.03/ 1.02	–0.03/ 1.17	–0.03/ 1.27	–0.02/ 0.23	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	–0.05/ 1.03	–0.05/ 1.13	–0.05/ 1.23	–0.05/ 0.24	ns
T_{OSCCK_OCE}/T_{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.12/ –0.03	0.15/ –0.03	0.24/ –0.03	0.28/ –0.17	ns
T_{OSCCK_TCE}/T_{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.14/ –0.08	0.17/ –0.08	0.27/ –0.08	0.31/ –0.16	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.94	1.11	1.51	1.89	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.94	1.11	1.51	1.91	ns
F_{CLKDIV}	CLKDIV maximum frequency	270	262.5	250	125	MHz

Notes:

1. T_{OSDCK_T2}/T_{OSCKD_T2} (T input setup/hold with respect to CLKDIV) are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Input/Output Delay Switching Characteristics

Table 39: **IODELAY2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L[3]	
T_{IODCCK_CAL} / T_{IODCKC_CAL}	CAL pin Setup/Hold with respect to CK	0.28/ –0.13	0.33/ –0.13	0.48/ –0.13	N/A	ns
T_{IODCCK_CE} / T_{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.17/ –0.03	0.17/ –0.03	0.25/ –0.02	N/A	ns
T_{IODCCK_INC}/ T_{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.10/ 0.02	0.12/ 0.03	0.18/ 0.06	N/A	ns
T_{IODCCK_RST}/ T_{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.12/ –0.02	0.15/ –0.02	0.22/ –0.01	N/A	ns
T_{TAP1}[2]	Maximum tap 1 delay	8	14	16	N/A	ps
T_{TAP2}	Maximum tap 2 delay	40	66	77	N/A	ps
T_{TAP3}	Maximum tap 3 delay	95	120	140	N/A	ps
T_{TAP4}	Maximum tap 4 delay	108	141	166	N/A	ps
T_{TAP5}	Maximum tap 5 delay	171	194	231	N/A	ps
T_{TAP6}	Maximum tap 6 delay	207	249	292	N/A	ps
T_{TAP7}	Maximum tap 7 delay	212	276	343	N/A	ps
T_{TAP8}	Maximum tap 8 delay	322	341	424	N/A	ps
F_{MINCAL}	Minimum allowed bit rate for calibration in variable mode: VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX, and DIFF_PHASE_DETECTOR.	188	188	188	N/A	Mb/s
$T_{IODDO\_IDATAIN}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	–
$T_{IODDO\_ODATAIN}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	–

Notes:

1. Delay depends on IODELAY2 tap setting. See TRACE report for actual values.
2. Maximum delay = integer (number of taps/8) × T_{TAP8} + T_{TAPn} (where n equals the remainder). For minimum delay consult the TRACE setup and hold report. Minimum delay is typically greater than 30% of the maximum delay. Tap delays can vary by device and overall conditions. See TRACE report for actual values.
3. Spartan-6 -1L devices only support tap 0. See TRACE report for actual values.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 41: **CLB Distributed RAM Switching Characteristics (SLICEM Only)**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Sequential Delays						
T_{SHCKO}	Clock to A – D outputs	1.26	1.55	1.55	2.35	ns, Max
	Clock to A – D outputs (direct output path)	0.96	1.20	1.20	1.87	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS}/T_{DH}	AX – DX or AI – DI inputs to CLK	0.59/ 0.17	0.73/ 0.22	0.73/ 0.22	1.17/ 0.33	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock for XC devices	0.28/ 0.35	0.32/ 0.42	0.32/ 0.42	0.26/ 0.71	ns, Min
	Address An inputs to clock for XA and XQ devices	0.28/ 0.51	N/A	0.32/ 0.51	0.26/ 0.71	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.31/ –0.08	0.37/ –0.08	0.37/ –0.08	0.59/ –0.27	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.31/ –0.08	0.37/ –0.08	0.37/ –0.08	0.59/ –0.27	ns, Min

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 42: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	1.35	1.78	1.78	2.74	ns, Max
	Clock to A – D outputs (direct output path)	1.24	1.65	1.65	2.48	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS}/T_{WH}	WE input to CLK	0.20/ –0.07	0.24/ –0.07	0.24/ –0.07	0.29/ –0.27	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK for XC devices	0.30/ 0.30	0.30/ 0.38	0.30/ 0.38	0.82/ –0.41	ns, Min
	CE input to CLK for XA and XQ devices	0.32/ 0.30	N/A	0.40/ 0.38	0.82/ –0.41	ns, Min
T_{DS}/T_{DH}	AX – DX or AI – DI inputs to CLK	0.07/ 0.11	0.09/ 0.14	0.09/ 0.14	0.11/ 0.23	ns, Min

Spartan-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 63 through Table 69. Values are expressed in nanoseconds unless otherwise noted.

Table 63: **Global Clock Input to Output Delay Without DCM or PLL**

Symbol	**Description**	**Device**	**Speed Grade**				**Units**
			-3	**-3N**	**-2**	**-1L**	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* DCM or PLL							
T_{ICKOF}	Global Clock and OUTFF *without* DCM or PLL	XC6SLX4	6.12	N/A	7.68	9.41	ns
		XC6SLX9	6.12	6.51	7.68	9.41	ns
		XC6SLX16	5.98	6.42	7.48	9.10	ns
		XC6SLX25	6.20	6.69	7.84	9.44	ns
		XC6SLX25T	6.20	6.69	7.84	N/A	ns
		XC6SLX45	6.37	6.88	8.10	9.61	ns
		XC6SLX45T	6.37	6.88	8.10	N/A	ns
		XC6SLX75	6.39	6.99	8.16	10.18	ns
		XC6SLX75T	6.39	6.99	8.16	N/A	ns
		XC6SLX100	6.59	7.18	8.41	10.31	ns
		XC6SLX100T	6.59	7.18	8.41	N/A	ns
		XC6SLX150	6.98	7.68	8.80	10.62	ns
		XC6SLX150T	6.98	7.68	8.80	N/A	ns
		XA6SLX4	6.44	N/A	7.68	N/A	ns
		XA6SLX9	6.44	N/A	7.68	N/A	ns
		XA6SLX16	6.30	N/A	7.48	N/A	ns
		XA6SLX25	6.52	N/A	7.84	N/A	ns
		XA6SLX25T	6.52	N/A	7.84	N/A	ns
		XA6SLX45	6.69	N/A	8.12	N/A	ns
		XA6SLX45T	6.69	N/A	8.12	N/A	ns
		XA6SLX75	6.89	N/A	8.16	N/A	ns
		XA6SLX75T	6.89	N/A	8.16	N/A	ns
		XA6SLX100	N/A	N/A	8.36	N/A	ns
		XQ6SLX75	N/A	N/A	8.16	10.18	ns
		XQ6SLX75T	6.89	N/A	8.16	N/A	ns
		XQ6SLX150	N/A	N/A	8.80	10.62	ns
		XQ6SLX150T	7.61	N/A	8.80	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 64: **Global Clock Input to Output Delay With DCM in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade -3	Speed Grade -3N	Speed Grade -2	Speed Grade -1L	Units
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in System-Synchronous Mode.							
$T_{ICKOFDCM}$	Global Clock and OUTFF *with* DCM	XC6SLX4	4.23	N/A	6.11	6.60	ns
		XC6SLX9	4.23	5.17	6.11	6.60	ns
		XC6SLX16	4.28	4.57	5.34	6.36	ns
		XC6SLX25	3.95	4.18	4.59	6.91	ns
		XC6SLX25T	3.95	4.18	4.59	N/A	ns
		XC6SLX45	4.37	4.70	5.50	6.85	ns
		XC6SLX45T	4.37	4.70	5.50	N/A	ns
		XC6SLX75	3.90	4.23	4.77	6.31	ns
		XC6SLX75T	3.90	4.23	4.77	N/A	ns
		XC6SLX100	3.86	4.16	4.66	7.25	ns
		XC6SLX100T	3.90	4.16	4.66	N/A	ns
		XC6SLX150	4.03	4.33	4.83	6.63	ns
		XC6SLX150T	4.03	4.33	4.83	N/A	ns
		XA6SLX4	4.55	N/A	6.11	N/A	ns
		XA6SLX9	4.55	N/A	6.11	N/A	ns
		XA6SLX16	4.62	N/A	5.33	N/A	ns
		XA6SLX25	4.27	N/A	4.59	N/A	ns
		XA6SLX25T	4.27	N/A	4.69	N/A	ns
		XA6SLX45	4.69	N/A	5.50	N/A	ns
		XA6SLX45T	4.69	N/A	5.50	N/A	ns
		XA6SLX75	4.22	N/A	4.77	N/A	ns
		XA6SLX75T	4.22	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.34	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	6.31	ns
		XQ6SLX75T	4.22	N/A	4.77	N/A	ns
		XQ6SLX150	N/A	N/A	4.96	6.63	ns
		XQ6SLX150T	4.62	N/A	4.96	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 66: **Global Clock Input to Output Delay With PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* PLL in System-Synchronous Mode.							
$T_{ICKOFPLL}$	Global Clock and OUTFF *with* PLL	XC6SLX4	4.57	N/A	6.25	7.34	ns
		XC6SLX9	4.57	5.25	6.25	7.34	ns
		XC6SLX16	4.41	4.64	5.39	6.92	ns
		XC6SLX25	4.03	4.32	4.91	7.64	ns
		XC6SLX25T	4.03	4.32	4.91	N/A	ns
		XC6SLX45	4.63	4.96	5.75	7.36	ns
		XC6SLX45T	4.63	4.96	5.75	N/A	ns
		XC6SLX75	4.01	4.30	4.88	7.15	ns
		XC6SLX75T	4.01	4.30	4.88	N/A	ns
		XC6SLX100	4.02	4.33	4.90	7.37	ns
		XC6SLX100T	4.06	4.33	4.90	N/A	ns
		XC6SLX150	3.65	3.98	4.58	6.94	ns
		XC6SLX150T	3.65	3.98	4.58	N/A	ns
		XA6SLX4	4.88	N/A	6.13	N/A	ns
		XA6SLX9	4.88	N/A	6.13	N/A	ns
		XA6SLX16	4.74	N/A	5.27	N/A	ns
		XA6SLX25	4.43	N/A	4.78	N/A	ns
		XA6SLX25T	4.43	N/A	4.88	N/A	ns
		XA6SLX45	4.94	N/A	5.62	N/A	ns
		XA6SLX45T	4.94	N/A	5.62	N/A	ns
		XA6SLX75	4.32	N/A	4.77	N/A	ns
		XA6SLX75T	4.32	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.41	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	7.15	ns
		XQ6SLX75T	4.32	N/A	4.77	N/A	ns
		XQ6SLX150	N/A	N/A	4.60	6.94	ns
		XQ6SLX150T	4.35	N/A	4.60	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 71: Global Clock Setup and Hold Without DCM or PLL (Default Delay)

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.[1]							
T_{PSFD}/ T_{PHFD}	Default Delay[2] Global Clock and IFF[3] without DCM or PLL	XC6SLX4	0.66/1.17	N/A	1.05/0.79	2.09/1.05	ns
		XC6SLX9	0.66/1.17	0.75/1.17	1.05/1.17	2.09/1.05	ns
		XC6SLX16	0.87/1.16	0.93/1.16	0.96/1.16	1.86/1.06	ns
		XC6SLX25	0.68/0.77	0.81/0.81	0.87/0.82	2.21/1.33	ns
		XC6SLX25T	0.68/0.77	0.81/0.81	0.87/0.82	N/A	ns
		XC6SLX45	0.40/1.05	0.42/1.17	0.64/1.20	1.61/1.67	ns
		XC6SLX45T	0.40/1.05	0.42/1.17	0.64/1.20	N/A	ns
		XC6SLX75	0.41/1.11	0.41/1.13	0.80/1.14	1.23/1.82	ns
		XC6SLX75T	0.41/1.11	0.41/1.13	0.80/1.14	N/A	ns
		XC6SLX100	0.39/1.12	0.39/1.23	0.39/1.28	1.13/1.94	ns
		XC6SLX100T	0.39/1.12	0.39/1.23	0.39/1.28	N/A	ns
		XC6SLX150	0.23/1.54	0.23/1.62	0.23/1.62	1.14/2.05	ns
		XC6SLX150T	0.23/1.54	0.23/1.62	0.23/1.62	N/A	ns
		XA6SLX4	0.73/1.18	N/A	1.05/0.80	N/A	ns
		XA6SLX9	0.73/1.18	N/A	1.05/0.80	N/A	ns
		XA6SLX16	0.90/1.20	N/A	0.96/0.75	N/A	ns
		XA6SLX25	0.70/0.81	N/A	0.87/0.91	N/A	ns
		XA6SLX25T	0.76/0.81	N/A	1.03/0.91	N/A	ns
		XA6SLX45	0.40/1.06	N/A	0.64/1.20	N/A	ns
		XA6SLX45T	0.40/1.06	N/A	0.64/1.20	N/A	ns
		XA6SLX75	0.41/1.24	N/A	0.80/1.18	N/A	ns
		XA6SLX75T	0.41/1.24	N/A	0.80/1.18	N/A	ns
		XA6SLX100	N/A	N/A	0.86/1.55	N/A	ns
		XQ6SLX75	N/A	N/A	0.80/1.18	1.23/1.82	ns
		XQ6SLX75T	0.41/1.24	N/A	0.80/1.18	N/A	ns
		XQ6SLX150	N/A	N/A	0.28/1.57	1.14/2.05	ns
		XQ6SLX150T	0.28/1.78	N/A	0.28/1.57	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Default delay uses IODELAY2 tap 0.
3. IFF = Input Flip-Flop or Latch.

Table 74: Global Clock Setup and Hold With PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSPLL}/ T_{PHPLL}	No Delay Global Clock and IFF(2) with PLL in System-Synchronous Mode	XC6SLX4	1.37/0.25	N/A	1.52/0.41	2.07/0.69	ns
		XC6SLX9	1.37/0.21	1.48/0.21	1.52/0.26	2.07/0.69	ns
		XC6SLX16	1.33/–0.03	1.53/–0.02	1.60/–0.02	1.57/0.48	ns
		XC6SLX25	1.65/0.28	1.71/0.28	1.91/0.28	2.44/0.76	ns
		XC6SLX25T	1.65/0.28	1.71/0.28	1.91/0.28	N/A	ns
		XC6SLX45	1.55/0.18	1.64/0.18	1.75/0.18	2.02/0.90	ns
		XC6SLX45T	1.55/0.18	1.64/0.18	1.75/0.18	N/A	ns
		XC6SLX75	1.77/0.21	1.89/0.21	2.13/0.21	2.46/0.53	ns
		XC6SLX75T	1.77/0.21	1.89/0.21	2.13/0.21	N/A	ns
		XC6SLX100	1.44/0.32	1.52/0.32	1.70/0.32	1.78/0.86	ns
		XC6SLX100T	1.44/0.32	1.52/0.32	1.70/0.32	N/A	ns
		XC6SLX150	1.39/0.49	1.48/0.49	1.67/0.49	1.94/0.94	ns
		XC6SLX150T	1.39/0.49	1.48/0.49	1.67/0.49	N/A	ns
		XA6SLX4	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX9	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX16	1.89/–0.08	N/A	1.72/–0.08	N/A	ns
		XA6SLX25	1.85/0.16	N/A	2.08/0.16	N/A	ns
		XA6SLX25T	1.85/0.16	N/A	2.17/0.16	N/A	ns
		XA6SLX45	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX45T	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX75	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX100	N/A	N/A	2.34/0.14	N/A	ns
		XQ6SLX75	N/A	N/A	2.25/0.06	2.46/0.53	ns
		XQ6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XQ6SLX150	N/A	N/A	1.79/0.37	1.94/0.94	ns
		XQ6SLX150T	1.43/0.37	N/A	1.79/0.37	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 75: **Global Clock Setup and Hold With PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSPLL0}/ T_{PHPLL0}	No Delay Global Clock and IFF(2) with PLL in Source-Synchronous Mode	XC6SLX4	0.47/1.08	N/A	0.47/1.60	1.15/1.68	ns
		XC6SLX9	0.47/1.08	0.47/1.35	0.47/1.60	1.15/1.68	ns
		XC6SLX16	0.37/0.75	0.37/0.82	0.51/0.94	0.57/1.31	ns
		XC6SLX25	0.69/1.06	0.69/1.06	0.69/1.06	1.86/1.67	ns
		XC6SLX25T	0.69/1.06	0.69/1.06	0.69/1.06	N/A	ns
		XC6SLX45	0.57/1.05	0.65/1.10	0.65/1.18	1.02/1.65	ns
		XC6SLX45T	0.57/1.06	0.65/1.10	0.65/1.18	N/A	ns
		XC6SLX75	0.86/1.04	0.87/1.04	0.90/1.04	1.34/1.55	ns
		XC6SLX75T	0.86/1.04	0.87/1.04	0.90/1.04	N/A	ns
		XC6SLX100	0.53/1.13	0.54/1.13	0.55/1.13	0.89/2.39	ns
		XC6SLX100T	0.53/1.13	0.54/1.13	0.55/1.13	N/A	ns
		XC6SLX150	0.50/1.31	0.51/1.31	0.52/1.31	1.02/1.72	ns
		XC6SLX150T	0.50/1.31	0.51/1.31	0.52/1.31	N/A	ns
		XA6SLX4	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX9	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX16	0.92/0.69	N/A	0.63/0.82	N/A	ns
		XA6SLX25	0.99/0.94	N/A	0.96/0.94	N/A	ns
		XA6SLX25T	0.99/0.94	N/A	1.04/0.94	N/A	ns
		XA6SLX45	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX45T	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX75	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX100	N/A	N/A	1.25/0.96	N/A	ns
		XQ6SLX75	N/A	N/A	1.02/0.89	1.34/1.55	ns
		XQ6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XQ6SLX150	N/A	N/A	0.63/1.19	1.02/1.72	ns
		XQ6SLX150T	0.60/1.19	N/A	0.63/1.19	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 76: **Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.[(1)]							
$T_{PSDCMPLL}$/ $T_{PHDCMPLL}$	No Delay Global Clock and IFF[(2)] with DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.	XC6SLX4	1.16/0.49	N/A	1.39/0.49	2.36/0.59	ns
		XC6SLX9	1.16/0.44	1.37/0.44	1.39/0.44	2.36/0.59	ns
		XC6SLX16	1.44/–0.08	1.49/–0.04	1.62/–0.04	2.06/0.55	ns
		XC6SLX25	1.52/0.42	1.65/0.42	1.83/0.42	2.52/0.43	ns
		XC6SLX25T	1.52/0.42	1.65/0.42	1.83/0.42	N/A	ns
		XC6SLX45	1.54/0.39	1.59/0.39	1.75/0.39	2.48/0.76	ns
		XC6SLX45T	1.54/0.39	1.59/0.39	1.75/0.39	N/A	ns
		XC6SLX75	1.72/0.41	1.80/0.41	1.99/0.41	2.60/0.75	ns
		XC6SLX75T	1.72/0.41	1.80/0.41	1.99/0.41	N/A	ns
		XC6SLX100	1.34/0.51	1.46/0.51	1.64/0.51	2.12/0.90	ns
		XC6SLX100T	1.34/0.51	1.46/0.51	1.64/0.51	N/A	ns
		XC6SLX150	1.30/0.60	1.40/0.60	1.55/0.60	2.57/0.97	ns
		XC6SLX150T	1.30/0.60	1.40/0.60	1.55/0.60	N/A	ns
		XA6SLX4	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX9	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX16	2.67/0.35	N/A	2.67/0.17	N/A	ns
		XA6SLX25	1.74/0.27	N/A	1.95/0.27	N/A	ns
		XA6SLX25T	1.74/0.27	N/A	2.03/0.27	N/A	ns
		XA6SLX45	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX45T	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX75	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX100	N/A	N/A	2.64/0.82	N/A	ns
		XQ6SLX75	N/A	N/A	2.11/0.24	2.60/0.75	ns
		XQ6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XQ6SLX150	N/A	N/A	1.67/0.70	2.57/0.97	ns
		XQ6SLX150T	1.50/0.70	N/A	1.67/0.70	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Spartan-6 FPGA source-synchronous transmitter and receiver data-valid windows.

Table 78: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device[1]	Speed Grade				Units
			-3	-3N	-2	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion[2]	LX4	0.20	N/A	0.20	0.35	ns
		LX9	0.20	0.20	0.20	0.35	ns
		LX16	0.20	0.20	0.20	0.35	ns
		LX25	0.20	0.20	0.20	0.35	ns
		LX25T	0.20	0.20	0.20	N/A	ns
		LX45	0.20	0.20	0.20	0.35	ns
		LX45T	0.20	0.20	0.20	N/A	ns
		LX75	0.20	0.20	0.20	0.35	ns
		LX75T	0.20	0.20	0.20	N/A	ns
		LX100	0.20	0.20	0.20	0.35	ns
		LX100T	0.20	0.20	0.20	N/A	ns
		LX150	0.35	0.35	0.35	0.35	ns
		LX150T	0.35	0.35	0.35	N/A	ns
T_{CKSKEW}	Global Clock Tree Skew[3]	LX4	0.25	N/A	0.25	0.29	ns
		LX9	0.25	0.25	0.25	0.29	ns
		LX16	0.15	0.15	0.15	0.22	ns
		LX25	0.26	0.26	0.26	0.41	ns
		LX25T	0.26	0.26	0.26	N/A	ns
		LX45	0.20	0.20	0.20	0.28	ns
		LX45T	0.20	0.20	0.20	N/A	ns
		LX75	0.56	0.56	0.56	0.50	ns
		LX75T	0.56	0.56	0.56	N/A	ns
		XC6SLX100[4]	0.22	0.22	0.22	0.21	ns
		XA6SLX100[4]	N/A	N/A	0.43	N/A	ns
		LX100T	0.22	0.22	0.22	N/A	ns
		LX150	0.48	0.48	0.48	0.35	ns
		LX150T	0.48	0.48	0.48	N/A	ns
T_{DCD_BUFIO2}	I/O clock tree duty cycle distortion	LX devices	0.25	0.25	0.25	0.50	ns
		LXT devices	0.25	0.25	0.25	N/A	ns

Date	Version	Description of Revisions
06/14/10	1.5	In Table 2, added note 5 and added temperature range to V_{FS} and R_{FUSE}. Removed speed grade delineation, revised I_{RPD} description, and updated note 2 in Table 4. Added note 2 to Table 7. Added DIFF_MOBILE_DDR to Table 8 and Table 10. Added note 4 to Table 15. Changed minimum DV_{PPIN} in Table 16. Updated $F_{GTPDRPCLK}$ in Table 19. Increased maximum T_{LLSKEW} in Table 22. Updated descriptions and added data to Table 23. Removed note 1 and added new data to the Networking Applications section in Table 25. Updated Table 26 and Table 27 to the data in ISE v12.1 software with speed specification v1.08. In Table 28, added DIFF_MOBILE_DDR and updated -4 speed grade data. Updated the maximum I/O pairs per bank in Table 33. Updated note 2 on Table 39. Revised the F_{MAX} in Table 44. In Table 47, updated description for $T_{SMCKCSO}$, revised values for T_{POR} and added Min value, added $T_{BPIICCK}$ and $T_{SPIICCK}$. Also in Table 47, added device dependencies to F_{SMCCK} and F_{RBCCK}. Updated and added data to Table 63 through Table 78, and Table 81. In Table 79, added data on the XC6SLX45-FG(G)676 and revised the XC6SLX45T and XC6SLX150T values. The following changes to this specification are addressed in the product change notice XCN10024, *MCB Performance and JTAG Revision Code for Spartan-6 LX16 and LX45 FPGAs*. In Table 2, revised the V_{CCINT} to add the memory controller block extended performance specifications. In Table 25, changed the standard specifications and added extended performance specifications for the memory controller block and note 2. Added note 4 and updated values in Table 34.
06/24/10	1.6	Production release of XC6SLX45T (-2 and -3 speed grades), XC6SLX16 and XC6SLX45 (-3 speed grade) devices which includes changes to Table 26 and Table 27 (ISE v12.1 software with speed specification v1.08). Added the -3N speed grade, which designates Spartan-6 devices that do not support MCB functionality. This includes changes to Table 2 (note 2), Table 25 (note 4), and Switching Characteristics (Table 26). Updated Simultaneously Switching Outputs discussion. Added -3 speed grade values for T_{TAP} and F_{MINCAL} values in Table 39. In Table 40, updated T_{RPW} (-2 and -3 speed grade) values and F_{TOG} (-3 speed grade) values. In Table 48, updated T_{GIO} (-2 and -3 speed grade) values. Updated -3 values in spread spectrum section of Table 57.
07/16/10	1.7	Production release of specific devices listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 4 advising designers of the patch which contains v1.11. Also updated the -1L speed specification to v1.04. Updated numerous -4 and -1L values. Added -4 T_{TAP} values and F_{MINCAL} to Table 39. Revised T_{CINCK}/T_{CKCIN} in Table 40. In Table 41, revised T_{SHCKO}. In Table 42, revised T_{REG}. Added new -1L values to Table 47. Added and updated values in Table 79.
07/26/10	1.8	Production release of XC6SLX25, XC6SLX25T, XC6SLX100 and XC6SLX100T in the specific speed grades listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 7 to Table 2 and moved V_{FS} and R_{FUSE} to a new Table 3. Added I_{HS} and note 4 to Table 4. Added note 1 to Table 28. Added and updated SSO limits per V_{CCO}/GND pairs in Table 34. Added note 3 to Table 47. In Table 54, removed -1L specifications for CLKOUT_PER_JITT_DV1/2 and revised CLKIN_CLKFB_PHASE and CLKOUT_PHASE_DLL values. Updated note 3 in both Table 56 and Table 57.
08/23/10	1.9	Updated values for $F_{GTPRANGE1}$, $F_{GTPRANGE2}$, and $F_{GPLLMIN}$ in Table 18. Revised -3 and -4 values in Table 21. Removed the -1L speed grade readback support restriction and note 3 in Table 47.
11/05/10	1.10	Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.3 software with speed specification v1.12 for the -2 speed grade available in the 12.3 *Speed Files Patch*. Added note 3 advising designers of the patch which contains v1.12. In Table 2, added note 4. In Table 4, added note 2. In Table 10, added notes 2 and 3. In Table 44, added note 2. In Table 47, updated symbol for T_{SMWCCK}/T_{SMCCKW}, changed -1L values for $T_{USERCCLKH}$ and $T_{USERCCLKL}$, and added and revised the modes for F_{MCCK} and F_{SMCCK}. In Table 53, redefined and expanded description for CLKIN_FREQ_DLL and rewrote note 3. Updated title of Table 58. Also in Table 78, revised T_{DCD_CLK} for XC6SLX150 and XC6SLX150T. Changed description of T_{PSFD}/ T_{PHFD} in Table 71. For the -1L speed grade, updated data sheet to ISE 12.3 software with speed specification v1.05 which revised the values in the following tables: Table 25, Table 28, Table 35, Table 36, Table 37, Table 40 through Table 43, Table 48 through Table 56, Table 62 through Table 78, Table 80, and Table 81. Updated Notice of Disclaimer.

Date	Version	Description of Revisions
09/14/11	2.4	Production release of the XA6SLX4 and XA6SLX9 devices in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added production released version of the XA6SLX100 to Table 26 and Table 27 using ISE v13.3 software with -2 speed specification v1.20. Updated R_{OUT_TERM} description in Table 4. Fixed the LVPECL V_H error in Table 31. Updated introduction in Simultaneously Switching Outputs. Added the XA6SLX100 to Table 63 through Table 78, and Table 81. Added Note 4 to Table 78 because the T_{CKSKEW} for the XC6SLX100 is not the same as the T_{CKSKEW} for the XA6SLX100. Revised the revision history for version 1.6 dated 06/24/10. Removed the parenthetical statement about the -3N speed grade: (specifications are identical to the -3 speed grade).
10/17/11	3.0	Changed the data sheet from Preliminary Product Specification to Product Specification. Updated the Switching Characteristics, page 19 speed specification version ISE v13.3 software to -2 and -3 speed specification v1.20 and -1L speed specification of v1.08. Also updated Note 1 in Table 27. In Table 43, *Block RAM Switching Characteristics*, the F_{MAX} value for the -2 speed grade has been changed from 260 MHz to 280 MHz. In Table 54, *Switching Characteristics for the DLL*, a Note 6 was added and linked to CLKIN_CLKFB_PHASE.