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### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### **Details**

Product Status	Obsolete
Number of LABs/CLBs	7911
Number of Logic Elements/Cells	101261
Total RAM Bits	4939776
Number of I/O	296
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xc6slx100t-n3fg484c">https://www.e-xfl.com/product-detail/xilinx/xc6slx100t-n3fg484c</a>

Table 1: Absolute Maximum Ratings<sup>(1)</sup> (Cont'd)

Symbol	Description			Units
$V_{IN}$ and $V_{TS}^{(3)}$	I/O input voltage or voltage applied to 3-state output, relative to GND <sup>(4)</sup> All user and dedicated I/Os	Commercial	DC	-0.60 to 4.10
			20% overshoot duration	-0.75 to 4.25
			8% overshoot duration <sup>(5)</sup>	-0.75 to 4.40
		Industrial	DC	-0.60 to 3.95
			20% overshoot duration	-0.75 to 4.15
			4% overshoot duration <sup>(5)</sup>	-0.75 to 4.40
		Expanded (Q)	DC	-0.60 to 3.95
			20% overshoot duration	-0.75 to 4.15
			4% overshoot duration <sup>(5)</sup>	-0.75 to 4.40
		Commercial	20% overshoot duration	-0.75 to 4.35
			15% overshoot duration <sup>(5)</sup>	-0.75 to 4.40
			10% overshoot duration	-0.75 to 4.45
		Industrial	20% overshoot duration	-0.75 to 4.25
			10% overshoot duration	-0.75 to 4.35
			8% overshoot duration <sup>(5)</sup>	-0.75 to 4.40
		Expanded (Q)	20% overshoot duration	-0.75 to 4.25
			10% overshoot duration	-0.75 to 4.35
			8% overshoot duration <sup>(5)</sup>	-0.75 to 4.40
$T_{STG}$	Storage temperature (ambient)			-65 to 150
$T_{SOL}$	Maximum soldering temperature <sup>(6)</sup> (TQG144, CPG196, CSG225, CSG324, CSG484, and FTG256)			+260
	Maximum soldering temperature <sup>(6)</sup> (Pb-free packages: FGG484, FGG676, and FGG900)			+250
	Maximum soldering temperature <sup>(6)</sup> (Pb packages: CS484, FT256, FG484, FG676, and FG900)			+220
$T_j$	Maximum junction temperature <sup>(6)</sup>			+125

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- When programming eFUSE,  $V_{FS} \leq V_{CCAUX}$ . Requires up to 40 mA current. For read mode,  $V_{FS}$  can be between GND and 3.45 V.
- I/O absolute maximum limit applied to DC and AC signals. Overshoot duration is the percentage of a data period that the I/O is stressed beyond 3.45V.
- For I/O operation, refer to [UG381: Spartan-6 FPGA SelectIO Resources User Guide](#).
- Maximum percent overshoot duration to meet 4.40V maximum.
- For soldering guidelines and thermal considerations, see [UG385: Spartan-6 FPGA Packaging and Pinout Specification](#).

## Quiescent Current

Typical values for quiescent supply current are specified at nominal voltage, 25°C junction temperatures ( $T_j$ ). Quiescent supply current is specified by speed grade for Spartan-6 devices. Xilinx recommends analyzing static power consumption using the XPOWER™ Estimator (XPE) tool (download at <http://www.xilinx.com/power>) for conditions other than those specified in Table 5.

Table 5: Typical Quiescent Supply Current

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
$I_{CCINTQ}$	Quiescent $V_{CCINT}$ supply current	LX4	4.0	4.0	4.0	2.4	mA
		LX9	4.0	4.0	4.0	2.4	mA
		LX16	6.0	6.0	6.0	4.0	mA
		LX25	11.0	11.0	11.0	6.6	mA
		LX25T	11.0	11.0	11.0	N/A	mA
		LX45	15.0	15.0	15.0	9.0	mA
		LX45T	15.0	15.0	15.0	N/A	mA
		LX75	29.0	29.0	29.0	17.4	mA
		LX75T	29.0	29.0	29.0	N/A	mA
		LX100	36.0	36.0	36.0	21.6	mA
		LX100T	36.0	36.0	36.0	N/A	mA
		LX150	51.0	51.0	51.0	31.0	mA
		LX150T	51.0	51.0	51.0	N/A	mA
$I_{CCOQ}$	Quiescent $V_{CCO}$ supply current	LX4	1.0	1.0	1.0	1.0	mA
		LX9	1.0	1.0	1.0	1.0	mA
		LX16	2.0	2.0	2.0	2.0	mA
		LX25	2.0	2.0	2.0	2.0	mA
		LX25T	2.0	2.0	2.0	N/A	mA
		LX45	3.0	3.0	3.0	3.0	mA
		LX45T	3.0	3.0	3.0	N/A	mA
		LX75	4.0	4.0	4.0	4.0	mA
		LX75T	4.0	4.0	4.0	N/A	mA
		LX100	5.0	5.0	5.0	5.0	mA
		LX100T	5.0	5.0	5.0	N/A	mA
		LX150	7.0	7.0	7.0	7.0	mA
		LX150T	7.0	7.0	7.0	N/A	mA

## SelectIO™ Interface DC Input and Output Levels

Table 7: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

I/O Standard	$V_{CCO}$ for Drivers <sup>(1)</sup>			$V_{REF}$ for Inputs		
	$V$ , Min	$V$ , Nom	$V$ , Max	$V$ , Min	$V$ , Nom	$V$ , Max
LV TTL	3.0	3.3	3.45			
LVC MOS33	3.0	3.3	3.45			
LVC MOS25	2.3	2.5	2.7			
LVC MOS18	1.65	1.8	1.95			
LVC MOS18_JEDEC	1.65	1.8	1.95			
LVC MOS15	1.4	1.5	1.6			
LVC MOS15_JEDEC	1.4	1.5	1.6			
LVC MOS12	1.1	1.2	1.3			
LVC MOS12_JEDEC	1.1	1.2	1.3			
PCI33_3 <sup>(2)</sup>	3.0	3.3	3.45			
PCI66_3 <sup>(2)</sup>	3.0	3.3	3.45			
I2C	2.7	3.0	3.45			
SMBUS	2.7	3.0	3.45			
SDIO	3.0	3.3	3.45			
MOBILE_DDR	1.7	1.8	1.9			
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_II	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_III	1.4	1.5	1.6	–	0.9	–
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–
HSTL_III_18	1.7	1.8	1.9	–	1.1	–
SSTL3_I	3.0	3.3	3.45	1.3	1.5	1.7
SSTL3_II	3.0	3.3	3.45	1.3	1.5	1.7
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38
SSTL18_I	1.7	1.8	1.9	0.833	0.9	0.969
SSTL18_II	1.7	1.8	1.9	0.833	0.9	0.969
SSTL15_II	1.425	1.5	1.575	0.69	0.75	0.81

**Notes:**

- $V_{CCO}$  range required when using I/O standard for an output. Also required for MOBILE\_DDR, PCI33\_3, LVC MOS18\_JEDEC, LVC MOS15\_JEDEC, and LVC MOS12\_JEDEC inputs, and for LVC MOS25 inputs when  $V_{CCAUX} = 3.3V$ .
- For PCI systems, the transmitter and receiver should have common supplies for  $V_{CCO}$ .

Table 27: Spartan-6 Device Production Software and Speed Specification Release<sup>(1)</sup> (Cont'd)

Device	Speed Grade Designations <sup>(2)</sup>			
	-3 <sup>(3)</sup>	-3N	-2 <sup>(4)</sup>	-1L
XQ6SLX75	N/A	N/A	ISE 13.2 v1.19	ISE 13.2 v1.07
XQ6SLX75T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XQ6SLX150	N/A	N/A	ISE 13.2 v1.19	ISE 13.2 v1.07
XQ6SLX150T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A

**Notes:**

1. ISE 13.3 software with v1.20 for -3, -3N, and -2; and v1.08 for -1L speed specification reflects the changes outlined in [XCN11028: Spartan-6 FPGA Speed File Changes](#).
2. As marked with an N/A, LXT devices and all XA devices are not available with a -1L speed grade; LX4 devices and all XA and XQ devices are not available with a -3N speed grade.
3. Improved -3 specifications reflected in this data sheet require ISE 12.4 software with v1.15 speed specification.
4. Improved -2 specifications reflected in this data sheet require ISE 12.4 software and the *12.4 Speed Files Patch* which contains the v1.17 speed specification available on the [Xilinx Download Center](#).
5. ISE 12.3 software with v1.12 speed specification is available using ISE 12.3 software and the *12.3 Speed Files Patch* available on the [Xilinx Download Center](#).
6. ISE 12.2 software with v1.11 speed specification is available using ISE 12.2 software and the *12.2 Speed Files Patch* available on the [Xilinx Download Center](#).
7. ISE 13.1 software with v1.18 speed specification is available using ISE 13.1 software and the *13.1 Update* available on the [Xilinx Download Center](#). See [XCN11012: Speed File Change for -3N Devices](#).

**IOB Pad Input/Output/3-State Switching Characteristics**

**Table 28** (for commercial (XC) Spartan-6 devices) and **Table 29** (for Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices) summarizes the values of standard-specific data input delays, output delays terminating at pads (based on standard), and 3-state delays.

- $T_{IOPI}$  is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{IOOP}$  is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{IOTP}$  is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

See the TRACE report for further information on delays when using an I/O standard with UNTUNED termination on inputs or outputs.

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices

I/O Standard	$T_{IOPI}$				$T_{IOOP}$				$T_{IOTP}$				Units	
	Speed Grade				Speed Grade				Speed Grade					
	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>		
LVDS_33	1.17	1.29	1.42	1.68	1.55	1.69	1.89	2.42	3000	3000	3000	3000	ns	
LVDS_25	1.01	1.13	1.26	1.57	1.65	1.79	1.99	2.47	3000	3000	3000	3000	ns	
BLVDS_25	1.02	1.14	1.27	1.57	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns	
MINI_LVDS_33	1.17	1.29	1.42	1.68	1.57	1.71	1.91	2.41	3000	3000	3000	3000	ns	
MINI_LVDS_25	1.01	1.13	1.26	1.57	1.65	1.79	1.99	2.47	3000	3000	3000	3000	ns	
LVPECL_33	1.18	1.30	1.43	1.68	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns	
LVPECL_25	1.02	1.14	1.27	1.57	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns	
RSDS_33 (point to point)	1.17	1.29	1.42	1.68	1.57	1.71	1.91	2.42	3000	3000	3000	3000	ns	
RSDS_25 (point to point)	1.01	1.13	1.26	1.56	1.65	1.79	1.99	2.47	3000	3000	3000	3000	ns	
TMDS_33	1.21	1.33	1.46	1.71	1.54	1.68	1.88	2.50	3000	3000	3000	3000	ns	

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T <sub>IOP</sub>				T <sub>IOPP</sub>				T <sub>IOTP</sub>				Units	
	Speed Grade				Speed Grade				Speed Grade					
	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>		
PPDS_33	1.17	1.29	1.42	1.68	1.57	1.71	1.91	2.43	3000	3000	3000	3000	ns	
PPDS_25	1.01	1.13	1.26	1.56	1.68	1.82	2.02	2.47	3000	3000	3000	3000	ns	
PCI33_3	1.07	1.19	1.32	1.57 <sup>(2)</sup>	3.51	3.65	3.85	4.38 <sup>(2)</sup>	3.51	3.65	3.85	4.38 <sup>(1)</sup>	ns	
PCI66_3	1.07	1.19	1.32	1.57 <sup>(2)</sup>	3.53	3.67	3.87	4.39 <sup>(2)</sup>	3.53	3.67	3.87	4.39 <sup>(1)</sup>	ns	
DISPLAY_PORT	1.02	1.14	1.27	1.56	3.15	3.29	3.49	4.08	3.15	3.29	3.49	4.08	ns	
I2C	1.33	1.45	1.58	1.82	11.56	11.70	11.90	12.52	11.56	11.70	11.90	12.52	ns	
SMBUS	1.33	1.45	1.58	1.82	11.56	11.70	11.90	12.52	11.56	11.70	11.90	12.52	ns	
SDIO	1.36	1.48	1.61	1.84	2.64	2.78	2.98	3.60	2.64	2.78	2.98	3.60	ns	
MOBILE_DDR	0.94	1.06	1.19	1.43	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns	
HSTL_I	0.90	1.02	1.15	1.39	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns	
HSTL_II	0.91	1.03	1.16	1.40	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns	
HSTL_III	0.95	1.07	1.20	1.44	1.67	1.81	2.01	2.61	1.67	1.81	2.01	2.61	ns	
HSTL_I_18	0.94	1.06	1.19	1.43	1.77	1.91	2.11	2.73	1.77	1.91	2.11	2.73	ns	
HSTL_II_18	0.94	1.06	1.19	1.43	1.85	1.99	2.19	2.81	1.85	1.99	2.19	2.81	ns	
HSTL_III_18	0.99	1.11	1.24	1.47	1.79	1.93	2.13	2.72	1.79	1.93	2.13	2.72	ns	
SSTL3_I	1.58	1.70	1.83	2.16	1.83	1.97	2.17	2.72	1.83	1.97	2.17	2.72	ns	
SSTL3_II	1.58	1.70	1.83	2.16	2.01	2.15	2.35	2.94	2.01	2.15	2.35	2.94	ns	
SSTL2_I	1.30	1.42	1.55	1.87	1.77	1.91	2.11	2.69	1.77	1.91	2.11	2.69	ns	
SSTL2_II	1.30	1.42	1.55	1.88	1.86	2.00	2.20	2.82	1.86	2.00	2.20	2.82	ns	
SSTL18_I	0.92	1.04	1.17	1.41	1.63	1.77	1.97	2.59	1.63	1.77	1.97	2.59	ns	
SSTL18_II	0.92	1.04	1.17	1.41	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns	
SSTL15_II	0.92	1.04	1.17	1.41	1.67	1.81	2.01	2.63	1.67	1.81	2.01	2.63	ns	
DIFF_HSTL_I	0.94	1.06	1.19	1.46	1.77	1.91	2.11	2.62	1.77	1.91	2.11	2.62	ns	
DIFF_HSTL_II	0.93	1.05	1.18	1.45	1.72	1.86	2.06	2.54	1.72	1.86	2.06	2.54	ns	
DIFF_HSTL_III	0.93	1.05	1.18	1.46	1.69	1.83	2.03	2.53	1.69	1.83	2.03	2.53	ns	
DIFF_HSTL_I_18	0.97	1.09	1.22	1.50	1.79	1.93	2.13	2.63	1.79	1.93	2.13	2.63	ns	
DIFF_HSTL_II_18	0.97	1.09	1.22	1.49	1.69	1.83	2.03	2.51	1.69	1.83	2.03	2.51	ns	
DIFF_HSTL_III_18	0.97	1.09	1.22	1.50	1.69	1.83	2.03	2.53	1.69	1.83	2.03	2.53	ns	
DIFF_SSTL3_I	1.18	1.30	1.43	1.68	1.81	1.95	2.15	2.64	1.81	1.95	2.15	2.64	ns	
DIFF_SSTL3_II	1.19	1.31	1.44	1.68	1.80	1.94	2.14	2.63	1.80	1.94	2.14	2.63	ns	
DIFF_SSTL2_I	1.02	1.14	1.27	1.57	1.80	1.94	2.14	2.62	1.80	1.94	2.14	2.62	ns	
DIFF_SSTL2_II	1.02	1.14	1.27	1.57	1.76	1.90	2.10	2.57	1.76	1.90	2.10	2.57	ns	
DIFF_SSTL18_I	0.97	1.09	1.22	1.51	1.72	1.86	2.06	2.56	1.72	1.86	2.06	2.56	ns	
DIFF_SSTL18_II	0.98	1.10	1.23	1.50	1.68	1.82	2.02	2.52	1.68	1.82	2.02	2.52	ns	
DIFF_SSTL15_II	0.94	1.06	1.19	1.46	1.67	1.81	2.01	2.50	1.67	1.81	2.01	2.50	ns	
DIFF_MOBILE_DDR	0.97	1.09	1.22	1.51	1.75	1.89	2.09	2.57	1.75	1.89	2.09	2.57	ns	

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T <sub>IOPI</sub>				T <sub>IOOP</sub>				T <sub>IOTP</sub>				Units	
	Speed Grade				Speed Grade				Speed Grade					
	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>		
LVCMOS33, Fast, 8 mA	1.34	1.46	1.59	1.82	2.07	2.21	2.41	3.03	2.07	2.21	2.41	3.03	ns	
LVCMOS33, Fast, 12 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns	
LVCMOS33, Fast, 16 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns	
LVCMOS33, Fast, 24 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns	
LVCMOS25, QUIETIO, 2 mA	0.82	0.94	1.07	1.31	4.81	4.95	5.15	5.79	4.81	4.95	5.15	5.79	ns	
LVCMOS25, QUIETIO, 4 mA	0.82	0.94	1.07	1.31	3.70	3.84	4.04	4.66	3.70	3.84	4.04	4.66	ns	
LVCMOS25, QUIETIO, 6 mA	0.82	0.94	1.07	1.31	3.46	3.60	3.80	4.38	3.46	3.60	3.80	4.38	ns	
LVCMOS25, QUIETIO, 8 mA	0.82	0.94	1.07	1.31	3.20	3.34	3.54	4.12	3.20	3.34	3.54	4.12	ns	
LVCMOS25, QUIETIO, 12 mA	0.82	0.94	1.07	1.31	2.83	2.97	3.17	3.75	2.83	2.97	3.17	3.75	ns	
LVCMOS25, QUIETIO, 16 mA	0.82	0.94	1.07	1.31	2.64	2.78	2.98	3.64	2.64	2.78	2.98	3.64	ns	
LVCMOS25, QUIETIO, 24 mA	0.82	0.94	1.07	1.31	2.45	2.59	2.79	3.42	2.45	2.59	2.79	3.42	ns	
LVCMOS25, Slow, 2 mA	0.82	0.94	1.07	1.31	3.78	3.92	4.12	4.76	3.78	3.92	4.12	4.76	ns	
LVCMOS25, Slow, 4 mA	0.82	0.94	1.07	1.31	2.79	2.93	3.13	3.73	2.79	2.93	3.13	3.73	ns	
LVCMOS25, Slow, 6 mA	0.82	0.94	1.07	1.31	2.73	2.87	3.07	3.66	2.73	2.87	3.07	3.66	ns	
LVCMOS25, Slow, 8 mA	0.82	0.94	1.07	1.31	2.48	2.62	2.82	3.42	2.48	2.62	2.82	3.42	ns	
LVCMOS25, Slow, 12 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.95	2.01	2.15	2.35	2.95	ns	
LVCMOS25, Slow, 16 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.95	2.01	2.15	2.35	2.95	ns	
LVCMOS25, Slow, 24 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.94	2.01	2.15	2.35	2.94	ns	
LVCMOS25, Fast, 2 mA	0.82	0.94	1.07	1.31	3.35	3.49	3.69	4.31	3.35	3.49	3.69	4.31	ns	
LVCMOS25, Fast, 4 mA	0.82	0.94	1.07	1.31	2.25	2.39	2.59	3.22	2.25	2.39	2.59	3.22	ns	
LVCMOS25, Fast, 6 mA	0.82	0.94	1.07	1.31	2.09	2.23	2.43	3.05	2.09	2.23	2.43	3.05	ns	
LVCMOS25, Fast, 8 mA	0.82	0.94	1.07	1.31	2.02	2.16	2.36	2.98	2.02	2.16	2.36	2.98	ns	
LVCMOS25, Fast, 12 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns	
LVCMOS25, Fast, 16 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns	
LVCMOS25, Fast, 24 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns	
LVCMOS18, QUIETIO, 2 mA	1.18	1.30	1.43	2.04	5.92	6.06	6.26	6.80	5.92	6.06	6.26	6.80	ns	
LVCMOS18, QUIETIO, 4 mA	1.18	1.30	1.43	2.04	4.74	4.88	5.08	5.63	4.74	4.88	5.08	5.63	ns	
LVCMOS18, QUIETIO, 6 mA	1.18	1.30	1.43	2.04	4.05	4.19	4.39	4.96	4.05	4.19	4.39	4.96	ns	
LVCMOS18, QUIETIO, 8 mA	1.18	1.30	1.43	2.04	3.71	3.85	4.05	4.63	3.71	3.85	4.05	4.63	ns	
LVCMOS18, QUIETIO, 12 mA	1.18	1.30	1.43	2.04	3.35	3.49	3.69	4.27	3.35	3.49	3.69	4.27	ns	
LVCMOS18, QUIETIO, 16 mA	1.18	1.30	1.43	2.04	3.20	3.34	3.54	4.14	3.20	3.34	3.54	4.14	ns	
LVCMOS18, QUIETIO, 24 mA	1.18	1.30	1.43	2.04	2.96	3.10	3.30	3.98	2.96	3.10	3.30	3.98	ns	
LVCMOS18, Slow, 2 mA	1.18	1.30	1.43	2.04	4.62	4.76	4.96	5.54	4.62	4.76	4.96	5.54	ns	
LVCMOS18, Slow, 4 mA	1.18	1.30	1.43	2.04	3.69	3.83	4.03	4.60	3.69	3.83	4.03	4.60	ns	
LVCMOS18, Slow, 6 mA	1.18	1.30	1.43	2.04	3.00	3.14	3.34	3.94	3.00	3.14	3.34	3.94	ns	
LVCMOS18, Slow, 8 mA	1.18	1.30	1.43	2.04	2.19	2.33	2.53	3.17	2.19	2.33	2.53	3.17	ns	
LVCMOS18, Slow, 12 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns	
LVCMOS18, Slow, 16 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns	

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices<sup>(1)</sup> (Cont'd)

I/O Standard	T <sub>IOP1</sub>		T <sub>IOOP</sub>		T <sub>IOTP</sub>		Units	
	Speed Grade		Speed Grade		Speed Grade			
	-3	-2	-3	-2	-3	-2		
DIFF_SSTL3_I	1.26	1.44	1.95	2.15	1.95	2.15	ns	
DIFF_SSTL3_II	1.26	1.44	1.94	2.14	1.94	2.14	ns	
DIFF_SSTL2_I	1.09	1.27	1.94	2.14	1.94	2.14	ns	
DIFF_SSTL2_II	1.09	1.27	1.90	2.10	1.90	2.10	ns	
DIFF_SSTL18_I	1.04	1.22	1.86	2.06	1.86	2.06	ns	
DIFF_SSTL18_II	1.05	1.23	1.82	2.02	1.82	2.02	ns	
DIFF_SSTL15_II	1.01	1.19	1.81	2.01	1.81	2.01	ns	
DIFF_MOBILE_DDR	1.04	1.22	1.89	2.09	1.89	2.09	ns	
LVTTL, QUIETIO, 2 mA	1.42	1.60	5.64	5.84	5.64	5.84	ns	
LVTTL, QUIETIO, 4 mA	1.42	1.60	4.46	4.66	4.46	4.66	ns	
LVTTL, QUIETIO, 6 mA	1.42	1.60	3.92	4.12	3.92	4.12	ns	
LVTTL, QUIETIO, 8 mA	1.42	1.60	3.37	3.57	3.37	3.57	ns	
LVTTL, QUIETIO, 12 mA	1.42	1.60	3.42	3.62	3.42	3.62	ns	
LVTTL, QUIETIO, 16 mA	1.42	1.60	3.09	3.29	3.09	3.29	ns	
LVTTL, QUIETIO, 24 mA	1.42	1.60	2.83	3.03	2.83	3.03	ns	
LVTTL, Slow, 2 mA	1.42	1.60	4.58	4.78	4.58	4.78	ns	
LVTTL, Slow, 4 mA	1.42	1.60	3.38	3.58	3.38	3.58	ns	
LVTTL, Slow, 6 mA	1.42	1.60	2.95	3.15	2.95	3.15	ns	
LVTTL, Slow, 8 mA	1.42	1.60	2.73	2.93	2.73	2.93	ns	
LVTTL, Slow, 12 mA	1.42	1.60	2.72	2.92	2.72	2.92	ns	
LVTTL, Slow, 16 mA	1.42	1.60	2.53	2.73	2.53	2.73	ns	
LVTTL, Slow, 24 mA	1.42	1.60	2.42	2.62	2.42	2.62	ns	
LVTTL, Fast, 2 mA	1.42	1.60	4.04	4.24	4.04	4.24	ns	
LVTTL, Fast, 4 mA	1.42	1.60	2.66	2.86	2.66	2.86	ns	
LVTTL, Fast, 6 mA	1.42	1.60	2.58	2.78	2.58	2.78	ns	
LVTTL, Fast, 8 mA	1.42	1.60	2.46	2.66	2.46	2.66	ns	
LVTTL, Fast, 12 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns	
LVTTL, Fast, 16 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns	
LVTTL, Fast, 24 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns	
LVCMOS33, QUIETIO, 2 mA	1.41	1.59	5.65	5.85	5.65	5.85	ns	
LVCMOS33, QUIETIO, 4 mA	1.41	1.59	4.20	4.40	4.20	4.40	ns	
LVCMOS33, QUIETIO, 6 mA	1.41	1.59	3.65	3.85	3.65	3.85	ns	
LVCMOS33, QUIETIO, 8 mA	1.41	1.59	3.51	3.71	3.51	3.71	ns	
LVCMOS33, QUIETIO, 12 mA	1.41	1.59	3.09	3.29	3.09	3.29	ns	
LVCMOS33, QUIETIO, 16 mA	1.41	1.59	2.91	3.11	2.91	3.11	ns	
LVCMOS33, QUIETIO, 24 mA	1.41	1.59	2.73	2.93	2.73	2.93	ns	
LVCMOS33, Slow, 2 mA	1.41	1.59	4.59	4.79	4.59	4.79	ns	
LVCMOS33, Slow, 4 mA	1.41	1.59	3.14	3.34	3.14	3.34	ns	

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices<sup>(1)</sup> (Cont'd)

I/O Standard	T <sub>IOP1</sub>		T <sub>IOOP</sub>		T <sub>IOTP</sub>		Units	
	Speed Grade		Speed Grade		Speed Grade			
	-3	-2	-3	-2	-3	-2		
LVCMOS18, QUIETIO, 16 mA	1.25	1.43	3.34	3.54	3.34	3.54	ns	
LVCMOS18, QUIETIO, 24 mA	1.25	1.43	3.18	3.38	3.18	3.38	ns	
LVCMOS18, Slow, 2 mA	1.25	1.43	4.79	4.99	4.79	4.99	ns	
LVCMOS18, Slow, 4 mA	1.25	1.43	3.84	4.04	3.84	4.04	ns	
LVCMOS18, Slow, 6 mA	1.25	1.43	3.17	3.37	3.17	3.37	ns	
LVCMOS18, Slow, 8 mA	1.25	1.43	2.37	2.57	2.37	2.57	ns	
LVCMOS18, Slow, 12 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns	
LVCMOS18, Slow, 16 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns	
LVCMOS18, Slow, 24 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns	
LVCMOS18, Fast, 2 mA	1.25	1.43	3.78	3.98	3.78	3.98	ns	
LVCMOS18, Fast, 4 mA	1.25	1.43	2.54	2.74	2.54	2.74	ns	
LVCMOS18, Fast, 6 mA	1.25	1.43	2.02	2.22	2.02	2.22	ns	
LVCMOS18, Fast, 8 mA	1.25	1.43	1.95	2.15	1.95	2.15	ns	
LVCMOS18, Fast, 12 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns	
LVCMOS18, Fast, 16 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns	
LVCMOS18, Fast, 24 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns	
LVCMOS18_JEDEC, QUIETIO, 2 mA	1.01	1.19	6.09	6.29	6.09	6.29	ns	
LVCMOS18_JEDEC, QUIETIO, 4 mA	1.01	1.19	4.89	5.09	4.89	5.09	ns	
LVCMOS18_JEDEC, QUIETIO, 6 mA	1.01	1.19	4.20	4.40	4.20	4.40	ns	
LVCMOS18_JEDEC, QUIETIO, 8 mA	1.01	1.19	3.87	4.07	3.87	4.07	ns	
LVCMOS18_JEDEC, QUIETIO, 12 mA	1.01	1.19	3.49	3.69	3.49	3.69	ns	
LVCMOS18_JEDEC, QUIETIO, 16 mA	1.01	1.19	3.34	3.54	3.34	3.54	ns	
LVCMOS18_JEDEC, QUIETIO, 24 mA	1.01	1.19	3.17	3.37	3.17	3.37	ns	
LVCMOS18_JEDEC, Slow, 2 mA	1.01	1.19	4.79	4.99	4.79	4.99	ns	
LVCMOS18_JEDEC, Slow, 4 mA	1.01	1.19	3.84	4.04	3.84	4.04	ns	
LVCMOS18_JEDEC, Slow, 6 mA	1.01	1.19	3.18	3.38	3.18	3.38	ns	
LVCMOS18_JEDEC, Slow, 8 mA	1.01	1.19	2.37	2.57	2.37	2.57	ns	
LVCMOS18_JEDEC, Slow, 12 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns	
LVCMOS18_JEDEC, Slow, 16 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns	
LVCMOS18_JEDEC, Slow, 24 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns	
LVCMOS18_JEDEC, Fast, 2 mA	1.01	1.19	3.75	3.95	3.75	3.95	ns	
LVCMOS18_JEDEC, Fast, 4 mA	1.01	1.19	2.54	2.74	2.54	2.74	ns	
LVCMOS18_JEDEC, Fast, 6 mA	1.01	1.19	2.02	2.22	2.02	2.22	ns	
LVCMOS18_JEDEC, Fast, 8 mA	1.01	1.19	1.94	2.14	1.94	2.14	ns	
LVCMOS18_JEDEC, Fast, 12 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns	
LVCMOS18_JEDEC, Fast, 16 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns	
LVCMOS18_JEDEC, Fast, 24 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns	

Table 34: SSO Limit per V<sub>CCO</sub>/GND Pair (Cont'd)

V <sub>CCO</sub>	I/O Standard	Drive	Slew	SSO Limit per V <sub>CCO</sub> /GND Pair					
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324			
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5		
1.5V	LVCMOS15, LVCMOS15_JEDEC	2	Fast	33	40	33	41		
			Slow	57	62	57	56		
			QuietIO	70	67	70	66		
		4	Fast	19	21	19	21		
			Slow	30	30	30	24		
			QuietIO	38	33	38	30		
		6	Fast	14	16	14	16		
			Slow	18	19	18	17		
			QuietIO	27	24	27	21		
		8	Fast	11	13	11	12		
			Slow	16	16	16	14		
			QuietIO	23	20	23	17		
		12	Fast	N/A	5	N/A	4		
			Slow	N/A	8	N/A	5		
			QuietIO	N/A	10	N/A	9		
		16	Fast	N/A	5	N/A	4		
			Slow	N/A	8	N/A	8		
			QuietIO	N/A	10	N/A	9		
HSTL_I				9	10	9	10		
HSTL_II				N/A	5	N/A	6		
HSTL_III				7	9	7	9		
DIFF_HSTL_I				27	30	27	30		
DIFF_HSTL_II				N/A	15	N/A	18		
DIFF_HSTL_III				21	27	21	27		
SSTL_15_II <sup>(3)</sup>				N/A	5	N/A	4		
DIFF_SSTL_15_II <sup>(3)</sup>				N/A	15	N/A	12		

Table 34: SSO Limit per V<sub>CCO</sub>/GND Pair (Cont'd)

V <sub>CCO</sub>	I/O Standard	Drive	Slew	SSO Limit per V <sub>CCO</sub> /GND Pair					
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324			
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5		
1.8V	LVCMOS18, LVCMOS18_JEDEC	2	Fast	39	46	39	47		
			Slow	65	75	65	74		
			QuietIO	80	80	80	85		
		4	Fast	22	25	22	25		
			Slow	38	36	38	29		
			QuietIO	45	40	45	35		
		6	Fast	16	18	16	17		
			Slow	27	25	27	19		
			QuietIO	30	28	30	23		
		8	Fast	13	15	13	14		
			Slow	16	18	16	16		
			QuietIO	25	22	25	18		
		12	Fast	5	7	5	5		
			Slow	7	8	7	6		
			QuietIO	11	10	11	8		
		16	Fast	4	5	4	4		
			Slow	7	8	7	5		
			QuietIO	11	10	11	8		
		24	Fast	N/A	5	N/A	3		
			Slow	N/A	8	N/A	8		
			QuietIO	N/A	10	N/A	8		
HSTL_I_18				9	10	9	9		
HSTL_II_18				N/A	5	N/A	6		
HSTL_III_18				9	10	9	11		
DIFF_HSTL_I_18				27	30	27	27		
DIFF_HSTL_II_18				N/A	15	N/A	18		
DIFF_HSTL_III_18				27	30	27	33		
MOBILE_DDR (3)				12	14	12	14		
DIFF_MOBILE_DDR (3)				36	42	36	42		
SSTL_18_I (3)				9	10	9	10		
SSTL_18_II (3)				N/A	5	N/A	4		
DIFF_SSTL_18_I (3)				27	30	27	30		
DIFF_SSTL_18_II (3)				N/A	15	N/A	12		

Table 34: SSO Limit per V<sub>CCO</sub>/GND Pair (Cont'd)

V <sub>CCO</sub>	I/O Standard	Drive	Slew	SSO Limit per V <sub>CCO</sub> /GND Pair					
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324			
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5		
2.5V	LVCMS25	2	Fast	38	43	38	43		
			Slow	46	52	46	48		
			QuietIO	57	64	57	59		
		4	Fast	21	24	21	23		
			Slow	26	31	26	27		
			QuietIO	33	32	33	30		
		6	Fast	15	17	15	16		
			Slow	19	22	19	19		
			QuietIO	25	23	25	19		
		8	Fast	12	15	12	14		
			Slow	15	18	15	16		
			QuietIO	21	19	21	16		
		12	Fast	1	3	1	1		
			Slow	2	7	2	4		
			QuietIO	3	8	3	8		
		16	Fast	1	3	1	1		
			Slow	3	7	3	3		
			QuietIO	4	9	4	8		
		24	Fast	N/A	3	N/A	1		
			Slow	N/A	5	N/A	2		
			QuietIO	N/A	8	N/A	6		
SSTL_2_I <sup>(3)</sup>				10	11	10	11		
SSTL_2_II <sup>(3)</sup>				N/A	7	N/A	7		
DIFF_SSTL_2_I <sup>(3)</sup>				30	33	30	33		
DIFF_SSTL_2_II <sup>(3)</sup>				N/A	21	N/A	24		

Table 34: SSO Limit per V<sub>CCO</sub>/GND Pair (Cont'd)

V <sub>CCO</sub>	I/O Standard	Drive	Slew	SSO Limit per V <sub>CCO</sub> /GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
3.3V	LVCMOS33	2	Fast	42	46	42	44
			Slow	50	55	50	49
			QuietIO	60	68	60	60
		4	Fast	21	27	21	25
			Slow	32	37	32	32
			QuietIO	39	42	39	37
		6	Fast	14	19	14	17
			Slow	19	25	19	22
			QuietIO	29	30	29	25
		8	Fast	11	15	11	14
			Slow	15	20	15	18
			QuietIO	25	24	25	20
		12	Fast	1	3	1	1
			Slow	2	5	2	2
			QuietIO	4	9	4	7
		16	Fast	1	2	1	1
			Slow	1	5	1	1
			QuietIO	3	10	3	8
		24	Fast	1	2	1	1
			Slow	2	5	2	1
			QuietIO	7	9	7	7

## Input/Output Logic Switching Characteristics

Table 35: ILOGIC2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
<b>Setup/Hold</b>						
T <sub>ICE0CK</sub> /T <sub>ICKCE0</sub>	CE0 pin Setup/Hold with respect to CLK	0.56/ -0.30	0.56/ -0.25	0.79/ -0.22	1.21/ -0.52	ns
T <sub>ISRCK</sub> /T <sub>ICKSR</sub>	SR pin Setup/Hold with respect to CLK	0.74/ -0.23	0.74/ -0.22	0.98/ -0.20	1.31/ -0.45	ns
T <sub>IDOCK</sub> /T <sub>IOCKD</sub>	D pin Setup/Hold with respect to CLK without Delay	1.19/ -0.83	1.36/ -0.83	1.73/ -0.83	2.18/ -1.77	ns
T <sub>IDOCKD</sub> /T <sub>IOCKDD</sub>	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	0.31/ 0.00	0.47/ 0.00	0.54/ 0.00	0.63/ -0.39	ns
<b>Combinatorial</b>						
T <sub>IDI</sub>	D pin to O pin propagation delay, no Delay	0.95	1.28	1.53	2.25	ns
T <sub>IDID</sub>	DDLY pin to O pin propagation delay (using IODELAY2)	0.23	0.39	0.44	0.74	ns
<b>Sequential Delays</b>						
T <sub>IDLO</sub>	D pin to Q pin using flip-flop as a latch without Delay	1.56	1.86	2.39	3.49	ns
T <sub>IDLOD</sub>	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY2)	0.68	0.97	1.20	1.94	ns
T <sub>ICKQ</sub>	CLK to Q outputs for XC devices	1.03	1.24	1.43	2.11	ns
	CLK to Q outputs for XA and XQ devices	1.38	N/A	1.78	2.11	ns
T <sub>TRQ_ILOGIC2</sub>	SR pin to Q outputs	1.81	1.81	2.50	3.05	ns

Table 36: OLOGIC2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
<b>Setup/Hold</b>						
T <sub>ODCK</sub> /T <sub>OCKD</sub>	D1/D2 pins Setup/Hold with respect to CLK	0.81/ -0.05	0.86/ -0.05	1.18/ 0.00	1.73/ -0.27	ns
T <sub>OOC ECK</sub> /T <sub>OCKOCE</sub>	OCE pin Setup/Hold with respect to CLK	0.75/ -0.10	0.75/ -0.10	1.01/ -0.05	1.66/ -0.23	ns
T <sub>OSRCK</sub> /T <sub>OCKSR</sub>	SR pin Setup/Hold with respect to CLK	0.70/ -0.28	0.79/ -0.28	1.03/ -0.23	1.39/ -0.47	ns
T <sub>OTCK</sub> /T <sub>OCKT</sub>	T1/T2 pins Setup/Hold with respect to CLK	0.24/ -0.08	0.56/ -0.06	0.83/ -0.01	0.99/ -0.19	ns
T <sub>OTCECK</sub> /T <sub>OCKTCE</sub>	TCE pin Setup/Hold with respect to CLK	0.58/ -0.06	0.72/ -0.06	1.18/ -0.01	1.51/ -0.13	ns
<b>Sequential Delays</b>						
T <sub>OCKQ</sub>	CLK to OQ/TQ out for XC devices	0.48	0.51	0.74	0.74	ns
	CLK to OQ/TQ out for XA and XQ devices	0.85	N/A	1.16	0.74	ns
T <sub>TRQ_OLOGIC2</sub>	SR pin to OQ/TQ out	1.81	1.81	2.50	3.05	ns

## Input Serializer/Deserializer Switching Characteristics

Table 37: ISERDES2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
<b>Setup/Hold for Control Lines</b>						
T <sub>ISCKC_BITSLIP</sub> / T <sub>ISCKC_BITSLIP</sub>	BITSLIP pin Setup/Hold with respect to CLKDIV	0.16/ -0.09	0.20/ -0.09	0.31/ -0.09	0.34/ -0.14	ns
T <sub>ISCKC_CE</sub> / T <sub>ISCKC_CE</sub>	CE pin Setup/Hold with respect to CLK	0.71/ -0.47	0.71/ -0.42	0.97/ -0.42	1.39/ -0.71	ns
<b>Setup/Hold for Data Lines</b>						
T <sub>ISDCK_D</sub> / T <sub>ISCKD_D</sub>	D pin Setup/Hold with respect to CLK	0.24/ -0.15	0.25/ -0.05	0.29/ -0.05	0.09/ -0.05	ns
T <sub>ISDCK_DDLY</sub> / T <sub>ISCKD_DDLY</sub>	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	-0.25/ 0.30	-0.25/ 0.42	-0.25/ 0.56	-0.54/ 0.67	ns
T <sub>ISDCK_D_DDR</sub> / T <sub>ISCKD_D_DDR</sub>	D pin Setup/Hold with respect to CLK at DDR mode	-0.03/ 0.04	-0.03/ 0.16	-0.03/ 0.18	-0.05/ 0.12	ns
T <sub>ISDCK_DDLY_DDR</sub> / T <sub>ISCKD_DDLY_DDR</sub>	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY2)	-0.40/ 0.48	-0.40/ 0.53	-0.40/ 0.71	-0.71/ 0.86	ns
<b>Sequential Delays</b>						
T <sub>ISCKO_Q</sub>	CLKDIV to out at Q pin	1.30	1.44	2.02	2.22	ns
F <sub>CLKDIV</sub>	CLKDIV maximum frequency	270	262.5	250	125	MHz

## Output Serializer/Deserializer Switching Characteristics

Table 38: OSERDES2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
<b>Setup/Hold</b>						
T <sub>OSDCK_D</sub> / T <sub>OSCKD_D</sub>	D input Setup/Hold with respect to CLKDIV	-0.03/ 1.02	-0.03/ 1.17	-0.03/ 1.27	-0.02/ 0.23	ns
T <sub>OSDCK_T</sub> / T <sub>OSCKD_T</sub> <sup>(1)</sup>	T input Setup/Hold with respect to CLK	-0.05/ 1.03	-0.05/ 1.13	-0.05/ 1.23	-0.05/ 0.24	ns
T <sub>OSCCK_OCE</sub> / T <sub>OSCKC_OCE</sub>	OCE input Setup/Hold with respect to CLK	0.12/ -0.03	0.15/ -0.03	0.24/ -0.03	0.28/ -0.17	ns
T <sub>OSCCK_TCE</sub> / T <sub>OSCKC_TCE</sub>	TCE input Setup/Hold with respect to CLK	0.14/ -0.08	0.17/ -0.08	0.27/ -0.08	0.31/ -0.16	ns
<b>Sequential Delays</b>						
T <sub>OSCKO_OQ</sub>	Clock to out from CLK to OQ	0.94	1.11	1.51	1.89	ns
T <sub>OSCKO_TQ</sub>	Clock to out from CLK to TQ	0.94	1.11	1.51	1.91	ns
F <sub>CLKDIV</sub>	CLKDIV maximum frequency	270	262.5	250	125	MHz

**Notes:**

1. T<sub>OSDCK\_T2</sub> / T<sub>OSCKD\_T2</sub> (T input setup/hold with respect to CLKDIV) are reported as T<sub>OSDCK\_T</sub> / T<sub>OSCKD\_T</sub> in TRACE report.

## Block RAM Switching Characteristics

Table 43: Block RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
<b>Block RAM Clock to Out Delays</b>						
T <sub>RCKO_DO</sub>	Clock CLK to DOUT output (without output register) <sup>(1)</sup>	1.85	2.10	2.10	3.50	ns, Max
T <sub>RCKO_DO_REG</sub>	Clock CLK to DOUT output (with output register) <sup>(2)</sup>	1.60	1.75	1.75	2.30	ns, Max
<b>Setup and Hold Times Before/After Clock CLK</b>						
T <sub>RCKC_ADDR</sub> /T <sub>RCKC_ADDR</sub>	ADDR inputs for XC devices <sup>(3)</sup>	0.35/ 0.10	0.40/ 0.12	0.40/ 0.12	0.50/ 0.15	ns, Min
	ADDR inputs for XA and XQ devices <sup>(3)</sup>	0.35/ 0.17	N/A	0.40/ 0.17	0.50/ 0.15	ns, Min
T <sub>RDCK_DI</sub> /T <sub>RCKD_DI</sub>	DIN inputs <sup>(4)</sup>	0.30/ 0.10	0.30/ 0.10	0.30/ 0.10	0.40/ 0.15	ns, Min
T <sub>RCKC_EN</sub> /T <sub>RCKC_EN</sub>	Block RAM Enable (EN) input	0.22/ 0.05	0.25/ 0.06	0.25/ 0.06	0.44/ 0.10	ns, Min
T <sub>RCKC_REGCE</sub> /T <sub>RCKC_REGCE</sub>	CE input of output register	0.20/ 0.10	0.20/ 0.10	0.20/ 0.10	0.28/ 0.15	ns, Min
T <sub>RCKC_WE</sub> /T <sub>RCKC_WE</sub>	Write Enable (WE) input	0.25/ 0.10	0.33/ 0.10	0.33/ 0.10	0.28/ 0.15	ns, Min
<b>Maximum Frequency</b>						
F <sub>MAX</sub>	Block RAM in all modes	320	280	280	150	MHz

**Notes:**

1. T<sub>RCKO\_DO</sub> includes T<sub>RCKO\_DOA</sub> and T<sub>RCKO\_DOPA</sub> as well as the B port equivalent timing parameters.
2. T<sub>RCKO\_DO\_REG</sub> includes T<sub>RCKO\_DOA\_REG</sub> and T<sub>RCKO\_DOPA\_REG</sub> as well as the B port equivalent timing parameters.
3. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
4. T<sub>RDCK\_DI</sub> includes both A and B inputs as well as the parity inputs of A and B.

Table 56: Switching Characteristics for the Digital Frequency Synthesizer (DFS) for DCM\_SP<sup>(1)</sup>

Symbol	Description	Speed Grade								Units	
		-3		-3N		-2		-1L			
		Min	Max	Min	Max	Min	Max	Min	Max		
<b>Output Frequency Ranges</b>											
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz	
<b>Output Clock Jitter<sup>(2)(3)</sup></b>											
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN < 20 MHz	Use the Clocking Wizard								ps	
	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN > 20 MHz	Typical = ±(1% of CLKFX period + 100)								ps	
<b>Duty Cycle<sup>(4)(5)</sup></b>											
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±(1% of CLKFX period + 350)								ps	
<b>Phase Alignment<sup>(5)</sup></b>											
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used	–	±200	–	±200	–	±200	–	±250	ps	
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used	Maximum = ±(1% of CLKFX period + 200)								ps	
<b>LOCKED Time</b>											
LOCK_FX <sup>(2)</sup>	When FCLKIN < 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	–	5	–	5	–	5	–	5	ms	
	When FCLKIN > 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	–	0.45	–	0.45	–	0.45	–	0.60	ms	

**Notes:**

- The values in this table are based on the operating conditions described in Table 2 and Table 55.
- For optimal jitter tolerance and a faster LOCK time, use the CLKIN\_PERIOD attribute.
- Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
- The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
- Some duty cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.

Table 59: Switching Characteristics for the Phase-Shift Clock in Variable Phase Mode<sup>(1)</sup>

Symbol	Description	Amount of Phase Shift	Units
<b>Phase Shifting Range</b>			
MAX_STEPS <sup>(2)</sup>	When CLKIN < 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period.	$\pm(\text{INTEGER}(10 \times (\text{CLKIN} - 3 \text{ ns})))$	steps
	When CLKIN $\geq$ 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period.	$\pm(\text{INTEGER}(15 \times (\text{CLKIN} - 3 \text{ ns})))$	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting.	$\pm(\text{MAX_STEPS} \times \text{DCM_DELAY_STEP_MIN})$	ps
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	$\pm(\text{MAX_STEPS} \times \text{DCM_DELAY_STEP_MAX})$	ps

**Notes:**

- The values in this table are based on the operating conditions described in Table 53 and Table 58.
- The maximum variable phase shift range, MAX\_STEPS, is only valid when the DCM has no initial fixed-phase shifting, that is, the PHASE\_SHIFT attribute is set to 0.
- The DCM\_DELAY\_STEP values are provided at the end of Table 54.

Table 60: Miscellaneous DCM Timing Parameters<sup>(1)</sup>

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	3	–	CLKIN cycles

**Notes:**

- This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFXDV, CLKFX180) are unaffected.

Table 61: Frequency Synthesis

Attribute	Min	Max
CLKFX_MULTIPLY (DCM_SP)	2	32
CLKFX_DIVIDE (DCM_SP)	1	32
CLKDV_DIVIDE (DCM_SP)	1.5	16
CLKFX_MULTIPLY (DCM_CLKGEN)	2	256
CLKFX_DIVIDE (DCM_CLKGEN)	1	256
CLKFXDV_DIVIDE (DCM_CLKGEN)	2	32

Table 62: DCM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T <sub>DMCCK_PSEN</sub> /T <sub>DMCKC_PSEN</sub>	PSEN Setup/Hold	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	ns
T <sub>DMCCK_PSINCDEC</sub> /T <sub>DMCKC_PSINCDEC</sub>	PSINCDEC Setup/Hold	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	ns
T <sub>DMCKO_PSDONE</sub>	Clock to out of PSDONE	1.50	1.50	1.50	1.50	ns

Table 65: Global Clock Input to Output Delay With DCM in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in Source-Synchronous Mode.							
T <sub>CLOCKOFDCM_0</sub>	Global Clock and OUTFF <i>with</i> DCM	XC6SLX4	5.03	N/A	7.21	8.05	ns
		XC6SLX9	5.03	6.13	7.21	8.05	ns
		XC6SLX16	5.08	5.51	6.44	7.96	ns
		XC6SLX25	4.81	5.13	5.69	7.94	ns
		XC6SLX25T	4.81	5.13	5.69	N/A	ns
		XC6SLX45	5.26	5.69	6.63	7.92	ns
		XC6SLX45T	5.26	5.69	6.63	N/A	ns
		XC6SLX75	4.77	5.18	5.88	7.95	ns
		XC6SLX75T	4.77	5.18	5.88	N/A	ns
		XC6SLX100	4.72	5.11	5.76	8.59	ns
		XC6SLX100T	4.76	5.11	5.76	N/A	ns
		XC6SLX150	4.90	5.30	5.93	7.93	ns
		XC6SLX150T	4.90	5.30	5.93	N/A	ns
		XA6SLX4	5.35	N/A	7.21	N/A	ns
		XA6SLX9	5.35	N/A	7.21	N/A	ns
		XA6SLX16	5.42	N/A	6.44	N/A	ns
		XA6SLX25	5.13	N/A	5.69	N/A	ns
		XA6SLX25T	5.13	N/A	5.79	N/A	ns
		XA6SLX45	5.58	N/A	6.63	N/A	ns
		XA6SLX45T	5.58	N/A	6.63	N/A	ns
		XA6SLX75	5.09	N/A	5.87	N/A	ns
		XA6SLX75T	5.09	N/A	5.87	N/A	ns
		XA6SLX100	N/A	N/A	6.44	N/A	ns
		XQ6SLX75	N/A	N/A	5.87	7.95	ns
		XQ6SLX75T	5.09	N/A	5.87	N/A	ns
		XQ6SLX150	N/A	N/A	6.06	7.93	ns
		XQ6SLX150T	5.50	N/A	6.06	N/A	ns

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 71: Global Clock Setup and Hold Without DCM or PLL (Default Delay)

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
<b>Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.<sup>(1)</sup></b>							
T <sub>PSFD</sub> / T <sub>PHFD</sub>	Default Delay <sup>(2)</sup> Global Clock and IFF <sup>(3)</sup> without DCM or PLL	XC6SLX4	0.66/1.17	N/A	1.05/0.79	2.09/1.05	ns
		XC6SLX9	0.66/1.17	0.75/1.17	1.05/1.17	2.09/1.05	ns
		XC6SLX16	0.87/1.16	0.93/1.16	0.96/1.16	1.86/1.06	ns
		XC6SLX25	0.68/0.77	0.81/0.81	0.87/0.82	2.21/1.33	ns
		XC6SLX25T	0.68/0.77	0.81/0.81	0.87/0.82	N/A	ns
		XC6SLX45	0.40/1.05	0.42/1.17	0.64/1.20	1.61/1.67	ns
		XC6SLX45T	0.40/1.05	0.42/1.17	0.64/1.20	N/A	ns
		XC6SLX75	0.41/1.11	0.41/1.13	0.80/1.14	1.23/1.82	ns
		XC6SLX75T	0.41/1.11	0.41/1.13	0.80/1.14	N/A	ns
		XC6SLX100	0.39/1.12	0.39/1.23	0.39/1.28	1.13/1.94	ns
		XC6SLX100T	0.39/1.12	0.39/1.23	0.39/1.28	N/A	ns
		XC6SLX150	0.23/1.54	0.23/1.62	0.23/1.62	1.14/2.05	ns
		XC6SLX150T	0.23/1.54	0.23/1.62	0.23/1.62	N/A	ns
		XA6SLX4	0.73/1.18	N/A	1.05/0.80	N/A	ns
		XA6SLX9	0.73/1.18	N/A	1.05/0.80	N/A	ns
		XA6SLX16	0.90/1.20	N/A	0.96/0.75	N/A	ns
		XA6SLX25	0.70/0.81	N/A	0.87/0.91	N/A	ns
		XA6SLX25T	0.76/0.81	N/A	1.03/0.91	N/A	ns
		XA6SLX45	0.40/1.06	N/A	0.64/1.20	N/A	ns
		XA6SLX45T	0.40/1.06	N/A	0.64/1.20	N/A	ns
		XA6SLX75	0.41/1.24	N/A	0.80/1.18	N/A	ns
		XA6SLX75T	0.41/1.24	N/A	0.80/1.18	N/A	ns
		XA6SLX100	N/A	N/A	0.86/1.55	N/A	ns
		XQ6SLX75	N/A	N/A	0.80/1.18	1.23/1.82	ns
		XQ6SLX75T	0.41/1.24	N/A	0.80/1.18	N/A	ns
		XQ6SLX150	N/A	N/A	0.28/1.57	1.14/2.05	ns
		XQ6SLX150T	0.28/1.78	N/A	0.28/1.57	N/A	ns

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Default delay uses IODELAY2 tap 0.
3. IFF = Input Flip-Flop or Latch.

## Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
08/26/09	1.1	Added $V_{FS}$ to <a href="#">Table 1</a> and <a href="#">Table 2</a> . Added $R_{FUSE}$ to <a href="#">Table 2</a> . Added XC6SLX75 and XC6SLX75T to $V_{BATT}$ and $I_{BATT}$ in <a href="#">Table 1</a> , <a href="#">Table 2</a> , and <a href="#">Table 4</a> . Corrected the quiescent supply current for the XC6SLX4 in <a href="#">Table 5</a> . Updated <a href="#">Table 11</a> . Removed $DV_{PPIN}$ from <a href="#">Figure 2</a> . Removed $F_{PCIECORE}$ from <a href="#">Table 24</a> and added values to $F_{PCIEUSER}$ . Added more networking applications to <a href="#">Table 25</a> . Updated values for $T_{SUSPENDLOW\_AWAKE}$ , $T_{SUSPEND\_ENABLE}$ , and $T_{SCP\_AWAKE}$ in <a href="#">Table 46</a> . Numerous changes to <a href="#">Table 47, page 54</a> including the addition of new values to various specifications, revising the $T_{SMCKCSO}$ description, and changing the units of $T_{POR}$ . Also, removed <i>Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK section</i> from <a href="#">Table 47</a> and updated all the notes. In <a href="#">Table 52</a> , added to $F_{INMAX}$ , revised $F_{OUTMAX}$ , and removed PLL Maximum Output Frequency for BUFI02. Revised values for DCM_DELAY_STEP in <a href="#">Table 54</a> . Updated CLKIN_FREQ_FX values in <a href="#">Table 55</a> .
01/04/10	1.2	Added -4 speed grade to entire document. Updated speed specification of -4, -3, -2 speed grades to version 1.03. Added -1L speed grade numbers per speed specification 1.00. Updated $T_{SOL}$ in <a href="#">Table 1</a> . Added -1L rows for LVCMOS12, LVCMOS15, and LVCMOS18 in <a href="#">Table 9</a> . Revised much of the detail in <a href="#">GTP Transceiver Specifications</a> in <a href="#">Table 12</a> through <a href="#">Table 23</a> . Added -2 data to <a href="#">Table 25</a> . Updated $F_{MAX}$ in <a href="#">Table 44</a> . Updated descriptions for $T_{DNACLKL}$ and $T_{DNACLKH}$ in <a href="#">Table 45</a> and revised values for all parameters. Removed $T_{INITADDR}$ from <a href="#">Table 47</a> and added new data. Updated values in <a href="#">Table 48</a> through <a href="#">Table 62</a> . Added <a href="#">Table 51</a> (BUFPLL) and <a href="#">Table 57</a> (DCM_CLKGEN). Removed $T_{LOCKMAX}$ note from <a href="#">Table 52</a> . Updated note 3 in <a href="#">Table 53</a> . In <a href="#">Table 79</a> : removed XC6SLX75CSG324 and XC6SLX75TCG324; added XC6SLX75FG(G)484 and XC6SLX75FG(G)484.
02/22/10	1.3	Production release of XC6SLX16 -2 speed grade devices. The changes to <a href="#">Table 26</a> and <a href="#">Table 27</a> includes updating this data sheet to the data in ISE v11.5 software with speed specification v1.06. Updated maximum of $V_{IN}$ and $V_{TS}$ and note 2 in <a href="#">Table 1</a> . In <a href="#">Table 2</a> , changed $V_{IN}$ , added $I_{IN}$ and note 5, revised notes 1, 6, and 7, and added note 8 to $R_{FUSE}$ . In <a href="#">Table 4</a> , removed previous note 1 and added data to $I_{RPU}$ , $I_{RPD}$ , and $I_{BATT}$ ; changed $C_{IN}$ , added $R_{DT}$ and $R_{IN\_TERM}$ , and added note 2 and 3. Updated $V_{CCO2}$ in <a href="#">Table 6</a> . Added <a href="#">Table 7</a> and <a href="#">Table 8</a> . Removed PCI66_3 from <a href="#">Table 9</a> . Updated PCI33_3 and I2C in <a href="#">Table 9</a> . Updated the description of <a href="#">Table 11</a> . Completely updated <a href="#">Table 25</a> . Updated <a href="#">Table 28</a> including adding values for PCI33_3. Updated $V_{REF}$ value for HSTL_III_18 in <a href="#">Table 31</a> . Updates missing $V_{REF}$ values in <a href="#">Table 32</a> . Added <a href="#">Simultaneously Switching Outputs, page 36</a> . Removed $T_{GSRQ}$ and $T_{RPW}$ from <a href="#">Table 35</a> and <a href="#">Table 36</a> . Also removed $T_{DOQ}$ from <a href="#">Table 36</a> . Removed $T_{ISPO\_DO}$ and note 1 from <a href="#">Table 37</a> . Removed $T_{OSCCK\_S}$ and combinatorial section from <a href="#">Table 38</a> . In <a href="#">Table 39</a> , removed $T_{IODDO\_T}$ and added new tap parameters and note 2. In <a href="#">Table 40</a> , <a href="#">Table 41</a> , and <a href="#">Table 42</a> , made typographical edits and removed notes. Removed clock CLK section in <a href="#">Table 41</a> . Removed clock CLK section and $T_{REG\_MUX}$ and $T_{REG\_M31}$ in <a href="#">Table 42</a> . Added block RAM $F_{MAX}$ values to <a href="#">Table 43</a> . Updated values and added note 2 to <a href="#">Table 45</a> . Added values to <a href="#">Table 46</a> and removed note 1. Numerous changes to <a href="#">Table 47</a> . Completely updated <a href="#">Table 57</a> . Revised data in <a href="#">Table 62</a> . Removed note 3 from <a href="#">Table 71</a> . Added values to <a href="#">Table 79</a> . Added data to <a href="#">Table 80</a> and <a href="#">Table 81</a> .
03/10/10	1.4	Production release of XC6SLX45 -2 speed grade devices, which includes changes to <a href="#">Table 26</a> and <a href="#">Table 27</a> updating this data sheet to the data in ISE v11.5 software with speed specification v1.07. Fixed $R_{IN\_TERM}$ description in <a href="#">Table 4</a> . Added PCI66_3 to <a href="#">Table 7</a> and replaced note 1. Corrected note 1 and the V <sub>Max</sub> for TMDS_33 in <a href="#">Table 8</a> . In <a href="#">Table 10</a> , added note 1 to LVPECL_33 and TMDS_33. Also updated specifications for TMDS_33. Updated the <a href="#">GTP Transceiver Specifications</a> section including adding values to <a href="#">Table 16</a> , <a href="#">Table 17</a> , and <a href="#">Table 20</a> through <a href="#">Table 23</a> . Added PCI66_3 back into <a href="#">Table 9</a> , <a href="#">Table 28</a> , <a href="#">Table 31</a> , <a href="#">Table 32</a> , and <a href="#">Table 34</a> . Updated note 3 on <a href="#">Table 32</a> . In <a href="#">Table 34</a> , corrected some typographical errors and fixed SSO limits for bank1/3 in FG(G)484 package. Corrected $T_{OSCCK\_OC_E}$ in <a href="#">Table 38</a> . In <a href="#">Table 57</a> , updated CLKFX_FREEZE_VAR and CLKFX_FREEZE_TEMP_SLOPE and added typical values to $T_{CENTER\_LOW\_SPREAD}$ and $T_{CENTER\_HIGH\_SPREAD}$ . Updated and added values to <a href="#">Table 63</a> through <a href="#">Table 78</a> , and <a href="#">Table 81</a> . In <a href="#">Table 79</a> , revised the XC6SLX16-CSG324 and the XC6SLX45-CSG484 and FG(G)484 values.