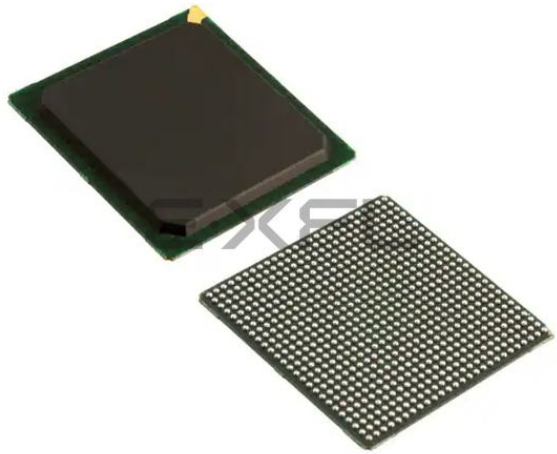

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	11519
Number of Logic Elements/Cells	147443
Total RAM Bits	4939776
Number of I/O	498
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx150-2fgg676i

Table 1: **Absolute Maximum Ratings[1] *(Cont'd)***

Symbol	Description					Units
V_{IN} and V_{TS}[3]	I/O input voltage or voltage applied to 3-state output, relative to GND[4]	All user and dedicated I/Os	Commercial	DC	–0.60 to 4.10	V
				20% overshoot duration	–0.75 to 4.25	V
				8% overshoot duration[5]	–0.75 to 4.40	V
			Industrial	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration[5]	–0.75 to 4.40	V
			Expanded (Q)	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration[5]	–0.75 to 4.40	V
		Restricted to maximum of 100 user I/Os	Commercial	20% overshoot duration	–0.75 to 4.35	V
				15% overshoot duration[5]	–0.75 to 4.40	V
				10% overshoot duration	–0.75 to 4.45	V
			Industrial	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration[5]	–0.75 to 4.40	V
			Expanded (Q)	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration[5]	–0.75 to 4.40	V
T_{STG}	Storage temperature (ambient)				–65 to 150	°C
T_{SOL}	Maximum soldering temperature[6] (TQG144, CPG196, CSG225, CSG324, CSG484, and FTG256)				+260	°C
	Maximum soldering temperature[6] (Pb-free packages: FGG484, FGG676, and FGG900)				+250	°C
	Maximum soldering temperature[6] (Pb packages: CS484, FT256, FG484, FG676, and FG900)				+220	°C
T_j	Maximum junction temperature[6]				+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When programming eFUSE, $V_{FS} \leq V_{CCAUX}$. Requires up to 40 mA current. For read mode, V_{FS} can be between GND and 3.45 V.
3. I/O absolute maximum limit applied to DC and AC signals. Overshoot duration is the percentage of a data period that the I/O is stressed beyond 3.45V.
4. For I/O operation, refer to UG381: *Spartan-6 FPGA SelectIO Resources User Guide*.
5. Maximum percent overshoot duration to meet 4.40V maximum.
6. For soldering guidelines and thermal considerations, see UG385: *Spartan-6 FPGA Packaging and Pinout Specification*.

Table 2: **Recommended Operating Conditions(1)**

Symbol	Description			Min	Typ	Max	Units
V_{CCINT}	Internal supply voltage relative to GND	-3, -3N, -2	Standard performance(2)	1.14	1.2	1.26	V
		-3, -2	Extended performance(2)	1.2	1.23	1.26	V
		-1L	Standard performance(2)	0.95	1.0	1.05	V
V_{CCAUX}(3)(4)	Auxiliary supply voltage relative to GND	V_{CCAUX} = 2.5V(5)		2.375	2.5	2.625	V
		V_{CCAUX} = 3.3V		3.15	3.3	3.45	V
V_{CCO}(6)(7)(8)	Output supply voltage relative to GND			1.1	–	3.45	V
V_{IN}	Input voltage relative to GND	All I/O standards (except PCI)	Commercial temperature (C)	–0.5	–	4.0	V
			Industrial temperature (I)	–0.5	–	3.95	V
			Expanded (Q) temperature	–0.5	–	3.95	V
		PCI I/O standard(9)		–0.5	–	V_{CCO} + 0.5	V
I_{IN}(10)	Maximum current through pin using PCI I/O standard when forward biasing the clamp diode.(9)		Commercial (C) and Industrial temperature (I)	–	–	10	mA
			Expanded (Q) temperature	–	–	7	mA
V_{BATT}(11)	Battery voltage relative to GND, T_j = 0°C to +85°C (LX75, LX75T, LX100, LX100T, LX150, and LX150T only)			1.0	–	3.6	V
T_j	Junction temperature operating range	Commercial (C) range		0	–	85	°C
		Industrial temperature (I) range		–40	–	100	°C
		Expanded (Q) temperature range		–40	–	125	°C

Notes:

1. All voltages are relative to ground.
2. See *Interface Performances for Memory Interfaces* in Table 25. The extended performance range is specified for designs not using the standard V_{CCINT} voltage range. The standard V_{CCINT} voltage range is used for:
   - Designs that do not use an MCB
   - LX4 devices
   - Devices in the TQG144 or CPG196 packages
   - Devices with the -3N speed grade
3. Recommended maximum voltage droop for V_{CCAUX} is 10 mV/ms.
4. During configuration, if V_{CCO_2} is 1.8V, then V_{CCAUX} must be 2.5V.
5. The -1L devices require V_{CCAUX} = 2.5V when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.
6. Configuration data is retained even if V_{CCO} drops to 0V.
7. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
8. For PCI systems, the transmitter and receiver should have common supplies for V_{CCO}.
9. Devices with a -1L speed grade do not support Xilinx PCI IP.
10. Do not exceed a total of 100 mA per bank.
11. V_{BATT} is required to maintain the battery backed RAM (BBR) AES key when V_{CCAUX} is not applied. Once V_{CCAUX} is applied, V_{BATT} can be unconnected. When BBR is not used, Xilinx recommends connecting to V_{CCAUX} or GND. However, V_{BATT} can be unconnected.

Quiescent Current

Typical values for quiescent supply current are specified at nominal voltage, 25°C junction temperatures (T_j). Quiescent supply current is specified by speed grade for Spartan-6 devices. Xilinx recommends analyzing static power consumption using the XPOWER™ Estimator (XPE) tool (download at http://www.xilinx.com/power) for conditions other than those specified in Table 5.

Table 5: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	LX4	4.0	4.0	4.0	2.4	mA
		LX9	4.0	4.0	4.0	2.4	mA
		LX16	6.0	6.0	6.0	4.0	mA
		LX25	11.0	11.0	11.0	6.6	mA
		LX25T	11.0	11.0	11.0	N/A	mA
		LX45	15.0	15.0	15.0	9.0	mA
		LX45T	15.0	15.0	15.0	N/A	mA
		LX75	29.0	29.0	29.0	17.4	mA
		LX75T	29.0	29.0	29.0	N/A	mA
		LX100	36.0	36.0	36.0	21.6	mA
		LX100T	36.0	36.0	36.0	N/A	mA
		LX150	51.0	51.0	51.0	31.0	mA
		LX150T	51.0	51.0	51.0	N/A	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	LX4	1.0	1.0	1.0	1.0	mA
		LX9	1.0	1.0	1.0	1.0	mA
		LX16	2.0	2.0	2.0	2.0	mA
		LX25	2.0	2.0	2.0	2.0	mA
		LX25T	2.0	2.0	2.0	N/A	mA
		LX45	3.0	3.0	3.0	3.0	mA
		LX45T	3.0	3.0	3.0	N/A	mA
		LX75	4.0	4.0	4.0	4.0	mA
		LX75T	4.0	4.0	4.0	N/A	mA
		LX100	5.0	5.0	5.0	5.0	mA
		LX100T	5.0	5.0	5.0	N/A	mA
		LX150	7.0	7.0	7.0	7.0	mA
		LX150T	7.0	7.0	7.0	N/A	mA

Table 8: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

I/O Standard	V_{CCO} for Drivers		
	V, Min	V, Nom	V, Max
LVDS_33	3.0	3.3	3.45
LVDS_25	2.25	2.5	2.75
BLVDS_25	2.25	2.5	2.75
MINI_LVDS_33	3.0	3.3	3.45
MINI_LVDS_25	2.25	2.5	2.75
LVPECL_33(1)	N/A–Inputs Only		
LVPECL_25	N/A–Inputs Only		
RSDS_33	3.0	3.3	3.45
RSDS_25	2.25	2.5	2.75
TMDS_33(1)	3.14	3.3	3.45
PPDS_33	3.0	3.3	3.45
PPDS_25	2.25	2.5	2.75
DISPLAY_PORT	2.3	2.5	2.7
DIFF_MOBILE_DDR	1.7	1.8	1.9
DIFF_HSTL_I	1.4	1.5	1.6
DIFF_HSTL_II	1.4	1.5	1.6
DIFF_HSTL_III	1.4	1.5	1.6
DIFF_HSTL_I_18	1.7	1.8	1.9
DIFF_HSTL_II_18	1.7	1.8	1.9
DIFF_HSTL_III_18	1.7	1.8	1.9
DIFF_SSTL3_I	3.0	3.3	3.45
DIFF_SSTL3_II	3.0	3.3	3.45
DIFF_SSTL2_I	2.3	2.5	2.7
DIFF_SSTL2_II	2.3	2.5	2.7
DIFF_SSTL18_I	1.7	1.8	1.9
DIFF_SSTL18_II	1.7	1.8	1.9
DIFF_SSTL15_II	1.425	1.5	1.575

Notes:

1. LVPECL_33 and TMDS_33 inputs require V_{CCAUX} = 3.3V nominal.

Table 23: **GTP Transceiver Receiver Switching Characteristics**

Symbol	Description			Min	Typ	Max	Units
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data			–	75	–	ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak			60	–	150	mV
R_{XSST}	Receiver spread-spectrum tracking(1)		Modulated @ 33 KHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)	Internal AC capacitor bypassed		–	–	150	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	CDR 2nd-order loop disabled		–200	–	200	ppm
		CDR 2nd-order loop enabled	PLL_RXDIVSEL_OUT = 1	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 2	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 4	–1000	–	1000	ppm
SJ Jitter Tolerance(2)							
$JT\_SJ_{3.125}$	Sinusoidal Jitter(3)		3.125 Gb/s	0.4	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(3)		2.5 Gb/s	0.4	–	–	UI
$JT\_SJ_{1.62}$	Sinusoidal Jitter(3)		1.62 Gb/s	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(3)		1.25 Gb/s	0.5	–	–	UI
JT_SJ_{614}	Sinusoidal Jitter(3)		614 Mb/s	0.5	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)(5)							
$JT\_TJSE_{3.125}$	Total Jitter with stressed eye(4)		3.125 Gb/s	0.65	–	–	UI
$JT\_SJSE_{3.125}$	Sinusoidal Jitter with stressed eye		3.125 Gb/s	0.1	–	–	UI
$JT\_TJSE_{2.7}$	Total Jitter with stressed eye(4)		2.7 Gb/s	0.65	–	–	UI
$JT\_SJSE_{2.7}$	Sinusoidal Jitter with stressed eye		2.7 Gb/s	0.1	–	–	UI

Notes:
1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a Bit Error Ratio of $1e^{-12}$.
3. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
4. Composed of 0.37 UI DJ in the form of ISI and 0.18 UI RJ.
5. Measured using PRBS7 data pattern.

Endpoint Block for PCI Express Designs Switching Characteristics

The Endpoint block for PCI Express is available in the Spartan-6 LXT devices. Consult the Spartan-6 FPGA Integrated Endpoint Block for PCI Express for further information.

Table 24: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
$F_{PCIEUSER}$	User clock maximum frequency	62.5	62.5	62.5	N/A	MHz

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics, page 19.

Table 25: **Interface Performances**

Description	I/O Resource	Clock Buffer	Data Width	Speed Grade				Units
				-3	-3N	-2	-1L	
Networking Applications(1)								
SDR LVDS transmitter or receiver	IOB SDR register	BUFG	–	400	400	375	250	Mb/s
DDR LVDS transmitter or receiver	ODDR2/IDDR2 register	2 BUFGs	–	800	800	750	500	Mb/s
SDR LVDS transmitter	OSERDES2	BUFPLL	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
DDR LVDS transmitter	OSERDES2	2 BUFIO2s	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
SDR LVDS receiver	ISERDES2 in RETIMED mode	BUFPLL	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
DDR LVDS receiver	ISERDES2 in RETIMED mode	2 BUFIO2s	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
Memory Interfaces (Implemented using the Spartan-6 FPGA Memory Controller Block)(2)								
Standard Performance (Standard V_{CCINT})								
DDR				400	Note 4	400	350	Mb/s
DDR2				667	Note 4	625	400	Mb/s
DDR3				800	Note 4	667	—	Mb/s
LPDDR (Mobile_DDR)				400	Note 4	400	350	Mb/s
Extended Performance (Requires Extended Performance V_{CCINT})(3)								
DDR2				800	Note 4	667	—	Mb/s

Notes:

1. Refer to XAPP1064, *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)* and UG381, *Spartan-6 FPGA SelectIO Resources User Guide.*
2. Refer to UG388, *Spartan-6 FPGA Memory Controller User Guide*.
3. Extended Memory Controller block performance for DDR2 can be achieved using the extended performance V_{CCINT} range from Table 2.
4. The LX4 device, all devices in the TQG144 and CPG196 packages, and the -3N speed grade do not support a Memory Controller Block.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 27 lists the production released Spartan-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE® software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 27: **Spartan-6 Device Production Software and Speed Specification Release(1)**

Device	Speed Grade Designations(2)			
	-3(3)	-3N	-2(4)	-1L
XC6SLX4	ISE 12.4 v1.15	N/A	ISE 12.3 v1.12(5)	ISE 13.2 v1.07
XC6SLX9	ISE 12.4 v1.15	ISE 13.1 Update v1.18(7)	ISE 12.3 v1.12(5)	ISE 13.2 v1.07
XC6SLX16	ISE 12.1 v1.08	ISE 13.1 Update v1.18(7)	ISE 11.5 v1.06	ISE 13.2 v1.07
XC6SLX25	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	ISE 13.2 v1.07
XC6SLX25T	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	N/A
XC6SLX45	ISE 12.1 v1.08	ISE 13.1 Update v1.18(7)	ISE 11.5 v1.07	ISE 13.1 v1.06
XC6SLX45T	ISE 12.1 v1.08	ISE 13.1 Update v1.18(7)	ISE 12.1 v1.08	N/A
XC6SLX75	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	ISE 13.2 v1.07
XC6SLX75T	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	N/A
XC6SLX100	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	ISE 13.1 v1.06
XC6SLX100T	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	N/A
XC6SLX150	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	ISE 13.1 v1.06
XC6SLX150T	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	N/A
XA6SLX4	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX9	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX16	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX25	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX25T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX45	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX45T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX75	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX75T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX100	N/A	N/A	ISE 13.3 v1.20	N/A

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	
LVCMOS18, Slow, 24 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18, Fast, 2 mA	1.18	1.30	1.43	2.04	3.59	3.73	3.93	4.53	3.59	3.73	3.93	4.53	ns
LVCMOS18, Fast, 4 mA	1.18	1.30	1.43	2.04	2.39	2.53	2.73	3.35	2.39	2.53	2.73	3.35	ns
LVCMOS18, Fast, 6 mA	1.18	1.30	1.43	2.04	1.88	2.02	2.22	2.84	1.88	2.02	2.22	2.84	ns
LVCMOS18, Fast, 8 mA	1.18	1.30	1.43	2.04	1.81	1.95	2.15	2.77	1.81	1.95	2.15	2.77	ns
LVCMOS18, Fast, 12 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVCMOS18, Fast, 16 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVCMOS18, Fast, 24 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVCMOS18_JEDEC, QUIETIO, 2 mA	0.94	1.06	1.19	1.41	5.91	6.05	6.25	6.79	5.91	6.05	6.25	6.79	ns
LVCMOS18_JEDEC, QUIETIO, 4 mA	0.94	1.06	1.19	1.41	4.75	4.89	5.09	5.64	4.75	4.89	5.09	5.64	ns
LVCMOS18_JEDEC, QUIETIO, 6 mA	0.94	1.06	1.19	1.41	4.04	4.18	4.38	4.96	4.04	4.18	4.38	4.96	ns
LVCMOS18_JEDEC, QUIETIO, 8 mA	0.94	1.06	1.19	1.41	3.71	3.85	4.05	4.62	3.71	3.85	4.05	4.62	ns
LVCMOS18_JEDEC, QUIETIO, 12 mA	0.94	1.06	1.19	1.41	3.35	3.49	3.69	4.28	3.35	3.49	3.69	4.28	ns
LVCMOS18_JEDEC, QUIETIO, 16 mA	0.94	1.06	1.19	1.41	3.20	3.34	3.54	4.13	3.20	3.34	3.54	4.13	ns
LVCMOS18_JEDEC, QUIETIO, 24 mA	0.94	1.06	1.19	1.41	2.96	3.10	3.30	3.98	2.96	3.10	3.30	3.98	ns
LVCMOS18_JEDEC, Slow, 2 mA	0.94	1.06	1.19	1.41	4.59	4.73	4.93	5.54	4.59	4.73	4.93	5.54	ns
LVCMOS18_JEDEC, Slow, 4 mA	0.94	1.06	1.19	1.41	3.69	3.83	4.03	4.60	3.69	3.83	4.03	4.60	ns
LVCMOS18_JEDEC, Slow, 6 mA	0.94	1.06	1.19	1.41	3.00	3.14	3.34	3.94	3.00	3.14	3.34	3.94	ns
LVCMOS18_JEDEC, Slow, 8 mA	0.94	1.06	1.19	1.41	2.19	2.33	2.53	3.18	2.19	2.33	2.53	3.18	ns
LVCMOS18_JEDEC, Slow, 12 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18_JEDEC, Slow, 16 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18_JEDEC, Slow, 24 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18_JEDEC, Fast, 2 mA	0.94	1.06	1.19	1.41	3.57	3.71	3.91	4.52	3.57	3.71	3.91	4.52	ns
LVCMOS18_JEDEC, Fast, 4 mA	0.94	1.06	1.19	1.41	2.39	2.53	2.73	3.35	2.39	2.53	2.73	3.35	ns
LVCMOS18_JEDEC, Fast, 6 mA	0.94	1.06	1.19	1.41	1.88	2.02	2.22	2.84	1.88	2.02	2.22	2.84	ns
LVCMOS18_JEDEC, Fast, 8 mA	0.94	1.06	1.19	1.41	1.80	1.94	2.14	2.76	1.80	1.94	2.14	2.76	ns
LVCMOS18_JEDEC, Fast, 12 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVCMOS18_JEDEC, Fast, 16 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVCMOS18_JEDEC, Fast, 24 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVCMOS15, QUIETIO, 2 mA	0.98	1.10	1.23	1.79	5.47	5.61	5.81	6.38	5.47	5.61	5.81	6.38	ns
LVCMOS15, QUIETIO, 4 mA	0.98	1.10	1.23	1.79	4.61	4.75	4.95	5.51	4.61	4.75	4.95	5.51	ns
LVCMOS15, QUIETIO, 6 mA	0.98	1.10	1.23	1.79	4.07	4.21	4.41	4.97	4.07	4.21	4.41	4.97	ns
LVCMOS15, QUIETIO, 8 mA	0.98	1.10	1.23	1.79	3.91	4.05	4.25	4.81	3.91	4.05	4.25	4.81	ns
LVCMOS15, QUIETIO, 12 mA	0.98	1.10	1.23	1.79	3.53	3.67	3.87	4.51	3.53	3.67	3.87	4.51	ns
LVCMOS15, QUIETIO, 16 mA	0.98	1.10	1.23	1.79	3.32	3.46	3.66	4.31	3.32	3.46	3.66	4.31	ns
LVCMOS15, Slow, 2 mA	0.98	1.10	1.23	1.79	4.18	4.32	4.52	5.11	4.18	4.32	4.52	5.11	ns
LVCMOS15, Slow, 4 mA	0.98	1.10	1.23	1.79	3.42	3.56	3.76	4.34	3.42	3.56	3.76	4.34	ns
LVCMOS15, Slow, 6 mA	0.98	1.10	1.23	1.79	2.29	2.43	2.63	3.24	2.29	2.43	2.63	3.24	ns

Table 29: **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices[1] *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVCMOS12, QUIETIO, 6 mA	0.98	1.16	4.79	4.99	4.79	4.99	ns
LVCMOS12, QUIETIO, 8 mA	0.98	1.16	4.43	4.63	4.43	4.63	ns
LVCMOS12, QUIETIO, 12 mA	0.98	1.16	4.18	4.38	4.18	4.38	ns
LVCMOS12, Slow, 2 mA	0.98	1.16	5.12	5.32	5.12	5.32	ns
LVCMOS12, Slow, 4 mA	0.98	1.16	3.00	3.20	3.00	3.20	ns
LVCMOS12, Slow, 6 mA	0.98	1.16	2.91	3.11	2.91	3.11	ns
LVCMOS12, Slow, 8 mA	0.98	1.16	2.51	2.71	2.51	2.71	ns
LVCMOS12, Slow, 12 mA	0.98	1.16	2.25	2.45	2.25	2.45	ns
LVCMOS12, Fast, 2 mA	0.98	1.16	3.60	3.80	3.60	3.80	ns
LVCMOS12, Fast, 4 mA	0.98	1.16	2.49	2.69	2.49	2.69	ns
LVCMOS12, Fast, 6 mA	0.98	1.16	1.94	2.14	1.94	2.14	ns
LVCMOS12, Fast, 8 mA	0.98	1.16	1.82	2.02	1.82	2.02	ns
LVCMOS12, Fast, 12 mA	0.98	1.16	1.80	2.00	1.80	2.00	ns
LVCMOS12_JEDEC, QUIETIO, 2 mA	1.57	1.75	6.53	6.73	6.53	6.73	ns
LVCMOS12_JEDEC, QUIETIO, 4 mA	1.57	1.75	5.12	5.32	5.12	5.32	ns
LVCMOS12_JEDEC, QUIETIO, 6 mA	1.57	1.75	4.81	5.01	4.81	5.01	ns
LVCMOS12_JEDEC, QUIETIO, 8 mA	1.57	1.75	4.44	4.64	4.44	4.64	ns
LVCMOS12_JEDEC, QUIETIO, 12 mA	1.57	1.75	4.20	4.40	4.20	4.40	ns
LVCMOS12_JEDEC, Slow, 2 mA	1.57	1.75	5.14	5.34	5.14	5.34	ns
LVCMOS12_JEDEC, Slow, 4 mA	1.57	1.75	2.99	3.19	2.99	3.19	ns
LVCMOS12_JEDEC, Slow, 6 mA	1.57	1.75	2.90	3.10	2.90	3.10	ns
LVCMOS12_JEDEC, Slow, 8 mA	1.57	1.75	2.50	2.70	2.50	2.70	ns
LVCMOS12_JEDEC, Slow, 12 mA	1.57	1.75	2.26	2.46	2.26	2.46	ns
LVCMOS12_JEDEC, Fast, 2 mA	1.57	1.75	3.60	3.80	3.60	3.80	ns
LVCMOS12_JEDEC, Fast, 4 mA	1.57	1.75	2.49	2.69	2.49	2.69	ns
LVCMOS12_JEDEC, Fast, 6 mA	1.57	1.75	1.94	2.14	1.94	2.14	ns
LVCMOS12_JEDEC, Fast, 8 mA	1.57	1.75	1.83	2.03	1.83	2.03	ns
LVCMOS12_JEDEC, Fast, 12 mA	1.57	1.75	1.80	2.00	1.80	2.00	ns

Notes:

1. The Spartan-6Q FPGA -1L values are listed in Table 28.

Table 30 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). These delays are measured using LVCMOS25, Fast, 12 mA.

Table 30: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T_{IOTPHZ}	T input to Pad high-impedance	1.39	1.59	1.59	1.91	ns

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 4 and Figure 5.

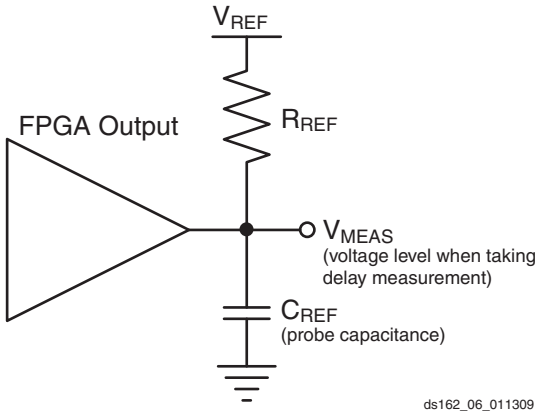

Figure 4: **Single-Ended Test Setup**

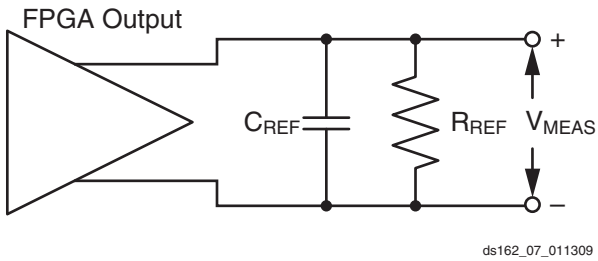

Figure 5: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 32.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 32: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF} (1) (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.4	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
PCI (Peripheral Component Interface) 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3 (rising edge)	25	10 (2)	0.94	0
	PCI33_3, PCI66_3 (falling edge)	25	10 (2)	2.03	3.3
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25

Table 34: **SSO Limit per V_{CCO}/GND Pair *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
2.5V	LVCMOS25	2	Fast	38	43	38	43
			Slow	46	52	46	48
			QuietIO	57	64	57	59
		4	Fast	21	24	21	23
			Slow	26	31	26	27
			QuietIO	33	32	33	30
		6	Fast	15	17	15	16
			Slow	19	22	19	19
			QuietIO	25	23	25	19
		8	Fast	12	15	12	14
			Slow	15	18	15	16
			QuietIO	21	19	21	16
		12	Fast	1	3	1	1
			Slow	2	7	2	4
			QuietIO	3	8	3	8
		16	Fast	1	3	1	1
			Slow	3	7	3	3
			QuietIO	4	9	4	8
		24	Fast	N/A	3	N/A	1
			Slow	N/A	5	N/A	2
			QuietIO	N/A	8	N/A	6
	SSTL_2_I (3)			10	11	10	11
	SSTL_2_II (3)			N/A	7	N/A	7
	DIFF_SSTL_2_I (3)			30	33	30	33
	DIFF_SSTL_2_II (3)			N/A	21	N/A	24

Table 34: **SSO Limit per V_{CCO}/GND Pair *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
3.3V	LVCMOS33	2	Fast	42	46	42	44
			Slow	50	55	50	49
			QuietIO	60	68	60	60
		4	Fast	21	27	21	25
			Slow	32	37	32	32
			QuietIO	39	42	39	37
		6	Fast	14	19	14	17
			Slow	19	25	19	22
			QuietIO	29	30	29	25
		8	Fast	11	15	11	14
			Slow	15	20	15	18
			QuietIO	25	24	25	20
		12	Fast	1	3	1	1
			Slow	2	5	2	2
			QuietIO	4	9	4	7
		16	Fast	1	2	1	1
			Slow	1	5	1	1
			QuietIO	3	10	3	8
		24	Fast	1	2	1	1
			Slow	2	5	2	1
			QuietIO	7	9	7	7

Input/Output Logic Switching Characteristics

Table 35: **ILOGIC2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T_{ICE0CK}/T_{ICKCE0}	CE0 pin Setup/Hold with respect to CLK	0.56/ –0.30	0.56/ –0.25	0.79/ –0.22	1.21/ –0.52	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.74/ –0.23	0.74/ –0.22	0.98/ –0.20	1.31/ –0.45	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	1.19/ –0.83	1.36/ –0.83	1.73/ –0.83	2.18/ –1.77	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	0.31/ 0.00	0.47/ 0.00	0.54/ 0.00	0.63/ –0.39	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.95	1.28	1.53	2.25	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY2)	0.23	0.39	0.44	0.74	ns
Sequential Delays						
T_{IDLO}	D pin to Q pin using flip-flop as a latch without Delay	1.56	1.86	2.39	3.49	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY2)	0.68	0.97	1.20	1.94	ns
T_{ICKQ}	CLK to Q outputs for XC devices	1.03	1.24	1.43	2.11	ns
	CLK to Q outputs for XA and XQ devices	1.38	N/A	1.78	2.11	ns
$T_{RQ\_ILOGIC2}$	SR pin to Q outputs	1.81	1.81	2.50	3.05	ns

Table 36: **OLOGIC2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.81/ –0.05	0.86/ –0.05	1.18/ 0.00	1.73/ –0.27	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.75/ –0.10	0.75/ –0.10	1.01/ –0.05	1.66/ –0.23	ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.70/ –0.28	0.79/ –0.28	1.03/ –0.23	1.39/ –0.47	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.24/ –0.08	0.56/ –0.06	0.83/ –0.01	0.99/ –0.19	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.58/ –0.06	0.72/ –0.06	1.18/ –0.01	1.51/ –0.13	ns
Sequential Delays						
T_{OCKQ}	CLK to OQ/TQ out for XC devices	0.48	0.51	0.74	0.74	ns
	CLK to OQ/TQ out for XA and XQ devices	0.85	N/A	1.16	0.74	ns
$T_{RQ\_OLOGIC2}$	SR pin to OQ/TQ out	1.81	1.81	2.50	3.05	ns

Table 52: **PLL Specification *(Cont'd)***

Symbol	Description	Device[1]	Speed Grade				Units
			-3	-3N	-2	-1L	
F_{INMIN}	Minimum Input Clock Frequency	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter: 19–200 MHz	All	1 ns Maximum				
	Maximum Input Clock Period Jitter: > 200 MHz	All	<20% of clock input period Maximum				
F_{INDUTY}	Allowable Input Duty Cycle: 19—199 MHz	All	25/75				%
	Allowable Input Duty Cycle: 200—299 MHz	All	35/65				%
	Allowable Input Duty Cycle: > 300 MHz	All	45/55				%
F_{VCOMIN}	Minimum PLL VCO Frequency	LX devices	400	400	400	400	MHz
		LXT devices	400	400	400	N/A	MHz
F_{VCOMAX}	Maximum PLL VCO Frequency	LX devices	1080	1050	1000	1000	MHz
		LXT devices	1080	1050	1000	N/A	MHz
$F_{BANDWIDTH}$	Low PLL Bandwidth at Typical[3]	All	1	1	1	1	MHz
	High PLL Bandwidth at Typical[3]	All	4	4	4	4	MHz
$T_{STAPHAOFFSET}$	Static Phase Offset of the PLL Outputs	All	0.12	0.12	0.12	0.15	ns
$T_{OUTJITTER}$	PLL Output Jitter[3]	All	Note 2				
$T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision[4]	All	0.15	0.15	0.20	0.25	ns
$T_{LOCKMAX}$	PLL Maximum Lock Time	All	100	100	100	100	µs
F_{OUTMAX}	PLL Maximum Output Frequency for BUFGMUX	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz
	PLL Maximum Output Frequency for BUFPLL	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz
F_{OUTMIN}	PLL Minimum Output Frequency[5]	All	3.125	3.125	3.125	3.125	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation: 19–200 MHz	All	1 ns Maximum				
	External Clock Feedback Variation: > 200 MHz	All	< 20% of clock input period Maximum				
$RST_{MINPULSE}$	Minimum Reset Pulse Width	All	5	5	5	5	ns
F_{PFDMAX}[5]	Maximum Frequency at the Phase Frequency Detector	LX devices	500	500	400	300	MHz
		LXT devices	500	500	400	N/A	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	All	3 ns Max or one CLKIN cycle				

Notes:

1. LXT devices are not available with a -1L speed grade.
2. Values for this parameter are available in the Clocking Wizard.
3. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When using CLK_FEEDBACK = CLKOUT0 with BUFIO2 feedback, the feedback frequency will be higher than the phase frequency detector frequency. $F_{PFDMAX} = F_{CLKFB}$ / CLKFBOUT_MULT

Table 57: **Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)[1]**

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges (DCM_CLKGEN)										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz
CLKOUT_FREQ_FXDV	Frequency for the CLKFXDV output	0.15625	187.5	0.15625	187.5	0.15625	166.5	0.15625	100	MHz
Output Clock Jitter[2][3]										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKOUT_PER_JITT_FXDV	Period jitter at the CLKFXDV output.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKFX_FREEZE_VAR	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX > 50 MHz	Maximum = ±3% of CLKFX period								ps
	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX < 50 MHz	Maximum = ±5% of CLKFX period								ps
CLKFX_FREEZE_TEMP_SLOPE	CLKFX period will change in free_oscillator mode over temperature. Add to CLKFX_FREEZE_VAR to determine total CLKFX period change. Percentage change for CLKFX period over 1°C.	Maximum = 0.1								%/°C
Duty Cycle[4][5]										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
CLKOUT_DUTY_CYCLE_FXDV	Duty cycle precision for the CLKFXDV outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
Lock Time										
LOCK_FX[2]	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX, CLKFX180, and CLKFXDV signals are valid. Lock time requires CLKFX_DIVIDE < F_{IN}/(0.50 MHz) when: F_{CLKIN} < 50 MHz	–	50	–	50	–	50	–	50	ms
	when: F_{CLKIN} > 50 MHz	–	5	–	5	–	5	–	5	ms

Spartan-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 63 through Table 69. Values are expressed in nanoseconds unless otherwise noted.

Table 63: **Global Clock Input to Output Delay Without DCM or PLL**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* DCM or PLL							
T_{ICKOF}	Global Clock and OUTFF *without* DCM or PLL	XC6SLX4	6.12	N/A	7.68	9.41	ns
		XC6SLX9	6.12	6.51	7.68	9.41	ns
		XC6SLX16	5.98	6.42	7.48	9.10	ns
		XC6SLX25	6.20	6.69	7.84	9.44	ns
		XC6SLX25T	6.20	6.69	7.84	N/A	ns
		XC6SLX45	6.37	6.88	8.10	9.61	ns
		XC6SLX45T	6.37	6.88	8.10	N/A	ns
		XC6SLX75	6.39	6.99	8.16	10.18	ns
		XC6SLX75T	6.39	6.99	8.16	N/A	ns
		XC6SLX100	6.59	7.18	8.41	10.31	ns
		XC6SLX100T	6.59	7.18	8.41	N/A	ns
		XC6SLX150	6.98	7.68	8.80	10.62	ns
		XC6SLX150T	6.98	7.68	8.80	N/A	ns
		XA6SLX4	6.44	N/A	7.68	N/A	ns
		XA6SLX9	6.44	N/A	7.68	N/A	ns
		XA6SLX16	6.30	N/A	7.48	N/A	ns
		XA6SLX25	6.52	N/A	7.84	N/A	ns
		XA6SLX25T	6.52	N/A	7.84	N/A	ns
		XA6SLX45	6.69	N/A	8.12	N/A	ns
		XA6SLX45T	6.69	N/A	8.12	N/A	ns
		XA6SLX75	6.89	N/A	8.16	N/A	ns
		XA6SLX75T	6.89	N/A	8.16	N/A	ns
		XA6SLX100	N/A	N/A	8.36	N/A	ns
		XQ6SLX75	N/A	N/A	8.16	10.18	ns
		XQ6SLX75T	6.89	N/A	8.16	N/A	ns
		XQ6SLX150	N/A	N/A	8.80	10.62	ns
		XQ6SLX150T	7.61	N/A	8.80	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 67: **Global Clock Input to Output Delay With PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* PLL in Source-Synchronous Mode.							
$T_{ICKOFPLL\_0}$	Global Clock and OUTFF *with* PLL	XC6SLX4	5.49	N/A	7.44	8.55	ns
		XC6SLX9	5.49	6.29	7.44	8.55	ns
		XC6SLX16	5.23	5.77	6.79	8.21	ns
		XC6SLX25	5.00	5.35	6.10	8.54	ns
		XC6SLX25T	5.00	5.35	6.10	N/A	ns
		XC6SLX45	5.59	6.03	7.02	8.39	ns
		XC6SLX45T	5.59	6.03	7.02	N/A	ns
		XC6SLX75	4.96	5.41	6.22	8.32	ns
		XC6SLX75T	4.96	5.41	6.22	N/A	ns
		XC6SLX100	4.97	5.42	6.21	9.08	ns
		XC6SLX100T	5.01	5.42	6.21	N/A	ns
		XC6SLX150	4.59	5.06	5.86	8.13	ns
		XC6SLX150T	4.59	5.06	5.86	N/A	ns
		XA6SLX4	5.79	N/A	7.32	N/A	ns
		XA6SLX9	5.79	N/A	7.32	N/A	ns
		XA6SLX16	5.56	N/A	6.66	N/A	ns
		XA6SLX25	5.40	N/A	5.97	N/A	ns
		XA6SLX25T	5.40	N/A	6.07	N/A	ns
		XA6SLX45	5.89	N/A	6.90	N/A	ns
		XA6SLX45T	5.89	N/A	6.90	N/A	ns
		XA6SLX75	5.27	N/A	6.12	N/A	ns
		XA6SLX75T	5.27	N/A	6.12	N/A	ns
		XA6SLX100	N/A	N/A	6.80	N/A	ns
		XQ6SLX75	N/A	N/A	6.12	8.32	ns
		XQ6SLX75T	5.27	N/A	6.12	N/A	ns
		XQ6SLX150	N/A	N/A	5.88	8.13	ns
		XQ6SLX150T	5.21	N/A	5.88	N/A	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Spartan-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 70 through Table 77. Values are expressed in nanoseconds unless otherwise noted.

Table 70: **Global Clock Setup and Hold Without DCM or PLL (No Delay)**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSND}/ T_{PHND}	No Delay Global Clock and IFF(3) without DCM or PLL	XC6SLX4	0.10/1.56	N/A	0.10/1.83	0.07/2.54	ns
		XC6SLX9	0.10/1.56	0.10/1.57	0.10/1.84	0.07/2.54	ns
		XC6SLX16	0.12/1.42	0.12/1.48	0.12/1.64	0.13/2.19	ns
		XC6SLX25	0.18/1.64	0.18/1.75	0.18/1.99	0.11/2.57	ns
		XC6SLX25T	0.18/1.64	0.18/1.75	0.18/1.99	N/A	ns
		XC6SLX45	–0.08/1.80	–0.08/1.95	–0.08/2.27	–0.17/2.74	ns
		XC6SLX45T	–0.08/1.80	–0.08/1.95	–0.08/2.27	N/A	ns
		XC6SLX75	0.13/1.81	0.13/2.06	0.13/2.27	–0.12/3.30	ns
		XC6SLX75T	0.13/1.81	0.13/2.06	0.13/2.27	N/A	ns
		XC6SLX100	–0.14/2.03	–0.14/2.24	–0.14/2.56	–0.17/3.44	ns
		XC6SLX100T	–0.14/2.03	–0.14/2.24	–0.14/2.56	N/A	ns
		XC6SLX150	–0.24/2.42	–0.24/2.74	–0.24/2.95	–0.60/3.75	ns
		XC6SLX150T	–0.24/2.42	–0.24/2.74	–0.24/2.95	N/A	ns
		XA6SLX4	0.10/1.57	N/A	0.10/1.84	N/A	ns
		XA6SLX9	0.10/1.57	N/A	0.10/1.84	N/A	ns
		XA6SLX16	0.12/1.43	N/A	0.12/1.64	N/A	ns
		XA6SLX25	0.18/1.65	N/A	0.18/1.99	N/A	ns
		XA6SLX25T	0.18/1.65	N/A	0.18/1.99	N/A	ns
		XA6SLX45	–0.08/1.82	N/A	–0.08/2.27	N/A	ns
		XA6SLX45T	–0.08/1.82	N/A	–0.08/2.27	N/A	ns
		XA6SLX75	0.13/2.02	N/A	0.13/2.32	N/A	ns
		XA6SLX75T	0.13/2.02	N/A	0.13/2.32	N/A	ns
		XA6SLX100	N/A	N/A	0.10/2.51	N/A	ns
		XQ6SLX75	N/A	N/A	0.13/2.32	–0.12/3.30	ns
		XQ6SLX75T	0.13/2.02	N/A	0.13/2.32	N/A	ns
		XQ6SLX150	N/A	N/A	–0.24/2.95	–0.60/3.75	ns
		XQ6SLX150T	–0.24/2.74	N/A	–0.24/2.95	N/A	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.

Table 73: **Global Clock Setup and Hold With DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSDCM0}/ T_{PHDCM0}	No Delay Global Clock and IFF(2) with DCM in Source-Synchronous Mode	XC6SLX4	0.71/0.65	N/A	0.72/1.22	1.58/1.18	ns
		XC6SLX9	0.71/0.69	0.71/1.19	0.72/1.36	1.58/1.18	ns
		XC6SLX16	0.86/0.52	0.92/0.57	1.04/0.60	1.02/1.06	ns
		XC6SLX25	0.84/0.58	0.90/0.59	1.01/0.59	1.58/1.07	ns
		XC6SLX25T	0.84/0.58	0.90/0.59	1.01/0.59	N/A	ns
		XC6SLX45	0.85/0.70	0.90/0.76	0.98/0.79	1.34/1.34	ns
		XC6SLX45T	0.85/0.70	0.90/0.76	0.98/0.79	N/A	ns
		XC6SLX75	1.00/0.62	1.06/0.63	1.15/0.63	1.65/1.46	ns
		XC6SLX75T	1.00/0.71	1.06/0.72	1.15/0.72	N/A	ns
		XC6SLX100	0.81/0.68	0.81/0.69	0.94/0.69	1.42/2.07	ns
		XC6SLX100T	0.81/0.68	0.81/0.69	0.94/0.69	N/A	ns
		XC6SLX150	0.68/0.98	0.69/0.99	0.79/0.99	1.45/1.60	ns
		XC6SLX150T	0.68/0.98	0.69/0.99	0.79/0.99	N/A	ns
		XA6SLX4	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX9	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX16	1.01/0.56	N/A	1.04/0.60	N/A	ns
		XA6SLX25	0.94/0.76	N/A	1.06/0.77	N/A	ns
		XA6SLX25T	0.94/0.76	N/A	1.14/0.77	N/A	ns
		XA6SLX45	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX45T	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX75	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX100	N/A	N/A	1.37/0.75	N/A	ns
		XQ6SLX75	N/A	N/A	1.15/0.72	1.65/1.46	ns
		XQ6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XQ6SLX150	N/A	N/A	0.79/1.15	1.45/1.60	ns
		XQ6SLX150T	0.73/1.15	N/A	0.79/1.15	N/A	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 76: **Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
$T_{PSDCMPLL}$/ $T_{PHDCMPLL}$	No Delay Global Clock and IFF(2) with DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.	XC6SLX4	1.16/0.49	N/A	1.39/0.49	2.36/0.59	ns
		XC6SLX9	1.16/0.44	1.37/0.44	1.39/0.44	2.36/0.59	ns
		XC6SLX16	1.44/–0.08	1.49/–0.04	1.62/–0.04	2.06/0.55	ns
		XC6SLX25	1.52/0.42	1.65/0.42	1.83/0.42	2.52/0.43	ns
		XC6SLX25T	1.52/0.42	1.65/0.42	1.83/0.42	N/A	ns
		XC6SLX45	1.54/0.39	1.59/0.39	1.75/0.39	2.48/0.76	ns
		XC6SLX45T	1.54/0.39	1.59/0.39	1.75/0.39	N/A	ns
		XC6SLX75	1.72/0.41	1.80/0.41	1.99/0.41	2.60/0.75	ns
		XC6SLX75T	1.72/0.41	1.80/0.41	1.99/0.41	N/A	ns
		XC6SLX100	1.34/0.51	1.46/0.51	1.64/0.51	2.12/0.90	ns
		XC6SLX100T	1.34/0.51	1.46/0.51	1.64/0.51	N/A	ns
		XC6SLX150	1.30/0.60	1.40/0.60	1.55/0.60	2.57/0.97	ns
		XC6SLX150T	1.30/0.60	1.40/0.60	1.55/0.60	N/A	ns
		XA6SLX4	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX9	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX16	2.67/0.35	N/A	2.67/0.17	N/A	ns
		XA6SLX25	1.74/0.27	N/A	1.95/0.27	N/A	ns
		XA6SLX25T	1.74/0.27	N/A	2.03/0.27	N/A	ns
		XA6SLX45	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX45T	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX75	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX100	N/A	N/A	2.64/0.82	N/A	ns
		XQ6SLX75	N/A	N/A	2.11/0.24	2.60/0.75	ns
		XQ6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XQ6SLX150	N/A	N/A	1.67/0.70	2.57/0.97	ns
		XQ6SLX150T	1.50/0.70	N/A	1.67/0.70	N/A	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.