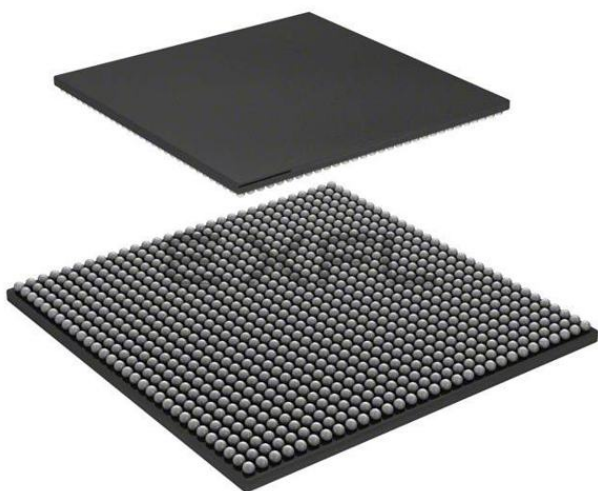




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	11519
Number of Logic Elements/Cells	147443
Total RAM Bits	4939776
Number of I/O	540
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx150t-3fgg900i

SelectIO™ Interface DC Input and Output Levels

Table 7: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

I/O Standard	V _{CCO} for Drivers ⁽¹⁾			V _{REF} for Inputs		
	V, Min	V, Nom	V, Max	V, Min	V, Nom	V, Max
LVTTTL	3.0	3.3	3.45	V _{REF} is not used for these I/O standards		
LVC MOS33	3.0	3.3	3.45			
LVC MOS25	2.3	2.5	2.7			
LVC MOS18	1.65	1.8	1.95			
LVC MOS18_JEDEC	1.65	1.8	1.95			
LVC MOS15	1.4	1.5	1.6			
LVC MOS15_JEDEC	1.4	1.5	1.6			
LVC MOS12	1.1	1.2	1.3			
LVC MOS12_JEDEC	1.1	1.2	1.3			
PCI33_3 ⁽²⁾	3.0	3.3	3.45			
PCI66_3 ⁽²⁾	3.0	3.3	3.45			
I2C	2.7	3.0	3.45			
SMBUS	2.7	3.0	3.45			
SDIO	3.0	3.3	3.45			
MOBILE_DDR	1.7	1.8	1.9			
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_II	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_III	1.4	1.5	1.6	–	0.9	–
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–
HSTL_III_18	1.7	1.8	1.9	–	1.1	–
SSTL3_I	3.0	3.3	3.45	1.3	1.5	1.7
SSTL3_II	3.0	3.3	3.45	1.3	1.5	1.7
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38
SSTL18_I	1.7	1.8	1.9	0.833	0.9	0.969
SSTL18_II	1.7	1.8	1.9	0.833	0.9	0.969
SSTL15_II	1.425	1.5	1.575	0.69	0.75	0.81

Notes:

1. V_{CCO} range required when using I/O standard for an output. Also required for MOBILE_DDR, PCI33_3, LVC MOS18_JEDEC, LVC MOS15_JEDEC, and LVC MOS12_JEDEC inputs, and for LVC MOS25 inputs when V_{CCAUX} = 3.3V.
2. For PCI systems, the transmitter and receiver should have common supplies for V_{CCO}.

In Table 9 and Table 10, values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: Single-Ended I/O Standard DC Input and Output Levels

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTTL	−0.5	0.8	2.0	4.1	0.4	2.4	Note 2	Note 2
LVC MOS33	−0.5	0.8	2.0	4.1	0.4	$V_{CCO} - 0.4$	Note 2	Note 2
LVC MOS25	−0.5	0.7	1.7	4.1	0.4	$V_{CCO} - 0.4$	Note 2	Note 2
LVC MOS18	−0.5	0.38	0.8	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS18 (−1L)	−0.5	0.33	0.71	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS18_JEDEC	−0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS15	−0.5	0.38	0.8	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVC MOS15 (−1L)	−0.5	0.33	0.71	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVC MOS15_JEDEC	−0.5	35% V_{CCO}	65% V_{CCO}	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVC MOS12	−0.5	0.38	0.8	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
LVC MOS12 (−1L)	−0.5	0.33	0.71	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
LVC MOS12_JEDEC	−0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
PCI33_3	−0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	1.5	−0.5
PCI66_3	−0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	1.5	−0.5
I2C	−0.5	25% V_{CCO}	70% V_{CCO}	4.1	20% V_{CCO}	—	3	—
SMBUS	−0.5	0.8	2.1	4.1	0.4	—	4	—
SDIO	−0.5	12.5% V_{CCO}	75% V_{CCO}	4.1	12.5% V_{CCO}	75% V_{CCO}	0.1	−0.1
MOBILE_DDR	−0.5	20% V_{CCO}	80% V_{CCO}	4.1	10% V_{CCO}	90% V_{CCO}	0.1	−0.1
HSTL_I	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	8	−8
HSTL_II	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	16	−16
HSTL_III	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	24	−8
HSTL_I_18	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	11	−11
HSTL_II_18	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	22	−22
HSTL_III_18	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	30	−11
SSTL3_I	−0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	4.1	$V_{TT} - 0.6$	$V_{TT} + 0.6$	8	−8
SSTL3_II	−0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	4.1	$V_{TT} - 0.8$	$V_{TT} + 0.8$	16	−16
SSTL2_I	−0.5	$V_{REF} - 0.15$	$V_{REF} + 0.15$	4.1	$V_{TT} - 0.61$	$V_{TT} + 0.61$	8.1	−8.1
SSTL2_II	−0.5	$V_{REF} - 0.15$	$V_{REF} + 0.15$	4.1	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	−16.2
SSTL18_I	−0.5	$V_{REF} - 0.125$	$V_{REF} + 0.125$	4.1	$V_{TT} - 0.47$	$V_{TT} + 0.47$	6.7	−6.7
SSTL18_II	−0.5	$V_{REF} - 0.125$	$V_{REF} + 0.125$	4.1	$V_{TT} - 0.60$	$V_{TT} + 0.60$	13.4	−13.4
SSTL15_II	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	$V_{TT} - 0.4$	$V_{TT} + 0.4$	13.4	−13.4

Notes:

1. Tested according to relevant specifications.
2. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
3. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
4. Using drive strengths of 2, 4, 6, 8, or 12 mA.
5. For more information, refer to [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.

eFUSE Read Endurance

Table 11 lists the minimum guaranteed number of read cycle operations for Device DNA and for the AES eFUSE key. For more information, see [UG380: Spartan-6 FPGA Configuration User Guide](#).

Table 11: eFUSE Read Endurance

Symbol	Description	Speed Grade				Units (Min)
		-3	-3N	-2	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTP Transceiver Specifications

GTP transceivers are available in the Spartan-6 LXT devices. See [DS160: Spartan-6 Family Overview](#) for more information.

GTP Transceiver DC Characteristics

Table 12: Absolute Maximum Ratings for GTP Transceivers⁽¹⁾

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	-0.5	1.32	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	-0.5	1.32	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	-0.5	1.32	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	-0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	-0.5	1.32	V
V _{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	-0.5	1.32	V
V _{MGTREFCLK}	Reference clock absolute input voltage	-0.5	1.32	V

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 13: Recommended Operating Conditions for GTP Transceivers⁽¹⁾⁽²⁾⁽³⁾

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	1.14	1.20	1.26	V

Notes:

- Each voltage listed requires the filter circuit described in [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#).
- Voltages are specified for the temperature range of T_j = -40°C to +125°C.
- The voltage level of MGTAVCCPLL must not exceed the voltage level of MGTAVCC +10mV. The voltage level of MGTAVCC must not exceed the voltage level of MGTAVCCPLL.

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVC MOS18, Slow, 24 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVC MOS18, Fast, 2 mA	1.18	1.30	1.43	2.04	3.59	3.73	3.93	4.53	3.59	3.73	3.93	4.53	ns
LVC MOS18, Fast, 4 mA	1.18	1.30	1.43	2.04	2.39	2.53	2.73	3.35	2.39	2.53	2.73	3.35	ns
LVC MOS18, Fast, 6 mA	1.18	1.30	1.43	2.04	1.88	2.02	2.22	2.84	1.88	2.02	2.22	2.84	ns
LVC MOS18, Fast, 8 mA	1.18	1.30	1.43	2.04	1.81	1.95	2.15	2.77	1.81	1.95	2.15	2.77	ns
LVC MOS18, Fast, 12 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVC MOS18, Fast, 16 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVC MOS18, Fast, 24 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVC MOS18_JEDEC, QUIETIO, 2 mA	0.94	1.06	1.19	1.41	5.91	6.05	6.25	6.79	5.91	6.05	6.25	6.79	ns
LVC MOS18_JEDEC, QUIETIO, 4 mA	0.94	1.06	1.19	1.41	4.75	4.89	5.09	5.64	4.75	4.89	5.09	5.64	ns
LVC MOS18_JEDEC, QUIETIO, 6 mA	0.94	1.06	1.19	1.41	4.04	4.18	4.38	4.96	4.04	4.18	4.38	4.96	ns
LVC MOS18_JEDEC, QUIETIO, 8 mA	0.94	1.06	1.19	1.41	3.71	3.85	4.05	4.62	3.71	3.85	4.05	4.62	ns
LVC MOS18_JEDEC, QUIETIO, 12 mA	0.94	1.06	1.19	1.41	3.35	3.49	3.69	4.28	3.35	3.49	3.69	4.28	ns
LVC MOS18_JEDEC, QUIETIO, 16 mA	0.94	1.06	1.19	1.41	3.20	3.34	3.54	4.13	3.20	3.34	3.54	4.13	ns
LVC MOS18_JEDEC, QUIETIO, 24 mA	0.94	1.06	1.19	1.41	2.96	3.10	3.30	3.98	2.96	3.10	3.30	3.98	ns
LVC MOS18_JEDEC, Slow, 2 mA	0.94	1.06	1.19	1.41	4.59	4.73	4.93	5.54	4.59	4.73	4.93	5.54	ns
LVC MOS18_JEDEC, Slow, 4 mA	0.94	1.06	1.19	1.41	3.69	3.83	4.03	4.60	3.69	3.83	4.03	4.60	ns
LVC MOS18_JEDEC, Slow, 6 mA	0.94	1.06	1.19	1.41	3.00	3.14	3.34	3.94	3.00	3.14	3.34	3.94	ns
LVC MOS18_JEDEC, Slow, 8 mA	0.94	1.06	1.19	1.41	2.19	2.33	2.53	3.18	2.19	2.33	2.53	3.18	ns
LVC MOS18_JEDEC, Slow, 12 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVC MOS18_JEDEC, Slow, 16 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVC MOS18_JEDEC, Slow, 24 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVC MOS18_JEDEC, Fast, 2 mA	0.94	1.06	1.19	1.41	3.57	3.71	3.91	4.52	3.57	3.71	3.91	4.52	ns
LVC MOS18_JEDEC, Fast, 4 mA	0.94	1.06	1.19	1.41	2.39	2.53	2.73	3.35	2.39	2.53	2.73	3.35	ns
LVC MOS18_JEDEC, Fast, 6 mA	0.94	1.06	1.19	1.41	1.88	2.02	2.22	2.84	1.88	2.02	2.22	2.84	ns
LVC MOS18_JEDEC, Fast, 8 mA	0.94	1.06	1.19	1.41	1.80	1.94	2.14	2.76	1.80	1.94	2.14	2.76	ns
LVC MOS18_JEDEC, Fast, 12 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVC MOS18_JEDEC, Fast, 16 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVC MOS18_JEDEC, Fast, 24 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVC MOS15, QUIETIO, 2 mA	0.98	1.10	1.23	1.79	5.47	5.61	5.81	6.38	5.47	5.61	5.81	6.38	ns
LVC MOS15, QUIETIO, 4 mA	0.98	1.10	1.23	1.79	4.61	4.75	4.95	5.51	4.61	4.75	4.95	5.51	ns
LVC MOS15, QUIETIO, 6 mA	0.98	1.10	1.23	1.79	4.07	4.21	4.41	4.97	4.07	4.21	4.41	4.97	ns
LVC MOS15, QUIETIO, 8 mA	0.98	1.10	1.23	1.79	3.91	4.05	4.25	4.81	3.91	4.05	4.25	4.81	ns
LVC MOS15, QUIETIO, 12 mA	0.98	1.10	1.23	1.79	3.53	3.67	3.87	4.51	3.53	3.67	3.87	4.51	ns
LVC MOS15, QUIETIO, 16 mA	0.98	1.10	1.23	1.79	3.32	3.46	3.66	4.31	3.32	3.46	3.66	4.31	ns
LVC MOS15, Slow, 2 mA	0.98	1.10	1.23	1.79	4.18	4.32	4.52	5.11	4.18	4.32	4.52	5.11	ns
LVC MOS15, Slow, 4 mA	0.98	1.10	1.23	1.79	3.42	3.56	3.76	4.34	3.42	3.56	3.76	4.34	ns
LVC MOS15, Slow, 6 mA	0.98	1.10	1.23	1.79	2.29	2.43	2.63	3.24	2.29	2.43	2.63	3.24	ns

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVC MOS12, Fast, 2 mA	0.91	1.03	1.16	1.51	3.46	3.60	3.80	4.44	3.46	3.60	3.80	4.44	ns
LVC MOS12, Fast, 4 mA	0.91	1.03	1.16	1.51	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVC MOS12, Fast, 6 mA	0.91	1.03	1.16	1.51	1.79	1.93	2.13	2.75	1.79	1.93	2.13	2.75	ns
LVC MOS12, Fast, 8 mA	0.91	1.03	1.16	1.51	1.68	1.82	2.02	2.64	1.68	1.82	2.02	2.64	ns
LVC MOS12, Fast, 12 mA	0.91	1.03	1.16	1.51	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
LVC MOS12_JEDEC, QUIETIO, 2 mA	1.50	1.62	1.75	1.88	6.39	6.53	6.73	7.31	6.39	6.53	6.73	7.31	ns
LVC MOS12_JEDEC, QUIETIO, 4 mA	1.50	1.62	1.75	1.88	4.98	5.12	5.32	5.88	4.98	5.12	5.32	5.88	ns
LVC MOS12_JEDEC, QUIETIO, 6 mA	1.50	1.62	1.75	1.88	4.67	4.81	5.01	5.54	4.67	4.81	5.01	5.54	ns
LVC MOS12_JEDEC, QUIETIO, 8 mA	1.50	1.62	1.75	1.88	4.23	4.37	4.57	5.22	4.23	4.37	4.57	5.22	ns
LVC MOS12_JEDEC, QUIETIO, 12 mA	1.50	1.62	1.75	1.88	3.99	4.13	4.33	4.94	3.99	4.13	4.33	4.94	ns
LVC MOS12_JEDEC, Slow, 2 mA	1.50	1.62	1.75	1.88	5.00	5.14	5.34	5.90	5.00	5.14	5.34	5.90	ns
LVC MOS12_JEDEC, Slow, 4 mA	1.50	1.62	1.75	1.88	2.85	2.99	3.19	3.80	2.85	2.99	3.19	3.80	ns
LVC MOS12_JEDEC, Slow, 6 mA	1.50	1.62	1.75	1.88	2.76	2.90	3.10	3.72	2.76	2.90	3.10	3.72	ns
LVC MOS12_JEDEC, Slow, 8 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVC MOS12_JEDEC, Slow, 12 mA	1.50	1.62	1.75	1.88	2.09	2.23	2.43	3.05	2.09	2.23	2.43	3.05	ns
LVC MOS12_JEDEC, Fast, 2 mA	1.50	1.62	1.75	1.88	3.46	3.60	3.80	4.42	3.46	3.60	3.80	4.42	ns
LVC MOS12_JEDEC, Fast, 4 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns
LVC MOS12_JEDEC, Fast, 6 mA	1.50	1.62	1.75	1.88	1.79	1.93	2.13	2.76	1.79	1.93	2.13	2.76	ns
LVC MOS12_JEDEC, Fast, 8 mA	1.50	1.62	1.75	1.88	1.69	1.83	2.03	2.65	1.69	1.83	2.03	2.65	ns
LVC MOS12_JEDEC, Fast, 12 mA	1.50	1.62	1.75	1.88	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns

Notes:

1. The -1L values listed in this table are also applicable to the Spartan-6Q devices.
2. Devices with a -1L speed grade do not support Xilinx PCI IP.

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS18, QUIETIO, 16 mA	1.25	1.43	3.34	3.54	3.34	3.54	ns
LVC MOS18, QUIETIO, 24 mA	1.25	1.43	3.18	3.38	3.18	3.38	ns
LVC MOS18, Slow, 2 mA	1.25	1.43	4.79	4.99	4.79	4.99	ns
LVC MOS18, Slow, 4 mA	1.25	1.43	3.84	4.04	3.84	4.04	ns
LVC MOS18, Slow, 6 mA	1.25	1.43	3.17	3.37	3.17	3.37	ns
LVC MOS18, Slow, 8 mA	1.25	1.43	2.37	2.57	2.37	2.57	ns
LVC MOS18, Slow, 12 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns
LVC MOS18, Slow, 16 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns
LVC MOS18, Slow, 24 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns
LVC MOS18, Fast, 2 mA	1.25	1.43	3.78	3.98	3.78	3.98	ns
LVC MOS18, Fast, 4 mA	1.25	1.43	2.54	2.74	2.54	2.74	ns
LVC MOS18, Fast, 6 mA	1.25	1.43	2.02	2.22	2.02	2.22	ns
LVC MOS18, Fast, 8 mA	1.25	1.43	1.95	2.15	1.95	2.15	ns
LVC MOS18, Fast, 12 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns
LVC MOS18, Fast, 16 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns
LVC MOS18, Fast, 24 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns
LVC MOS18_JEDEC, QUIETIO, 2 mA	1.01	1.19	6.09	6.29	6.09	6.29	ns
LVC MOS18_JEDEC, QUIETIO, 4 mA	1.01	1.19	4.89	5.09	4.89	5.09	ns
LVC MOS18_JEDEC, QUIETIO, 6 mA	1.01	1.19	4.20	4.40	4.20	4.40	ns
LVC MOS18_JEDEC, QUIETIO, 8 mA	1.01	1.19	3.87	4.07	3.87	4.07	ns
LVC MOS18_JEDEC, QUIETIO, 12 mA	1.01	1.19	3.49	3.69	3.49	3.69	ns
LVC MOS18_JEDEC, QUIETIO, 16 mA	1.01	1.19	3.34	3.54	3.34	3.54	ns
LVC MOS18_JEDEC, QUIETIO, 24 mA	1.01	1.19	3.17	3.37	3.17	3.37	ns
LVC MOS18_JEDEC, Slow, 2 mA	1.01	1.19	4.79	4.99	4.79	4.99	ns
LVC MOS18_JEDEC, Slow, 4 mA	1.01	1.19	3.84	4.04	3.84	4.04	ns
LVC MOS18_JEDEC, Slow, 6 mA	1.01	1.19	3.18	3.38	3.18	3.38	ns
LVC MOS18_JEDEC, Slow, 8 mA	1.01	1.19	2.37	2.57	2.37	2.57	ns
LVC MOS18_JEDEC, Slow, 12 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns
LVC MOS18_JEDEC, Slow, 16 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns
LVC MOS18_JEDEC, Slow, 24 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns
LVC MOS18_JEDEC, Fast, 2 mA	1.01	1.19	3.75	3.95	3.75	3.95	ns
LVC MOS18_JEDEC, Fast, 4 mA	1.01	1.19	2.54	2.74	2.54	2.74	ns
LVC MOS18_JEDEC, Fast, 6 mA	1.01	1.19	2.02	2.22	2.02	2.22	ns
LVC MOS18_JEDEC, Fast, 8 mA	1.01	1.19	1.94	2.14	1.94	2.14	ns
LVC MOS18_JEDEC, Fast, 12 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns
LVC MOS18_JEDEC, Fast, 16 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns
LVC MOS18_JEDEC, Fast, 24 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS12, QUIETIO, 6 mA	0.98	1.16	4.79	4.99	4.79	4.99	ns
LVC MOS12, QUIETIO, 8 mA	0.98	1.16	4.43	4.63	4.43	4.63	ns
LVC MOS12, QUIETIO, 12 mA	0.98	1.16	4.18	4.38	4.18	4.38	ns
LVC MOS12, Slow, 2 mA	0.98	1.16	5.12	5.32	5.12	5.32	ns
LVC MOS12, Slow, 4 mA	0.98	1.16	3.00	3.20	3.00	3.20	ns
LVC MOS12, Slow, 6 mA	0.98	1.16	2.91	3.11	2.91	3.11	ns
LVC MOS12, Slow, 8 mA	0.98	1.16	2.51	2.71	2.51	2.71	ns
LVC MOS12, Slow, 12 mA	0.98	1.16	2.25	2.45	2.25	2.45	ns
LVC MOS12, Fast, 2 mA	0.98	1.16	3.60	3.80	3.60	3.80	ns
LVC MOS12, Fast, 4 mA	0.98	1.16	2.49	2.69	2.49	2.69	ns
LVC MOS12, Fast, 6 mA	0.98	1.16	1.94	2.14	1.94	2.14	ns
LVC MOS12, Fast, 8 mA	0.98	1.16	1.82	2.02	1.82	2.02	ns
LVC MOS12, Fast, 12 mA	0.98	1.16	1.80	2.00	1.80	2.00	ns
LVC MOS12_JEDEC, QUIETIO, 2 mA	1.57	1.75	6.53	6.73	6.53	6.73	ns
LVC MOS12_JEDEC, QUIETIO, 4 mA	1.57	1.75	5.12	5.32	5.12	5.32	ns
LVC MOS12_JEDEC, QUIETIO, 6 mA	1.57	1.75	4.81	5.01	4.81	5.01	ns
LVC MOS12_JEDEC, QUIETIO, 8 mA	1.57	1.75	4.44	4.64	4.44	4.64	ns
LVC MOS12_JEDEC, QUIETIO, 12 mA	1.57	1.75	4.20	4.40	4.20	4.40	ns
LVC MOS12_JEDEC, Slow, 2 mA	1.57	1.75	5.14	5.34	5.14	5.34	ns
LVC MOS12_JEDEC, Slow, 4 mA	1.57	1.75	2.99	3.19	2.99	3.19	ns
LVC MOS12_JEDEC, Slow, 6 mA	1.57	1.75	2.90	3.10	2.90	3.10	ns
LVC MOS12_JEDEC, Slow, 8 mA	1.57	1.75	2.50	2.70	2.50	2.70	ns
LVC MOS12_JEDEC, Slow, 12 mA	1.57	1.75	2.26	2.46	2.26	2.46	ns
LVC MOS12_JEDEC, Fast, 2 mA	1.57	1.75	3.60	3.80	3.60	3.80	ns
LVC MOS12_JEDEC, Fast, 4 mA	1.57	1.75	2.49	2.69	2.49	2.69	ns
LVC MOS12_JEDEC, Fast, 6 mA	1.57	1.75	1.94	2.14	1.94	2.14	ns
LVC MOS12_JEDEC, Fast, 8 mA	1.57	1.75	1.83	2.03	1.83	2.03	ns
LVC MOS12_JEDEC, Fast, 12 mA	1.57	1.75	1.80	2.00	1.80	2.00	ns

Notes:

1. The Spartan-6Q FPGA -1L values are listed in Table 28.

Table 30 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). These delays are measured using LVC MOS25, Fast, 12 mA.

Table 30: IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T _{IOTPHZ}	T input to Pad high-impedance	1.39	1.59	1.59	1.91	ns

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

V _{CCO}	I/O Standard	Drive	Slew	SSO Limit per V _{CCO} /GND Pair				
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324		
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5	
3.3V	LVTTTL	2	Fast	53	65	53	62	
			Slow	70	80	70	73	
			QuietIO	79	89	79	91	
		4	Fast	23	30	23	27	
			Slow	34	41	34	37	
			QuietIO	44	49	44	46	
		6	Fast	16	21	16	20	
			Slow	21	28	21	25	
			QuietIO	34	39	34	34	
		8	Fast	12	16	12	15	
			Slow	16	22	16	19	
			QuietIO	27	28	27	24	
		12	Fast	1	3	1	1	
			Slow	2	5	2	4	
			QuietIO	2	10	2	8	
		16	Fast	1	3	1	1	
			Slow	1	7	1	2	
			QuietIO	3	11	3	8	
		24	Fast	1	2	1	1	
			Slow	2	5	2	2	
			QuietIO	8	9	8	8	
	PCI33_3				18	19	18	19
	PCI66_3				18	19	18	19
	SSTL_3_I				5	8	5	8
	SSTL_3_II				3	5	3	3
	DIFF_SSTL_3_I				15	24	15	24
	DIFF_SSTL_3_II				9	15	9	9
	SDIO				17	18	17	15

CLB Switching Characteristics (SLICEM Only)

Table 40: CLB Switching Characteristics (SLICEM Only)

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT inputs to A to D outputs	0.21	0.26	0.26	0.46	ns, Max
	An – Dn LUT inputs through F7AMUX/F7BMUX to AMUX/CMUX output	0.37	0.43	0.43	0.77	ns, Max
T _{OPAB}	An – Dn LUT inputs through F7AMUX or F7BMUX and F8MUX to BMUX output	0.37	0.46	0.46	0.84	ns, Max
T _{ITO}	An – Dn LUT inputs through latch to AQ – DQ outputs	0.82	0.95	0.95	1.64	ns, Max
T _{TITO_LOGIC}	An – Dn LUT inputs to AQ – DQ outputs (latch as logic)	0.82	0.95	0.95	1.64	ns, Max
T _{OPCYA}	An LUT inputs to COUT output	0.38	0.48	0.48	0.69	ns, Max
T _{OPCYB}	Bn LUT inputs to COUT output	0.38	0.49	0.49	0.71	ns, Max
T _{OPCYC}	Cn LUT inputs to COUT output	0.28	0.33	0.33	0.55	ns, Max
T _{OPCYD}	Dn LUT inputs to COUT output	0.28	0.35	0.35	0.52	ns, Max
T _{AXCY}	AX input to COUT output	0.21	0.26	0.26	0.36	ns, Max
T _{BXCy}	BX input to COUT output	0.13	0.16	0.16	0.18	ns, Max
T _{CXCy}	CX input to COUT output	0.10	0.12	0.12	0.09	ns, Max
T _{DXCy}	DX input to COUT output	0.09	0.11	0.11	0.09	ns, Max
T _{BYP}	CIN input to COUT output	0.08	0.10	0.10	0.06	ns, Max
T _{CINA}	CIN input to AMUX output	0.21	0.22	0.22	0.47	ns, Max
T _{CINB}	CIN input to BMUX output	0.30	0.31	0.31	0.57	ns, Max
T _{CINC}	CIN input to CMUX output	0.29	0.31	0.31	0.58	ns, Max
T _{CIND}	CIN input to DMUX output	0.31	0.32	0.32	0.68	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.45	0.53	0.53	0.74	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{DICK} /T _{CKDI}	AX – DX input to CLK on A – D flip-flops	0.42/ 0.28	0.47/ 0.39	0.47/ 0.39	0.90/ 0.56	ns, Min
T _{CECK} /T _{CKCE}	CE input to CLK on A – D flip-flops	0.31/ –0.07	0.37/ –0.07	0.37/ –0.07	0.59/ –0.27	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D flip-flops for XC devices	0.41/ 0.02	0.42/ 0.02	0.42/ 0.02	0.68/ –0.29	ns, Min
	SR input to CLK on A – D flip-flops for XA and XQ devices	0.41/ 0.02	N/A	0.44/ 0.02	0.68/ –0.29	ns, Min
T _{CINCK} /T _{CKCIN}	CIN input to CLK on A – D flip-flops	0.31/ –0.17	0.31/ –0.13	0.31/ –0.13	0.81/ –0.42	ns, Min
Set/Reset						
T _{RPW}	SR input minimum pulse width	0.41	0.48	0.48	1.37	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.60	0.70	0.70	0.88	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.60	0.65	0.65	0.90	ns, Max
F _{TOG}	Toggle frequency (for export control)	862	806	667	500	MHz

Table 44: DSP48A1 Switching Characteristics (Cont'd)

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-3	-3N	-2	-1L	
T _{DSPDCK_OPMODE_PREG} / T _{DSPCKD_OPMODE_PREG}	OPMODE input to P register CLK	Yes	Yes	Yes	6.21/ −0.84	7.27/ −0.84	7.27/ −0.84	10.43/ −0.84	ns
		No	Yes	Yes	1.69/ −0.87	1.98/ −0.87	1.98/ −0.87	3.62/ −0.87	ns
		No	No	Yes	2.09/ −0.22	2.30/ −0.22	2.30/ −0.22	3.79/ −0.22	ns
Clock to Out from Output Register Clock to Output Pin									
T _{DSPCKO_P_PREG}	CLK (PREG) to P output	N/A	N/A	N/A	1.20	1.34	1.34	1.90	ns
Clock to Out from Pipeline Register Clock to Output Pins									
T _{DSPCKO_P_MREG}	CLK (MREG) to P output	N/A	N/A	Yes	3.38	3.95	3.95	5.83	ns
Clock to Out from Input Register Clock to Output Pins									
T _{DSPCKO_P_A1REG}	CLK (A1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.65	ns
T _{DSPCKO_P_B1REG}	CLK (B1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.63	ns
T _{DSPCKO_P_CREG}	CLK (CREG) to P output	N/A	N/A	Yes	3.12	3.64	3.64	5.24	ns
T _{DSPCKO_P_DREG}	CLK (DREG) to P output	Yes	Yes	Yes	6.77	7.92	7.92	12.53	ns
Combinatorial Delays from Input Pins to Output Pins									
T _{DSPDO_A_P}	A input to P output	N/A	No	Yes	2.85	3.33	3.33	4.73	ns
		N/A	Yes	No ⁽²⁾	3.35	3.93	3.93	6.74	ns
		N/A	Yes	Yes	4.56	5.22	5.22	8.94	ns
T _{DSPDO_B_P}	B input to P output	Yes	No	No ⁽²⁾	3.22	3.76	3.76	5.55	ns
		Yes	Yes	No ⁽²⁾	6.01	6.54	6.54	9.76	ns
		Yes	Yes	Yes	6.27	7.34	7.34	11.96	ns
T _{DSPDO_C_P}	C input to P output	N/A	N/A	Yes	2.69	3.15	3.15	4.68	ns
T _{DSPDO_D_P}	D input to P output	Yes	Yes	Yes	6.31	7.38	7.38	11.81	ns
T _{DSPDO_OPMODE_P}	OPMODE input to P output	Yes	Yes	Yes	6.43	7.52	7.52	11.84	ns
		No	Yes	Yes	4.84	5.66	5.66	9.25	ns
		No	No	Yes	3.11	3.49	3.49	5.03	ns
Maximum Frequency									
F _{MAX}	All registers used	Yes	Yes	Yes	390	333	333	213	MHz

Notes:

1. A Yes signifies that the component is in the path. A No signifies that the component is being bypassed. N/A signifies not applicable because no path exists.
2. Implemented in the post-adder by adding to zero.

Configuration Switching Characteristics

Table 47: Configuration Switching Characteristics⁽¹⁾

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Power-up Timing Characteristics						
T _{PL} ⁽²⁾	PROGRAM_B Latency	4	4	4	5	ms, Max
T _{POR} ⁽²⁾	Power-on reset (50 ms ramp time) ⁽³⁾	5/30	5/34	5/40	5/40	ms, Min/Max
	Power-on reset (10 ms ramp time)	5/25	5/29	5/35	5/40	ms, Min/Max
T _{PROGRAM}	PROGRAM_B Pulse Width	500	500	500	500	ns, Min
Slave Serial Mode Programming Switching						
T _{DCCK} /T _{CCKD}	DIN Setup/Hold, slave mode	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T _{CCO}	CCLK to DOUT	12	12	12	17	ns, Max
F _{SCCK}	Slave mode external CCLK	80	80	80	50	MHz, Max
Slave SelectMAP Mode Programming Switching						
T _{SMDCK} /T _{SMCCKD}	SelectMAP Data Setup/Hold	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T _{SMCSCCK} /T _{SMCCKCS}	CSI_B Setup/Hold	7.0/0.0	7.0/0.0	7.0/0.0	9.0/2.0	ns, Min
T _{SMWCK} /T _{SMCCKW}	RDWR_B Setup/Hold	17.0/1.0	17.0/1.0	17.0/1.0	27.0/2.0	ns, Min
T _{SMCKCSO}	CSO_B clock to out	16	16	16	26	ns, Max
T _{SMCO}	CCLK to DATA out in readback	13	13	13	25	ns, Max
T _{SMCKBY}	CCLK to BUSY out in readback	12	12	12	17	ns, Max
F _{SMCK}	Maximum CCLK frequency (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	25	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x8 mode, LX150, and LX150T only)	40	40	40	20	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x16 mode only)	35	35	35	20	MHz, Max
F _{RBCK}	Maximum Readback CCLK frequency, including block RAM (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	20	20	20	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	30	MHz, Max
	Maximum Readback CCLK frequency, including block RAM (LX100, LX100T, LX150, and LX150T only)	12	12	12	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX100, LX100T, LX150, and LX150T only)	35	35	35	20	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK}	TMS and TDI Setup time before TCK	10	10	10	17	ns, Min
T _{TCKTAP}	TMS and TDI Hold time after TCK	5.5	5.5	5.5	5.5	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output valid	6.5	6.5	6.5	8	ns, Max
T _{TCKH}	TCK clock minimum High time	12	12	12	21	ns, Min
T _{TCKL}	TCK clock minimum Low time	12	12	12	21	ns, Min
F _{TCK}	Maximum configuration TCK clock frequency	33	33	33	18	MHz, Max
F _{TCKB}	Maximum boundary-scan TCK clock frequency	33	33	33	18	MHz, Max
F _{TCKAES}	Maximum AES key TCK clock frequency	2	2	2	2	MHz, Max

Table 52: PLL Specification (Cont'd)

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
F _{INMIN}	Minimum Input Clock Frequency	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
F _{INJITTER}	Maximum Input Clock Period Jitter: 19–200 MHz	All	1 ns Maximum				
	Maximum Input Clock Period Jitter: > 200 MHz	All	<20% of clock input period Maximum				
F _{INDUTY}	Allowable Input Duty Cycle: 19—199 MHz	All	25/75				%
	Allowable Input Duty Cycle: 200—299 MHz	All	35/65				%
	Allowable Input Duty Cycle: > 300 MHz	All	45/55				%
F _{VCOMIN}	Minimum PLL VCO Frequency	LX devices	400	400	400	400	MHz
		LXT devices	400	400	400	N/A	MHz
F _{VCOMAX}	Maximum PLL VCO Frequency	LX devices	1080	1050	1000	1000	MHz
		LXT devices	1080	1050	1000	N/A	MHz
F _{BANDWIDTH}	Low PLL Bandwidth at Typical ⁽³⁾	All	1	1	1	1	MHz
	High PLL Bandwidth at Typical ⁽³⁾	All	4	4	4	4	MHz
T _{STAPHAOFFSET}	Static Phase Offset of the PLL Outputs	All	0.12	0.12	0.12	0.15	ns
T _{OUTJITTER}	PLL Output Jitter ⁽³⁾	All	Note 2				
T _{OUTDUTY}	PLL Output Clock Duty Cycle Precision ⁽⁴⁾	All	0.15	0.15	0.20	0.25	ns
T _{LOCKMAX}	PLL Maximum Lock Time	All	100	100	100	100	μs
F _{OUTMAX}	PLL Maximum Output Frequency for BUFGMUX	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz
	PLL Maximum Output Frequency for BUFPLL	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz
F _{OUTMIN}	PLL Minimum Output Frequency ⁽⁵⁾	All	3.125	3.125	3.125	3.125	MHz
T _{EXTFDVAR}	External Clock Feedback Variation: 19–200 MHz	All	1 ns Maximum				
	External Clock Feedback Variation: > 200 MHz	All	< 20% of clock input period Maximum				
RST _{MINPULSE}	Minimum Reset Pulse Width	All	5	5	5	5	ns
F _{PFDMAX} ⁽⁵⁾	Maximum Frequency at the Phase Frequency Detector	LX devices	500	500	400	300	MHz
		LXT devices	500	500	400	N/A	MHz
F _{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
T _{FBDELAY}	Maximum Delay in the Feedback Path	All	3 ns Max or one CLKIN cycle				

Notes:

1. LXT devices are not available with a -1L speed grade.
2. Values for this parameter are available in the Clocking Wizard.
3. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When using CLK_FEEDBACK = CLKOUT0 with BUFIO2 feedback, the feedback frequency will be higher than the phase frequency detector frequency. $F_{PFDMAX} = F_{CLKFB} / CLKFBOUT_MULT$

Table 64: Global Clock Input to Output Delay With DCM in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in System-Synchronous Mode.							
T _{ICKOFDCM}	Global Clock and OUTFF <i>with</i> DCM	XC6SLX4	4.23	N/A	6.11	6.60	ns
		XC6SLX9	4.23	5.17	6.11	6.60	ns
		XC6SLX16	4.28	4.57	5.34	6.36	ns
		XC6SLX25	3.95	4.18	4.59	6.91	ns
		XC6SLX25T	3.95	4.18	4.59	N/A	ns
		XC6SLX45	4.37	4.70	5.50	6.85	ns
		XC6SLX45T	4.37	4.70	5.50	N/A	ns
		XC6SLX75	3.90	4.23	4.77	6.31	ns
		XC6SLX75T	3.90	4.23	4.77	N/A	ns
		XC6SLX100	3.86	4.16	4.66	7.25	ns
		XC6SLX100T	3.90	4.16	4.66	N/A	ns
		XC6SLX150	4.03	4.33	4.83	6.63	ns
		XC6SLX150T	4.03	4.33	4.83	N/A	ns
		XA6SLX4	4.55	N/A	6.11	N/A	ns
		XA6SLX9	4.55	N/A	6.11	N/A	ns
		XA6SLX16	4.62	N/A	5.33	N/A	ns
		XA6SLX25	4.27	N/A	4.59	N/A	ns
		XA6SLX25T	4.27	N/A	4.69	N/A	ns
		XA6SLX45	4.69	N/A	5.50	N/A	ns
		XA6SLX45T	4.69	N/A	5.50	N/A	ns
		XA6SLX75	4.22	N/A	4.77	N/A	ns
		XA6SLX75T	4.22	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.34	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	6.31	ns
		XQ6SLX75T	4.22	N/A	4.77	N/A	ns
		XQ6SLX150	N/A	N/A	4.96	6.63	ns
		XQ6SLX150T	4.62	N/A	4.96	N/A	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
- DCM output jitter is already included in the timing calculation.

Table 68: Global Clock Input to Output Delay With DCM and PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.							
T _{ICKOFDCM_PLL}	Global Clock and OUTFF with DCM and PLL	XC6SLX4	4.78	N/A	6.32	7.09	ns
		XC6SLX9	4.78	5.24	6.32	7.09	ns
		XC6SLX16	4.70	5.12	5.94	6.63	ns
		XC6SLX25	4.70	5.09	5.92	7.30	ns
		XC6SLX25T	4.70	5.09	5.92	N/A	ns
		XC6SLX45	4.63	4.98	5.83	7.26	ns
		XC6SLX45T	4.63	4.98	5.83	N/A	ns
		XC6SLX75	4.68	5.04	5.88	6.90	ns
		XC6SLX75T	4.68	5.04	5.88	N/A	ns
		XC6SLX100	4.72	5.07	5.92	7.77	ns
		XC6SLX100T	4.76	5.07	5.92	N/A	ns
		XC6SLX150	4.44	4.73	5.31	6.96	ns
		XC6SLX150T	4.44	4.73	5.31	N/A	ns
		XA6SLX4	5.07	N/A	6.18	N/A	ns
		XA6SLX9	5.07	N/A	6.18	N/A	ns
		XA6SLX16	5.22	N/A	5.77	N/A	ns
		XA6SLX25	5.01	N/A	5.80	N/A	ns
		XA6SLX25T	5.01	N/A	5.90	N/A	ns
		XA6SLX45	4.93	N/A	5.67	N/A	ns
		XA6SLX45T	4.93	N/A	5.67	N/A	ns
		XA6SLX75	4.94	N/A	5.70	N/A	ns
		XA6SLX75T	4.94	N/A	5.70	N/A	ns
		XA6SLX100	N/A	N/A	5.77	N/A	ns
		XQ6SLX75	N/A	N/A	5.70	6.90	ns
		XQ6SLX75T	4.94	N/A	5.70	N/A	ns
		XQ6SLX150	N/A	N/A	5.31	6.96	ns
		XQ6SLX150T	5.02	N/A	5.31	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 74: Global Clock Setup and Hold With PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.(1)							
T _{PSPLL} / T _{PHPLL}	No Delay Global Clock and IFF(2) with PLL in System-Synchronous Mode	XC6SLX4	1.37/0.25	N/A	1.52/0.41	2.07/0.69	ns
		XC6SLX9	1.37/0.21	1.48/0.21	1.52/0.26	2.07/0.69	ns
		XC6SLX16	1.33/−0.03	1.53/−0.02	1.60/−0.02	1.57/0.48	ns
		XC6SLX25	1.65/0.28	1.71/0.28	1.91/0.28	2.44/0.76	ns
		XC6SLX25T	1.65/0.28	1.71/0.28	1.91/0.28	N/A	ns
		XC6SLX45	1.55/0.18	1.64/0.18	1.75/0.18	2.02/0.90	ns
		XC6SLX45T	1.55/0.18	1.64/0.18	1.75/0.18	N/A	ns
		XC6SLX75	1.77/0.21	1.89/0.21	2.13/0.21	2.46/0.53	ns
		XC6SLX75T	1.77/0.21	1.89/0.21	2.13/0.21	N/A	ns
		XC6SLX100	1.44/0.32	1.52/0.32	1.70/0.32	1.78/0.86	ns
		XC6SLX100T	1.44/0.32	1.52/0.32	1.70/0.32	N/A	ns
		XC6SLX150	1.39/0.49	1.48/0.49	1.67/0.49	1.94/0.94	ns
		XC6SLX150T	1.39/0.49	1.48/0.49	1.67/0.49	N/A	ns
		XA6SLX4	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX9	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX16	1.89/−0.08	N/A	1.72/−0.08	N/A	ns
		XA6SLX25	1.85/0.16	N/A	2.08/0.16	N/A	ns
		XA6SLX25T	1.85/0.16	N/A	2.17/0.16	N/A	ns
		XA6SLX45	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX45T	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX75	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX100	N/A	N/A	2.34/0.14	N/A	ns
		XQ6SLX75	N/A	N/A	2.25/0.06	2.46/0.53	ns
		XQ6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XQ6SLX150	N/A	N/A	1.79/0.37	1.94/0.94	ns
		XQ6SLX150T	1.43/0.37	N/A	1.79/0.37	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 78: Duty Cycle Distortion and Clock-Tree Skew (Cont'd)

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{BUFIOSKEW}	I/O clock tree skew across one clock region	LX4	0.06	N/A	0.06	0.07	ns
		LX9	0.06	0.06	0.06	0.07	ns
		LX16	0.06	0.06	0.06	0.07	ns
		LX25	0.06	0.06	0.06	0.07	ns
		LX25T	0.06	0.06	0.06	N/A	ns
		LX45	0.06	0.06	0.06	0.07	ns
		LX45T	0.06	0.06	0.06	N/A	ns
		LX75	0.06	0.06	0.06	0.07	ns
		LX75T	0.06	0.06	0.06	N/A	ns
		LX100	0.06	0.06	0.06	0.07	ns
		LX100T	0.06	0.06	0.06	N/A	ns
		LX150	0.06	0.06	0.06	0.07	ns
		LX150T	0.06	0.06	0.06	N/A	ns

Notes:

1. LXT devices are not available with a -1L speed grade. The LX4 is not available in -3N speed grade.
2. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
3. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
4. The T_{CKSKEW} is 0.43 ns for the XA6SLX100 device using a -2 speed grade and 0.22 ns for the XC6SLX100 devices using the -2 speed grade.

Table 79: Package Skew

Symbol	Description	Device	Package ⁽²⁾	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	LX4	TQG144	N/A	ps
			CPG196	23	ps
			CSG225	58	ps
		LX9	TQG144	N/A	ps
			CPG196	23	ps
			CSG225	58	ps
			FT(G)256	88	ps
			CSG324	64	ps
		LX16	CPG196	19	ps
			CSG225	70	ps
			FT(G)256	71	ps
			CSG324	54	ps
		LX25	FT(G)256	90	ps
			CSG324	61	ps
			FG(G)484	84	ps
		LX25T	CSG324	48	ps
			FG(G)484	112	ps

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
08/26/09	1.1	Added V_{FS} to Table 1 and Table 2 . Added R_{FUSE} to Table 2 . Added XC6SLX75 and XC6SLX75T to V_{BATT} and I_{BATT} in Table 1 , Table 2 , and Table 4 . Corrected the quiescent supply current for the XC6SLX4 in Table 5 . Updated Table 11 . Removed DV_{PPIN} from Figure 2 . Removed $F_{PCIECORE}$ from Table 24 and added values to $F_{PCIEUSER}$. Added more networking applications to Table 25 . Updated values for $T_{SUSPENDLOW_AWAKE}$, $T_{SUSPEND_ENABLE}$, and T_{SCP_AWAKE} in Table 46 . Numerous changes to Table 47 , page 54 including the addition of new values to various specifications, revising the $T_{SMCKCSO}$ description, and changing the units of T_{POR} . Also, removed <i>Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK</i> section from Table 47 and updated all the notes. In Table 52 , added to F_{INMAX} , revised F_{OUTMAX} , and removed PLL Maximum Output Frequency for BUFIO2. Revised values for DCM_DELAY_STEP in Table 54 . Updated CLKIN_FREQ_FX values in Table 55 .
01/04/10	1.2	Added -4 speed grade to entire document. Updated speed specification of -4, -3, -2 speed grades to version 1.03. Added -1L speed grade numbers per speed specification 1.00. Updated T_{SOL} in Table 1 . Added -1L rows for LVCMOS12, LVCMOS15, and LVCMOS18 in Table 9 . Revised much of the detail in GTP Transceiver Specifications in Table 12 through Table 23 . Added -2 data to Table 25 . Updated F_{MAX} in Table 44 . Updated descriptions for T_{DNACKL} and T_{DNACKH} in Table 45 and revised values for all parameters. Removed $T_{INITADDR}$ from Table 47 and added new data. Updated values in Table 48 through Table 62 . Added Table 51 (BUFPLL) and Table 57 (DCM_CLKGEN). Removed $T_{LOCKMAX}$ note from Table 52 . Updated note 3 in Table 53 . In Table 79 : removed XC6SLX75CSG324 and XC6SLX75TCSG324; added XC6SLX75FG(G)484 and XC6SLX75FG(G)484.
02/22/10	1.3	Production release of XC6SLX16 -2 speed grade devices. The changes to Table 26 and Table 27 includes updating this data sheet to the data in ISE v11.5 software with speed specification v1.06. Updated maximum of V_{IN} and V_{TS} and note 2 in Table 1 . In Table 2 , changed V_{IN} , added I_{IN} and note 5, revised notes 1, 6, and 7, and added note 8 to R_{FUSE} . In Table 4 , removed previous note 1 and added data to I_{RPU} , I_{RPD} , and I_{BATT} , changed C_{IN} , added R_{DT} and R_{IN_TERM} , and added note 2 and 3. Updated V_{CCO2} in Table 6 . Added Table 7 and Table 8 . Removed PCI66_3 from Table 9 . Updated PCI33_3 and I2C in Table 9 . Updated the description of Table 11 . Completely updated Table 25 . Updated Table 28 including adding values for PCI33_3. Updated V_{REF} value for HSTL_III_18 in Table 31 . Updates missing V_{REF} values in Table 32 . Added Simultaneously Switching Outputs , page 36 . Removed T_{GSRQ} and T_{RPW} from Table 35 and Table 36 . Also removed T_{DOQ} from Table 36 . Removed T_{ISDO_DO} and note 1 from Table 37 . Removed T_{OSCK_S} and combinatorial section from Table 38 . In Table 39 , removed T_{IODDO_T} and added new tap parameters and note 2. In Table 40 , Table 41 , and Table 42 , made typographical edits and removed notes. Removed clock CLK section in Table 41 . Removed clock CLK section and T_{REG_MUX} and T_{REG_M31} in Table 42 . Added block RAM F_{MAX} values to Table 43 . Updated values and added note 2 to Table 45 . Added values to Table 46 and removed note 1. Numerous changes to Table 47 . Completely updated Table 57 . Revised data in Table 62 . Removed note 3 from Table 71 . Added values to Table 79 . Added data to Table 80 and Table 81 .
03/10/10	1.4	Production release of XC6SLX45 -2 speed grade devices, which includes changes to Table 26 and Table 27 updating this data sheet to the data in ISE v11.5 software with speed specification v1.07. Fixed R_{IN_TERM} description in Table 4 . Added PCI66_3 to Table 7 and replaced note 1. Corrected note 1 and the V, Max for TMDS_33 in Table 8 . In Table 10 , added note 1 to LVPECL_33 and TMDS_33. Also updated specifications for TMDS_33. Updated the GTP Transceiver Specifications section including adding values to Table 16 , Table 17 , and Table 20 through Table 23 . Added PCI66_3 back into Table 9 , Table 28 , Table 31 , Table 32 , and Table 34 . Updated note 3 on Table 32 . In Table 34 , corrected some typographical errors and fixed SSO limits for bank1/3 in FG(G)484 package. Corrected T_{OSCK_OCE} in Table 38 . In Table 57 , updated CLKFX_FREEZE_VAR and CLKFX_FREEZE_TEMP_SLOPE and added typical values to $T_{CENTER_LOW_SPREAD}$ and $T_{CENTER_HIGH_SPREAD}$. Updated and added values to Table 63 through Table 78 , and Table 81 . In Table 79 , revised the XC6SLX16-CSG324 and the XC6SLX45-CSG484 and FG(G)484 values.

Date	Version	Description of Revisions
06/14/10	1.5	In Table 2, added note 5 and added temperature range to V_{FS} and R_{FUSE}. Removed speed grade delineation, revised I_{RPD} description, and updated note 2 in Table 4. Added note 2 to Table 7. Added $DIFF_MOBILE_DDR$ to Table 8 and Table 10. Added note 4 to Table 15. Changed minimum DV_{PPIN} in Table 16. Updated $F_{GTPDRCLK}$ in Table 19. Increased maximum T_{LLSKEW} in Table 22. Updated descriptions and added data to Table 23. Removed note 1 and added new data to the Networking Applications section in Table 25. Updated Table 26 and Table 27 to the data in ISE v12.1 software with speed specification v1.08. In Table 28, added $DIFF_MOBILE_DDR$ and updated -4 speed grade data. Updated the maximum I/O pairs per bank in Table 33. Updated note 2 on Table 39. Revised the F_{MAX} in Table 44. In Table 47, updated description for $T_{SMCKCSO}$, revised values for T_{POR} and added Min value, added $T_{BPIICCK}$ and $T_{SPIICCK}$. Also in Table 47, added device dependencies to F_{SMCKCK} and F_{RBCKCK}. Updated and added data to Table 63 through Table 78, and Table 81. In Table 79, added data on the XC6SLX45-FG(G)676 and revised the XC6SLX45T and XC6SLX150T values. The following changes to this specification are addressed in the product change notice XC6SLX45-FG(G)676, <i>MCB Performance and JTAG Revision Code for Spartan-6 LX16 and LX45 FPGAs</i>. In Table 2, revised the V_{CCINT} to add the memory controller block extended performance specifications. In Table 25, changed the standard specifications and added extended performance specifications for the memory controller block and note 2. Added note 4 and updated values in Table 34.
06/24/10	1.6	Production release of XC6SLX45T (-2 and -3 speed grades), XC6SLX16 and XC6SLX45 (-3 speed grade) devices which includes changes to Table 26 and Table 27 (ISE v12.1 software with speed specification v1.08). Added the -3N speed grade, which designates Spartan-6 devices that do not support MCB functionality. This includes changes to Table 2 (note 2), Table 25 (note 4), and Switching Characteristics (Table 26). Updated Simultaneously Switching Outputs discussion. Added -3 speed grade values for T_{TAP} and F_{MINCAL} values in Table 39. In Table 40, updated T_{RPW} (-2 and -3 speed grade) values and F_{TOG} (-3 speed grade) values. In Table 48, updated T_{GIO} (-2 and -3 speed grade) values. Updated -3 values in spread spectrum section of Table 57.
07/16/10	1.7	Production release of specific devices listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 4 advising designers of the patch which contains v1.11. Also updated the -1L speed specification to v1.04. Updated numerous -4 and -1L values. Added -4 T_{TAP} values and F_{MINCAL} to Table 39. Revised T_{CINCK}/T_{CKCIN} in Table 40. In Table 41, revised T_{SHCKO}. In Table 42, revised T_{REQ}. Added new -1L values to Table 47. Added and updated values in Table 79.
07/26/10	1.8	Production release of XC6SLX25, XC6SLX25T, XC6SLX100 and XC6SLX100T in the specific speed grades listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 7 to Table 2 and moved V_{FS} and R_{FUSE} to a new Table 3. Added I_{HS} and note 4 to Table 4. Added note 1 to Table 28. Added and updated SSO limits per V_{CCO}/GND pairs in Table 34. Added note 3 to Table 47. In Table 54, removed -1L specifications for $CLKOUT_PER_JITT_DV1/2$ and revised $CLKIN_CLKFB_PHASE$ and $CLKOUT_PHASE_DLL$ values. Updated note 3 in both Table 56 and Table 57.
08/23/10	1.9	Updated values for $F_{GTPRANGE1}$, $F_{GTPRANGE2}$, and $F_{GPLLMIN}$ in Table 18. Revised -3 and -4 values in Table 21. Removed the -1L speed grade readback support restriction and note 3 in Table 47.
11/05/10	1.10	Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.3 software with speed specification v1.12 for the -2 speed grade available in the 12.3 <i>Speed Files Patch</i>. Added note 3 advising designers of the patch which contains v1.12. In Table 2, added note 4. In Table 4, added note 2. In Table 10, added notes 2 and 3. In Table 44, added note 2. In Table 47, updated symbol for $T_{SMWCKCK}/T_{SMCKCKW}$, changed -1L values for $T_{USERCCLKH}$ and $T_{USERCCLKL}$, and added and revised the modes for F_{MCKCK} and F_{SMCKCK}. In Table 53, redefined and expanded description for $CLKIN_FREQ_DLL$ and rewrote note 3. Updated title of Table 58. Also in Table 78, revised T_{DCD_CLK} for XC6SLX150 and XC6SLX150T. Changed description of T_{PSFD}/T_{PHFD} in Table 71. For the -1L speed grade, updated data sheet to ISE 12.3 software with speed specification v1.05 which revised the values in the following tables: Table 25, Table 28, Table 35, Table 36, Table 37, Table 40 through Table 43, Table 48 through Table 56, Table 62 through Table 78, Table 80, and Table 81. Updated Notice of Disclaimer.

Date	Version	Description of Revisions
01/10/11	1.11	Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.4 software with speed specification v1.15 for the -4, -3, -3N, and -2 speed grades. Added note 3 to Table 27. Also updated the -1L speed grade requirements to ISE v12.4 software with speed specification v1.06. Revised -3N definition throughout the document. Added note 4 to Table 2 and updated note 5. Added information on V_{CCINT} to note 1 in Table 5. Updated Networking Applications -3 values in Table 25 to match improvements made in ISE v12.4. In Table 28, added note 1 and revised the T_{IOTP} values for LVDS_33, LVDS_25, MINI_LVDS_33, MINI_LVDS_25, RSDS_33, RSDS_25, TMDS_33, PPDS_33, and PPDS_25. Added note 3 to Table 55.
02/11/11	1.12	As described in XCEN11008: Product Discontinuation Notice For Spartan-6 LXT -4 Devices, the -4 speed specifications have been discontinued. As outlined in page 2 of the XCN, designers currently using -4 speed specifications should rerun timing analysis using the new -3 speed specifications before moving to a replacement device. Updated the networking applications section of Table 25. Updated -2 speed specifications throughout document and added note 3 to Table 27 advising designers to use the -2 speed specification update (v1.17) with the ISE 12.4 software patch. Added F_{CLKDIV} to Table 37 and Table 38. Updated note 2 in Table 39. Updated units for $T_{SMCKCSO}$ and T_{BPICCO} in Table 47. Updated -1L in Table 71. Removed Note 2: <i>Package delay information is available for these device/package combinations. This information can be used to deskew the package</i> from Table 79.
03/31/11	2.0	Production release of XC6SLX45 in the -1L speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. In Table 39, removed values in the -1L column and added note 3 as IODELAY2 only supports Tap0 for lower-power devices. Updated copyright page 1 and Notice of Disclaimer.
05/20/11	2.1	Production release of XC6SLX100 and XC6SLX150 in the specific speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. Updated Table 27 and Note 7 with changes per XCEN11012: Speed File Change for -3N Devices. Revised Switching Characteristics section for speed specifications: v1.18 for -3, -3N, and -2; including improvements in Table 73 through Table 77 and Table 81. Removed <i>Memory Controller Block</i> from the performance heading in Table 2 and revised Note 2. In Table 4, added Note 1 to C_{IN} and updated the description of R_{IN_TERM}. Updated Note 1 in Table 5. Updated Note 1 of Table 7. In Table 25, added and removed -1L specifications, increased the standard performance DDR3 specifications, removed the extended performance DDR3 row and updated Note 3 and Note 4. Clarified the introductory information for Table 28 and Table 30. In Table 32: Revised V_{MEAS} value for LVCMOS12; revised V_{REF} for LVDS_25, LVDS_33, BLVDS_25, MINI_LVDS_25, MINI_LVDS_33, RSDS_25, and RSDS_33; revised R_{REF} for BLVDS_25 and TMDS_33; and added Note 4 and Note 5. Updated Note 2 and Note 3 in Table 39. In Table 47, revised the values and description of T_{POR} including adding Note 3. Also in Table 47, augmented the description and added specifications for F_{RBCKK} and removed XC6SLX4 from F_{MCKK} (maximum frequency, parallel mode (Master SelectMAP/BPI)). Added BUFGMUX to Table 48 title. Added Table 50. In Table 52, revised specifications for $T_{EXTFVAR}$ and $F_{INJITTER}$. In Table 54 removed the 5 MHz < CLKIN_FREQ_DLL parameter in the LOCK_DLL description. In both Table 56 and Table 57, removed the 5 MHz < F_{CLKIN} parameter in the LOCK_FX description. In Table 58, updated description for PSCLK_FREQ and PSCLK_PULSE. Revised title and symbol of Table 70, added new speed specifications for -1L, and added Note 2. Added Table 71.
07/11/11	2.2	Added the Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices to all appropriate tables while sometimes removing the XC6S nomenclature. Added expanded temperature range (Q) to all appropriate tables. Updated T_{SOL} packages in Table 1. Added R_{OUT_TERM} to Table 4. Updated Note 2 on Table 13. Production release of the XC6SLX4, XC6SLX9, XC6SLX16, XC6SLX25, XC6SLX75, XQ6SLX75, and XQ6SLX150 in Table 26 and Table 27 using ISE v13.2 software with -1L speed specification v1.07. Production release of the XA6SLX16, XA6SLX25T, XA6SLX45, XA6SLX45T, XQ6SLX75, XQ6SLX75T, XQ6SLX150, and XQ6SLX150T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices(1). Updated CS(G)484 from CSG484 throughout data sheet. Clarified Note 3 in Table 39.
08/08/11	2.3	Production release of the XA6SLX25, XA6SLX75, and XA6SLX75T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19.

Date	Version	Description of Revisions
09/14/11	2.4	Production release of the XA6SLX4 and XA6SLX9 devices in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added production released version of the XA6SLX100 to Table 26 and Table 27 using ISE v13.3 software with -2 speed specification v1.20. Updated R_{OUT_TERM} description in Table 4. Fixed the LVPECL V_H error in Table 31. Updated introduction in Simultaneously Switching Outputs. Added the XA6SLX100 to Table 63 through Table 78, and Table 81. Added Note 4 to Table 78 because the T_{CKSKEW} for the XC6SLX100 is not the same as the T_{CKSKEW} for the XA6SLX100. Revised the revision history for version 1.6 dated 06/24/10. Removed the parenthetical statement about the -3N speed grade: (specifications are identical to the -3 speed grade).
10/17/11	3.0	Changed the data sheet from Preliminary Product Specification to Product Specification. Updated the Switching Characteristics, page 19 speed specification version ISE v13.3 software to -2 and -3 speed specification v1.20 and -1L speed specification of v1.08. Also updated Note 1 in Table 27. In Table 43, <i>Block RAM Switching Characteristics</i>, the F_{MAX} value for the -2 speed grade has been changed from 260 MHz to 280 MHz. In Table 54, <i>Switching Characteristics for the DLL</i>, a Note 6 was added and linked to CLKIN_CLKFB_PHASE.