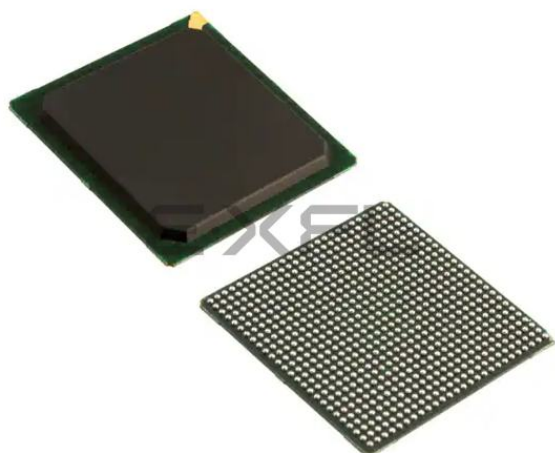




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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	11519
Number of Logic Elements/Cells	147443
Total RAM Bits	4939776
Number of I/O	396
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx150t-n3fgg676i

Table 8: Recommended Operating Conditions for User I/Os Using Differential Signal Standards

I/O Standard	V _{CCO} for Drivers		
	V, Min	V, Nom	V, Max
LVDS_33	3.0	3.3	3.45
LVDS_25	2.25	2.5	2.75
BLVDS_25	2.25	2.5	2.75
MINI_LVDS_33	3.0	3.3	3.45
MINI_LVDS_25	2.25	2.5	2.75
LVPECL_33 ⁽¹⁾	N/A—Inputs Only		
LVPECL_25	N/A—Inputs Only		
RSDS_33	3.0	3.3	3.45
RSDS_25	2.25	2.5	2.75
TMDS_33 ⁽¹⁾	3.14	3.3	3.45
PPDS_33	3.0	3.3	3.45
PPDS_25	2.25	2.5	2.75
DISPLAY_PORT	2.3	2.5	2.7
DIFF_MOBILE_DDR	1.7	1.8	1.9
DIFF_HSTL_I	1.4	1.5	1.6
DIFF_HSTL_II	1.4	1.5	1.6
DIFF_HSTL_III	1.4	1.5	1.6
DIFF_HSTL_I_18	1.7	1.8	1.9
DIFF_HSTL_II_18	1.7	1.8	1.9
DIFF_HSTL_III_18	1.7	1.8	1.9
DIFF_SSTL3_I	3.0	3.3	3.45
DIFF_SSTL3_II	3.0	3.3	3.45
DIFF_SSTL2_I	2.3	2.5	2.7
DIFF_SSTL2_II	2.3	2.5	2.7
DIFF_SSTL18_I	1.7	1.8	1.9
DIFF_SSTL18_II	1.7	1.8	1.9
DIFF_SSTL15_II	1.425	1.5	1.575

Notes:

1. LVPECL_33 and TMDS_33 inputs require V_{CCAUX} = 3.3V nominal.

In Table 9 and Table 10, values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: Single-Ended I/O Standard DC Input and Output Levels

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTTL	−0.5	0.8	2.0	4.1	0.4	2.4	Note 2	Note 2
LVC MOS33	−0.5	0.8	2.0	4.1	0.4	$V_{CCO} - 0.4$	Note 2	Note 2
LVC MOS25	−0.5	0.7	1.7	4.1	0.4	$V_{CCO} - 0.4$	Note 2	Note 2
LVC MOS18	−0.5	0.38	0.8	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS18 (−1L)	−0.5	0.33	0.71	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS18_JEDEC	−0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS15	−0.5	0.38	0.8	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVC MOS15 (−1L)	−0.5	0.33	0.71	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVC MOS15_JEDEC	−0.5	35% V_{CCO}	65% V_{CCO}	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVC MOS12	−0.5	0.38	0.8	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
LVC MOS12 (−1L)	−0.5	0.33	0.71	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
LVC MOS12_JEDEC	−0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
PCI33_3	−0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	1.5	−0.5
PCI66_3	−0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	1.5	−0.5
I2C	−0.5	25% V_{CCO}	70% V_{CCO}	4.1	20% V_{CCO}	—	3	—
SMBUS	−0.5	0.8	2.1	4.1	0.4	—	4	—
SDIO	−0.5	12.5% V_{CCO}	75% V_{CCO}	4.1	12.5% V_{CCO}	75% V_{CCO}	0.1	−0.1
MOBILE_DDR	−0.5	20% V_{CCO}	80% V_{CCO}	4.1	10% V_{CCO}	90% V_{CCO}	0.1	−0.1
HSTL_I	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	8	−8
HSTL_II	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	16	−16
HSTL_III	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	24	−8
HSTL_I_18	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	11	−11
HSTL_II_18	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	22	−22
HSTL_III_18	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	30	−11
SSTL3_I	−0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	4.1	$V_{TT} - 0.6$	$V_{TT} + 0.6$	8	−8
SSTL3_II	−0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	4.1	$V_{TT} - 0.8$	$V_{TT} + 0.8$	16	−16
SSTL2_I	−0.5	$V_{REF} - 0.15$	$V_{REF} + 0.15$	4.1	$V_{TT} - 0.61$	$V_{TT} + 0.61$	8.1	−8.1
SSTL2_II	−0.5	$V_{REF} - 0.15$	$V_{REF} + 0.15$	4.1	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	−16.2
SSTL18_I	−0.5	$V_{REF} - 0.125$	$V_{REF} + 0.125$	4.1	$V_{TT} - 0.47$	$V_{TT} + 0.47$	6.7	−6.7
SSTL18_II	−0.5	$V_{REF} - 0.125$	$V_{REF} + 0.125$	4.1	$V_{TT} - 0.60$	$V_{TT} + 0.60$	13.4	−13.4
SSTL15_II	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	$V_{TT} - 0.4$	$V_{TT} + 0.4$	13.4	−13.4

Notes:

1. Tested according to relevant specifications.
2. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
3. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
4. Using drive strengths of 2, 4, 6, 8, or 12 mA.
5. For more information, refer to [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
PPDS_33	1.17	1.29	1.42	1.68	1.57	1.71	1.91	2.43	3000	3000	3000	3000	ns
PPDS_25	1.01	1.13	1.26	1.56	1.68	1.82	2.02	2.47	3000	3000	3000	3000	ns
PCI33_3	1.07	1.19	1.32	1.57 ⁽²⁾	3.51	3.65	3.85	4.38 ⁽²⁾	3.51	3.65	3.85	4.38 ⁽¹⁾	ns
PCI66_3	1.07	1.19	1.32	1.57 ⁽²⁾	3.53	3.67	3.87	4.39 ⁽²⁾	3.53	3.67	3.87	4.39 ⁽¹⁾	ns
DISPLAY_PORT	1.02	1.14	1.27	1.56	3.15	3.29	3.49	4.08	3.15	3.29	3.49	4.08	ns
I2C	1.33	1.45	1.58	1.82	11.56	11.70	11.90	12.52	11.56	11.70	11.90	12.52	ns
SMBUS	1.33	1.45	1.58	1.82	11.56	11.70	11.90	12.52	11.56	11.70	11.90	12.52	ns
SDIO	1.36	1.48	1.61	1.84	2.64	2.78	2.98	3.60	2.64	2.78	2.98	3.60	ns
MOBILE_DDR	0.94	1.06	1.19	1.43	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns
HSTL_I	0.90	1.02	1.15	1.39	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
HSTL_II	0.91	1.03	1.16	1.40	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
HSTL_III	0.95	1.07	1.20	1.44	1.67	1.81	2.01	2.61	1.67	1.81	2.01	2.61	ns
HSTL_I_18	0.94	1.06	1.19	1.43	1.77	1.91	2.11	2.73	1.77	1.91	2.11	2.73	ns
HSTL_II_18	0.94	1.06	1.19	1.43	1.85	1.99	2.19	2.81	1.85	1.99	2.19	2.81	ns
HSTL_III_18	0.99	1.11	1.24	1.47	1.79	1.93	2.13	2.72	1.79	1.93	2.13	2.72	ns
SSTL3_I	1.58	1.70	1.83	2.16	1.83	1.97	2.17	2.72	1.83	1.97	2.17	2.72	ns
SSTL3_II	1.58	1.70	1.83	2.16	2.01	2.15	2.35	2.94	2.01	2.15	2.35	2.94	ns
SSTL2_I	1.30	1.42	1.55	1.87	1.77	1.91	2.11	2.69	1.77	1.91	2.11	2.69	ns
SSTL2_II	1.30	1.42	1.55	1.88	1.86	2.00	2.20	2.82	1.86	2.00	2.20	2.82	ns
SSTL18_I	0.92	1.04	1.17	1.41	1.63	1.77	1.97	2.59	1.63	1.77	1.97	2.59	ns
SSTL18_II	0.92	1.04	1.17	1.41	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
SSTL15_II	0.92	1.04	1.17	1.41	1.67	1.81	2.01	2.63	1.67	1.81	2.01	2.63	ns
DIFF_HSTL_I	0.94	1.06	1.19	1.46	1.77	1.91	2.11	2.62	1.77	1.91	2.11	2.62	ns
DIFF_HSTL_II	0.93	1.05	1.18	1.45	1.72	1.86	2.06	2.54	1.72	1.86	2.06	2.54	ns
DIFF_HSTL_III	0.93	1.05	1.18	1.46	1.69	1.83	2.03	2.53	1.69	1.83	2.03	2.53	ns
DIFF_HSTL_I_18	0.97	1.09	1.22	1.50	1.79	1.93	2.13	2.63	1.79	1.93	2.13	2.63	ns
DIFF_HSTL_II_18	0.97	1.09	1.22	1.49	1.69	1.83	2.03	2.51	1.69	1.83	2.03	2.51	ns
DIFF_HSTL_III_18	0.97	1.09	1.22	1.50	1.69	1.83	2.03	2.53	1.69	1.83	2.03	2.53	ns
DIFF_SSTL3_I	1.18	1.30	1.43	1.68	1.81	1.95	2.15	2.64	1.81	1.95	2.15	2.64	ns
DIFF_SSTL3_II	1.19	1.31	1.44	1.68	1.80	1.94	2.14	2.63	1.80	1.94	2.14	2.63	ns
DIFF_SSTL2_I	1.02	1.14	1.27	1.57	1.80	1.94	2.14	2.62	1.80	1.94	2.14	2.62	ns
DIFF_SSTL2_II	1.02	1.14	1.27	1.57	1.76	1.90	2.10	2.57	1.76	1.90	2.10	2.57	ns
DIFF_SSTL18_I	0.97	1.09	1.22	1.51	1.72	1.86	2.06	2.56	1.72	1.86	2.06	2.56	ns
DIFF_SSTL18_II	0.98	1.10	1.23	1.50	1.68	1.82	2.02	2.52	1.68	1.82	2.02	2.52	ns
DIFF_SSTL15_II	0.94	1.06	1.19	1.46	1.67	1.81	2.01	2.50	1.67	1.81	2.01	2.50	ns
DIFF_MOBILE_DDR	0.97	1.09	1.22	1.51	1.75	1.89	2.09	2.57	1.75	1.89	2.09	2.57	ns

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVTTL, QUIETIO, 2 mA	1.35	1.47	1.60	1.82	5.39	5.53	5.73	6.37	5.39	5.53	5.73	6.37	ns
LVTTL, QUIETIO, 4 mA	1.35	1.47	1.60	1.82	4.29	4.43	4.63	5.22	4.29	4.43	4.63	5.22	ns
LVTTL, QUIETIO, 6 mA	1.35	1.47	1.60	1.82	3.75	3.89	4.09	4.69	3.75	3.89	4.09	4.69	ns
LVTTL, QUIETIO, 8 mA	1.35	1.47	1.60	1.82	3.23	3.37	3.57	4.20	3.23	3.37	3.57	4.20	ns
LVTTL, QUIETIO, 12 mA	1.35	1.47	1.60	1.82	3.28	3.42	3.62	4.22	3.28	3.42	3.62	4.22	ns
LVTTL, QUIETIO, 16 mA	1.35	1.47	1.60	1.82	2.94	3.08	3.28	3.92	2.94	3.08	3.28	3.92	ns
LVTTL, QUIETIO, 24 mA	1.35	1.47	1.60	1.82	2.69	2.83	3.03	3.67	2.69	2.83	3.03	3.67	ns
LVTTL, Slow, 2 mA	1.35	1.47	1.60	1.82	4.36	4.50	4.70	5.30	4.36	4.50	4.70	5.30	ns
LVTTL, Slow, 4 mA	1.35	1.47	1.60	1.82	3.17	3.31	3.51	4.16	3.17	3.31	3.51	4.16	ns
LVTTL, Slow, 6 mA	1.35	1.47	1.60	1.82	2.76	2.90	3.10	3.75	2.76	2.90	3.10	3.75	ns
LVTTL, Slow, 8 mA	1.35	1.47	1.60	1.82	2.59	2.73	2.93	3.55	2.59	2.73	2.93	3.55	ns
LVTTL, Slow, 12 mA	1.35	1.47	1.60	1.82	2.58	2.72	2.92	3.54	2.58	2.72	2.92	3.54	ns
LVTTL, Slow, 16 mA	1.35	1.47	1.60	1.82	2.39	2.53	2.73	3.40	2.39	2.53	2.73	3.40	ns
LVTTL, Slow, 24 mA	1.35	1.47	1.60	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVTTL, Fast, 2 mA	1.35	1.47	1.60	1.82	3.78	3.92	4.12	4.74	3.78	3.92	4.12	4.74	ns
LVTTL, Fast, 4 mA	1.35	1.47	1.60	1.82	2.49	2.63	2.83	3.45	2.49	2.63	2.83	3.45	ns
LVTTL, Fast, 6 mA	1.35	1.47	1.60	1.82	2.44	2.58	2.78	3.40	2.44	2.58	2.78	3.40	ns
LVTTL, Fast, 8 mA	1.35	1.47	1.60	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns
LVTTL, Fast, 12 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTL, Fast, 16 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTL, Fast, 24 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVC MOS33, QUIETIO, 2 mA	1.34	1.46	1.59	1.82	5.40	5.54	5.74	6.37	5.40	5.54	5.74	6.37	ns
LVC MOS33, QUIETIO, 4 mA	1.34	1.46	1.59	1.82	4.03	4.17	4.37	5.01	4.03	4.17	4.37	5.01	ns
LVC MOS33, QUIETIO, 6 mA	1.34	1.46	1.59	1.82	3.51	3.65	3.85	4.47	3.51	3.65	3.85	4.47	ns
LVC MOS33, QUIETIO, 8 mA	1.34	1.46	1.59	1.82	3.37	3.51	3.71	4.33	3.37	3.51	3.71	4.33	ns
LVC MOS33, QUIETIO, 12 mA	1.34	1.46	1.59	1.82	2.94	3.08	3.28	3.93	2.94	3.08	3.28	3.93	ns
LVC MOS33, QUIETIO, 16 mA	1.34	1.46	1.59	1.82	2.77	2.91	3.11	3.78	2.77	2.91	3.11	3.78	ns
LVC MOS33, QUIETIO, 24 mA	1.34	1.46	1.59	1.82	2.59	2.73	2.93	3.58	2.59	2.73	2.93	3.58	ns
LVC MOS33, Slow, 2 mA	1.34	1.46	1.59	1.82	4.37	4.51	4.71	5.28	4.37	4.51	4.71	5.28	ns
LVC MOS33, Slow, 4 mA	1.34	1.46	1.59	1.82	2.98	3.12	3.32	3.94	2.98	3.12	3.32	3.94	ns
LVC MOS33, Slow, 6 mA	1.34	1.46	1.59	1.82	2.58	2.72	2.92	3.61	2.58	2.72	2.92	3.61	ns
LVC MOS33, Slow, 8 mA	1.34	1.46	1.59	1.82	2.65	2.79	2.99	3.61	2.65	2.79	2.99	3.61	ns
LVC MOS33, Slow, 12 mA	1.34	1.46	1.59	1.82	2.39	2.53	2.73	3.31	2.39	2.53	2.73	3.31	ns
LVC MOS33, Slow, 16 mA	1.34	1.46	1.59	1.82	2.31	2.45	2.65	3.27	2.31	2.45	2.65	3.27	ns
LVC MOS33, Slow, 24 mA	1.34	1.46	1.59	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVC MOS33, Fast, 2 mA	1.34	1.46	1.59	1.82	3.76	3.90	4.10	4.70	3.76	3.90	4.10	4.70	ns
LVC MOS33, Fast, 4 mA	1.34	1.46	1.59	1.82	2.48	2.62	2.82	3.44	2.48	2.62	2.82	3.44	ns
LVC MOS33, Fast, 6 mA	1.34	1.46	1.59	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVC MOS12, Fast, 2 mA	0.91	1.03	1.16	1.51	3.46	3.60	3.80	4.44	3.46	3.60	3.80	4.44	ns
LVC MOS12, Fast, 4 mA	0.91	1.03	1.16	1.51	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVC MOS12, Fast, 6 mA	0.91	1.03	1.16	1.51	1.79	1.93	2.13	2.75	1.79	1.93	2.13	2.75	ns
LVC MOS12, Fast, 8 mA	0.91	1.03	1.16	1.51	1.68	1.82	2.02	2.64	1.68	1.82	2.02	2.64	ns
LVC MOS12, Fast, 12 mA	0.91	1.03	1.16	1.51	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
LVC MOS12_JEDEC, QUIETIO, 2 mA	1.50	1.62	1.75	1.88	6.39	6.53	6.73	7.31	6.39	6.53	6.73	7.31	ns
LVC MOS12_JEDEC, QUIETIO, 4 mA	1.50	1.62	1.75	1.88	4.98	5.12	5.32	5.88	4.98	5.12	5.32	5.88	ns
LVC MOS12_JEDEC, QUIETIO, 6 mA	1.50	1.62	1.75	1.88	4.67	4.81	5.01	5.54	4.67	4.81	5.01	5.54	ns
LVC MOS12_JEDEC, QUIETIO, 8 mA	1.50	1.62	1.75	1.88	4.23	4.37	4.57	5.22	4.23	4.37	4.57	5.22	ns
LVC MOS12_JEDEC, QUIETIO, 12 mA	1.50	1.62	1.75	1.88	3.99	4.13	4.33	4.94	3.99	4.13	4.33	4.94	ns
LVC MOS12_JEDEC, Slow, 2 mA	1.50	1.62	1.75	1.88	5.00	5.14	5.34	5.90	5.00	5.14	5.34	5.90	ns
LVC MOS12_JEDEC, Slow, 4 mA	1.50	1.62	1.75	1.88	2.85	2.99	3.19	3.80	2.85	2.99	3.19	3.80	ns
LVC MOS12_JEDEC, Slow, 6 mA	1.50	1.62	1.75	1.88	2.76	2.90	3.10	3.72	2.76	2.90	3.10	3.72	ns
LVC MOS12_JEDEC, Slow, 8 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVC MOS12_JEDEC, Slow, 12 mA	1.50	1.62	1.75	1.88	2.09	2.23	2.43	3.05	2.09	2.23	2.43	3.05	ns
LVC MOS12_JEDEC, Fast, 2 mA	1.50	1.62	1.75	1.88	3.46	3.60	3.80	4.42	3.46	3.60	3.80	4.42	ns
LVC MOS12_JEDEC, Fast, 4 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns
LVC MOS12_JEDEC, Fast, 6 mA	1.50	1.62	1.75	1.88	1.79	1.93	2.13	2.76	1.79	1.93	2.13	2.76	ns
LVC MOS12_JEDEC, Fast, 8 mA	1.50	1.62	1.75	1.88	1.69	1.83	2.03	2.65	1.69	1.83	2.03	2.65	ns
LVC MOS12_JEDEC, Fast, 12 mA	1.50	1.62	1.75	1.88	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns

Notes:

1. The -1L values listed in this table are also applicable to the Spartan-6Q devices.
2. Devices with a -1L speed grade do not support Xilinx PCI IP.

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS18, QUIETIO, 16 mA	1.25	1.43	3.34	3.54	3.34	3.54	ns
LVC MOS18, QUIETIO, 24 mA	1.25	1.43	3.18	3.38	3.18	3.38	ns
LVC MOS18, Slow, 2 mA	1.25	1.43	4.79	4.99	4.79	4.99	ns
LVC MOS18, Slow, 4 mA	1.25	1.43	3.84	4.04	3.84	4.04	ns
LVC MOS18, Slow, 6 mA	1.25	1.43	3.17	3.37	3.17	3.37	ns
LVC MOS18, Slow, 8 mA	1.25	1.43	2.37	2.57	2.37	2.57	ns
LVC MOS18, Slow, 12 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns
LVC MOS18, Slow, 16 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns
LVC MOS18, Slow, 24 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns
LVC MOS18, Fast, 2 mA	1.25	1.43	3.78	3.98	3.78	3.98	ns
LVC MOS18, Fast, 4 mA	1.25	1.43	2.54	2.74	2.54	2.74	ns
LVC MOS18, Fast, 6 mA	1.25	1.43	2.02	2.22	2.02	2.22	ns
LVC MOS18, Fast, 8 mA	1.25	1.43	1.95	2.15	1.95	2.15	ns
LVC MOS18, Fast, 12 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns
LVC MOS18, Fast, 16 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns
LVC MOS18, Fast, 24 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns
LVC MOS18_JEDEC, QUIETIO, 2 mA	1.01	1.19	6.09	6.29	6.09	6.29	ns
LVC MOS18_JEDEC, QUIETIO, 4 mA	1.01	1.19	4.89	5.09	4.89	5.09	ns
LVC MOS18_JEDEC, QUIETIO, 6 mA	1.01	1.19	4.20	4.40	4.20	4.40	ns
LVC MOS18_JEDEC, QUIETIO, 8 mA	1.01	1.19	3.87	4.07	3.87	4.07	ns
LVC MOS18_JEDEC, QUIETIO, 12 mA	1.01	1.19	3.49	3.69	3.49	3.69	ns
LVC MOS18_JEDEC, QUIETIO, 16 mA	1.01	1.19	3.34	3.54	3.34	3.54	ns
LVC MOS18_JEDEC, QUIETIO, 24 mA	1.01	1.19	3.17	3.37	3.17	3.37	ns
LVC MOS18_JEDEC, Slow, 2 mA	1.01	1.19	4.79	4.99	4.79	4.99	ns
LVC MOS18_JEDEC, Slow, 4 mA	1.01	1.19	3.84	4.04	3.84	4.04	ns
LVC MOS18_JEDEC, Slow, 6 mA	1.01	1.19	3.18	3.38	3.18	3.38	ns
LVC MOS18_JEDEC, Slow, 8 mA	1.01	1.19	2.37	2.57	2.37	2.57	ns
LVC MOS18_JEDEC, Slow, 12 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns
LVC MOS18_JEDEC, Slow, 16 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns
LVC MOS18_JEDEC, Slow, 24 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns
LVC MOS18_JEDEC, Fast, 2 mA	1.01	1.19	3.75	3.95	3.75	3.95	ns
LVC MOS18_JEDEC, Fast, 4 mA	1.01	1.19	2.54	2.74	2.54	2.74	ns
LVC MOS18_JEDEC, Fast, 6 mA	1.01	1.19	2.02	2.22	2.02	2.22	ns
LVC MOS18_JEDEC, Fast, 8 mA	1.01	1.19	1.94	2.14	1.94	2.14	ns
LVC MOS18_JEDEC, Fast, 12 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns
LVC MOS18_JEDEC, Fast, 16 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns
LVC MOS18_JEDEC, Fast, 24 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns

Table 34: SSO Limit per V_{CCO} /GND Pair

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO} /GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
1.2V	LVCMOS12, LVCMOS12_JEDEC	2	Fast	30 ⁽¹⁾	35	30	35
			Slow	51	55	51	52
			QuietIO	71	58	71	70
		4	Fast	17	17	17	19
			Slow	23	25	23	22
			QuietIO	35	32	35	32
		6	Fast	13	15	13	14
			Slow	19	20	19	17
			QuietIO	26	24	26	24
		8	Fast	N/A	12	N/A	12
			Slow	N/A	15	N/A	13
			QuietIO	N/A	20	N/A	19
		12	Fast	N/A	5	N/A	4
			Slow	N/A	8	N/A	5
			QuietIO	N/A	11	N/A	10

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

V _{CCO}	I/O Standard	Drive	Slew	SSO Limit per V _{CCO} /GND Pair				
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324		
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5	
3.3V	LVTTTL	2	Fast	53	65	53	62	
			Slow	70	80	70	73	
			QuietIO	79	89	79	91	
		4	Fast	23	30	23	27	
			Slow	34	41	34	37	
			QuietIO	44	49	44	46	
		6	Fast	16	21	16	20	
			Slow	21	28	21	25	
			QuietIO	34	39	34	34	
		8	Fast	12	16	12	15	
			Slow	16	22	16	19	
			QuietIO	27	28	27	24	
		12	Fast	1	3	1	1	
			Slow	2	5	2	4	
			QuietIO	2	10	2	8	
		16	Fast	1	3	1	1	
			Slow	1	7	1	2	
			QuietIO	3	11	3	8	
		24	Fast	1	2	1	1	
			Slow	2	5	2	2	
			QuietIO	8	9	8	8	
	PCI33_3				18	19	18	19
	PCI66_3				18	19	18	19
	SSTL_3_I				5	8	5	8
	SSTL_3_II				3	5	3	3
	DIFF_SSTL_3_I				15	24	15	24
	DIFF_SSTL_3_II				9	15	9	9
	SDIO				17	18	17	15

Input/Output Logic Switching Characteristics

Table 35: ILOGIC2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T _{ICE0CK} /T _{ICKCE0}	CE0 pin Setup/Hold with respect to CLK	0.56/ −0.30	0.56/ −0.25	0.79/ −0.22	1.21/ −0.52	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.74/ −0.23	0.74/ −0.22	0.98/ −0.20	1.31/ −0.45	ns
T _{IDOCK} /T _{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	1.19/ −0.83	1.36/ −0.83	1.73/ −0.83	2.18/ −1.77	ns
T _{IDOCKD} /T _{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	0.31/ 0.00	0.47/ 0.00	0.54/ 0.00	0.63/ −0.39	ns
Combinatorial						
T _{IDI}	D pin to O pin propagation delay, no Delay	0.95	1.28	1.53	2.25	ns
T _{IDID}	DDLY pin to O pin propagation delay (using IODELAY2)	0.23	0.39	0.44	0.74	ns
Sequential Delays						
T _{IDLO}	D pin to Q pin using flip-flop as a latch without Delay	1.56	1.86	2.39	3.49	ns
T _{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY2)	0.68	0.97	1.20	1.94	ns
T _{ICKQ}	CLK to Q outputs for XC devices	1.03	1.24	1.43	2.11	ns
	CLK to Q outputs for XA and XQ devices	1.38	N/A	1.78	2.11	ns
T _{RQ_ILOGIC2}	SR pin to Q outputs	1.81	1.81	2.50	3.05	ns

Table 36: OLOGIC2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T _{ODCK} /T _{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.81/ −0.05	0.86/ −0.05	1.18/ 0.00	1.73/ −0.27	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.75/ −0.10	0.75/ −0.10	1.01/ −0.05	1.66/ −0.23	ns
T _{OSRCK} /T _{OCKSR}	SR pin Setup/Hold with respect to CLK	0.70/ −0.28	0.79/ −0.28	1.03/ −0.23	1.39/ −0.47	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.24/ −0.08	0.56/ −0.06	0.83/ −0.01	0.99/ −0.19	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.58/ −0.06	0.72/ −0.06	1.18/ −0.01	1.51/ −0.13	ns
Sequential Delays						
T _{OCKQ}	CLK to OQ/TQ out for XC devices	0.48	0.51	0.74	0.74	ns
	CLK to OQ/TQ out for XA and XQ devices	0.85	N/A	1.16	0.74	ns
T _{RQ_OLOGIC2}	SR pin to OQ/TQ out	1.81	1.81	2.50	3.05	ns

Input/Output Delay Switching Characteristics

Table 39: IODELAY2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L ⁽³⁾	
$T_{\text{IODCCK_CAL}} / T_{\text{IODCKC_CAL}}$	CAL pin Setup/Hold with respect to CK	0.28/ -0.13	0.33/ -0.13	0.48/ -0.13	N/A	ns
$T_{\text{IODCCK_CE}} / T_{\text{IODCKC_CE}}$	CE pin Setup/Hold with respect to CK	0.17/ -0.03	0.17/ -0.03	0.25/ -0.02	N/A	ns
$T_{\text{IODCCK_INC}} / T_{\text{IODCKC_INC}}$	INC pin Setup/Hold with respect to CK	0.10/ 0.02	0.12/ 0.03	0.18/ 0.06	N/A	ns
$T_{\text{IODCCK_RST}} / T_{\text{IODCKC_RST}}$	RST pin Setup/Hold with respect to CK	0.12/ -0.02	0.15/ -0.02	0.22/ -0.01	N/A	ns
T_{TAP1} ⁽²⁾	Maximum tap 1 delay	8	14	16	N/A	ps
T_{TAP2}	Maximum tap 2 delay	40	66	77	N/A	ps
T_{TAP3}	Maximum tap 3 delay	95	120	140	N/A	ps
T_{TAP4}	Maximum tap 4 delay	108	141	166	N/A	ps
T_{TAP5}	Maximum tap 5 delay	171	194	231	N/A	ps
T_{TAP6}	Maximum tap 6 delay	207	249	292	N/A	ps
T_{TAP7}	Maximum tap 7 delay	212	276	343	N/A	ps
T_{TAP8}	Maximum tap 8 delay	322	341	424	N/A	ps
F_{MINCAL}	Minimum allowed bit rate for calibration in variable mode: VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX, and DIFF_PHASE_DETECTOR.	188	188	188	N/A	Mb/s
$T_{\text{IODDO_IDATAIN}}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	—
$T_{\text{IODDO_ODATAIN}}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	—

Notes:

- Delay depends on IODELAY2 tap setting. See TRACE report for actual values.
- Maximum delay = integer (number of taps/8) $\times$ T_{TAP8} + T_{TAPn} (where n equals the remainder). For minimum delay consult the TRACE setup and hold report. Minimum delay is typically greater than 30% of the maximum delay. Tap delays can vary by device and overall conditions. See TRACE report for actual values.
- Spartan-6 -1L devices only support tap 0. See TRACE report for actual values.

Configuration Switching Characteristics

Table 47: Configuration Switching Characteristics⁽¹⁾

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Power-up Timing Characteristics						
T _{PL} ⁽²⁾	PROGRAM_B Latency	4	4	4	5	ms, Max
T _{POR} ⁽²⁾	Power-on reset (50 ms ramp time) ⁽³⁾	5/30	5/34	5/40	5/40	ms, Min/Max
	Power-on reset (10 ms ramp time)	5/25	5/29	5/35	5/40	ms, Min/Max
T _{PROGRAM}	PROGRAM_B Pulse Width	500	500	500	500	ns, Min
Slave Serial Mode Programming Switching						
T _{DCCK} /T _{CCKD}	DIN Setup/Hold, slave mode	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T _{CCO}	CCLK to DOUT	12	12	12	17	ns, Max
F _{SCCK}	Slave mode external CCLK	80	80	80	50	MHz, Max
Slave SelectMAP Mode Programming Switching						
T _{SMDCK} /T _{SMCCKD}	SelectMAP Data Setup/Hold	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T _{SMCSCCK} /T _{SMCCKCS}	CSI_B Setup/Hold	7.0/0.0	7.0/0.0	7.0/0.0	9.0/2.0	ns, Min
T _{SMWCCK} /T _{SMCKKW}	RDWR_B Setup/Hold	17.0/1.0	17.0/1.0	17.0/1.0	27.0/2.0	ns, Min
T _{SMCKCSO}	CSO_B clock to out	16	16	16	26	ns, Max
T _{SMCO}	CCLK to DATA out in readback	13	13	13	25	ns, Max
T _{SMCKBY}	CCLK to BUSY out in readback	12	12	12	17	ns, Max
F _{SMCK}	Maximum CCLK frequency (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	25	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x8 mode, LX150, and LX150T only)	40	40	40	20	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x16 mode only)	35	35	35	20	MHz, Max
F _{RBCK}	Maximum Readback CCLK frequency, including block RAM (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	20	20	20	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	30	MHz, Max
	Maximum Readback CCLK frequency, including block RAM (LX100, LX100T, LX150, and LX150T only)	12	12	12	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX100, LX100T, LX150, and LX150T only)	35	35	35	20	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK}	TMS and TDI Setup time before TCK	10	10	10	17	ns, Min
T _{TCKTAP}	TMS and TDI Hold time after TCK	5.5	5.5	5.5	5.5	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output valid	6.5	6.5	6.5	8	ns, Max
T _{TCKH}	TCK clock minimum High time	12	12	12	21	ns, Min
T _{TCKL}	TCK clock minimum Low time	12	12	12	21	ns, Min
F _{TCK}	Maximum configuration TCK clock frequency	33	33	33	18	MHz, Max
F _{TCKB}	Maximum boundary-scan TCK clock frequency	33	33	33	18	MHz, Max
F _{TCKAES}	Maximum AES key TCK clock frequency	2	2	2	2	MHz, Max

Table 52: PLL Specification (Cont'd)

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
F _{INMIN}	Minimum Input Clock Frequency	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
F _{INJITTER}	Maximum Input Clock Period Jitter: 19–200 MHz	All	1 ns Maximum				
	Maximum Input Clock Period Jitter: > 200 MHz	All	<20% of clock input period Maximum				
F _{INDUTY}	Allowable Input Duty Cycle: 19—199 MHz	All	25/75				%
	Allowable Input Duty Cycle: 200—299 MHz	All	35/65				%
	Allowable Input Duty Cycle: > 300 MHz	All	45/55				%
F _{VCOMIN}	Minimum PLL VCO Frequency	LX devices	400	400	400	400	MHz
		LXT devices	400	400	400	N/A	MHz
F _{VCOMAX}	Maximum PLL VCO Frequency	LX devices	1080	1050	1000	1000	MHz
		LXT devices	1080	1050	1000	N/A	MHz
F _{BANDWIDTH}	Low PLL Bandwidth at Typical ⁽³⁾	All	1	1	1	1	MHz
	High PLL Bandwidth at Typical ⁽³⁾	All	4	4	4	4	MHz
T _{STAPHAOFFSET}	Static Phase Offset of the PLL Outputs	All	0.12	0.12	0.12	0.15	ns
T _{OUTJITTER}	PLL Output Jitter ⁽³⁾	All	Note 2				
T _{OUTDUTY}	PLL Output Clock Duty Cycle Precision ⁽⁴⁾	All	0.15	0.15	0.20	0.25	ns
T _{LOCKMAX}	PLL Maximum Lock Time	All	100	100	100	100	μs
F _{OUTMAX}	PLL Maximum Output Frequency for BUFGMUX	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz
	PLL Maximum Output Frequency for BUFPLL	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz
F _{OUTMIN}	PLL Minimum Output Frequency ⁽⁵⁾	All	3.125	3.125	3.125	3.125	MHz
T _{EXTFDVAR}	External Clock Feedback Variation: 19–200 MHz	All	1 ns Maximum				
	External Clock Feedback Variation: > 200 MHz	All	< 20% of clock input period Maximum				
RST _{MINPULSE}	Minimum Reset Pulse Width	All	5	5	5	5	ns
F _{PFDMAX} ⁽⁵⁾	Maximum Frequency at the Phase Frequency Detector	LX devices	500	500	400	300	MHz
		LXT devices	500	500	400	N/A	MHz
F _{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
T _{FBDELAY}	Maximum Delay in the Feedback Path	All	3 ns Max or one CLKIN cycle				

Notes:

1. LXT devices are not available with a -1L speed grade.
2. Values for this parameter are available in the Clocking Wizard.
3. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When using CLK_FEEDBACK = CLKOUT0 with BUFIO2 feedback, the feedback frequency will be higher than the phase frequency detector frequency. $F_{PFDMAX} = F_{CLKFB} / CLKFBOUT_MULT$

Table 54: Switching Characteristics for the Delay-Locked Loop (DLL)⁽¹⁾

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges										
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs.	5	280	5	280	5	250	5	175	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs.	5	200	5	200	5	200	5	175	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs.	10	375	10	375	10	334	10	250	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output.	0.3125	186	0.3125	186	0.3125	166	0.3125	88.6	MHz
Output Clock Jitter ⁽²⁾⁽³⁾⁽⁴⁾										
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output.	–	±100	–	±100	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs.	Maximum = ±[0.5% of CLKIN period + 100]								ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division.	Maximum = ±[0.5% of CLKIN period + 100]								ps
Duty Cycle ⁽⁴⁾										
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion.	Typical = ±[1% of CLKIN period + 350]								ps
Phase Alignment ⁽⁴⁾										
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 1X).	–	±150	–	±150	–	±150	–	±250	ps
	Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 2X). ⁽⁶⁾	–	±250	–	±250	–	±250	–	±350	
CLKOUT_PHASE_DLL	Phase offset between DLL outputs for CLK0 to CLK2X (not CLK2X180).	Maximum = ±[1% of CLKIN period + 100]								ps
	Phase offset between DLL outputs for all others.	Maximum = ±[1% of CLKIN period + 150]						Maximum = ±[1% of CLKIN period + 200]		ps

Table 57: Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)⁽¹⁾ (Cont'd)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Spread Spectrum										
F _{CLKIN_FIXED_SPREAD_SPECTRUM}	Frequency of the CLKIN input for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD/ CENTER_HIGH_SPREAD)	30	200	30	200	30	200	30	200	MHz
T _{CENTER_LOW_SPREAD} ⁽⁶⁾	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD)	Typical = $\frac{100}{\text{CLKFX_DIVIDE}}$ Maximum = 250								ps
T _{CENTER_HIGH_SPREAD} ⁽⁶⁾	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM= CENTER_HIGH_SPREAD)	Typical = $\frac{240}{\text{CLKFX_DIVIDE}}$ Maximum = 400								ps
F _{MOD_FIXED_SPREAD_SPECTRUM} ⁽⁶⁾	Average modulation frequency when using fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD / CENTER_HIGH_SPREAD)	Typical = F _{IN} /1024								MHz

Notes:

- The values in this table are based on the operating conditions described in Table 2 and Table 55.
- For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
- Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
- The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
- Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of $\pm(1\% \text{ of CLKFX period} + 200 \text{ ps})$. Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is $\pm(100 \text{ ps} + 200 \text{ ps}) = \pm 300 \text{ ps}$.
- When using CENTER_LOW_SPREAD, CENTER_HIGH_SPREAD, the valid values for CLKFX_MULTIPLY are limited to 2 through 32, and the valid values for CLKFX_DIVIDE are limited to 1 through 4.

Table 58: Recommended Operating Conditions for the Phase-Shift Clock in Variable Phase Mode (DCM_SP) or Dynamic Frequency Synthesis (DCM_CLKGEN)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Operating Frequency Ranges										
PSCLK_FREQ	Frequency for the PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) input.	1	167	1	167	1	167	1	100	MHz
Input Pulse Requirements										
PSCLK_PULSE	PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) pulse width as a percentage of the clock period.	40	60	40	60	40	60	40	60	%

Table 59: Switching Characteristics for the Phase-Shift Clock in Variable Phase Mode⁽¹⁾

Symbol	Description	Amount of Phase Shift	Units
Phase Shifting Range			
MAX_STEPS ⁽²⁾	When CLKIN < 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period.	$\pm(\text{INTEGER}(10 \times (\text{TCLKIN} - 3 \text{ ns})))$	steps
	When CLKIN ≥ 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period.	$\pm(\text{INTEGER}(15 \times (\text{TCLKIN} - 3 \text{ ns})))$	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting.	$\pm(\text{MAX_STEPS} \times \text{DCM_DELAY_STEP_MIN})$	ps
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	$\pm(\text{MAX_STEPS} \times \text{DCM_DELAY_STEP_MAX})$	ps

Notes:

1. The values in this table are based on the operating conditions described in Table 53 and Table 58.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM has no initial fixed-phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the end of Table 54.

Table 60: Miscellaneous DCM Timing Parameters⁽¹⁾

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	3	–	CLKIN cycles

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFXDV, CLKFX180) are unaffected.

Table 61: Frequency Synthesis

Attribute	Min	Max
CLKFX_MULTIPLY (DCM_SP)	2	32
CLKFX_DIVIDE (DCM_SP)	1	32
CLKDV_DIVIDE (DCM_SP)	1.5	16
CLKFX_MULTIPLY (DCM_CLKGEN)	2	256
CLKFX_DIVIDE (DCM_CLKGEN)	1	256
CLKFXDV_DIVIDE (DCM_CLKGEN)	2	32

Table 62: DCM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T _{DMCK_PSEN} /T _{DMCKC_PSEN}	PSEN Setup/Hold	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	ns
T _{DMCK_PSINCDEC} /T _{DMCKC_PSINCDEC}	PSINCDEC Setup/Hold	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	ns
T _{DMCKO_PSDONE}	Clock to out of PSDONE	1.50	1.50	1.50	1.50	ns

Table 65: Global Clock Input to Output Delay With DCM in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in Source-Synchronous Mode.							
T _{ICKOFDCM_0}	Global Clock and OUTFF <i>with</i> DCM	XC6SLX4	5.03	N/A	7.21	8.05	ns
		XC6SLX9	5.03	6.13	7.21	8.05	ns
		XC6SLX16	5.08	5.51	6.44	7.96	ns
		XC6SLX25	4.81	5.13	5.69	7.94	ns
		XC6SLX25T	4.81	5.13	5.69	N/A	ns
		XC6SLX45	5.26	5.69	6.63	7.92	ns
		XC6SLX45T	5.26	5.69	6.63	N/A	ns
		XC6SLX75	4.77	5.18	5.88	7.95	ns
		XC6SLX75T	4.77	5.18	5.88	N/A	ns
		XC6SLX100	4.72	5.11	5.76	8.59	ns
		XC6SLX100T	4.76	5.11	5.76	N/A	ns
		XC6SLX150	4.90	5.30	5.93	7.93	ns
		XC6SLX150T	4.90	5.30	5.93	N/A	ns
		XA6SLX4	5.35	N/A	7.21	N/A	ns
		XA6SLX9	5.35	N/A	7.21	N/A	ns
		XA6SLX16	5.42	N/A	6.44	N/A	ns
		XA6SLX25	5.13	N/A	5.69	N/A	ns
		XA6SLX25T	5.13	N/A	5.79	N/A	ns
		XA6SLX45	5.58	N/A	6.63	N/A	ns
		XA6SLX45T	5.58	N/A	6.63	N/A	ns
		XA6SLX75	5.09	N/A	5.87	N/A	ns
		XA6SLX75T	5.09	N/A	5.87	N/A	ns
		XA6SLX100	N/A	N/A	6.44	N/A	ns
		XQ6SLX75	N/A	N/A	5.87	7.95	ns
		XQ6SLX75T	5.09	N/A	5.87	N/A	ns
		XQ6SLX150	N/A	N/A	6.06	7.93	ns
		XQ6SLX150T	5.50	N/A	6.06	N/A	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
- DCM output jitter is already included in the timing calculation.

Table 66: Global Clock Input to Output Delay With PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> PLL in System-Synchronous Mode.							
T _{ICKOFPLL}	Global Clock and OUTFF <i>with</i> PLL	XC6SLX4	4.57	N/A	6.25	7.34	ns
		XC6SLX9	4.57	5.25	6.25	7.34	ns
		XC6SLX16	4.41	4.64	5.39	6.92	ns
		XC6SLX25	4.03	4.32	4.91	7.64	ns
		XC6SLX25T	4.03	4.32	4.91	N/A	ns
		XC6SLX45	4.63	4.96	5.75	7.36	ns
		XC6SLX45T	4.63	4.96	5.75	N/A	ns
		XC6SLX75	4.01	4.30	4.88	7.15	ns
		XC6SLX75T	4.01	4.30	4.88	N/A	ns
		XC6SLX100	4.02	4.33	4.90	7.37	ns
		XC6SLX100T	4.06	4.33	4.90	N/A	ns
		XC6SLX150	3.65	3.98	4.58	6.94	ns
		XC6SLX150T	3.65	3.98	4.58	N/A	ns
		XA6SLX4	4.88	N/A	6.13	N/A	ns
		XA6SLX9	4.88	N/A	6.13	N/A	ns
		XA6SLX16	4.74	N/A	5.27	N/A	ns
		XA6SLX25	4.43	N/A	4.78	N/A	ns
		XA6SLX25T	4.43	N/A	4.88	N/A	ns
		XA6SLX45	4.94	N/A	5.62	N/A	ns
		XA6SLX45T	4.94	N/A	5.62	N/A	ns
		XA6SLX75	4.32	N/A	4.77	N/A	ns
		XA6SLX75T	4.32	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.41	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	7.15	ns
		XQ6SLX75T	4.32	N/A	4.77	N/A	ns
		XQ6SLX150	N/A	N/A	4.60	6.94	ns
		XQ6SLX150T	4.35	N/A	4.60	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 69: Global Clock Input to Output Delay With DCM and PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode.							
T _{ICKOFDCM0_PLL}	Global Clock and OUTFF with DCM and PLL	XC6SLX4	5.58	N/A	7.42	8.54	ns
		XC6SLX9	5.58	6.19	7.42	8.54	ns
		XC6SLX16	5.50	6.06	7.05	8.24	ns
		XC6SLX25	5.57	6.04	7.02	8.33	ns
		XC6SLX25T	5.57	6.04	7.02	N/A	ns
		XC6SLX45	5.53	5.97	6.96	8.32	ns
		XC6SLX45T	5.53	5.97	6.96	N/A	ns
		XC6SLX75	5.55	6.00	6.99	8.54	ns
		XC6SLX75T	5.55	6.00	6.99	N/A	ns
		XC6SLX100	5.58	6.03	7.02	9.11	ns
		XC6SLX100T	5.62	6.03	7.02	N/A	ns
		XC6SLX150	5.32	5.70	6.41	8.26	ns
		XC6SLX150T	5.32	5.70	6.41	N/A	ns
		XA6SLX4	5.87	N/A	7.28	N/A	ns
		XA6SLX9	5.87	N/A	7.28	N/A	ns
		XA6SLX16	6.02	N/A	6.87	N/A	ns
		XA6SLX25	5.88	N/A	6.90	N/A	ns
		XA6SLX25T	5.88	N/A	7.00	N/A	ns
		XA6SLX45	5.82	N/A	6.81	N/A	ns
		XA6SLX45T	5.82	N/A	6.81	N/A	ns
		XA6SLX75	5.81	N/A	6.80	N/A	ns
		XA6SLX75T	5.81	N/A	6.80	N/A	ns
		XA6SLX100	N/A	N/A	6.88	N/A	ns
		XQ6SLX75	N/A	N/A	6.80	8.54	ns
		XQ6SLX75T	5.81	N/A	6.80	N/A	ns
		XQ6SLX150	N/A	N/A	6.41	8.26	ns
		XQ6SLX150T	5.90	N/A	6.41	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 73: Global Clock Setup and Hold With DCM in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾							
T _{PSDCM0} / T _{PHDCM0}	No Delay Global Clock and IFF ⁽²⁾ with DCM in Source-Synchronous Mode	XC6SLX4	0.71/0.65	N/A	0.72/1.22	1.58/1.18	ns
		XC6SLX9	0.71/0.69	0.71/1.19	0.72/1.36	1.58/1.18	ns
		XC6SLX16	0.86/0.52	0.92/0.57	1.04/0.60	1.02/1.06	ns
		XC6SLX25	0.84/0.58	0.90/0.59	1.01/0.59	1.58/1.07	ns
		XC6SLX25T	0.84/0.58	0.90/0.59	1.01/0.59	N/A	ns
		XC6SLX45	0.85/0.70	0.90/0.76	0.98/0.79	1.34/1.34	ns
		XC6SLX45T	0.85/0.70	0.90/0.76	0.98/0.79	N/A	ns
		XC6SLX75	1.00/0.62	1.06/0.63	1.15/0.63	1.65/1.46	ns
		XC6SLX75T	1.00/0.71	1.06/0.72	1.15/0.72	N/A	ns
		XC6SLX100	0.81/0.68	0.81/0.69	0.94/0.69	1.42/2.07	ns
		XC6SLX100T	0.81/0.68	0.81/0.69	0.94/0.69	N/A	ns
		XC6SLX150	0.68/0.98	0.69/0.99	0.79/0.99	1.45/1.60	ns
		XC6SLX150T	0.68/0.98	0.69/0.99	0.79/0.99	N/A	ns
		XA6SLX4	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX9	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX16	1.01/0.56	N/A	1.04/0.60	N/A	ns
		XA6SLX25	0.94/0.76	N/A	1.06/0.77	N/A	ns
		XA6SLX25T	0.94/0.76	N/A	1.14/0.77	N/A	ns
		XA6SLX45	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX45T	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX75	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX100	N/A	N/A	1.37/0.75	N/A	ns
		XQ6SLX75	N/A	N/A	1.15/0.72	1.65/1.46	ns
		XQ6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XQ6SLX150	N/A	N/A	0.79/1.15	1.45/1.60	ns
		XQ6SLX150T	0.73/1.15	N/A	0.79/1.15	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 77: Global Clock Setup and Hold With DCM and PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Example Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin, ⁽¹⁾ Using DCM, PLL, and Global Clock Buffer for the LVCMOS25 standard.							
T _{PSDCMPLL_0} / T _{PHDCMPLL_0}	No Delay Global Clock and IFF ⁽²⁾ with DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode.	XC6SLX4	0.43/1.07	N/A	0.43/1.43	1.10/1.67	ns
		XC6SLX9	0.43/1.03	0.45/1.14	0.45/1.43	1.10/1.67	ns
		XC6SLX16	0.74/0.93	0.74/1.12	0.74/1.21	0.77/1.35	ns
		XC6SLX25	0.67/1.02	0.76/1.11	0.84/1.18	1.23/1.46	ns
		XC6SLX25T	0.67/1.02	0.76/1.11	0.84/1.18	N/A	ns
		XC6SLX45	0.65/0.99	0.65/1.04	0.71/1.12	1.18/1.58	ns
		XC6SLX45T	0.65/1.00	0.65/1.04	0.71/1.12	N/A	ns
		XC6SLX75	0.86/1.01	0.88/1.06	0.94/1.14	1.29/1.67	ns
		XC6SLX75T	0.86/1.01	0.88/1.06	0.94/1.14	N/A	ns
		XC6SLX100	0.50/1.10	0.56/1.10	0.61/1.17	0.84/2.24	ns
		XC6SLX100T	0.50/1.10	0.56/1.10	0.61/1.17	N/A	ns
		XC6SLX150	0.45/1.28	0.47/1.28	0.52/1.28	1.27/1.56	ns
		XC6SLX150T	0.45/1.28	0.47/1.28	0.52/1.28	N/A	ns
		XA6SLX4	0.74/1.00	N/A	0.74/1.43	N/A	ns
		XA6SLX9	0.74/1.00	N/A	0.74/1.43	N/A	ns
		XA6SLX16	1.81/1.15	N/A	1.81/1.03	N/A	ns
		XA6SLX25	0.89/1.01	N/A	0.96/1.05	N/A	ns
		XA6SLX25T	0.89/1.01	N/A	1.04/1.15	N/A	ns
		XA6SLX45	0.69/0.95	N/A	0.83/0.96	N/A	ns
		XA6SLX45T	0.69/0.95	N/A	0.83/0.96	N/A	ns
		XA6SLX75	0.88/0.94	N/A	1.06/0.96	N/A	ns
		XA6SLX75T	0.88/0.94	N/A	1.06/0.96	N/A	ns
		XA6SLX100	N/A	N/A	1.55/1.33	N/A	ns
		XQ6SLX75	N/A	N/A	1.06/0.96	1.29/1.67	ns
		XQ6SLX75T	0.88/0.94	N/A	1.06/0.96	N/A	ns
		XQ6SLX150	N/A	N/A	0.64/1.30	1.27/1.56	ns
		XQ6SLX150T	0.58/1.30	N/A	0.64/1.30	N/A	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG. Package skew is not included in these measurements.
- IFF = Input Flip-Flop