# AMD Xilinx - XC6SLX16-2FTG256I Datasheet

**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 1139 |
| Number of Logic Elements/Cells | 14579 |
| Total RAM Bits | 589824 |
| Number of I/O | 186 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FTBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc6slx16-2ftg256i |

*Table 1:* **Absolute Maximum Ratings[1] *(Cont'd)***

| Symbol | Description | | | | | Units |
|---|---|---|---|---|---|---|
| $V_{IN}$ and $V_{TS}$[3] | I/O input voltage or voltage applied to 3-state output, relative to GND[4] | All user and dedicated I/Os | Commercial | DC | –0.60 to 4.10 | V |
| | | | | 20% overshoot duration | –0.75 to 4.25 | V |
| | | | | 8% overshoot duration[5] | –0.75 to 4.40 | V |
| | | | Industrial | DC | –0.60 to 3.95 | V |
| | | | | 20% overshoot duration | –0.75 to 4.15 | V |
| | | | | 4% overshoot duration[5] | –0.75 to 4.40 | V |
| | | | Expanded (Q) | DC | –0.60 to 3.95 | V |
| | | | | 20% overshoot duration | –0.75 to 4.15 | V |
| | | | | 4% overshoot duration[5] | –0.75 to 4.40 | V |
| | | Restricted to maximum of 100 user I/Os | Commercial | 20% overshoot duration | –0.75 to 4.35 | V |
| | | | | 15% overshoot duration[5] | –0.75 to 4.40 | V |
| | | | | 10% overshoot duration | –0.75 to 4.45 | V |
| | | | Industrial | 20% overshoot duration | –0.75 to 4.25 | V |
| | | | | 10% overshoot duration | –0.75 to 4.35 | V |
| | | | | 8% overshoot duration[5] | –0.75 to 4.40 | V |
| | | | Expanded (Q) | 20% overshoot duration | –0.75 to 4.25 | V |
| | | | | 10% overshoot duration | –0.75 to 4.35 | V |
| | | | | 8% overshoot duration[5] | –0.75 to 4.40 | V |
| $T_{STG}$ | Storage temperature (ambient) | | | | –65 to 150 | °C |
| $T_{SOL}$ | Maximum soldering temperature[6] (TQG144, CPG196, CSG225, CSG324, CSG484, and FTG256) | | | | +260 | °C |
| | Maximum soldering temperature[6] (Pb-free packages: FGG484, FGG676, and FGG900) | | | | +250 | °C |
| | Maximum soldering temperature[6] (Pb packages: CS484, FT256, FG484, FG676, and FG900) | | | | +220 | °C |
| $T_j$ | Maximum junction temperature[6] | | | | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When programming eFUSE, $V_{FS} \leq V_{CCAUX}$. Requires up to 40 mA current. For read mode, $V_{FS}$ can be between GND and 3.45 V.
3. I/O absolute maximum limit applied to DC and AC signals. Overshoot duration is the percentage of a data period that the I/O is stressed beyond 3.45V.
4. For I/O operation, refer to UG381: *Spartan-6 FPGA SelectIO Resources User Guide*.
5. Maximum percent overshoot duration to meet 4.40V maximum.
6. For soldering guidelines and thermal considerations, see UG385: *Spartan-6 FPGA Packaging and Pinout Specification*.

*Table 3:* **eFUSE Programming Conditions(1)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{FS}$(2) | External voltage supply | 3.2 | 3.3 | 3.4 | V |
| $I_{FS}$ | $V_{FS}$ supply current | – | – | 40 | mA |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND | 3.2 | 3.3 | 3.45 | V |
| $R_{FUSE}$(3) | External resistor from $R_{FUSE}$ pin to GND | 1129 | 1140 | 1151 | Ω |
| $V_{CCINT}$ | Internal supply voltage relative to GND | 1.14 | 1.2 | 1.26 | V |
| $t_j$ | Temperature range | 15 | – | 85 | °C |

**Notes:**

1. These specifications apply during programming of the eFUSE AES key. Programming is only supported through JTAG.The AES key is only supported in the following devices: LX75, LX75T, LX100, LX100T, LX150, and LX150T.
2. When programming eFUSE, $V_{FS}$ must be less than or equal to $V_{CCAUX}$. When not programming or when eFUSE is not used, Xilinx recommends connecting $V_{FS}$ to GND. However, $V_{FS}$ can be between GND and 3.45 V.
3. An $R_{FUSE}$ resistor is required when programming the eFUSE AES key. When not programming or when eFUSE is not used, Xilinx recommends connecting the $R_{FUSE}$ pin to $V_{CCAUX}$ or GND. However, $R_{FUSE}$ can be unconnected.

*Table 4:* **DC Characteristics Over Recommended Operating Conditions**

| Symbol | Description | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{DRINT}$ | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) | | 0.8 | – | – | V |
| $V_{DRAUX}$ | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) | | 2.0 | – | – | V |
| $I_{REF}$ | $V_{REF}$ leakage current per pin for commercial (C) and industrial (I) devices | | –10 | – | 10 | µA |
| | $V_{REF}$ leakage current per pin for expanded (Q) devices | | –15 | – | 15 | µA |
| $I_L$ | Input or output leakage current per pin (sample-tested) for commercial (C) and industrial (I) devices | | –10 | – | 10 | µA |
| | Input or output leakage current per pin (sample-tested) for expanded (Q) devices | | –15 | – | 15 | µA |
| $I_{HS}$ | Leakage current on pins during hot socketing with FPGA unpowered | All pins except PROGRAM_B, DONE, and JTAG pins when HSWAPEN = 1 | –20 | – | 20 | µA |
| | | PROGRAM_B, DONE, and JTAG pins, or other pins when HSWAPEN = 0 | $I_{HS} + I_{RPU}$ | | | µA |
| $C_{IN}$[1] | Die input capacitance at the pad | | – | – | 10 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V or $V_{CCAUX}$ = 3.3V | | 200 | – | 500 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V or $V_{CCAUX}$ = 2.5V | | 120 | – | 350 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | | 60 | – | 200 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | | 40 | – | 150 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | | 12 | – | 100 | µA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{IN}$ = $V_{CCO}$, $V_{CCAUX}$ = 3.3V | | 200 | – | 550 | µA |
| | Pad pull-down (when selected) @ $V_{IN}$ = $V_{CCO}$, $V_{CCAUX}$ = 2.5V | | 140 | – | 400 | µA |
| $I_{BATT}$[2] | Battery supply current | | – | – | 150 | nA |
| $R_{DT}$[3] | Resistance of optional input differential termination circuit, $V_{CCAUX}$ = 3.3V | | – | 100 | – | Ω |
| $R_{IN\_TERM}$[5] | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_25) for commercial (C) and industrial (I) devices | | 23 | 25 | 55 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_25) for expanded (Q) devices | | 20 | 25 | 55 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_50) for commercial (C) and industrial (I) devices | | 39 | 50 | 72 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_50) for expanded (Q) devices | | 32 | 50 | 74 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_75) for commercial (C) and industrial (I) devices | | 56 | 75 | 109 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_75) for expanded (Q) devices | | 47 | 75 | 115 | Ω |
| $R_{OUT\_TERM}$ | Thevenin equivalent resistance of programmable output termination (UNTUNED_25) | | 11 | 25 | 52 | Ω |
| | Thevenin equivalent resistance of programmable output termination (UNTUNED_50) | | 21 | 50 | 96 | Ω |
| | Thevenin equivalent resistance of programmable output termination (UNTUNED_75) | | 29 | 75 | 145 | Ω |

**Notes:**

1. The $C_{IN}$ measurement represents the die capacitance at the pad, not including the package.
2. Maximum value specified for worst case process at 25°C. LX75, LX75T, LX100, LX100T, LX150, and LX150T only.
3. Refer to IBIS models for $R_{DT}$ variation and for values at $V_{CCAUX}$ = 2.5V. IBIS values for $R_{DT}$ are valid for all temperature ranges.
4. $V_{CCO2}$ is not required for data retention. The minimum $V_{CCO2}$ for power-on reset and configuration is 1.65V.
5. Termination resistance to a $V_{CCO}$/2 level.

*Table 14:* **GTP Transceiver Current Supply (per Lane)**

| Symbol | Description | Typ[1] | Max | Units |
|---|---|---|---|---|
| $I_{MGTAVCC}$ | GTP transceiver internal analog supply current | 40.4 | Note 2 | mA |
| $I_{MGTAVTTTX}$ | GTP transmitter termination supply current | 27.4 | | mA |
| $I_{MGTAVTTRX}$ | GTP receiver termination supply current | 13.6 | | mA |
| $I_{MGTAVCCPLL}$ | GTP transmitter and receiver PLL supply current | 28.7 | | mA |
| $R_{MGTRREF}$ | Precision reference resistor for internal calibration termination | 50.0 ± 1% tolerance | | Ω |

**Notes:**
1. Typical values are specified at nominal voltage, 25°C, with a 2.5 Gb/s line rate, with a shared PLL use mode.
2. Values for currents of other transceiver configurations and conditions can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

*Table 15:* **GTP Transceiver Quiescent Supply Current (per Lane)[1][2][3][4]**

| Symbol | Description | Typ[5] | Max | Units |
|---|---|---|---|---|
| $I_{MGTAVCCQ}$ | Quiescent MGTAVCC supply current | 1.7 | Note 2 | mA |
| $I_{MGTAVTTTXQ}$ | Quiescent MGTAVTTTX supply current | 0.1 | | mA |
| $I_{MGTAVTTRXQ}$ | Quiescent MGTAVTTRX supply current | 1.2 | | mA |
| $I_{MGTAVCCPLLQ}$ | Quiescent MGTAVCCPLL supply current | 1.0 | | mA |

**Notes:**
1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
3. GTP transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTP transceivers.
4. Does not include power-up MGTAVTTRCAL supply current during device configuration.
5. Typical values are specified at nominal voltage, 25°C.

*Table 21:* **GTP Transceiver User Clock Switching Characteristics(1)**

| Symbol | Description | Conditions | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| $F_{TXOUT}$ | TXOUTCLK maximum frequency | | 320 | 320 | 270 | N/A | MHz |
| $F_{RXREC}$ | RXRECCLK maximum frequency | | 320 | 320 | 270 | N/A | MHz |
| $T_{RX}$ | RXUSRCLK maximum frequency | | 320 | 320 | 270 | N/A | MHz |
| $T_{RX2}$ | RXUSRCLK2 maximum frequency | 1 byte interface | 156.25 | 156.25 | 125 | N/A | MHz |
| | | 2 byte interface | 160 | 160 | 125 | N/A | MHz |
| | | 4 byte interface | 80 | 80 | 67.5 | N/A | MHz |
| $T_{TX}$ | TXUSRCLK maximum frequency | | 320 | 320 | 270 | N/A | MHz |
| $T_{TX2}$ | TXUSRCLK2 maximum frequency | 1 byte interface | 156.25 | 156.25 | 125 | N/A | MHz |
| | | 2 byte interface | 160 | 160 | 125 | N/A | MHz |
| | | 4 byte interface | 80 | 80 | 67.5 | N/A | MHz |

**Notes:**
1. Clocking must be implemented as described in UG386: *Spartan-6 FPGA GTP Transceivers User Guide*.

*Table 22:* **GTP Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{RTX}$ | TX Rise time | 20%–80% | – | 140 | – | ps |
| $T_{FTX}$ | TX Fall time | 80%–20% | – | 120 | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | – | – | 400 | ps |
| $V_{TXOOBVDPP}$ | Electrical idle amplitude | | – | – | 20 | mV |
| $T_{TXOOBTRANSITION}$ | Electrical idle transition time | | – | – | 50 | ns |
| $T_{J3.125}$ | Total Jitter(2) | 3.125 Gb/s | – | – | 0.35 | UI |
| $D_{J3.125}$ | Deterministic Jitter(2) | | – | – | 0.15 | UI |
| $T_{J2.5}$ | Total Jitter(2) | 2.5 Gb/s | – | – | 0.33 | UI |
| $D_{J2.5}$ | Deterministic Jitter(2) | | – | – | 0.15 | UI |
| $T_{J1.62}$ | Total Jitter(2) | 1.62 Gb/s | – | – | 0.20 | UI |
| $D_{J1.62}$ | Deterministic Jitter(2) | | – | – | 0.10 | UI |
| $T_{J1.25}$ | Total Jitter(2) | 1.25 Gb/s | – | – | 0.20 | UI |
| $D_{J1.25}$ | Deterministic Jitter(2) | | – | – | 0.10 | UI |
| $T_{J614}$ | Total Jitter(2) | 614 Mb/s | – | – | 0.10 | UI |
| $D_{J614}$ | Deterministic Jitter(2) | | – | – | 0.05 | UI |

**Notes:**
1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP transceiver sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.

*Table 23:* **GTP Transceiver Receiver Switching Characteristics**

| Symbol | Description | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $T_{RXELECIDLE}$ | Time for RXELECIDLE to respond to loss or restoration of data | | | – | 75 | – | ns |
| $R_{XOOBVDPP}$ | OOB detect threshold peak-to-peak | | | 60 | – | 150 | mV |
| $R_{XSST}$ | Receiver spread-spectrum tracking(1) | | Modulated @ 33 KHz | –5000 | – | 0 | ppm |
| $R_{XRL}$ | Run length (CID) | Internal AC capacitor bypassed | | – | – | 150 | UI |
| $R_{XPPMTOL}$ | Data/REFCLK PPM offset tolerance | CDR 2nd-order loop disabled | | –200 | – | 200 | ppm |
| | | CDR 2nd-order loop enabled | PLL_RXDIVSEL_OUT = 1 | –2000 | – | 2000 | ppm |
| | | | PLL_RXDIVSEL_OUT = 2 | –2000 | – | 2000 | ppm |
| | | | PLL_RXDIVSEL_OUT = 4 | –1000 | – | 1000 | ppm |
| **SJ Jitter Tolerance(2)** | | | | | | | |
| $JT\_SJ_{3.125}$ | Sinusoidal Jitter(3) | | 3.125 Gb/s | 0.4 | – | – | UI |
| $JT\_SJ_{2.5}$ | Sinusoidal Jitter(3) | | 2.5 Gb/s | 0.4 | – | – | UI |
| $JT\_SJ_{1.62}$ | Sinusoidal Jitter(3) | | 1.62 Gb/s | 0.5 | – | – | UI |
| $JT\_SJ_{1.25}$ | Sinusoidal Jitter(3) | | 1.25 Gb/s | 0.5 | – | – | UI |
| $JT\_SJ_{614}$ | Sinusoidal Jitter(3) | | 614 Mb/s | 0.5 | – | – | UI |
| **SJ Jitter Tolerance with Stressed Eye(2)(5)** | | | | | | | |
| $JT\_TJSE_{3.125}$ | Total Jitter with stressed eye(4) | | 3.125 Gb/s | 0.65 | – | – | UI |
| $JT\_SJSE_{3.125}$ | Sinusoidal Jitter with stressed eye | | 3.125 Gb/s | 0.1 | – | – | UI |
| $JT\_TJSE_{2.7}$ | Total Jitter with stressed eye(4) | | 2.7 Gb/s | 0.65 | – | – | UI |
| $JT\_SJSE_{2.7}$ | Sinusoidal Jitter with stressed eye | | 2.7 Gb/s | 0.1 | – | – | UI |

**Notes:**
1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a Bit Error Ratio of $1e^{-12}$.
3. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
4. Composed of 0.37 UI DJ in the form of ISI and 0.18 UI RJ.
5. Measured using PRBS7 data pattern.

## Endpoint Block for PCI Express Designs Switching Characteristics

The Endpoint block for PCI Express is available in the Spartan-6 LXT devices. Consult the Spartan-6 FPGA Integrated Endpoint Block for PCI Express for further information.

*Table 24:* **Maximum Performance for PCI Express Designs**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| $F_{PCIEUSER}$ | User clock maximum frequency | 62.5 | 62.5 | 62.5 | N/A | MHz |

## Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 27 lists the production released Spartan-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE® software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

*Table 27:* **Spartan-6 Device Production Software and Speed Specification Release(1)**

| Device | Speed Grade Designations(2) | | | |
|---|---|---|---|---|
| | -3(3) | -3N | -2(4) | -1L |
| XC6SLX4 | ISE 12.4 v1.15 | N/A | ISE 12.3 v1.12(5) | ISE 13.2 v1.07 |
| XC6SLX9 | ISE 12.4 v1.15 | ISE 13.1 Update v1.18(7) | ISE 12.3 v1.12(5) | ISE 13.2 v1.07 |
| XC6SLX16 | ISE 12.1 v1.08 | ISE 13.1 Update v1.18(7) | ISE 11.5 v1.06 | ISE 13.2 v1.07 |
| XC6SLX25 | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | ISE 13.2 v1.07 |
| XC6SLX25T | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | N/A |
| XC6SLX45 | ISE 12.1 v1.08 | ISE 13.1 Update v1.18(7) | ISE 11.5 v1.07 | ISE 13.1 v1.06 |
| XC6SLX45T | ISE 12.1 v1.08 | ISE 13.1 Update v1.18(7) | ISE 12.1 v1.08 | N/A |
| XC6SLX75 | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | ISE 13.2 v1.07 |
| XC6SLX75T | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | N/A |
| XC6SLX100 | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | ISE 13.1 v1.06 |
| XC6SLX100T | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | N/A |
| XC6SLX150 | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | ISE 13.1 v1.06 |
| XC6SLX150T | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | N/A |
| XA6SLX4 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX9 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX16 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX25 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX25T | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX45 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX45T | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX75 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX75T | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX100 | N/A | N/A | ISE 13.3 v1.20 | N/A |

*Table 28:* **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -3N | -2 | -1L[1] | -3 | -3N | -2 | -1L[1] | -3 | -3N | -2 | -1L[1] | |
| LVCMOS12, Fast, 2 mA | 0.91 | 1.03 | 1.16 | 1.51 | 3.46 | 3.60 | 3.80 | 4.44 | 3.46 | 3.60 | 3.80 | 4.44 | ns |
| LVCMOS12, Fast, 4 mA | 0.91 | 1.03 | 1.16 | 1.51 | 2.35 | 2.49 | 2.69 | 3.30 | 2.35 | 2.49 | 2.69 | 3.30 | ns |
| LVCMOS12, Fast, 6 mA | 0.91 | 1.03 | 1.16 | 1.51 | 1.79 | 1.93 | 2.13 | 2.75 | 1.79 | 1.93 | 2.13 | 2.75 | ns |
| LVCMOS12, Fast, 8 mA | 0.91 | 1.03 | 1.16 | 1.51 | 1.68 | 1.82 | 2.02 | 2.64 | 1.68 | 1.82 | 2.02 | 2.64 | ns |
| LVCMOS12, Fast, 12 mA | 0.91 | 1.03 | 1.16 | 1.51 | 1.66 | 1.80 | 2.00 | 2.62 | 1.66 | 1.80 | 2.00 | 2.62 | ns |
| LVCMOS12_JEDEC, QUIETIO, 2 mA | 1.50 | 1.62 | 1.75 | 1.88 | 6.39 | 6.53 | 6.73 | 7.31 | 6.39 | 6.53 | 6.73 | 7.31 | ns |
| LVCMOS12_JEDEC, QUIETIO, 4 mA | 1.50 | 1.62 | 1.75 | 1.88 | 4.98 | 5.12 | 5.32 | 5.88 | 4.98 | 5.12 | 5.32 | 5.88 | ns |
| LVCMOS12_JEDEC, QUIETIO, 6 mA | 1.50 | 1.62 | 1.75 | 1.88 | 4.67 | 4.81 | 5.01 | 5.54 | 4.67 | 4.81 | 5.01 | 5.54 | ns |
| LVCMOS12_JEDEC, QUIETIO, 8 mA | 1.50 | 1.62 | 1.75 | 1.88 | 4.23 | 4.37 | 4.57 | 5.22 | 4.23 | 4.37 | 4.57 | 5.22 | ns |
| LVCMOS12_JEDEC, QUIETIO, 12 mA | 1.50 | 1.62 | 1.75 | 1.88 | 3.99 | 4.13 | 4.33 | 4.94 | 3.99 | 4.13 | 4.33 | 4.94 | ns |
| LVCMOS12_JEDEC, Slow, 2 mA | 1.50 | 1.62 | 1.75 | 1.88 | 5.00 | 5.14 | 5.34 | 5.90 | 5.00 | 5.14 | 5.34 | 5.90 | ns |
| LVCMOS12_JEDEC, Slow, 4 mA | 1.50 | 1.62 | 1.75 | 1.88 | 2.85 | 2.99 | 3.19 | 3.80 | 2.85 | 2.99 | 3.19 | 3.80 | ns |
| LVCMOS12_JEDEC, Slow, 6 mA | 1.50 | 1.62 | 1.75 | 1.88 | 2.76 | 2.90 | 3.10 | 3.72 | 2.76 | 2.90 | 3.10 | 3.72 | ns |
| LVCMOS12_JEDEC, Slow, 8 mA | 1.50 | 1.62 | 1.75 | 1.88 | 2.35 | 2.49 | 2.69 | 3.30 | 2.35 | 2.49 | 2.69 | 3.30 | ns |
| LVCMOS12_JEDEC, Slow, 12 mA | 1.50 | 1.62 | 1.75 | 1.88 | 2.09 | 2.23 | 2.43 | 3.05 | 2.09 | 2.23 | 2.43 | 3.05 | ns |
| LVCMOS12_JEDEC, Fast, 2 mA | 1.50 | 1.62 | 1.75 | 1.88 | 3.46 | 3.60 | 3.80 | 4.42 | 3.46 | 3.60 | 3.80 | 4.42 | ns |
| LVCMOS12_JEDEC, Fast, 4 mA | 1.50 | 1.62 | 1.75 | 1.88 | 2.35 | 2.49 | 2.69 | 3.31 | 2.35 | 2.49 | 2.69 | 3.31 | ns |
| LVCMOS12_JEDEC, Fast, 6 mA | 1.50 | 1.62 | 1.75 | 1.88 | 1.79 | 1.93 | 2.13 | 2.76 | 1.79 | 1.93 | 2.13 | 2.76 | ns |
| LVCMOS12_JEDEC, Fast, 8 mA | 1.50 | 1.62 | 1.75 | 1.88 | 1.69 | 1.83 | 2.03 | 2.65 | 1.69 | 1.83 | 2.03 | 2.65 | ns |
| LVCMOS12_JEDEC, Fast, 12 mA | 1.50 | 1.62 | 1.75 | 1.88 | 1.66 | 1.80 | 2.00 | 2.62 | 1.66 | 1.80 | 2.00 | 2.62 | ns |

**Notes:**

1. The -1L values listed in this table are also applicable to the Spartan-6Q devices.
2. Devices with a -1L speed grade do not support Xilinx PCI IP.

*Table 34:* **SSO Limit per $V_{CCO}$/GND Pair**

| $V_{CCO}$ | I/O Standard | Drive | Slew | SSO Limit per $V_{CCO}$/GND Pair | | | |
|---|---|---|---|---|---|---|---|
| | | | | All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324 | | All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324 | |
| | | | | Bank 0/2 | Bank 1/3 | Bank 0/2 | Bank 1/3/4/5 |
| 1.2V | LVCMOS12, LVCMOS12_JEDEC | 2 | Fast | 30 (1) | 35 | 30 | 35 |
| | | | Slow | 51 | 55 | 51 | 52 |
| | | | QuietIO | 71 | 58 | 71 | 70 |
| | | 4 | Fast | 17 | 17 | 17 | 19 |
| | | | Slow | 23 | 25 | 23 | 22 |
| | | | QuietIO | 35 | 32 | 35 | 32 |
| | | 6 | Fast | 13 | 15 | 13 | 14 |
| | | | Slow | 19 | 20 | 19 | 17 |
| | | | QuietIO | 26 | 24 | 26 | 24 |
| | | 8 | Fast | N/A | 12 | N/A | 12 |
| | | | Slow | N/A | 15 | N/A | 13 |
| | | | QuietIO | N/A | 20 | N/A | 19 |
| | | 12 | Fast | N/A | 5 | N/A | 4 |
| | | | Slow | N/A | 8 | N/A | 5 |
| | | | QuietIO | N/A | 11 | N/A | 10 |

*Table 34:* **SSO Limit per $V_{CCO}$/GND Pair *(Cont'd)***

| $V_{CCO}$ | I/O Standard | Drive | Slew | SSO Limit per $V_{CCO}$/GND Pair | | | |
|---|---|---|---|---|---|---|---|
| | | | | All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324 | | All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324 | |
| | | | | Bank 0/2 | Bank 1/3 | Bank 0/2 | Bank 1/3/4/5 |
| 1.8V | LVCMOS18, LVCMOS18_JEDEC | 2 | Fast | 39 | 46 | 39 | 47 |
| | | | Slow | 65 | 75 | 65 | 74 |
| | | | QuietIO | 80 | 80 | 80 | 85 |
| | | 4 | Fast | 22 | 25 | 22 | 25 |
| | | | Slow | 38 | 36 | 38 | 29 |
| | | | QuietIO | 45 | 40 | 45 | 35 |
| | | 6 | Fast | 16 | 18 | 16 | 17 |
| | | | Slow | 27 | 25 | 27 | 19 |
| | | | QuietIO | 30 | 28 | 30 | 23 |
| | | 8 | Fast | 13 | 15 | 13 | 14 |
| | | | Slow | 16 | 18 | 16 | 16 |
| | | | QuietIO | 25 | 22 | 25 | 18 |
| | | 12 | Fast | 5 | 7 | 5 | 5 |
| | | | Slow | 7 | 8 | 7 | 6 |
| | | | QuietIO | 11 | 10 | 11 | 8 |
| | | 16 | Fast | 4 | 5 | 4 | 4 |
| | | | Slow | 7 | 8 | 7 | 5 |
| | | | QuietIO | 11 | 10 | 11 | 8 |
| | | 24 | Fast | N/A | 5 | N/A | 3 |
| | | | Slow | N/A | 8 | N/A | 8 |
| | | | QuietIO | N/A | 10 | N/A | 8 |
| | HSTL_I_18 | | | 9 | 10 | 9 | 9 |
| | HSTL_II_18 | | | N/A | 5 | N/A | 6 |
| | HSTL_III_18 | | | 9 | 10 | 9 | 11 |
| | DIFF_HSTL_I_18 | | | 27 | 30 | 27 | 27 |
| | DIFF_HSTL_II_18 | | | N/A | 15 | N/A | 18 |
| | DIFF_HSTL_III_18 | | | 27 | 30 | 27 | 33 |
| | MOBILE_DDR (3) | | | 12 | 14 | 12 | 14 |
| | DIFF_MOBILE_DDR (3) | | | 36 | 42 | 36 | 42 |
| | SSTL_18_I (3) | | | 9 | 10 | 9 | 10 |
| | SSTL_18_II (3) | | | N/A | 5 | N/A | 4 |
| | DIFF_SSTL_18_I (3) | | | 27 | 30 | 27 | 30 |
| | DIFF_SSTL_18_II (3) | | | N/A | 15 | N/A | 12 |

*Table 34:* **SSO Limit per $V_{CCO}$/GND Pair *(Cont'd)***

| $V_{CCO}$ | I/O Standard | Drive | Slew | SSO Limit per $V_{CCO}$/GND Pair | | | |
|---|---|---|---|---|---|---|---|
| | | | | All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324 | | All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324 | |
| | | | | Bank 0/2 | Bank 1/3 | Bank 0/2 | Bank 1/3/4/5 |
| 2.5V | LVCMOS25 | 2 | Fast | 38 | 43 | 38 | 43 |
| | | | Slow | 46 | 52 | 46 | 48 |
| | | | QuietIO | 57 | 64 | 57 | 59 |
| | | 4 | Fast | 21 | 24 | 21 | 23 |
| | | | Slow | 26 | 31 | 26 | 27 |
| | | | QuietIO | 33 | 32 | 33 | 30 |
| | | 6 | Fast | 15 | 17 | 15 | 16 |
| | | | Slow | 19 | 22 | 19 | 19 |
| | | | QuietIO | 25 | 23 | 25 | 19 |
| | | 8 | Fast | 12 | 15 | 12 | 14 |
| | | | Slow | 15 | 18 | 15 | 16 |
| | | | QuietIO | 21 | 19 | 21 | 16 |
| | | 12 | Fast | 1 | 3 | 1 | 1 |
| | | | Slow | 2 | 7 | 2 | 4 |
| | | | QuietIO | 3 | 8 | 3 | 8 |
| | | 16 | Fast | 1 | 3 | 1 | 1 |
| | | | Slow | 3 | 7 | 3 | 3 |
| | | | QuietIO | 4 | 9 | 4 | 8 |
| | | 24 | Fast | N/A | 3 | N/A | 1 |
| | | | Slow | N/A | 5 | N/A | 2 |
| | | | QuietIO | N/A | 8 | N/A | 6 |
| | SSTL_2_I (3) | | | 10 | 11 | 10 | 11 |
| | SSTL_2_II (3) | | | N/A | 7 | N/A | 7 |
| | DIFF_SSTL_2_I (3) | | | 30 | 33 | 30 | 33 |
| | DIFF_SSTL_2_II (3) | | | N/A | 21 | N/A | 24 |

*Table 34:* **SSO Limit per $V_{CCO}$/GND Pair *(Cont'd)***

| $V_{CCO}$ | I/O Standard | Drive | Slew | SSO Limit per $V_{CCO}$/GND Pair | | | |
|---|---|---|---|---|---|---|---|
| | | | | All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324 | | All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324 | |
| | | | | Bank 0/2 | Bank 1/3 | Bank 0/2 | Bank 1/3/4/5 |
| 3.3V | LVCMOS33 | 2 | Fast | 42 | 46 | 42 | 44 |
| | | | Slow | 50 | 55 | 50 | 49 |
| | | | QuietIO | 60 | 68 | 60 | 60 |
| | | 4 | Fast | 21 | 27 | 21 | 25 |
| | | | Slow | 32 | 37 | 32 | 32 |
| | | | QuietIO | 39 | 42 | 39 | 37 |
| | | 6 | Fast | 14 | 19 | 14 | 17 |
| | | | Slow | 19 | 25 | 19 | 22 |
| | | | QuietIO | 29 | 30 | 29 | 25 |
| | | 8 | Fast | 11 | 15 | 11 | 14 |
| | | | Slow | 15 | 20 | 15 | 18 |
| | | | QuietIO | 25 | 24 | 25 | 20 |
| | | 12 | Fast | 1 | 3 | 1 | 1 |
| | | | Slow | 2 | 5 | 2 | 2 |
| | | | QuietIO | 4 | 9 | 4 | 7 |
| | | 16 | Fast | 1 | 2 | 1 | 1 |
| | | | Slow | 1 | 5 | 1 | 1 |
| | | | QuietIO | 3 | 10 | 3 | 8 |
| | | 24 | Fast | 1 | 2 | 1 | 1 |
| | | | Slow | 2 | 5 | 2 | 1 |
| | | | QuietIO | 7 | 9 | 7 | 7 |

## Input/Output Logic Switching Characteristics

*Table 35:* **ILOGIC2 Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| **Setup/Hold** | | | | | | |
| $T_{ICE0CK}/T_{ICKCE0}$ | CE0 pin Setup/Hold with respect to CLK | 0.56/ –0.30 | 0.56/ –0.25 | 0.79/ –0.22 | 1.21/ –0.52 | ns |
| $T_{ISRCK}/T_{ICKSR}$ | SR pin Setup/Hold with respect to CLK | 0.74/ –0.23 | 0.74/ –0.22 | 0.98/ –0.20 | 1.31/ –0.45 | ns |
| $T_{IDOCK}/T_{IOCKD}$ | D pin Setup/Hold with respect to CLK without Delay | 1.19/ –0.83 | 1.36/ –0.83 | 1.73/ –0.83 | 2.18/ –1.77 | ns |
| $T_{IDOCKD}/T_{IOCKDD}$ | DDLY pin Setup/Hold with respect to CLK (using IODELAY2) | 0.31/ 0.00 | 0.47/ 0.00 | 0.54/ 0.00 | 0.63/ –0.39 | ns |
| **Combinatorial** | | | | | | |
| $T_{IDI}$ | D pin to O pin propagation delay, no Delay | 0.95 | 1.28 | 1.53 | 2.25 | ns |
| $T_{IDID}$ | DDLY pin to O pin propagation delay (using IODELAY2) | 0.23 | 0.39 | 0.44 | 0.74 | ns |
| **Sequential Delays** | | | | | | |
| $T_{IDLO}$ | D pin to Q pin using flip-flop as a latch without Delay | 1.56 | 1.86 | 2.39 | 3.49 | ns |
| $T_{IDLOD}$ | DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY2) | 0.68 | 0.97 | 1.20 | 1.94 | ns |
| $T_{ICKQ}$ | CLK to Q outputs for XC devices | 1.03 | 1.24 | 1.43 | 2.11 | ns |
| | CLK to Q outputs for XA and XQ devices | 1.38 | N/A | 1.78 | 2.11 | ns |
| $T_{RQ\_ILOGIC2}$ | SR pin to Q outputs | 1.81 | 1.81 | 2.50 | 3.05 | ns |

*Table 36:* **OLOGIC2 Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| **Setup/Hold** | | | | | | |
| $T_{ODCK}/T_{OCKD}$ | D1/D2 pins Setup/Hold with respect to CLK | 0.81/ –0.05 | 0.86/ –0.05 | 1.18/ 0.00 | 1.73/ –0.27 | ns |
| $T_{OOCECK}/T_{OCKOCE}$ | OCE pin Setup/Hold with respect to CLK | 0.75/ –0.10 | 0.75/ –0.10 | 1.01/ –0.05 | 1.66/ –0.23 | ns |
| $T_{OSRCK}/T_{OCKSR}$ | SR pin Setup/Hold with respect to CLK | 0.70/ –0.28 | 0.79/ –0.28 | 1.03/ –0.23 | 1.39/ –0.47 | ns |
| $T_{OTCK}/T_{OCKT}$ | T1/T2 pins Setup/Hold with respect to CLK | 0.24/ –0.08 | 0.56/ –0.06 | 0.83/ –0.01 | 0.99/ –0.19 | ns |
| $T_{OTCECK}/T_{OCKTCE}$ | TCE pin Setup/Hold with respect to CLK | 0.58/ –0.06 | 0.72/ –0.06 | 1.18/ –0.01 | 1.51/ –0.13 | ns |
| **Sequential Delays** | | | | | | |
| $T_{OCKQ}$ | CLK to OQ/TQ out for XC devices | 0.48 | 0.51 | 0.74 | 0.74 | ns |
| | CLK to OQ/TQ out for XA and XQ devices | 0.85 | N/A | 1.16 | 0.74 | ns |
| $T_{RQ\_OLOGIC2}$ | SR pin to OQ/TQ out | 1.81 | 1.81 | 2.50 | 3.05 | ns |

*Table 47:* **Configuration Switching Characteristics[1] *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| **BPI Master Flash Mode Programming Switching[4]** | | | | | | |
| $T_{BPICCO}$[5] | A[25:0], FCS_B, FOE_B, FWE_B, LDC outputs valid after CCLK falling edge | 15 | 15 | 15 | 20 | ns, Max |
| $T_{BPIICCK}$ | Master BPI CCLK (output) delay | 10/100 | 10/100 | 10/100 | 10/130 | µs, Min/Max |
| $T_{BPIDCC}/T_{BPICCD}$ | Setup/Hold on D[15:0] data input pins | 5.0/1.0 | 5.0/1.0 | 5.0/1.0 | 6.0/2.0 | ns, Min |
| **SPI Master Flash Mode Programming Switching[6]** | | | | | | |
| $T_{SPIDCC}/T_{SPIDCCD}$ | DIN, MISO0, MISO1, MISO2, MISO3, Setup/Hold before/after the rising CCLK edge | 5.0/1.0 | 5.0/1.0 | 5.0/1.0 | 7.0/1.0 | ns, Min |
| $T_{SPIICCK}$ | Master SPI CCLK (output) delay | 0.4/7.0 | 0.4/7.0 | 0.4/7.0 | 0.4/10.0 | µs, Min/Max |
| $T_{SPICCM}$ | MOSI clock to out | 13 | 13 | 13 | 19 | ns, Max |
| $T_{SPICCFC}$ | CSO_B clock to out | 16 | 16 | 16 | 26 | ns, Max |
| **CCLK Output (Master Modes)** | | | | | | |
| $T_{MCCKL}$ | Master CCLK clock duty cycle Low | 40/60 | | | | %, Min/Max |
| $T_{MCCKH}$ | Master CCLK clock duty cycle High | 40/60 | | | | %, Min/Max |
| $F_{MCCK}$ | Maximum frequency, serial mode (Master Serial/SPI) All devices | 40 | 40 | 40 | 30 | MHz, Max |
| | Maximum frequency, parallel mode (Master SelectMAP/BPI) LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T | 40 | 40 | 40 | 25 | MHz, Max |
| | Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x8 mode, LX150, and LX150T | 40 | 40 | 40 | 20 | MHz, Max |
| | Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x16 mode | 35 | 35 | 35 | 20 | MHz, Max |
| $F_{MCCKTOL}$ | Frequency Tolerance, master mode | ±50 | ±50 | ±50 | ±50 | % |
| **CCLK Input (Slave Modes)** | | | | | | |
| $T_{SCCKL}$ | Slave CCLK clock minimum Low time | 5 | 5 | 5 | 8 | ns, Min |
| $T_{SCCKH}$ | Slave CCLK clock minimum High time | 5 | 5 | 5 | 8 | ns, Min |
| **USERCCLK Input** | | | | | | |
| $T_{USERCCLKL}$ | USERCCLK clock minimum Low time | 12 | 12 | 12 | 16 | ns, Min |
| $T_{USERCCLKH}$ | USERCCLK clock minimum High time | 12 | 12 | 12 | 16 | ns, Min |
| $F_{USERCCLK}$ | Maximum USERCCLK frequency | 40 | 40 | 40 | 30 | MHz, Max |

**Notes:**

1. Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
2. To support longer delays in configuration, use the design solutions described in UG380: *Spartan-6 FPGA Configuration User Guide*.
3. Table 6 specifies the power supply ramp time.
4. BPI mode is not supported in:
   - LX4, LX25, or LX25T devices
   - LX9 devices in the TQG144 package
   - LX9 or LX16 devices in the CPG196 package.
5. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
6. Defense-grade Spartan-6Q -2Q devices configure in single default SPI Master (x1) mode at $T_j$ = –55°C. During operation and when using all other configuration functions, the minimum operating temperature is –40°C.

## DCM Switching Characteristics

*Table 53:* **Operating Frequency Ranges and Conditions for the Delay-Locked Loop (DLL)[1]**

| Symbol | Description | Speed Grade | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| **Input Frequency Ranges** | | | | | | | | | | |
| CLKIN_FREQ_DLL | Frequency of the CLKIN clock input when the CLKDV output is not used. | 5[2] | 280[3] | 5[2] | 280[3] | 5[2] | 250[3] | 5[2] | 175[3] | MHz |
| | Frequency of the CLKIN clock input when using the CLKDV output. | 5[2] | 280[3] | 5[2] | 280[3] | 5[2] | 250[3] | 5[2] | 133[3] | MHz |
| **Input Pulse Requirements** | | | | | | | | | | |
| CLKIN_PULSE | CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL < 150 MHz | 40 | 60 | 40 | 60 | 40 | 60 | 40 | 60 | % |
| | CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL > 150 MHz | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |
| **Input Clock Jitter Tolerance and Delay Path Variation[4]** | | | | | | | | | | |
| CLKIN_CYC_JITT_DLL_LF | Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL < 150 MHz | – | ±300 | – | ±300 | – | ±300 | – | ±300 | ps |
| CLKIN_CYC_JITT_DLL_HF | Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL > 150 MHz. | – | ±150 | – | ±150 | – | ±150 | – | ±150 | ps |
| CLKIN_PER_JITT_DLL | Period jitter at the CLKIN input. | – | ±1 | – | ±1 | – | ±1 | – | ±1 | ns |
| CLKFB_DELAY_VAR_EXT | Allowable variation of the off-chip feedback delay from the DCM output to the CLKFB input. | – | ±1 | – | ±1 | – | ±1 | – | ±1 | ns |

**Notes:**
1. DLL specifications apply when using any of the DLL outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV.
2. When operating independently of the DLL, the DFS supports lower CLKIN_FREQ_DLL frequencies. See Table 55.
3. The CLKIN_DIVIDE_BY_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the $F_{MAX}$ (see Table 48 and Table 49 for BUFG and BUFIO2 limits). When used with CLK_FEEDBACK=2X, the input clock frequency matches the frequency for CLK2X, and is limited to CLKOUT_FREQ_2X.
4. CLKIN_FREQ_DLL input jitter beyond these limits can cause the DCM to lose LOCK, indicated by the LOCKED output deasserting. The user must then reset the DCM.
5. When using both DCMs in a CMT, both DCMs must be LOCKED.

*Table 56:* **Switching Characteristics for the Digital Frequency Synthesizer (DFS) for DCM_SP[1]**

| Symbol | Description | Speed Grade | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| **Output Frequency Ranges** | | | | | | | | | | |
| CLKOUT_FREQ_FX | Frequency for the CLKFX and CLKFX180 outputs | 5 | 375 | 5 | 375 | 5 | 333 | 5 | 200 | MHz |
| **Output Clock Jitter[2][3]** | | | | | | | | | | |
| CLKOUT_PER_JITT_FX | Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN < 20 MHz | Use the Clocking Wizard | | | | | | | | ps |
| | Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN > 20 MHz | Typical = ±(1% of CLKFX period + 100) | | | | | | | | ps |
| **Duty Cycle[4][5]** | | | | | | | | | | |
| CLKOUT_DUTY_CYCLE_FX | Duty cycle precision for the CLKFX and CLKFX180 outputs including the BUFGMUX and clock tree duty-cycle distortion | Maximum = ±(1% of CLKFX period + 350) | | | | | | | | ps |
| **Phase Alignment[5]** | | | | | | | | | | |
| CLKOUT_PHASE_FX | Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used | – | ±200 | – | ±200 | – | ±200 | – | ±250 | ps |
| CLKOUT_PHASE_FX180 | Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used | Maximum = ±(1% of CLKFX period + 200) | | | | | | | | ps |
| **LOCKED Time** | | | | | | | | | | |
| LOCK_FX[2] | When FCLKIN < 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time. | – | 5 | – | 5 | – | 5 | – | 5 | ms |
| | When FCLKIN > 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time. | – | 0.45 | – | 0.45 | – | 0.45 | – | 0.60 | ms |

**Notes:**
1. The values in this table are based on the operating conditions described in Table 2 and Table 55.
2. For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
3. Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
5. Some duty cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.

## Spartan-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 63 through Table 69. Values are expressed in nanoseconds unless otherwise noted.

*Table 63:* **Global Clock Input to Output Delay Without DCM or PLL**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* DCM or PLL | | | | | | | |
| $T_{ICKOF}$ | Global Clock and OUTFF *without* DCM or PLL | XC6SLX4 | 6.12 | N/A | 7.68 | 9.41 | ns |
| | | XC6SLX9 | 6.12 | 6.51 | 7.68 | 9.41 | ns |
| | | XC6SLX16 | 5.98 | 6.42 | 7.48 | 9.10 | ns |
| | | XC6SLX25 | 6.20 | 6.69 | 7.84 | 9.44 | ns |
| | | XC6SLX25T | 6.20 | 6.69 | 7.84 | N/A | ns |
| | | XC6SLX45 | 6.37 | 6.88 | 8.10 | 9.61 | ns |
| | | XC6SLX45T | 6.37 | 6.88 | 8.10 | N/A | ns |
| | | XC6SLX75 | 6.39 | 6.99 | 8.16 | 10.18 | ns |
| | | XC6SLX75T | 6.39 | 6.99 | 8.16 | N/A | ns |
| | | XC6SLX100 | 6.59 | 7.18 | 8.41 | 10.31 | ns |
| | | XC6SLX100T | 6.59 | 7.18 | 8.41 | N/A | ns |
| | | XC6SLX150 | 6.98 | 7.68 | 8.80 | 10.62 | ns |
| | | XC6SLX150T | 6.98 | 7.68 | 8.80 | N/A | ns |
| | | XA6SLX4 | 6.44 | N/A | 7.68 | N/A | ns |
| | | XA6SLX9 | 6.44 | N/A | 7.68 | N/A | ns |
| | | XA6SLX16 | 6.30 | N/A | 7.48 | N/A | ns |
| | | XA6SLX25 | 6.52 | N/A | 7.84 | N/A | ns |
| | | XA6SLX25T | 6.52 | N/A | 7.84 | N/A | ns |
| | | XA6SLX45 | 6.69 | N/A | 8.12 | N/A | ns |
| | | XA6SLX45T | 6.69 | N/A | 8.12 | N/A | ns |
| | | XA6SLX75 | 6.89 | N/A | 8.16 | N/A | ns |
| | | XA6SLX75T | 6.89 | N/A | 8.16 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 8.36 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 8.16 | 10.18 | ns |
| | | XQ6SLX75T | 6.89 | N/A | 8.16 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | 8.80 | 10.62 | ns |
| | | XQ6SLX150T | 7.61 | N/A | 8.80 | N/A | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

*Table 74:* **Global Clock Setup and Hold With PLL in System-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)** | | | | | | | |
| $T_{PSPLL}$/ $T_{PHPLL}$ | No Delay Global Clock and IFF(2) with PLL in System-Synchronous Mode | XC6SLX4 | 1.37/0.25 | N/A | 1.52/0.41 | 2.07/0.69 | ns |
| | | XC6SLX9 | 1.37/0.21 | 1.48/0.21 | 1.52/0.26 | 2.07/0.69 | ns |
| | | XC6SLX16 | 1.33/–0.03 | 1.53/–0.02 | 1.60/–0.02 | 1.57/0.48 | ns |
| | | XC6SLX25 | 1.65/0.28 | 1.71/0.28 | 1.91/0.28 | 2.44/0.76 | ns |
| | | XC6SLX25T | 1.65/0.28 | 1.71/0.28 | 1.91/0.28 | N/A | ns |
| | | XC6SLX45 | 1.55/0.18 | 1.64/0.18 | 1.75/0.18 | 2.02/0.90 | ns |
| | | XC6SLX45T | 1.55/0.18 | 1.64/0.18 | 1.75/0.18 | N/A | ns |
| | | XC6SLX75 | 1.77/0.21 | 1.89/0.21 | 2.13/0.21 | 2.46/0.53 | ns |
| | | XC6SLX75T | 1.77/0.21 | 1.89/0.21 | 2.13/0.21 | N/A | ns |
| | | XC6SLX100 | 1.44/0.32 | 1.52/0.32 | 1.70/0.32 | 1.78/0.86 | ns |
| | | XC6SLX100T | 1.44/0.32 | 1.52/0.32 | 1.70/0.32 | N/A | ns |
| | | XC6SLX150 | 1.39/0.49 | 1.48/0.49 | 1.67/0.49 | 1.94/0.94 | ns |
| | | XC6SLX150T | 1.39/0.49 | 1.48/0.49 | 1.67/0.49 | N/A | ns |
| | | XA6SLX4 | 1.61/0.10 | N/A | 1.64/0.28 | N/A | ns |
| | | XA6SLX9 | 1.61/0.10 | N/A | 1.64/0.28 | N/A | ns |
| | | XA6SLX16 | 1.89/–0.08 | N/A | 1.72/–0.08 | N/A | ns |
| | | XA6SLX25 | 1.85/0.16 | N/A | 2.08/0.16 | N/A | ns |
| | | XA6SLX25T | 1.85/0.16 | N/A | 2.17/0.16 | N/A | ns |
| | | XA6SLX45 | 1.58/0.07 | N/A | 1.87/0.03 | N/A | ns |
| | | XA6SLX45T | 1.58/0.07 | N/A | 1.87/0.03 | N/A | ns |
| | | XA6SLX75 | 1.80/0.06 | N/A | 2.25/0.06 | N/A | ns |
| | | XA6SLX75T | 1.80/0.06 | N/A | 2.25/0.06 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 2.34/0.14 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 2.25/0.06 | 2.46/0.53 | ns |
| | | XQ6SLX75T | 1.80/0.06 | N/A | 2.25/0.06 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | 1.79/0.37 | 1.94/0.94 | ns |
| | | XQ6SLX150T | 1.43/0.37 | N/A | 1.79/0.37 | N/A | ns |

**Notes:**
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

| Date | Version | Description of Revisions |
|---|---|---|
| 06/14/10 | 1.5 | In Table 2, added note 5 and added temperature range to $V_{FS}$ and $R_{FUSE}$. Removed speed grade delineation, revised $I_{RPD}$ description, and updated note 2 in Table 4. Added note 2 to Table 7. Added DIFF_MOBILE_DDR to Table 8 and Table 10. Added note 4 to Table 15. Changed minimum $DV_{PPIN}$ in Table 16. Updated $F_{GTPDRPCLK}$ in Table 19. Increased maximum $T_{LLSKEW}$ in Table 22. Updated descriptions and added data to Table 23. Removed note 1 and added new data to the Networking Applications section in Table 25. Updated Table 26 and Table 27 to the data in ISE v12.1 software with speed specification v1.08. In Table 28, added DIFF_MOBILE_DDR and updated -4 speed grade data. Updated the maximum I/O pairs per bank in Table 33. Updated note 2 on Table 39. Revised the $F_{MAX}$ in Table 44. In Table 47, updated description for $T_{SMCKCSO}$, revised values for $T_{POR}$ and added Min value, added $T_{BPIICCK}$ and $T_{SPIICCK}$. Also in Table 47, added device dependencies to $F_{SMCCK}$ and $F_{RBCCK}$. Updated and added data to Table 63 through Table 78, and Table 81. In Table 79, added data on the XC6SLX45-FG(G)676 and revised the XC6SLX45T and XC6SLX150T values.<br><br>The following changes to this specification are addressed in the product change notice XCN10024, *MCB Performance and JTAG Revision Code for Spartan-6 LX16 and LX45 FPGAs*.<br>In Table 2, revised the $V_{CCINT}$ to add the memory controller block extended performance specifications. In Table 25, changed the standard specifications and added extended performance specifications for the memory controller block and note 2. Added note 4 and updated values in Table 34. |
| 06/24/10 | 1.6 | Production release of XC6SLX45T (-2 and -3 speed grades), XC6SLX16 and XC6SLX45 (-3 speed grade) devices which includes changes to Table 26 and Table 27 (ISE v12.1 software with speed specification v1.08).<br>Added the -3N speed grade, which designates Spartan-6 devices that do not support MCB functionality. This includes changes to Table 2 (note 2), Table 25 (note 4), and Switching Characteristics (Table 26).<br>Updated Simultaneously Switching Outputs discussion. Added -3 speed grade values for $T_{TAP}$ and $F_{MINCAL}$ values in Table 39. In Table 40, updated $T_{RPW}$ (-2 and -3 speed grade) values and $F_{TOG}$ (-3 speed grade) values. In Table 48, updated $T_{GIO}$ (-2 and -3 speed grade) values. Updated -3 values in spread spectrum section of Table 57. |
| 07/16/10 | 1.7 | Production release of specific devices listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 4 advising designers of the patch which contains v1.11. Also updated the -1L speed specification to v1.04. Updated numerous -4 and -1L values. Added -4 $T_{TAP}$ values and $F_{MINCAL}$ to Table 39. Revised $T_{CINCK}$/$T_{CKCIN}$ in Table 40. In Table 41, revised $T_{SHCKO}$. In Table 42, revised $T_{REG}$. Added new -1L values to Table 47. Added and updated values in Table 79. |
| 07/26/10 | 1.8 | Production release of XC6SLX25, XC6SLX25T, XC6SLX100 and XC6SLX100T in the specific speed grades listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 7 to Table 2 and moved $V_{FS}$ and $R_{FUSE}$ to a new Table 3. Added $I_{HS}$ and note 4 to Table 4. Added note 1 to Table 28. Added and updated SSO limits per $V_{CCO}$/GND pairs in Table 34. Added note 3 to Table 47. In Table 54, removed -1L specifications for CLKOUT_PER_JITT_DV1/2 and revised CLKIN_CLKFB_PHASE and CLKOUT_PHASE_DLL values. Updated note 3 in both Table 56 and Table 57. |
| 08/23/10 | 1.9 | Updated values for $F_{GTPRANGE1}$, $F_{GTPRANGE2}$, and $F_{GPLLMIN}$ in Table 18. Revised -3 and -4 values in Table 21. Removed the -1L speed grade readback support restriction and note 3 in Table 47. |
| 11/05/10 | 1.10 | Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.3 software with speed specification v1.12 for the -2 speed grade available in the 12.3 *Speed Files Patch*. Added note 3 advising designers of the patch which contains v1.12.<br>In Table 2, added note 4. In Table 4, added note 2. In Table 10, added notes 2 and 3. In Table 44, added note 2. In Table 47, updated symbol for $T_{SMWCCK}$/$T_{SMCCKW}$, changed -1L values for $T_{USERCCLKH}$ and $T_{USERCCLKL}$ , and added and revised the modes for $F_{MCCK}$ and $F_{SMCCK}$. In Table 53, redefined and expanded description for CLKIN_FREQ_DLL and rewrote note 3. Updated title of Table 58. Also in Table 78, revised $T_{DCD\_CLK}$ for XC6SLX150 and XC6SLX150T. Changed description of $T_{PSFD}$/ $T_{PHFD}$ in Table 71.<br>For the -1L speed grade, updated data sheet to ISE 12.3 software with speed specification v1.05 which revised the values in the following tables: Table 25, Table 28, Table 35, Table 36, Table 37, Table 40 through Table 43, Table 48 through Table 56, Table 62 through Table 78, Table 80, and Table 81.<br>Updated Notice of Disclaimer. |

## Notice of Disclaimer