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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1139
Number of Logic Elements/Cells	14579
Total RAM Bits	589824
Number of I/O	232
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	324-LFBGA, CSPBGA
Supplier Device Package	324-CSPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx16-3csg324i

Table 4: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.8	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin for commercial (C) and industrial (I) devices	–10	–	10	μ A
	V_{REF} leakage current per pin for expanded (Q) devices	–15	–	15	μ A
I_L	Input or output leakage current per pin (sample-tested) for commercial (C) and industrial (I) devices	–10	–	10	μ A
	Input or output leakage current per pin (sample-tested) for expanded (Q) devices	–15	–	15	μ A
I_{HS}	Leakage current on pins during hot socketing with FPGA unpowered	–20	–	20	μ A
	All pins except PROGRAM_B, DONE, and JTAG pins when HSWAPEN = 1				
	PROGRAM_B, DONE, and JTAG pins, or other pins when HSWAPEN = 0	$I_{HS} + I_{RPU}$			μ A
$C_{IN}^{(1)}$	Die input capacitance at the pad	–	–	10	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 3.3V$ or $V_{CCAUX} = 3.3V$	200	–	500	μ A
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 2.5V$ or $V_{CCAUX} = 2.5V$	120	–	350	μ A
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.8V$	60	–	200	μ A
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.5V$	40	–	150	μ A
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.2V$	12	–	100	μ A
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = V_{CCO}$, $V_{CCAUX} = 3.3V$	200	–	550	μ A
	Pad pull-down (when selected) @ $V_{IN} = V_{CCO}$, $V_{CCAUX} = 2.5V$	140	–	400	μ A
$I_{BATT}^{(2)}$	Battery supply current	–	–	150	nA
$R_{DT}^{(3)}$	Resistance of optional input differential termination circuit, $V_{CCAUX} = 3.3V$	–	100	–	Ω
$R_{IN_TERM}^{(5)}$	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for commercial (C) and industrial (I) devices	23	25	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for expanded (Q) devices	20	25	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for commercial (C) and industrial (I) devices	39	50	72	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for expanded (Q) devices	32	50	74	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for commercial (C) and industrial (I) devices	56	75	109	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for expanded (Q) devices	47	75	115	Ω
R_{OUT_TERM}	Thevenin equivalent resistance of programmable output termination (UNTUNED_25)	11	25	52	Ω
	Thevenin equivalent resistance of programmable output termination (UNTUNED_50)	21	50	96	Ω
	Thevenin equivalent resistance of programmable output termination (UNTUNED_75)	29	75	145	Ω

Notes:

1. The C_{IN} measurement represents the die capacitance at the pad, not including the package.
2. Maximum value specified for worst case process at 25°C. LX75, LX75T, LX100, LX100T, LX150, and LX150T only.
3. Refer to IBIS models for R_{DT} variation and for values at $V_{CCAUX} = 2.5V$. IBIS values for R_{DT} are valid for all temperature ranges.
4. V_{CCO2} is not required for data retention. The minimum V_{CCO2} for power-on reset and configuration is 1.65V.
5. Termination resistance to a $V_{CCO}/2$ level.

Table 17: GTP Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	200	800	2000	mV
R_{IN}	Differential input resistance	80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult [UG386](#): *Spartan-6 FPGA GTP Transceivers User Guide* for further information.

Table 18: GTP Transceiver Performance

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
F_{GTPMAX}	Maximum GTP transceiver data rate	3.2	3.2	2.7	N/A	Gb/s
$F_{GTPRANGE1}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 1	1.88 to 3.2	1.88 to 3.2	1.88 to 2.7	N/A	Gb/s
$F_{GTPRANGE2}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 2	0.94 to 1.62	0.94 to 1.62	0.94 to 1.62	N/A	Gb/s
$F_{GTPRANGE3}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 4	0.6 to 0.81	0.6 to 0.81	0.6 to 0.81	N/A	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	1.62	1.62	1.62	N/A	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	0.94	0.94	0.94	N/A	GHz

Table 19: GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
$F_{GTPDRPCLK}$	GTP transceiver DCLK (DRP clock) maximum frequency	125	125	100	N/A	MHz

Table 20: GTP Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All LXT Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	160	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	μ s

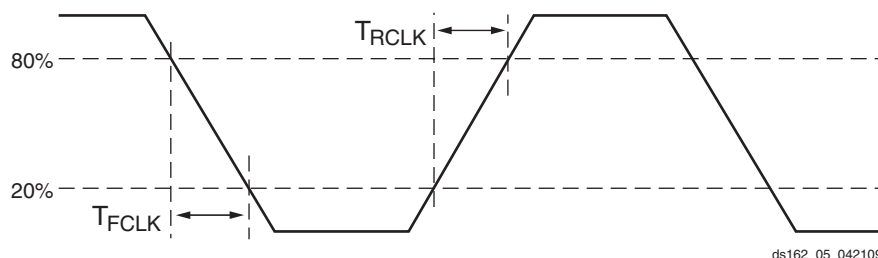


Figure 3: Reference Clock Timing Parameters

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVTTTL, QUIETIO, 2 mA	1.35	1.47	1.60	1.82	5.39	5.53	5.73	6.37	5.39	5.53	5.73	6.37	ns
LVTTTL, QUIETIO, 4 mA	1.35	1.47	1.60	1.82	4.29	4.43	4.63	5.22	4.29	4.43	4.63	5.22	ns
LVTTTL, QUIETIO, 6 mA	1.35	1.47	1.60	1.82	3.75	3.89	4.09	4.69	3.75	3.89	4.09	4.69	ns
LVTTTL, QUIETIO, 8 mA	1.35	1.47	1.60	1.82	3.23	3.37	3.57	4.20	3.23	3.37	3.57	4.20	ns
LVTTTL, QUIETIO, 12 mA	1.35	1.47	1.60	1.82	3.28	3.42	3.62	4.22	3.28	3.42	3.62	4.22	ns
LVTTTL, QUIETIO, 16 mA	1.35	1.47	1.60	1.82	2.94	3.08	3.28	3.92	2.94	3.08	3.28	3.92	ns
LVTTTL, QUIETIO, 24 mA	1.35	1.47	1.60	1.82	2.69	2.83	3.03	3.67	2.69	2.83	3.03	3.67	ns
LVTTTL, Slow, 2 mA	1.35	1.47	1.60	1.82	4.36	4.50	4.70	5.30	4.36	4.50	4.70	5.30	ns
LVTTTL, Slow, 4 mA	1.35	1.47	1.60	1.82	3.17	3.31	3.51	4.16	3.17	3.31	3.51	4.16	ns
LVTTTL, Slow, 6 mA	1.35	1.47	1.60	1.82	2.76	2.90	3.10	3.75	2.76	2.90	3.10	3.75	ns
LVTTTL, Slow, 8 mA	1.35	1.47	1.60	1.82	2.59	2.73	2.93	3.55	2.59	2.73	2.93	3.55	ns
LVTTTL, Slow, 12 mA	1.35	1.47	1.60	1.82	2.58	2.72	2.92	3.54	2.58	2.72	2.92	3.54	ns
LVTTTL, Slow, 16 mA	1.35	1.47	1.60	1.82	2.39	2.53	2.73	3.40	2.39	2.53	2.73	3.40	ns
LVTTTL, Slow, 24 mA	1.35	1.47	1.60	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVTTTL, Fast, 2 mA	1.35	1.47	1.60	1.82	3.78	3.92	4.12	4.74	3.78	3.92	4.12	4.74	ns
LVTTTL, Fast, 4 mA	1.35	1.47	1.60	1.82	2.49	2.63	2.83	3.45	2.49	2.63	2.83	3.45	ns
LVTTTL, Fast, 6 mA	1.35	1.47	1.60	1.82	2.44	2.58	2.78	3.40	2.44	2.58	2.78	3.40	ns
LVTTTL, Fast, 8 mA	1.35	1.47	1.60	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns
LVTTTL, Fast, 12 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTTL, Fast, 16 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTTL, Fast, 24 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVC MOS33, QUIETIO, 2 mA	1.34	1.46	1.59	1.82	5.40	5.54	5.74	6.37	5.40	5.54	5.74	6.37	ns
LVC MOS33, QUIETIO, 4 mA	1.34	1.46	1.59	1.82	4.03	4.17	4.37	5.01	4.03	4.17	4.37	5.01	ns
LVC MOS33, QUIETIO, 6 mA	1.34	1.46	1.59	1.82	3.51	3.65	3.85	4.47	3.51	3.65	3.85	4.47	ns
LVC MOS33, QUIETIO, 8 mA	1.34	1.46	1.59	1.82	3.37	3.51	3.71	4.33	3.37	3.51	3.71	4.33	ns
LVC MOS33, QUIETIO, 12 mA	1.34	1.46	1.59	1.82	2.94	3.08	3.28	3.93	2.94	3.08	3.28	3.93	ns
LVC MOS33, QUIETIO, 16 mA	1.34	1.46	1.59	1.82	2.77	2.91	3.11	3.78	2.77	2.91	3.11	3.78	ns
LVC MOS33, QUIETIO, 24 mA	1.34	1.46	1.59	1.82	2.59	2.73	2.93	3.58	2.59	2.73	2.93	3.58	ns
LVC MOS33, Slow, 2 mA	1.34	1.46	1.59	1.82	4.37	4.51	4.71	5.28	4.37	4.51	4.71	5.28	ns
LVC MOS33, Slow, 4 mA	1.34	1.46	1.59	1.82	2.98	3.12	3.32	3.94	2.98	3.12	3.32	3.94	ns
LVC MOS33, Slow, 6 mA	1.34	1.46	1.59	1.82	2.58	2.72	2.92	3.61	2.58	2.72	2.92	3.61	ns
LVC MOS33, Slow, 8 mA	1.34	1.46	1.59	1.82	2.65	2.79	2.99	3.61	2.65	2.79	2.99	3.61	ns
LVC MOS33, Slow, 12 mA	1.34	1.46	1.59	1.82	2.39	2.53	2.73	3.31	2.39	2.53	2.73	3.31	ns
LVC MOS33, Slow, 16 mA	1.34	1.46	1.59	1.82	2.31	2.45	2.65	3.27	2.31	2.45	2.65	3.27	ns
LVC MOS33, Slow, 24 mA	1.34	1.46	1.59	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVC MOS33, Fast, 2 mA	1.34	1.46	1.59	1.82	3.76	3.90	4.10	4.70	3.76	3.90	4.10	4.70	ns
LVC MOS33, Fast, 4 mA	1.34	1.46	1.59	1.82	2.48	2.62	2.82	3.44	2.48	2.62	2.82	3.44	ns
LVC MOS33, Fast, 6 mA	1.34	1.46	1.59	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS33, Slow, 6 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVC MOS33, Slow, 8 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVC MOS33, Slow, 12 mA	1.41	1.59	2.53	2.73	2.53	2.73	ns
LVC MOS33, Slow, 16 mA	1.41	1.59	2.45	2.65	2.45	2.65	ns
LVC MOS33, Slow, 24 mA	1.41	1.59	2.42	2.62	2.42	2.62	ns
LVC MOS33, Fast, 2 mA	1.41	1.59	4.05	4.25	4.05	4.25	ns
LVC MOS33, Fast, 4 mA	1.41	1.59	2.66	2.86	2.66	2.86	ns
LVC MOS33, Fast, 6 mA	1.41	1.59	2.46	2.66	2.46	2.66	ns
LVC MOS33, Fast, 8 mA	1.41	1.59	2.21	2.41	2.21	2.41	ns
LVC MOS33, Fast, 12 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVC MOS33, Fast, 16 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVC MOS33, Fast, 24 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVC MOS25, QUIETIO, 2 mA	0.89	1.07	5.00	5.20	5.00	5.20	ns
LVC MOS25, QUIETIO, 4 mA	0.89	1.07	3.85	4.05	3.85	4.05	ns
LVC MOS25, QUIETIO, 6 mA	0.89	1.07	3.60	3.80	3.60	3.80	ns
LVC MOS25, QUIETIO, 8 mA	0.89	1.07	3.34	3.54	3.34	3.54	ns
LVC MOS25, QUIETIO, 12 mA	0.89	1.07	2.98	3.18	2.98	3.18	ns
LVC MOS25, QUIETIO, 16 mA	0.89	1.07	2.79	2.99	2.79	2.99	ns
LVC MOS25, QUIETIO, 24 mA	0.89	1.07	2.64	2.84	2.64	2.84	ns
LVC MOS25, Slow, 2 mA	0.89	1.07	3.96	4.16	3.96	4.16	ns
LVC MOS25, Slow, 4 mA	0.89	1.07	2.96	3.16	2.96	3.16	ns
LVC MOS25, Slow, 6 mA	0.89	1.07	2.88	3.08	2.88	3.08	ns
LVC MOS25, Slow, 8 mA	0.89	1.07	2.63	2.83	2.63	2.83	ns
LVC MOS25, Slow, 12 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVC MOS25, Slow, 16 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVC MOS25, Slow, 24 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVC MOS25, Fast, 2 mA	0.89	1.07	3.52	3.72	3.52	3.72	ns
LVC MOS25, Fast, 4 mA	0.89	1.07	2.43	2.63	2.43	2.63	ns
LVC MOS25, Fast, 6 mA	0.89	1.07	2.23	2.43	2.23	2.43	ns
LVC MOS25, Fast, 8 mA	0.89	1.07	2.16	2.36	2.16	2.36	ns
LVC MOS25, Fast, 12 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVC MOS25, Fast, 16 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVC MOS25, Fast, 24 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVC MOS18, QUIETIO, 2 mA	1.25	1.43	6.11	6.31	6.11	6.31	ns
LVC MOS18, QUIETIO, 4 mA	1.25	1.43	4.88	5.08	4.88	5.08	ns
LVC MOS18, QUIETIO, 6 mA	1.25	1.43	4.20	4.40	4.20	4.40	ns
LVC MOS18, QUIETIO, 8 mA	1.25	1.43	3.86	4.06	3.86	4.06	ns
LVC MOS18, QUIETIO, 12 mA	1.25	1.43	3.49	3.69	3.49	3.69	ns

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS15, QUIETIO, 2 mA	1.05	1.23	5.63	5.83	5.63	5.83	ns
LVC MOS15, QUIETIO, 4 mA	1.05	1.23	4.75	4.95	4.75	4.95	ns
LVC MOS15, QUIETIO, 6 mA	1.05	1.23	4.21	4.41	4.21	4.41	ns
LVC MOS15, QUIETIO, 8 mA	1.05	1.23	4.05	4.25	4.05	4.25	ns
LVC MOS15, QUIETIO, 12 mA	1.05	1.23	3.74	3.94	3.74	3.94	ns
LVC MOS15, QUIETIO, 16 mA	1.05	1.23	3.52	3.72	3.52	3.72	ns
LVC MOS15, Slow, 2 mA	1.05	1.23	4.32	4.52	4.32	4.52	ns
LVC MOS15, Slow, 4 mA	1.05	1.23	3.58	3.78	3.58	3.78	ns
LVC MOS15, Slow, 6 mA	1.05	1.23	2.45	2.65	2.45	2.65	ns
LVC MOS15, Slow, 8 mA	1.05	1.23	2.46	2.66	2.46	2.66	ns
LVC MOS15, Slow, 12 mA	1.05	1.23	2.17	2.37	2.17	2.37	ns
LVC MOS15, Slow, 16 mA	1.05	1.23	2.15	2.35	2.15	2.35	ns
LVC MOS15, Fast, 2 mA	1.05	1.23	3.43	3.63	3.43	3.63	ns
LVC MOS15, Fast, 4 mA	1.05	1.23	2.42	2.62	2.42	2.62	ns
LVC MOS15, Fast, 6 mA	1.05	1.23	1.92	2.12	1.92	2.12	ns
LVC MOS15, Fast, 8 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVC MOS15, Fast, 12 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVC MOS15, Fast, 16 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVC MOS15_JEDEC, QUIETIO, 2 mA	1.10	1.28	5.64	5.84	5.64	5.84	ns
LVC MOS15_JEDEC, QUIETIO, 4 mA	1.10	1.28	4.75	4.95	4.75	4.95	ns
LVC MOS15_JEDEC, QUIETIO, 6 mA	1.10	1.28	4.21	4.41	4.21	4.41	ns
LVC MOS15_JEDEC, QUIETIO, 8 mA	1.10	1.28	4.06	4.26	4.06	4.26	ns
LVC MOS15_JEDEC, QUIETIO, 12 mA	1.10	1.28	3.75	3.95	3.75	3.95	ns
LVC MOS15_JEDEC, QUIETIO, 16 mA	1.10	1.28	3.53	3.73	3.53	3.73	ns
LVC MOS15_JEDEC, Slow, 2 mA	1.10	1.28	4.32	4.52	4.32	4.52	ns
LVC MOS15_JEDEC, Slow, 4 mA	1.10	1.28	3.56	3.76	3.56	3.76	ns
LVC MOS15_JEDEC, Slow, 6 mA	1.10	1.28	2.44	2.64	2.44	2.64	ns
LVC MOS15_JEDEC, Slow, 8 mA	1.10	1.28	2.47	2.67	2.47	2.67	ns
LVC MOS15_JEDEC, Slow, 12 mA	1.10	1.28	2.15	2.35	2.15	2.35	ns
LVC MOS15_JEDEC, Slow, 16 mA	1.10	1.28	2.15	2.35	2.15	2.35	ns
LVC MOS15_JEDEC, Fast, 2 mA	1.10	1.28	3.43	3.63	3.43	3.63	ns
LVC MOS15_JEDEC, Fast, 4 mA	1.10	1.28	2.42	2.62	2.42	2.62	ns
LVC MOS15_JEDEC, Fast, 6 mA	1.10	1.28	1.92	2.12	1.92	2.12	ns
LVC MOS15_JEDEC, Fast, 8 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVC MOS15_JEDEC, Fast, 12 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVC MOS15_JEDEC, Fast, 16 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVC MOS12, QUIETIO, 2 mA	0.98	1.16	6.54	6.74	6.54	6.74	ns
LVC MOS12, QUIETIO, 4 mA	0.98	1.16	5.12	5.32	5.12	5.32	ns

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

V _{CCO}	I/O Standard	Drive	Slew	SSO Limit per V _{CCO} /GND Pair					
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324			
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5		
1.8V	LVCMOS18, LVCMOS18_JEDEC	2	Fast	39	46	39	47		
			Slow	65	75	65	74		
			QuietIO	80	80	80	85		
		4	Fast	22	25	22	25		
			Slow	38	36	38	29		
			QuietIO	45	40	45	35		
		6	Fast	16	18	16	17		
			Slow	27	25	27	19		
			QuietIO	30	28	30	23		
		8	Fast	13	15	13	14		
			Slow	16	18	16	16		
			QuietIO	25	22	25	18		
		12	Fast	5	7	5	5		
			Slow	7	8	7	6		
			QuietIO	11	10	11	8		
		16	Fast	4	5	4	4		
			Slow	7	8	7	5		
			QuietIO	11	10	11	8		
		24	Fast	N/A	5	N/A	3		
			Slow	N/A	8	N/A	8		
			QuietIO	N/A	10	N/A	8		
		HSTL_I_18				9	10	9	9
		HSTL_II_18				N/A	5	N/A	6
		HSTL_III_18				9	10	9	11
		DIFF_HSTL_I_18				27	30	27	27
		DIFF_HSTL_II_18				N/A	15	N/A	18
		DIFF_HSTL_III_18				27	30	27	33
MOBILE_DDR ⁽³⁾				12	14	12	14		
DIFF_MOBILE_DDR ⁽³⁾				36	42	36	42		
SSTL_18_I ⁽³⁾				9	10	9	10		
SSTL_18_II ⁽³⁾				N/A	5	N/A	4		
DIFF_SSTL_18_I ⁽³⁾				27	30	27	30		
DIFF_SSTL_18_II ⁽³⁾				N/A	15	N/A	12		

Configuration Switching Characteristics

Table 47: Configuration Switching Characteristics⁽¹⁾

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Power-up Timing Characteristics						
T _{PL} ⁽²⁾	PROGRAM_B Latency	4	4	4	5	ms, Max
T _{POR} ⁽²⁾	Power-on reset (50 ms ramp time) ⁽³⁾	5/30	5/34	5/40	5/40	ms, Min/Max
	Power-on reset (10 ms ramp time)	5/25	5/29	5/35	5/40	ms, Min/Max
T _{PROGRAM}	PROGRAM_B Pulse Width	500	500	500	500	ns, Min
Slave Serial Mode Programming Switching						
T _{DCCK} /T _{CCKD}	DIN Setup/Hold, slave mode	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T _{CCO}	CCLK to DOUT	12	12	12	17	ns, Max
F _{SCCK}	Slave mode external CCLK	80	80	80	50	MHz, Max
Slave SelectMAP Mode Programming Switching						
T _{SMDCCK} /T _{SMCCKD}	SelectMAP Data Setup/Hold	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T _{SMCSCCK} /T _{SMCCKCS}	CSI_B Setup/Hold	7.0/0.0	7.0/0.0	7.0/0.0	9.0/2.0	ns, Min
T _{SMWCCK} /T _{SMCCKW}	RDWR_B Setup/Hold	17.0/1.0	17.0/1.0	17.0/1.0	27.0/2.0	ns, Min
T _{SMCKCSO}	CSO_B clock to out	16	16	16	26	ns, Max
T _{SMCO}	CCLK to DATA out in readback	13	13	13	25	ns, Max
T _{SMCKBY}	CCLK to BUSY out in readback	12	12	12	17	ns, Max
F _{SMCCK}	Maximum CCLK frequency (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	25	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x8 mode, LX150, and LX150T only)	40	40	40	20	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x16 mode only)	35	35	35	20	MHz, Max
F _{RBCK}	Maximum Readback CCLK frequency, including block RAM (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	20	20	20	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	30	MHz, Max
	Maximum Readback CCLK frequency, including block RAM (LX100, LX100T, LX150, and LX150T only)	12	12	12	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX100, LX100T, LX150, and LX150T only)	35	35	35	20	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK}	TMS and TDI Setup time before TCK	10	10	10	17	ns, Min
T _{TCKTAP}	TMS and TDI Hold time after TCK	5.5	5.5	5.5	5.5	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output valid	6.5	6.5	6.5	8	ns, Max
T _{TCKH}	TCK clock minimum High time	12	12	12	21	ns, Min
T _{TCKL}	TCK clock minimum Low time	12	12	12	21	ns, Min
F _{TCK}	Maximum configuration TCK clock frequency	33	33	33	18	MHz, Max
F _{TCKB}	Maximum boundary-scan TCK clock frequency	33	33	33	18	MHz, Max
F _{TCKAES}	Maximum AES key TCK clock frequency	2	2	2	2	MHz, Max

Table 47: Configuration Switching Characteristics⁽¹⁾ (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
BPI Master Flash Mode Programming Switching⁽⁴⁾						
T _{BPICCO} ⁽⁵⁾	A[25:0], FCS_B, FOE_B, FWE_B, LDC outputs valid after CCLK falling edge	15	15	15	20	ns, Max
T _{BPIICCK}	Master BPI CCLK (output) delay	10/100	10/100	10/100	10/130	μs, Min/Max
T _{BPIDCC} /T _{BPICCD}	Setup/Hold on D[15:0] data input pins	5.0/1.0	5.0/1.0	5.0/1.0	6.0/2.0	ns, Min
SPI Master Flash Mode Programming Switching⁽⁶⁾						
T _{SPIDCC} /T _{SPIDCCD}	DIN, MISO0, MISO1, MISO2, MISO3, Setup/Hold before/after the rising CCLK edge	5.0/1.0	5.0/1.0	5.0/1.0	7.0/1.0	ns, Min
T _{SPIICCK}	Master SPI CCLK (output) delay	0.4/7.0	0.4/7.0	0.4/7.0	0.4/10.0	μs, Min/Max
T _{SPICCM}	MOSI clock to out	13	13	13	19	ns, Max
T _{SPICCFC}	CSO_B clock to out	16	16	16	26	ns, Max
CCLK Output (Master Modes)						
T _{MCCKL}	Master CCLK clock duty cycle Low	40/60				%, Min/Max
T _{MCCKH}	Master CCLK clock duty cycle High	40/60				%, Min/Max
F _{MCCK}	Maximum frequency, serial mode (Master Serial/SPI) All devices	40	40	40	30	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T	40	40	40	25	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x8 mode, LX150, and LX150T	40	40	40	20	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x16 mode	35	35	35	20	MHz, Max
F _{MCCKTOL}	Frequency Tolerance, master mode	±50	±50	±50	±50	%
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time	5	5	5	8	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time	5	5	5	8	ns, Min
USERCCLK Input						
T _{USERCCLKL}	USERCCLK clock minimum Low time	12	12	12	16	ns, Min
T _{USERCCLKH}	USERCCLK clock minimum High time	12	12	12	16	ns, Min
F _{USERCCLK}	Maximum USERCCLK frequency	40	40	40	30	MHz, Max

Notes:

- Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
- To support longer delays in configuration, use the design solutions described in [UG380: Spartan-6 FPGA Configuration User Guide](#).
- [Table 6](#) specifies the power supply ramp time.
- BPI mode is not supported in:
 - LX4, LX25, or LX25T devices
 - LX9 devices in the TQG144 package
 - LX9 or LX16 devices in the CPG196 package.
- Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
- Defense-grade Spartan-6Q -2Q devices configure in single default SPI Master (x1) mode at T_j = -55°C. During operation and when using all other configuration functions, the minimum operating temperature is -40°C.

Clock Buffers and Networks

Table 48: Global Clock Switching Characteristics (BUFGMUX)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{GSI}	S pin Setup to I0/I1 inputs	LX devices	0.25	0.31	0.48	0.48	ns
		LXT devices	0.25	0.31	0.48	N/A	ns
T _{GIO}	BUFGMUX delay from I0/I1 to O	LX devices	0.21	0.21	0.21	0.21	ns
		LXT devices	0.21	0.21	0.21	N/A	ns
Maximum Frequency							
F _{MAX}	Global clock tree (BUFGMUX)	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 49: Input/Output Clock Switching Characteristics (BUFIO2)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{BUFCO_O}	Clock to out delay from I to O	LX devices	0.67	0.82	1.09	1.50	ns
		LXT devices	0.67	0.82	1.09	N/A	ns
Maximum Frequency							
F _{MAX}	I/O clock tree (BUFIO2)	LX devices	540	525	500	300	MHz
		LXT devices	540	525	500	N/A	MHz

Table 50: Input/Output Clock Switching Characteristics (BUFIO2FB)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
Maximum Frequency							
F _{MAX}	I/O clock tree (BUFIO2FB)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

Table 51: Input/Output Clock Switching Characteristics (BUFPLL)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
Maximum Frequency							
F _{MAX}	BUFPLL clock tree (BUFPLL)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

PLL Switching Characteristics

Table 52: PLL Specification

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
F _{INMAX}	Maximum Input Clock Frequency from I/O Clock	LX devices	540	525	450	300	MHz
		LXT devices	540	525	450	N/A	MHz
	Maximum Input Clock Frequency from Global Clock	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 52: PLL Specification (Cont'd)

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
F _{INMIN}	Minimum Input Clock Frequency	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
F _{INJITTER}	Maximum Input Clock Period Jitter: 19–200 MHz	All	1 ns Maximum				
	Maximum Input Clock Period Jitter: > 200 MHz	All	<20% of clock input period Maximum				
F _{INDUTY}	Allowable Input Duty Cycle: 19—199 MHz	All	25/75				%
	Allowable Input Duty Cycle: 200—299 MHz	All	35/65				%
	Allowable Input Duty Cycle: > 300 MHz	All	45/55				%
F _{VCOMIN}	Minimum PLL VCO Frequency	LX devices	400	400	400	400	MHz
		LXT devices	400	400	400	N/A	MHz
F _{VCOMAX}	Maximum PLL VCO Frequency	LX devices	1080	1050	1000	1000	MHz
		LXT devices	1080	1050	1000	N/A	MHz
F _{BANDWIDTH}	Low PLL Bandwidth at Typical ⁽³⁾	All	1	1	1	1	MHz
	High PLL Bandwidth at Typical ⁽³⁾	All	4	4	4	4	MHz
T _{STAPHAOFFSET}	Static Phase Offset of the PLL Outputs	All	0.12	0.12	0.12	0.15	ns
T _{OUTJITTER}	PLL Output Jitter ⁽³⁾	All	Note 2				
T _{OUTDUTY}	PLL Output Clock Duty Cycle Precision ⁽⁴⁾	All	0.15	0.15	0.20	0.25	ns
T _{LOCKMAX}	PLL Maximum Lock Time	All	100	100	100	100	µs
F _{OUTMAX}	PLL Maximum Output Frequency for BUFGMUX	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz
	PLL Maximum Output Frequency for BUFPLL	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz
F _{OUTMIN}	PLL Minimum Output Frequency ⁽⁵⁾	All	3.125	3.125	3.125	3.125	MHz
T _{EXTFDVAR}	External Clock Feedback Variation: 19–200 MHz	All	1 ns Maximum				
	External Clock Feedback Variation: > 200 MHz	All	< 20% of clock input period Maximum				
RST _{MINPULSE}	Minimum Reset Pulse Width	All	5	5	5	5	ns
F _{PFDMAX} ⁽⁵⁾	Maximum Frequency at the Phase Frequency Detector	LX devices	500	500	400	300	MHz
		LXT devices	500	500	400	N/A	MHz
F _{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
T _{FBDELAY}	Maximum Delay in the Feedback Path	All	3 ns Max or one CLKIN cycle				

Notes:

1. LXT devices are not available with a -1L speed grade.
2. Values for this parameter are available in the Clocking Wizard.
3. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When using $CLK_FEEDBACK = CLKOUT0$ with $BUFIO2$ feedback, the feedback frequency will be higher than the phase frequency detector frequency. $F_{PFDMAX} = F_{CLKFB} / CLKFBOUT_MULT$

Table 54: Switching Characteristics for the Delay-Locked Loop (DLL)⁽¹⁾ (Cont'd)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
LOCK_DLL ⁽³⁾	When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. CLKIN_FREQ_DLL < 50 MHz.	-	5	-	5	-	5	-	5	ms
	When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. CLKIN_FREQ_DLL > 50 MHz	-	0.60	-	0.60	-	0.60	-	0.60	ms
Delay Lines										
DCM_DELAY_STEP ⁽⁵⁾	Finest delay resolution, averaged over all steps.	10	40	10	40	10	40	10	40	ps

Notes:

1. The values in this table are based on the operating conditions described in Table 2 and Table 53.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster LOCK time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, this data sheet specifies a maximum jitter of ±(1% of CLKIN period + 150 ps). Assuming that the CLKIN frequency is 100 MHz, the equivalent CLKIN period is 10 ns. Since 1% of 10 ns is 0.1 ns or 100 ps, the maximum jitter is ±(100 ps + 150 ps) = ±250 ps.
5. A typical delay step size is 23 ps.
6. The timing analysis tools use the CLK_FEEDBACK = 1X condition for the CLKIN_CLKFB_PHASE value (reported as phase error). When using CLK_FEEDBACK = 2X, add 100 ps to the phase error for the CLKIN_CLKFB_PHASE value (as shown in this table).

Table 55: Recommended Operating Conditions for the Digital Frequency Synthesizer (DFS)⁽¹⁾

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Input Frequency Ranges⁽²⁾										
CLKIN_FREQ_FX	Frequency for the CLKIN input. Also described as F _{CLKIN} .	0.5	375 ⁽³⁾	0.5	375 ⁽³⁾	0.5	333 ⁽³⁾	0.5	200 ⁽³⁾	MHz
Input Clock Jitter Tolerance⁽⁴⁾										
CLKIN_CYC_JITT_FX_LF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: F _{CLKFX} < 150 MHz.	-	±300	-	±300	-	±300	-	±300	ps
CLKIN_CYC_JITT_FX_HF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: F _{CLKFX} > 150 MHz.	-	±150	-	±150	-	±150	-	±150	ps
CLKIN_PER_JITT_FX	Period jitter at the CLKIN input.	-	±1	-	±1	-	±1	-	±1	ns

Notes:

1. DFS specifications apply when using either of the DFS outputs (CLKFX or CLKFX180).
2. When using both DFS and DLL outputs on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 53.
3. The CLKIN_DIVIDE_BY_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the F_{MAX} (see Table 48 and Table 49 for BUFIO2 and BUFI02 limits).
4. CLKIN input jitter beyond these limits can cause the DCM to lose LOCK.

Table 57: Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)⁽¹⁾

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges (DCM_CLKGEN)										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz
CLKOUT_FREQ_FXDV	Frequency for the CLKFXDV output	0.15625	187.5	0.15625	187.5	0.15625	166.5	0.15625	100	MHz
Output Clock Jitter⁽²⁾⁽³⁾										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	Typical = $\pm[0.2\%$ of CLKFX period + 100]								ps
CLKOUT_PER_JITT_FXDV	Period jitter at the CLKFXDV output.	Typical = $\pm[0.2\%$ of CLKFX period + 100]								ps
CLKFX_FREEZE_VAR	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX > 50 MHz	Maximum = $\pm 3\%$ of CLKFX period								ps
	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX < 50 MHz	Maximum = $\pm 5\%$ of CLKFX period								ps
CLKFX_FREEZE_TEMP_SLOPE	CLKFX period will change in free_oscillator mode over temperature. Add to CLKFX_FREEZE_VAR to determine total CLKFX period change. Percentage change for CLKFX period over 1°C.	Maximum = 0.1								%/°C
Duty Cycle⁽⁴⁾⁽⁵⁾										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = $\pm[1\%$ of CLKFX period + 350]								ps
CLKOUT_DUTY_CYCLE_FXDV	Duty cycle precision for the CLKFXDV outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = $\pm[1\%$ of CLKFX period + 350]								ps
Lock Time										
LOCK_FX ⁽²⁾	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX, CLKFX180, and CLKFXDV signals are valid. Lock time requires CLKFX_DIVIDE < F _{IN} /(0.50 MHz) when: F _{CLKIN} < 50 MHz	–	50	–	50	–	50	–	50	ms
	when: F _{CLKIN} > 50 MHz	–	5	–	5	–	5	–	5	ms

Spartan-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 63 through Table 69. Values are expressed in nanoseconds unless otherwise noted.

Table 63: Global Clock Input to Output Delay Without DCM or PLL

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>without</i> DCM or PLL							
T _{ICKOF}	Global Clock and OUTFF <i>without</i> DCM or PLL	XC6SLX4	6.12	N/A	7.68	9.41	ns
		XC6SLX9	6.12	6.51	7.68	9.41	ns
		XC6SLX16	5.98	6.42	7.48	9.10	ns
		XC6SLX25	6.20	6.69	7.84	9.44	ns
		XC6SLX25T	6.20	6.69	7.84	N/A	ns
		XC6SLX45	6.37	6.88	8.10	9.61	ns
		XC6SLX45T	6.37	6.88	8.10	N/A	ns
		XC6SLX75	6.39	6.99	8.16	10.18	ns
		XC6SLX75T	6.39	6.99	8.16	N/A	ns
		XC6SLX100	6.59	7.18	8.41	10.31	ns
		XC6SLX100T	6.59	7.18	8.41	N/A	ns
		XC6SLX150	6.98	7.68	8.80	10.62	ns
		XC6SLX150T	6.98	7.68	8.80	N/A	ns
		XA6SLX4	6.44	N/A	7.68	N/A	ns
		XA6SLX9	6.44	N/A	7.68	N/A	ns
		XA6SLX16	6.30	N/A	7.48	N/A	ns
		XA6SLX25	6.52	N/A	7.84	N/A	ns
		XA6SLX25T	6.52	N/A	7.84	N/A	ns
		XA6SLX45	6.69	N/A	8.12	N/A	ns
		XA6SLX45T	6.69	N/A	8.12	N/A	ns
		XA6SLX75	6.89	N/A	8.16	N/A	ns
		XA6SLX75T	6.89	N/A	8.16	N/A	ns
		XA6SLX100	N/A	N/A	8.36	N/A	ns
		XQ6SLX75	N/A	N/A	8.16	10.18	ns
XQ6SLX75T	6.89	N/A	8.16	N/A	ns		
XQ6SLX150	N/A	N/A	8.80	10.62	ns		
XQ6SLX150T	7.61	N/A	8.80	N/A	ns		

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 66: Global Clock Input to Output Delay With PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, with PLL in System-Synchronous Mode.							
T _{ICKOFFPLL}	Global Clock and OUTFF with PLL	XC6SLX4	4.57	N/A	6.25	7.34	ns
		XC6SLX9	4.57	5.25	6.25	7.34	ns
		XC6SLX16	4.41	4.64	5.39	6.92	ns
		XC6SLX25	4.03	4.32	4.91	7.64	ns
		XC6SLX25T	4.03	4.32	4.91	N/A	ns
		XC6SLX45	4.63	4.96	5.75	7.36	ns
		XC6SLX45T	4.63	4.96	5.75	N/A	ns
		XC6SLX75	4.01	4.30	4.88	7.15	ns
		XC6SLX75T	4.01	4.30	4.88	N/A	ns
		XC6SLX100	4.02	4.33	4.90	7.37	ns
		XC6SLX100T	4.06	4.33	4.90	N/A	ns
		XC6SLX150	3.65	3.98	4.58	6.94	ns
		XC6SLX150T	3.65	3.98	4.58	N/A	ns
		XA6SLX4	4.88	N/A	6.13	N/A	ns
		XA6SLX9	4.88	N/A	6.13	N/A	ns
		XA6SLX16	4.74	N/A	5.27	N/A	ns
		XA6SLX25	4.43	N/A	4.78	N/A	ns
		XA6SLX25T	4.43	N/A	4.88	N/A	ns
		XA6SLX45	4.94	N/A	5.62	N/A	ns
		XA6SLX45T	4.94	N/A	5.62	N/A	ns
		XA6SLX75	4.32	N/A	4.77	N/A	ns
		XA6SLX75T	4.32	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.41	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	7.15	ns
XQ6SLX75T	4.32	N/A	4.77	N/A	ns		
XQ6SLX150	N/A	N/A	4.60	6.94	ns		
XQ6SLX150T	4.35	N/A	4.60	N/A	ns		

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 69: Global Clock Input to Output Delay With DCM and PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode.							
T _{ICKOFDCM0_PLL}	Global Clock and OUTFF with DCM and PLL	XC6SLX4	5.58	N/A	7.42	8.54	ns
		XC6SLX9	5.58	6.19	7.42	8.54	ns
		XC6SLX16	5.50	6.06	7.05	8.24	ns
		XC6SLX25	5.57	6.04	7.02	8.33	ns
		XC6SLX25T	5.57	6.04	7.02	N/A	ns
		XC6SLX45	5.53	5.97	6.96	8.32	ns
		XC6SLX45T	5.53	5.97	6.96	N/A	ns
		XC6SLX75	5.55	6.00	6.99	8.54	ns
		XC6SLX75T	5.55	6.00	6.99	N/A	ns
		XC6SLX100	5.58	6.03	7.02	9.11	ns
		XC6SLX100T	5.62	6.03	7.02	N/A	ns
		XC6SLX150	5.32	5.70	6.41	8.26	ns
		XC6SLX150T	5.32	5.70	6.41	N/A	ns
		XA6SLX4	5.87	N/A	7.28	N/A	ns
		XA6SLX9	5.87	N/A	7.28	N/A	ns
		XA6SLX16	6.02	N/A	6.87	N/A	ns
		XA6SLX25	5.88	N/A	6.90	N/A	ns
		XA6SLX25T	5.88	N/A	7.00	N/A	ns
		XA6SLX45	5.82	N/A	6.81	N/A	ns
		XA6SLX45T	5.82	N/A	6.81	N/A	ns
		XA6SLX75	5.81	N/A	6.80	N/A	ns
		XA6SLX75T	5.81	N/A	6.80	N/A	ns
		XA6SLX100	N/A	N/A	6.88	N/A	ns
		XQ6SLX75	N/A	N/A	6.80	8.54	ns
XQ6SLX75T	5.81	N/A	6.80	N/A	ns		
XQ6SLX150	N/A	N/A	6.41	8.26	ns		
XQ6SLX150T	5.90	N/A	6.41	N/A	ns		

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 75: Global Clock Setup and Hold With PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.⁽¹⁾							
T _{PSPLL0} / T _{PHPLL0}	No Delay Global Clock and IFF ⁽²⁾ with PLL in Source-Synchronous Mode	XC6SLX4	0.47/1.08	N/A	0.47/1.60	1.15/1.68	ns
		XC6SLX9	0.47/1.08	0.47/1.35	0.47/1.60	1.15/1.68	ns
		XC6SLX16	0.37/0.75	0.37/0.82	0.51/0.94	0.57/1.31	ns
		XC6SLX25	0.69/1.06	0.69/1.06	0.69/1.06	1.86/1.67	ns
		XC6SLX25T	0.69/1.06	0.69/1.06	0.69/1.06	N/A	ns
		XC6SLX45	0.57/1.05	0.65/1.10	0.65/1.18	1.02/1.65	ns
		XC6SLX45T	0.57/1.06	0.65/1.10	0.65/1.18	N/A	ns
		XC6SLX75	0.86/1.04	0.87/1.04	0.90/1.04	1.34/1.55	ns
		XC6SLX75T	0.86/1.04	0.87/1.04	0.90/1.04	N/A	ns
		XC6SLX100	0.53/1.13	0.54/1.13	0.55/1.13	0.89/2.39	ns
		XC6SLX100T	0.53/1.13	0.54/1.13	0.55/1.13	N/A	ns
		XC6SLX150	0.50/1.31	0.51/1.31	0.52/1.31	1.02/1.72	ns
		XC6SLX150T	0.50/1.31	0.51/1.31	0.52/1.31	N/A	ns
		XA6SLX4	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX9	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX16	0.92/0.69	N/A	0.63/0.82	N/A	ns
		XA6SLX25	0.99/0.94	N/A	0.96/0.94	N/A	ns
		XA6SLX25T	0.99/0.94	N/A	1.04/0.94	N/A	ns
		XA6SLX45	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX45T	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX75	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX100	N/A	N/A	1.25/0.96	N/A	ns
		XQ6SLX75	N/A	N/A	1.02/0.89	1.34/1.55	ns
XQ6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns		
XQ6SLX150	N/A	N/A	0.63/1.19	1.02/1.72	ns		
XQ6SLX150T	0.60/1.19	N/A	0.63/1.19	N/A	ns		

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 76: Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.⁽¹⁾							
T _{PSDCMPLL} / T _{PHDCMPLL}	No Delay Global Clock and IFF ⁽²⁾ with DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.	XC6SLX4	1.16/0.49	N/A	1.39/0.49	2.36/0.59	ns
		XC6SLX9	1.16/0.44	1.37/0.44	1.39/0.44	2.36/0.59	ns
		XC6SLX16	1.44/-0.08	1.49/-0.04	1.62/-0.04	2.06/0.55	ns
		XC6SLX25	1.52/0.42	1.65/0.42	1.83/0.42	2.52/0.43	ns
		XC6SLX25T	1.52/0.42	1.65/0.42	1.83/0.42	N/A	ns
		XC6SLX45	1.54/0.39	1.59/0.39	1.75/0.39	2.48/0.76	ns
		XC6SLX45T	1.54/0.39	1.59/0.39	1.75/0.39	N/A	ns
		XC6SLX75	1.72/0.41	1.80/0.41	1.99/0.41	2.60/0.75	ns
		XC6SLX75T	1.72/0.41	1.80/0.41	1.99/0.41	N/A	ns
		XC6SLX100	1.34/0.51	1.46/0.51	1.64/0.51	2.12/0.90	ns
		XC6SLX100T	1.34/0.51	1.46/0.51	1.64/0.51	N/A	ns
		XC6SLX150	1.30/0.60	1.40/0.60	1.55/0.60	2.57/0.97	ns
		XC6SLX150T	1.30/0.60	1.40/0.60	1.55/0.60	N/A	ns
		XA6SLX4	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX9	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX16	2.67/0.35	N/A	2.67/0.17	N/A	ns
		XA6SLX25	1.74/0.27	N/A	1.95/0.27	N/A	ns
		XA6SLX25T	1.74/0.27	N/A	2.03/0.27	N/A	ns
		XA6SLX45	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX45T	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX75	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX100	N/A	N/A	2.64/0.82	N/A	ns
		XQ6SLX75	N/A	N/A	2.11/0.24	2.60/0.75	ns
		XQ6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XQ6SLX150	N/A	N/A	1.67/0.70	2.57/0.97	ns
XQ6SLX150T	1.50/0.70	N/A	1.67/0.70	N/A	ns		

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 78: Duty Cycle Distortion and Clock-Tree Skew (Cont'd)

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{BUFIOSKEW}	I/O clock tree skew across one clock region	LX4	0.06	N/A	0.06	0.07	ns
		LX9	0.06	0.06	0.06	0.07	ns
		LX16	0.06	0.06	0.06	0.07	ns
		LX25	0.06	0.06	0.06	0.07	ns
		LX25T	0.06	0.06	0.06	N/A	ns
		LX45	0.06	0.06	0.06	0.07	ns
		LX45T	0.06	0.06	0.06	N/A	ns
		LX75	0.06	0.06	0.06	0.07	ns
		LX75T	0.06	0.06	0.06	N/A	ns
		LX100	0.06	0.06	0.06	0.07	ns
		LX100T	0.06	0.06	0.06	N/A	ns
		LX150	0.06	0.06	0.06	0.07	ns
		LX150T	0.06	0.06	0.06	N/A	ns

Notes:

- LXT devices are not available with a -1L speed grade. The LX4 is not available in -3N speed grade.
- These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
- The T_{CKSKEW} is 0.43 ns for the XA6SLX100 device using a -2 speed grade and 0.22 ns for the XC6SLX100 devices using the -2 speed grade.

Table 79: Package Skew

Symbol	Description	Device	Package ⁽²⁾	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	LX4	TQG144	N/A	ps
			CPG196	23	ps
			CSG225	58	ps
		LX9	TQG144	N/A	ps
			CPG196	23	ps
			CSG225	58	ps
			FT(G)256	88	ps
			CSG324	64	ps
		LX16	CPG196	19	ps
			CSG225	70	ps
			FT(G)256	71	ps
			CSG324	54	ps
		LX25	FT(G)256	90	ps
			CSG324	61	ps
			FG(G)484	84	ps
LX25T	CSG324	48	ps		
	FG(G)484	112	ps		

Table 79: Package Skew (Cont'd)

Symbol	Description	Device	Package ⁽²⁾	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	LX45	CSG324	70	ps
			CS(G)484	99	ps
			FG(G)484	109	ps
			FG(G)676	138	ps
		LX45T	CSG324	75	ps
			CS(G)484	100	ps
			FG(G)484	95	ps
		LX75	CS(G)484	101	ps
			FG(G)484	107	ps
		LX75T	FG(G)676	161	ps
			CS(G)484	107	ps
			FG(G)484	110	ps
		LX100	FG(G)676	134	ps
			CS(G)484	95	ps
			FG(G)484	155	ps
		LX100T	FG(G)676	144	ps
			CS(G)484	88	ps
			FG(G)484	111	ps
			FG(G)676	147	ps
		LX150	FG(G)900	134	ps
			CS(G)484	84	ps
			FG(G)484	103	ps
			FG(G)676	115	ps
		LX150T	FG(G)900	121	ps
CS(G)484	83		ps		
FG(G)484	88		ps		
FG(G)676	141		ps		
			FG(G)900	120	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from Pad to Ball.
2. Some of the devices are available in both Pb and Pb-free (additional G) packages as standard ordering options. See [DS160: Spartan-6 Family Overview](#) for more information.

Table 80: Sample Window

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{SAMP}	Sampling Error at Receiver Pins ⁽²⁾	All	510	510	530	740	ps
T _{SAMP_BUFIO2}	Sampling Error at Receiver Pins using BUFIO2 ⁽³⁾	All	430	430	450	590	ps

Notes:

1. LXT devices are not available with a -1L speed grade.
2. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 DCM jitter
 - DCM accuracy (phase offset)
 - DCM phase shift resolution
 These measurements do not include package or clock tree skew.
3. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO2 clock network and IODELAY2 to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
08/26/09	1.1	Added V_{FS} to Table 1 and Table 2 . Added R_{FUSE} to Table 2 . Added XC6SLX75 and XC6SLX75T to V_{BATT} and I_{BATT} in Table 1 , Table 2 , and Table 4 . Corrected the quiescent supply current for the XC6SLX4 in Table 5 . Updated Table 11 . Removed DV_{PPIN} from Figure 2 . Removed $F_{PCIECORE}$ from Table 24 and added values to $F_{PCIEUSER}$. Added more networking applications to Table 25 . Updated values for $T_{SUSPENDLOW_AWAKE}$, $T_{SUSPEND_ENABLE}$, and T_{SCP_AWAKE} in Table 46 . Numerous changes to Table 47 , page 54 including the addition of new values to various specifications, revising the $T_{SMCKCSO}$ description, and changing the units of T_{POR} . Also, removed <i>Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK section</i> from Table 47 and updated all the notes. In Table 52 , added to F_{INMAX} , revised F_{OUTMAX} , and removed PLL Maximum Output Frequency for BUFIO2. Revised values for DCM_DELAY_STEP in Table 54 . Updated CLKIN_FREQ_FX values in Table 55 .
01/04/10	1.2	Added -4 speed grade to entire document. Updated speed specification of -4, -3, -2 speed grades to version 1.03. Added -1L speed grade numbers per speed specification 1.00. Updated T_{SOL} in Table 1 . Added -1L rows for LVCMOS12, LVCMOS15, and LVCMOS18 in Table 9 . Revised much of the detail in GTP Transceiver Specifications in Table 12 through Table 23 . Added -2 data to Table 25 . Updated F_{MAX} in Table 44 . Updated descriptions for $T_{DNACLKL}$ and $T_{DNACLKH}$ in Table 45 and revised values for all parameters. Removed $T_{INITADDR}$ from Table 47 and added new data. Updated values in Table 48 through Table 62 . Added Table 51 (BUFPLL) and Table 57 (DCM_CLKGEN). Removed $T_{LOCKMAX}$ note from Table 52 . Updated note 3 in Table 53 . In Table 79 : removed XC6SLX75CSG324 and XC6SLX75TCSG324; added XC6SLX75FG(G)484 and XC6SLX75FG(G)484.
02/22/10	1.3	Production release of XC6SLX16 -2 speed grade devices. The changes to Table 26 and Table 27 includes updating this data sheet to the data in ISE v11.5 software with speed specification v1.06. Updated maximum of V_{IN} and V_{TS} and note 2 in Table 1 . In Table 2 , changed V_{IN} , added I_{IN} and note 5, revised notes 1, 6, and 7, and added note 8 to R_{FUSE} . In Table 4 , removed previous note 1 and added data to I_{RPU} , I_{RPD} , and I_{BATT} , changed C_{IN} , added R_{DT} and R_{IN_TERM} , and added note 2 and 3. Updated V_{CCO2} in Table 6 . Added Table 7 and Table 8 . Removed PCI66_3 from Table 9 . Updated PCI33_3 and I2C in Table 9 . Updated the description of Table 11 . Completely updated Table 25 . Updated Table 28 including adding values for PCI33_3. Updated V_{REF} value for HSTL_III_18 in Table 31 . Updates missing V_{REF} values in Table 32 . Added Simultaneously Switching Outputs , page 36 . Removed T_{GSRQ} and T_{RPW} from Table 35 and Table 36 . Also removed T_{DOQ} from Table 36 . Removed T_{ISDO_DO} and note 1 from Table 37 . Removed T_{OSCK_S} and combinatorial section from Table 38 . In Table 39 , removed T_{IODDO_T} and added new tap parameters and note 2. In Table 40 , Table 41 , and Table 42 , made typographical edits and removed notes. Removed clock CLK section in Table 41 . Removed clock CLK section and T_{REG_MUX} and T_{REG_M31} in Table 42 . Added block RAM F_{MAX} values to Table 43 . Updated values and added note 2 to Table 45 . Added values to Table 46 and removed note 1. Numerous changes to Table 47 . Completely updated Table 57 . Revised data in Table 62 . Removed note 3 from Table 71 . Added values to Table 79 . Added data to Table 80 and Table 81 .
03/10/10	1.4	Production release of XC6SLX45 -2 speed grade devices, which includes changes to Table 26 and Table 27 updating this data sheet to the data in ISE v11.5 software with speed specification v1.07. Fixed R_{IN_TERM} description in Table 4 . Added PCI66_3 to Table 7 and replaced note 1. Corrected note 1 and the V, Max for TMDS_33 in Table 8 . In Table 10 , added note 1 to LVPECL_33 and TMDS_33. Also updated specifications for TMDS_33. Updated the GTP Transceiver Specifications section including adding values to Table 16 , Table 17 , and Table 20 through Table 23 . Added PCI66_3 back into Table 9 , Table 28 , Table 31 , Table 32 , and Table 34 . Updated note 3 on Table 32 . In Table 34 , corrected some typographical errors and fixed SSO limits for bank1/3 in FG(G)484 package. Corrected T_{OSCKC_OCE} in Table 38 . In Table 57 , updated CLKFX_FREEZE_VAR and CLKFX_FREEZE_TEMP_SLOPE and added typical values to $T_{CENTER_LOW_SPREAD}$ and $T_{CENTER_HIGH_SPREAD}$. Updated and added values to Table 63 through Table 78 , and Table 81 . In Table 79 , revised the XC6SLX16-CSG324 and the XC6SLX45-CSG484 and FG(G)484 values.