AMD Xilinx - XC6SLX16-L1CSG324I Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1139
Number of Logic Elements/Cells	14579
Total RAM Bits	589824
Number of I/O	232
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	324-LFBGA, CSPBGA
Supplier Device Package	324-CSPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx16-l1csg324i

Table 2: **Recommended Operating Conditions(1)**

Symbol	Description			Min	Typ	Max	Units
V_{CCINT}	Internal supply voltage relative to GND	-3, -3N, -2	Standard performance(2)	1.14	1.2	1.26	V
		-3, -2	Extended performance(2)	1.2	1.23	1.26	V
		-1L	Standard performance(2)	0.95	1.0	1.05	V
V_{CCAUX}(3)(4)	Auxiliary supply voltage relative to GND	V_{CCAUX} = 2.5V(5)		2.375	2.5	2.625	V
		V_{CCAUX} = 3.3V		3.15	3.3	3.45	V
V_{CCO}(6)(7)(8)	Output supply voltage relative to GND			1.1	–	3.45	V
V_{IN}	Input voltage relative to GND	All I/O standards (except PCI)	Commercial temperature (C)	–0.5	–	4.0	V
			Industrial temperature (I)	–0.5	–	3.95	V
			Expanded (Q) temperature	–0.5	–	3.95	V
		PCI I/O standard(9)		–0.5	–	V_{CCO} + 0.5	V
I_{IN}(10)	Maximum current through pin using PCI I/O standard when forward biasing the clamp diode.(9)		Commercial (C) and Industrial temperature (I)	–	–	10	mA
			Expanded (Q) temperature	–	–	7	mA
V_{BATT}(11)	Battery voltage relative to GND, T_j = 0°C to +85°C (LX75, LX75T, LX100, LX100T, LX150, and LX150T only)			1.0	–	3.6	V
T_j	Junction temperature operating range	Commercial (C) range		0	–	85	°C
		Industrial temperature (I) range		–40	–	100	°C
		Expanded (Q) temperature range		–40	–	125	°C

Notes:

1. All voltages are relative to ground.
2. See *Interface Performances for Memory Interfaces* in Table 25. The extended performance range is specified for designs not using the standard V_{CCINT} voltage range. The standard V_{CCINT} voltage range is used for:
   - Designs that do not use an MCB
   - LX4 devices
   - Devices in the TQG144 or CPG196 packages
   - Devices with the -3N speed grade
3. Recommended maximum voltage droop for V_{CCAUX} is 10 mV/ms.
4. During configuration, if V_{CCO_2} is 1.8V, then V_{CCAUX} must be 2.5V.
5. The -1L devices require V_{CCAUX} = 2.5V when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.
6. Configuration data is retained even if V_{CCO} drops to 0V.
7. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
8. For PCI systems, the transmitter and receiver should have common supplies for V_{CCO}.
9. Devices with a -1L speed grade do not support Xilinx PCI IP.
10. Do not exceed a total of 100 mA per bank.
11. V_{BATT} is required to maintain the battery backed RAM (BBR) AES key when V_{CCAUX} is not applied. Once V_{CCAUX} is applied, V_{BATT} can be unconnected. When BBR is not used, Xilinx recommends connecting to V_{CCAUX} or GND. However, V_{BATT} can be unconnected.

SelectIO™ Interface DC Input and Output Levels

Table 7: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

I/O Standard	V_{CCO} for Drivers[1]			V_{REF} for Inputs		
	V, Min	V, Nom	V, Max	V, Min	V, Nom	V, Max
LVTTL	3.0	3.3	3.45	V_{REF} is not used for these I/O standards		
LVCMOS33	3.0	3.3	3.45			
LVCMOS25	2.3	2.5	2.7			
LVCMOS18	1.65	1.8	1.95			
LVCMOS18_JEDEC	1.65	1.8	1.95			
LVCMOS15	1.4	1.5	1.6			
LVCMOS15_JEDEC	1.4	1.5	1.6			
LVCMOS12	1.1	1.2	1.3			
LVCMOS12_JEDEC	1.1	1.2	1.3			
PCI33_3[2]	3.0	3.3	3.45			
PCI66_3[2]	3.0	3.3	3.45			
I2C	2.7	3.0	3.45			
SMBUS	2.7	3.0	3.45			
SDIO	3.0	3.3	3.45			
MOBILE_DDR	1.7	1.8	1.9			
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_II	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_III	1.4	1.5	1.6	–	0.9	–
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–
HSTL_III_18	1.7	1.8	1.9	–	1.1	–
SSTL3_I	3.0	3.3	3.45	1.3	1.5	1.7
SSTL3_II	3.0	3.3	3.45	1.3	1.5	1.7
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38
SSTL18_I	1.7	1.8	1.9	0.833	0.9	0.969
SSTL18_II	1.7	1.8	1.9	0.833	0.9	0.969
SSTL15_II	1.425	1.5	1.575	0.69	0.75	0.81

Notes:

1. V_{CCO} range required when using I/O standard for an output. Also required for MOBILE_DDR, PCI33_3, LVCMOS18_JEDEC, LVCMOS15_JEDEC, and LVCMOS12_JEDEC inputs, and for LVCMOS25 inputs when V_{CCAUX} = 3.3V.
2. For PCI systems, the transmitter and receiver should have common supplies for V_{CCO}.

eFUSE Read Endurance

Table 11 lists the minimum guaranteed number of read cycle operations for Device DNA and for the AES eFUSE key. For more information, see UG380: *Spartan-6 FPGA Configuration User Guide*.

Table 11: **eFUSE Read Endurance**

Symbol	Description	Speed Grade				Units (Min)
		-3	-3N	-2	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTP Transceiver Specifications

GTP transceivers are available in the Spartan-6 LXT devices. See DS160: *Spartan-6 Family Overview* for more information.

GTP Transceiver DC Characteristics

Table 12: **Absolute Maximum Ratings for GTP Transceivers(1)**

Symbol	Description	Mln	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	–0.5	1.32	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	–0.5	1.32	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	–0.5	1.32	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 13: **Recommended Operating Conditions for GTP Transceivers(1)(2)(3)**

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	1.14	1.20	1.26	V

Notes:
1. Each voltage listed requires the filter circuit described in UG386: *Spartan-6 FPGA GTP Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +125°C.
3. The voltage level of MGTAVCCPLL must not exceed the voltage level of MGTAVCC +10mV. The voltage level of MGTAVCC must not exceed the voltage level of MGTAVCCPLL.

Table 23: **GTP Transceiver Receiver Switching Characteristics**

Symbol	Description			Min	Typ	Max	Units
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data			–	75	–	ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak			60	–	150	mV
R_{XSST}	Receiver spread-spectrum tracking(1)		Modulated @ 33 KHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)	Internal AC capacitor bypassed		–	–	150	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	CDR 2nd-order loop disabled		–200	–	200	ppm
		CDR 2nd-order loop enabled	PLL_RXDIVSEL_OUT = 1	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 2	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 4	–1000	–	1000	ppm
SJ Jitter Tolerance(2)							
$JT\_SJ_{3.125}$	Sinusoidal Jitter(3)		3.125 Gb/s	0.4	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(3)		2.5 Gb/s	0.4	–	–	UI
$JT\_SJ_{1.62}$	Sinusoidal Jitter(3)		1.62 Gb/s	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(3)		1.25 Gb/s	0.5	–	–	UI
JT_SJ_{614}	Sinusoidal Jitter(3)		614 Mb/s	0.5	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)(5)							
$JT\_TJSE_{3.125}$	Total Jitter with stressed eye(4)		3.125 Gb/s	0.65	–	–	UI
$JT\_SJSE_{3.125}$	Sinusoidal Jitter with stressed eye		3.125 Gb/s	0.1	–	–	UI
$JT\_TJSE_{2.7}$	Total Jitter with stressed eye(4)		2.7 Gb/s	0.65	–	–	UI
$JT\_SJSE_{2.7}$	Sinusoidal Jitter with stressed eye		2.7 Gb/s	0.1	–	–	UI

Notes:
1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a Bit Error Ratio of $1e^{-12}$.
3. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
4. Composed of 0.37 UI DJ in the form of ISI and 0.18 UI RJ.
5. Measured using PRBS7 data pattern.

Endpoint Block for PCI Express Designs Switching Characteristics

The Endpoint block for PCI Express is available in the Spartan-6 LXT devices. Consult the Spartan-6 FPGA Integrated Endpoint Block for PCI Express for further information.

Table 24: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
$F_{PCIEUSER}$	User clock maximum frequency	62.5	62.5	62.5	N/A	MHz

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	
LVTTL, QUIETIO, 2 mA	1.35	1.47	1.60	1.82	5.39	5.53	5.73	6.37	5.39	5.53	5.73	6.37	ns
LVTTL, QUIETIO, 4 mA	1.35	1.47	1.60	1.82	4.29	4.43	4.63	5.22	4.29	4.43	4.63	5.22	ns
LVTTL, QUIETIO, 6 mA	1.35	1.47	1.60	1.82	3.75	3.89	4.09	4.69	3.75	3.89	4.09	4.69	ns
LVTTL, QUIETIO, 8 mA	1.35	1.47	1.60	1.82	3.23	3.37	3.57	4.20	3.23	3.37	3.57	4.20	ns
LVTTL, QUIETIO, 12 mA	1.35	1.47	1.60	1.82	3.28	3.42	3.62	4.22	3.28	3.42	3.62	4.22	ns
LVTTL, QUIETIO, 16 mA	1.35	1.47	1.60	1.82	2.94	3.08	3.28	3.92	2.94	3.08	3.28	3.92	ns
LVTTL, QUIETIO, 24 mA	1.35	1.47	1.60	1.82	2.69	2.83	3.03	3.67	2.69	2.83	3.03	3.67	ns
LVTTL, Slow, 2 mA	1.35	1.47	1.60	1.82	4.36	4.50	4.70	5.30	4.36	4.50	4.70	5.30	ns
LVTTL, Slow, 4 mA	1.35	1.47	1.60	1.82	3.17	3.31	3.51	4.16	3.17	3.31	3.51	4.16	ns
LVTTL, Slow, 6 mA	1.35	1.47	1.60	1.82	2.76	2.90	3.10	3.75	2.76	2.90	3.10	3.75	ns
LVTTL, Slow, 8 mA	1.35	1.47	1.60	1.82	2.59	2.73	2.93	3.55	2.59	2.73	2.93	3.55	ns
LVTTL, Slow, 12 mA	1.35	1.47	1.60	1.82	2.58	2.72	2.92	3.54	2.58	2.72	2.92	3.54	ns
LVTTL, Slow, 16 mA	1.35	1.47	1.60	1.82	2.39	2.53	2.73	3.40	2.39	2.53	2.73	3.40	ns
LVTTL, Slow, 24 mA	1.35	1.47	1.60	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVTTL, Fast, 2 mA	1.35	1.47	1.60	1.82	3.78	3.92	4.12	4.74	3.78	3.92	4.12	4.74	ns
LVTTL, Fast, 4 mA	1.35	1.47	1.60	1.82	2.49	2.63	2.83	3.45	2.49	2.63	2.83	3.45	ns
LVTTL, Fast, 6 mA	1.35	1.47	1.60	1.82	2.44	2.58	2.78	3.40	2.44	2.58	2.78	3.40	ns
LVTTL, Fast, 8 mA	1.35	1.47	1.60	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns
LVTTL, Fast, 12 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTL, Fast, 16 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTL, Fast, 24 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVCMOS33, QUIETIO, 2 mA	1.34	1.46	1.59	1.82	5.40	5.54	5.74	6.37	5.40	5.54	5.74	6.37	ns
LVCMOS33, QUIETIO, 4 mA	1.34	1.46	1.59	1.82	4.03	4.17	4.37	5.01	4.03	4.17	4.37	5.01	ns
LVCMOS33, QUIETIO, 6 mA	1.34	1.46	1.59	1.82	3.51	3.65	3.85	4.47	3.51	3.65	3.85	4.47	ns
LVCMOS33, QUIETIO, 8 mA	1.34	1.46	1.59	1.82	3.37	3.51	3.71	4.33	3.37	3.51	3.71	4.33	ns
LVCMOS33, QUIETIO, 12 mA	1.34	1.46	1.59	1.82	2.94	3.08	3.28	3.93	2.94	3.08	3.28	3.93	ns
LVCMOS33, QUIETIO, 16 mA	1.34	1.46	1.59	1.82	2.77	2.91	3.11	3.78	2.77	2.91	3.11	3.78	ns
LVCMOS33, QUIETIO, 24 mA	1.34	1.46	1.59	1.82	2.59	2.73	2.93	3.58	2.59	2.73	2.93	3.58	ns
LVCMOS33, Slow, 2 mA	1.34	1.46	1.59	1.82	4.37	4.51	4.71	5.28	4.37	4.51	4.71	5.28	ns
LVCMOS33, Slow, 4 mA	1.34	1.46	1.59	1.82	2.98	3.12	3.32	3.94	2.98	3.12	3.32	3.94	ns
LVCMOS33, Slow, 6 mA	1.34	1.46	1.59	1.82	2.58	2.72	2.92	3.61	2.58	2.72	2.92	3.61	ns
LVCMOS33, Slow, 8 mA	1.34	1.46	1.59	1.82	2.65	2.79	2.99	3.61	2.65	2.79	2.99	3.61	ns
LVCMOS33, Slow, 12 mA	1.34	1.46	1.59	1.82	2.39	2.53	2.73	3.31	2.39	2.53	2.73	3.31	ns
LVCMOS33, Slow, 16 mA	1.34	1.46	1.59	1.82	2.31	2.45	2.65	3.27	2.31	2.45	2.65	3.27	ns
LVCMOS33, Slow, 24 mA	1.34	1.46	1.59	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVCMOS33, Fast, 2 mA	1.34	1.46	1.59	1.82	3.76	3.90	4.10	4.70	3.76	3.90	4.10	4.70	ns
LVCMOS33, Fast, 4 mA	1.34	1.46	1.59	1.82	2.48	2.62	2.82	3.44	2.48	2.62	2.82	3.44	ns
LVCMOS33, Fast, 6 mA	1.34	1.46	1.59	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	
LVCMOS12, Fast, 2 mA	0.91	1.03	1.16	1.51	3.46	3.60	3.80	4.44	3.46	3.60	3.80	4.44	ns
LVCMOS12, Fast, 4 mA	0.91	1.03	1.16	1.51	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVCMOS12, Fast, 6 mA	0.91	1.03	1.16	1.51	1.79	1.93	2.13	2.75	1.79	1.93	2.13	2.75	ns
LVCMOS12, Fast, 8 mA	0.91	1.03	1.16	1.51	1.68	1.82	2.02	2.64	1.68	1.82	2.02	2.64	ns
LVCMOS12, Fast, 12 mA	0.91	1.03	1.16	1.51	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
LVCMOS12_JEDEC, QUIETIO, 2 mA	1.50	1.62	1.75	1.88	6.39	6.53	6.73	7.31	6.39	6.53	6.73	7.31	ns
LVCMOS12_JEDEC, QUIETIO, 4 mA	1.50	1.62	1.75	1.88	4.98	5.12	5.32	5.88	4.98	5.12	5.32	5.88	ns
LVCMOS12_JEDEC, QUIETIO, 6 mA	1.50	1.62	1.75	1.88	4.67	4.81	5.01	5.54	4.67	4.81	5.01	5.54	ns
LVCMOS12_JEDEC, QUIETIO, 8 mA	1.50	1.62	1.75	1.88	4.23	4.37	4.57	5.22	4.23	4.37	4.57	5.22	ns
LVCMOS12_JEDEC, QUIETIO, 12 mA	1.50	1.62	1.75	1.88	3.99	4.13	4.33	4.94	3.99	4.13	4.33	4.94	ns
LVCMOS12_JEDEC, Slow, 2 mA	1.50	1.62	1.75	1.88	5.00	5.14	5.34	5.90	5.00	5.14	5.34	5.90	ns
LVCMOS12_JEDEC, Slow, 4 mA	1.50	1.62	1.75	1.88	2.85	2.99	3.19	3.80	2.85	2.99	3.19	3.80	ns
LVCMOS12_JEDEC, Slow, 6 mA	1.50	1.62	1.75	1.88	2.76	2.90	3.10	3.72	2.76	2.90	3.10	3.72	ns
LVCMOS12_JEDEC, Slow, 8 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVCMOS12_JEDEC, Slow, 12 mA	1.50	1.62	1.75	1.88	2.09	2.23	2.43	3.05	2.09	2.23	2.43	3.05	ns
LVCMOS12_JEDEC, Fast, 2 mA	1.50	1.62	1.75	1.88	3.46	3.60	3.80	4.42	3.46	3.60	3.80	4.42	ns
LVCMOS12_JEDEC, Fast, 4 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns
LVCMOS12_JEDEC, Fast, 6 mA	1.50	1.62	1.75	1.88	1.79	1.93	2.13	2.76	1.79	1.93	2.13	2.76	ns
LVCMOS12_JEDEC, Fast, 8 mA	1.50	1.62	1.75	1.88	1.69	1.83	2.03	2.65	1.69	1.83	2.03	2.65	ns
LVCMOS12_JEDEC, Fast, 12 mA	1.50	1.62	1.75	1.88	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns

Notes:

1. The -1L values listed in this table are also applicable to the Spartan-6Q devices.
2. Devices with a -1L speed grade do not support Xilinx PCI IP.

Table 29: **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices(1)**

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVDS_33	1.24	1.42	1.69	1.89	3000	3000	ns
LVDS_25	1.08	1.26	1.79	1.99	3000	3000	ns
BLVDS_25	1.09	1.27	1.86	2.06	1.86	2.06	ns
MINI_LVDS_33	1.25	1.43	1.71	1.91	3000	3000	ns
MINI_LVDS_25	1.08	1.26	1.79	1.99	3000	3000	ns
LVPECL_33	1.25	1.43	N/A	N/A	N/A	N/A	ns
LVPECL_25	1.09	1.27	N/A	N/A	N/A	N/A	ns
RSDS_33 (point to point)	1.24	1.42	1.71	1.91	3000	3000	ns
RSDS_25 (point to point)	1.08	1.26	1.79	1.99	3000	3000	ns
TMDS_33	1.29	1.47	1.68	1.88	3000	3000	ns
PPDS_33	1.25	1.43	1.71	1.91	3000	3000	ns
PPDS_25	1.08	1.26	1.82	2.02	3000	3000	ns
PCI33_3	1.14	1.32	3.81	4.01	3.81	4.01	ns
PCI66_3	1.14	1.32	3.81	4.01	3.81	4.01	ns
DISPLAY_PORT	1.09	1.27	3.29	3.49	3.29	3.49	ns
I2C	1.40	1.58	11.70	11.90	11.70	11.90	ns
SMBUS	1.40	1.58	11.70	11.90	11.70	11.90	ns
SDIO	1.43	1.61	2.78	2.98	2.78	2.98	ns
MOBILE_DDR	1.01	1.19	2.50	2.70	2.50	2.70	ns
HSTL_I	1.01	1.19	1.80	2.00	1.80	2.00	ns
HSTL_II	1.01	1.19	1.86	2.06	1.86	2.06	ns
HSTL_III	1.07	1.25	1.81	2.01	1.81	2.01	ns
HSTL_I _18	1.05	1.23	1.91	2.11	1.91	2.11	ns
HSTL_II _18	1.05	1.23	1.99	2.19	1.99	2.19	ns
HSTL_III _18	1.13	1.31	1.93	2.13	1.93	2.13	ns
SSTL3_I	1.65	1.83	1.97	2.17	1.97	2.17	ns
SSTL3_II	1.65	1.83	2.15	2.35	2.15	2.35	ns
SSTL2_I	1.37	1.55	1.91	2.11	1.91	2.11	ns
SSTL2_II	1.37	1.55	2.00	2.20	2.00	2.20	ns
SSTL18_I	0.99	1.17	1.77	1.97	1.77	1.97	ns
SSTL18_II	1.00	1.18	1.80	2.00	1.80	2.00	ns
SSTL15_II	1.00	1.18	1.81	2.01	1.81	2.01	ns
DIFF_HSTL_I	1.01	1.19	1.91	2.11	1.91	2.11	ns
DIFF_HSTL_II	1.00	1.18	1.86	2.06	1.86	2.06	ns
DIFF_HSTL_III	1.00	1.18	1.83	2.03	1.83	2.03	ns
DIFF_HSTL_I_18	1.04	1.22	1.93	2.13	1.93	2.13	ns
DIFF_HSTL_II_18	1.04	1.22	1.83	2.03	1.83	2.03	ns
DIFF_HSTL_III_18	1.04	1.22	1.83	2.03	1.83	2.03	ns

Table 29: **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices[1] *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVCMOS33, Slow, 6 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVCMOS33, Slow, 8 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVCMOS33, Slow, 12 mA	1.41	1.59	2.53	2.73	2.53	2.73	ns
LVCMOS33, Slow, 16 mA	1.41	1.59	2.45	2.65	2.45	2.65	ns
LVCMOS33, Slow, 24 mA	1.41	1.59	2.42	2.62	2.42	2.62	ns
LVCMOS33, Fast, 2 mA	1.41	1.59	4.05	4.25	4.05	4.25	ns
LVCMOS33, Fast, 4 mA	1.41	1.59	2.66	2.86	2.66	2.86	ns
LVCMOS33, Fast, 6 mA	1.41	1.59	2.46	2.66	2.46	2.66	ns
LVCMOS33, Fast, 8 mA	1.41	1.59	2.21	2.41	2.21	2.41	ns
LVCMOS33, Fast, 12 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVCMOS33, Fast, 16 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVCMOS33, Fast, 24 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVCMOS25, QUIETIO, 2 mA	0.89	1.07	5.00	5.20	5.00	5.20	ns
LVCMOS25, QUIETIO, 4 mA	0.89	1.07	3.85	4.05	3.85	4.05	ns
LVCMOS25, QUIETIO, 6 mA	0.89	1.07	3.60	3.80	3.60	3.80	ns
LVCMOS25, QUIETIO, 8 mA	0.89	1.07	3.34	3.54	3.34	3.54	ns
LVCMOS25, QUIETIO, 12 mA	0.89	1.07	2.98	3.18	2.98	3.18	ns
LVCMOS25, QUIETIO, 16 mA	0.89	1.07	2.79	2.99	2.79	2.99	ns
LVCMOS25, QUIETIO, 24 mA	0.89	1.07	2.64	2.84	2.64	2.84	ns
LVCMOS25, Slow, 2 mA	0.89	1.07	3.96	4.16	3.96	4.16	ns
LVCMOS25, Slow, 4 mA	0.89	1.07	2.96	3.16	2.96	3.16	ns
LVCMOS25, Slow, 6 mA	0.89	1.07	2.88	3.08	2.88	3.08	ns
LVCMOS25, Slow, 8 mA	0.89	1.07	2.63	2.83	2.63	2.83	ns
LVCMOS25, Slow, 12 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVCMOS25, Slow, 16 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVCMOS25, Slow, 24 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVCMOS25, Fast, 2 mA	0.89	1.07	3.52	3.72	3.52	3.72	ns
LVCMOS25, Fast, 4 mA	0.89	1.07	2.43	2.63	2.43	2.63	ns
LVCMOS25, Fast, 6 mA	0.89	1.07	2.23	2.43	2.23	2.43	ns
LVCMOS25, Fast, 8 mA	0.89	1.07	2.16	2.36	2.16	2.36	ns
LVCMOS25, Fast, 12 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVCMOS25, Fast, 16 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVCMOS25, Fast, 24 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVCMOS18, QUIETIO, 2 mA	1.25	1.43	6.11	6.31	6.11	6.31	ns
LVCMOS18, QUIETIO, 4 mA	1.25	1.43	4.88	5.08	4.88	5.08	ns
LVCMOS18, QUIETIO, 6 mA	1.25	1.43	4.20	4.40	4.20	4.40	ns
LVCMOS18, QUIETIO, 8 mA	1.25	1.43	3.86	4.06	3.86	4.06	ns
LVCMOS18, QUIETIO, 12 mA	1.25	1.43	3.49	3.69	3.49	3.69	ns

I/O Standard Measurement Methodology

Input Delay Measurements

Table 31 shows the test setup parameters used for measuring input delay.

Table 31: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L[1]	V_H[1]	V_{MEAS}[3][4]	V_{REF}[2][4]
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	0	3.0	1.4	–
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	0	3.3	1.65	–
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
LVCMOS, 1.2V	LVCMOS12	0	1.2	0.6	–
PCI (Peripheral Component Interface), 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3	Per PCI Specification			–
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III	HSTL_III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.1
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
SSTL, Class II, 1.5V	SSTL15_II	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	1.25 – 0.125	1.25 + 0.125	0[5]	–
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V & 3.3V	LVPECL_25, LVPECL_33	1.2 – 0.3	1.2 + 0.3	0[5]	–
BLVDS (Bus LVDS), 2.5V	BLVDS_25	1.3 – 0.125	1.3 + 0.125	0[5]	–
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	1.2 – 0.125	1.2 + 0.125	0[5]	–
RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RSDS_25, RSDS_33	1.2 – 0.1	1.2 + 0.1	0[5]	–
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	3.0 – 0.1	3.0 + 0.1	0[5]	–
PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V	PPDS_25, PPDS_33	1.25 – 0.1	1.25 + 0.1	0[5]	–

Notes:
1. Input waveform switches between V_L and V_H.
2. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 4.
5. The value given is the differential input voltage.

Table 33: **Spartan-6 FPGA V_{CCO}/GND Pairs per Bank**

Package	Devices	Description	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5
TQG144	LX	V_{CCO}/GND Pairs	3	3	2	3	N/A	N/A
		Maximum I/O per Pair	8	8	13	8	N/A	N/A
CPG196	LX	VCCO/GND Pairs	4	6	4	6	N/A	N/A
		Maximum I/O per Pair	6	4	7	4	N/A	N/A
CSG225	LX	V_{CCO}/GND Pairs	4	4	4	4	N/A	N/A
		Maximum I/O per Pair	10	10	9	10	N/A	N/A
FT(G)256	LX	V_{CCO}/GND Pairs	5	6	4	5	N/A	N/A
		Maximum I/O per Pair	8	9	9	10	N/A	N/A
CSG324	LX	V_{CCO}/GND Pairs	6	6	6	6	N/A	N/A
		Maximum I/O per Pair	10	9	10	9	N/A	N/A
	LXT	V_{CCO}/GND Pairs	4	6	6	6	N/A	N/A
		Maximum I/O per Pair	4	9	10	9	N/A	N/A
CS(G)484	LX	V_{CCO}/GND Pairs	8	13	8	13	N/A	N/A
		Maximum I/O per Pair	7	8	7	8	N/A	N/A
	LXT	V_{CCO}/GND Pairs	7	12	8	13	N/A	N/A
		Maximum I/O per Pair	5	8	6	8	N/A	N/A
FG(G)484	LX	V_{CCO}/GND Pairs	10	10	11	11	N/A	N/A
		Maximum I/O per Pair	6	8	9	8	N/A	N/A
	LXT	V_{CCO}/GND Pairs	6	10	11	10	N/A	N/A
		Maximum I/O per Pair	7	8	7	8	N/A	N/A
FG(G)676	LX45	V_{CCO}/GND Pairs	12	15	10	16	N/A	N/A
		Maximum I/O per Pair	3	7	8	7	N/A	N/A
	LX75, LX100, LX150	V_{CCO}/GND Pairs	12	9	10	10	6	6
		Maximum I/O per Pair	9	10	9	9	8	9
	LXT	V_{CCO}/GND Pairs	10	8	10	8	7	7
		Maximum I/O per Pair	8	7	8	8	7	7
FG(G)900	LX	V_{CCO}/GND Pairs	17	14	17	14	7	8
		Maximum I/O per Pair	7	6	7	8	7	6
	LXT	V_{CCO}/GND Pairs	15	14	13	14	7	8
		Maximum I/O per Pair	7	6	8	8	7	6

CLB Switching Characteristics (SLICEM Only)

Table 40: **CLB Switching Characteristics (SLICEM Only)**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Combinatorial Delays						
T_{ILO}	An – Dn LUT inputs to A to D outputs	0.21	0.26	0.26	0.46	ns, Max
	An – Dn LUT inputs through F7AMUX/F7BMUX to AMUX/CMUX output	0.37	0.43	0.43	0.77	ns, Max
T_{OPAB}	An – Dn LUT inputs through F7AMUX or F7BMUX and F8MUX to BMUX output	0.37	0.46	0.46	0.84	ns, Max
T_{ITO}	An – Dn LUT inputs through latch to AQ – DQ outputs	0.82	0.95	0.95	1.64	ns, Max
T_{TITO_LOGIC}	An – Dn LUT inputs to AQ – DQ outputs (latch as logic)	0.82	0.95	0.95	1.64	ns, Max
T_{OPCYA}	An LUT inputs to COUT output	0.38	0.48	0.48	0.69	ns, Max
T_{OPCYB}	Bn LUT inputs to COUT output	0.38	0.49	0.49	0.71	ns, Max
T_{OPCYC}	Cn LUT inputs to COUT output	0.28	0.33	0.33	0.55	ns, Max
T_{OPCYD}	Dn LUT inputs to COUT output	0.28	0.35	0.35	0.52	ns, Max
T_{AXCY}	AX input to COUT output	0.21	0.26	0.26	0.36	ns, Max
T_{BXCY}	BX input to COUT output	0.13	0.16	0.16	0.18	ns, Max
T_{CXCY}	CX input to COUT output	0.10	0.12	0.12	0.09	ns, Max
T_{DXCY}	DX input to COUT output	0.09	0.11	0.11	0.09	ns, Max
T_{BYP}	CIN input to COUT output	0.08	0.10	0.10	0.06	ns, Max
T_{CINA}	CIN input to AMUX output	0.21	0.22	0.22	0.47	ns, Max
T_{CINB}	CIN input to BMUX output	0.30	0.31	0.31	0.57	ns, Max
T_{CINC}	CIN input to CMUX output	0.29	0.31	0.31	0.58	ns, Max
T_{CIND}	CIN input to DMUX output	0.31	0.32	0.32	0.68	ns, Max
Sequential Delays						
T_{CKO}	Clock to AQ – DQ outputs	0.45	0.53	0.53	0.74	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{DICK}/T_{CKDI}	AX – DX input to CLK on A – D flip-flops	0.42/ 0.28	0.47/ 0.39	0.47/ 0.39	0.90/ 0.56	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK on A – D flip-flops	0.31/ –0.07	0.37/ –0.07	0.37/ –0.07	0.59/ –0.27	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D flip-flops for XC devices	0.41/ 0.02	0.42/ 0.02	0.42/ 0.02	0.68/ –0.29	ns, Min
	SR input to CLK on A – D flip-flops for XA and XQ devices	0.41/ 0.02	N/A	0.44/ 0.02	0.68/ –0.29	ns, Min
T_{CINCK}/T_{CKCIN}	CIN input to CLK on A – D flip-flops	0.31/ –0.17	0.31/ –0.13	0.31/ –0.13	0.81/ –0.42	ns, Min
Set/Reset						
T_{RPW}	SR input minimum pulse width	0.41	0.48	0.48	1.37	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.60	0.70	0.70	0.88	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.60	0.65	0.65	0.90	ns, Max
F_{TOG}	Toggle frequency (for export control)	862	806	667	500	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 41: **CLB Distributed RAM Switching Characteristics (SLICEM Only)**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Sequential Delays						
T_{SHCKO}	Clock to A – D outputs	1.26	1.55	1.55	2.35	ns, Max
	Clock to A – D outputs (direct output path)	0.96	1.20	1.20	1.87	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS}/T_{DH}	AX – DX or AI – DI inputs to CLK	0.59/ 0.17	0.73/ 0.22	0.73/ 0.22	1.17/ 0.33	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock for XC devices	0.28/ 0.35	0.32/ 0.42	0.32/ 0.42	0.26/ 0.71	ns, Min
	Address An inputs to clock for XA and XQ devices	0.28/ 0.51	N/A	0.32/ 0.51	0.26/ 0.71	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.31/ –0.08	0.37/ –0.08	0.37/ –0.08	0.59/ –0.27	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.31/ –0.08	0.37/ –0.08	0.37/ –0.08	0.59/ –0.27	ns, Min

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 42: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	1.35	1.78	1.78	2.74	ns, Max
	Clock to A – D outputs (direct output path)	1.24	1.65	1.65	2.48	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS}/T_{WH}	WE input to CLK	0.20/ –0.07	0.24/ –0.07	0.24/ –0.07	0.29/ –0.27	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK for XC devices	0.30/ 0.30	0.30/ 0.38	0.30/ 0.38	0.82/ –0.41	ns, Min
	CE input to CLK for XA and XQ devices	0.32/ 0.30	N/A	0.40/ 0.38	0.82/ –0.41	ns, Min
T_{DS}/T_{DH}	AX – DX or AI – DI inputs to CLK	0.07/ 0.11	0.09/ 0.14	0.09/ 0.14	0.11/ 0.23	ns, Min

Table 47: **Configuration Switching Characteristics[1] *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
BPI Master Flash Mode Programming Switching[4]						
T_{BPICCO}[5]	A[25:0], FCS_B, FOE_B, FWE_B, LDC outputs valid after CCLK falling edge	15	15	15	20	ns, Max
$T_{BPIICCK}$	Master BPI CCLK (output) delay	10/100	10/100	10/100	10/130	µs, Min/Max
T_{BPIDCC}/T_{BPICCD}	Setup/Hold on D[15:0] data input pins	5.0/1.0	5.0/1.0	5.0/1.0	6.0/2.0	ns, Min
SPI Master Flash Mode Programming Switching[6]						
$T_{SPIDCC}/T_{SPIDCCD}$	DIN, MISO0, MISO1, MISO2, MISO3, Setup/Hold before/after the rising CCLK edge	5.0/1.0	5.0/1.0	5.0/1.0	7.0/1.0	ns, Min
$T_{SPIICCK}$	Master SPI CCLK (output) delay	0.4/7.0	0.4/7.0	0.4/7.0	0.4/10.0	µs, Min/Max
T_{SPICCM}	MOSI clock to out	13	13	13	19	ns, Max
$T_{SPICCFC}$	CSO_B clock to out	16	16	16	26	ns, Max
CCLK Output (Master Modes)						
T_{MCCKL}	Master CCLK clock duty cycle Low	40/60				%, Min/Max
T_{MCCKH}	Master CCLK clock duty cycle High	40/60				%, Min/Max
F_{MCCK}	Maximum frequency, serial mode (Master Serial/SPI) All devices	40	40	40	30	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T	40	40	40	25	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x8 mode, LX150, and LX150T	40	40	40	20	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x16 mode	35	35	35	20	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode	±50	±50	±50	±50	%
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time	5	5	5	8	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	5	5	5	8	ns, Min
USERCCLK Input						
$T_{USERCCLKL}$	USERCCLK clock minimum Low time	12	12	12	16	ns, Min
$T_{USERCCLKH}$	USERCCLK clock minimum High time	12	12	12	16	ns, Min
$F_{USERCCLK}$	Maximum USERCCLK frequency	40	40	40	30	MHz, Max

Notes:

1. Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
2. To support longer delays in configuration, use the design solutions described in UG380: *Spartan-6 FPGA Configuration User Guide*.
3. Table 6 specifies the power supply ramp time.
4. BPI mode is not supported in:
   - LX4, LX25, or LX25T devices
   - LX9 devices in the TQG144 package
   - LX9 or LX16 devices in the CPG196 package.
5. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
6. Defense-grade Spartan-6Q -2Q devices configure in single default SPI Master (x1) mode at T_j = –55°C. During operation and when using all other configuration functions, the minimum operating temperature is –40°C.

Table 52: **PLL Specification *(Cont'd)***

Symbol	Description	Device[1]	Speed Grade				Units
			-3	-3N	-2	-1L	
F_{INMIN}	Minimum Input Clock Frequency	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter: 19–200 MHz	All	1 ns Maximum				
	Maximum Input Clock Period Jitter: > 200 MHz	All	<20% of clock input period Maximum				
F_{INDUTY}	Allowable Input Duty Cycle: 19—199 MHz	All	25/75				%
	Allowable Input Duty Cycle: 200—299 MHz	All	35/65				%
	Allowable Input Duty Cycle: > 300 MHz	All	45/55				%
F_{VCOMIN}	Minimum PLL VCO Frequency	LX devices	400	400	400	400	MHz
		LXT devices	400	400	400	N/A	MHz
F_{VCOMAX}	Maximum PLL VCO Frequency	LX devices	1080	1050	1000	1000	MHz
		LXT devices	1080	1050	1000	N/A	MHz
$F_{BANDWIDTH}$	Low PLL Bandwidth at Typical[3]	All	1	1	1	1	MHz
	High PLL Bandwidth at Typical[3]	All	4	4	4	4	MHz
$T_{STAPHAOFFSET}$	Static Phase Offset of the PLL Outputs	All	0.12	0.12	0.12	0.15	ns
$T_{OUTJITTER}$	PLL Output Jitter[3]	All	Note 2				
$T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision[4]	All	0.15	0.15	0.20	0.25	ns
$T_{LOCKMAX}$	PLL Maximum Lock Time	All	100	100	100	100	µs
F_{OUTMAX}	PLL Maximum Output Frequency for BUFGMUX	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz
	PLL Maximum Output Frequency for BUFPLL	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz
F_{OUTMIN}	PLL Minimum Output Frequency[5]	All	3.125	3.125	3.125	3.125	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation: 19–200 MHz	All	1 ns Maximum				
	External Clock Feedback Variation: > 200 MHz	All	< 20% of clock input period Maximum				
$RST_{MINPULSE}$	Minimum Reset Pulse Width	All	5	5	5	5	ns
F_{PFDMAX}[5]	Maximum Frequency at the Phase Frequency Detector	LX devices	500	500	400	300	MHz
		LXT devices	500	500	400	N/A	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	All	3 ns Max or one CLKIN cycle				

Notes:

1. LXT devices are not available with a -1L speed grade.
2. Values for this parameter are available in the Clocking Wizard.
3. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When using CLK_FEEDBACK = CLKOUT0 with BUFIO2 feedback, the feedback frequency will be higher than the phase frequency detector frequency. $F_{PFDMAX} = F_{CLKFB}$ / CLKFBOUT_MULT

DCM Switching Characteristics

Table 53: **Operating Frequency Ranges and Conditions for the Delay-Locked Loop (DLL)[1]**

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Input Frequency Ranges										
CLKIN_FREQ_DLL	Frequency of the CLKIN clock input when the CLKDV output is not used.	5[2]	280[3]	5[2]	280[3]	5[2]	250[3]	5[2]	175[3]	MHz
	Frequency of the CLKIN clock input when using the CLKDV output.	5[2]	280[3]	5[2]	280[3]	5[2]	250[3]	5[2]	133[3]	MHz
Input Pulse Requirements										
CLKIN_PULSE	CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL < 150 MHz	40	60	40	60	40	60	40	60	%
	CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL > 150 MHz	45	55	45	55	45	55	45	55	%
Input Clock Jitter Tolerance and Delay Path Variation[4]										
CLKIN_CYC_JITT_DLL_LF	Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL < 150 MHz	–	±300	–	±300	–	±300	–	±300	ps
CLKIN_CYC_JITT_DLL_HF	Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL > 150 MHz.	–	±150	–	±150	–	±150	–	±150	ps
CLKIN_PER_JITT_DLL	Period jitter at the CLKIN input.	–	±1	–	±1	–	±1	–	±1	ns
CLKFB_DELAY_VAR_EXT	Allowable variation of the off-chip feedback delay from the DCM output to the CLKFB input.	–	±1	–	±1	–	±1	–	±1	ns

Notes:
1. DLL specifications apply when using any of the DLL outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV.
2. When operating independently of the DLL, the DFS supports lower CLKIN_FREQ_DLL frequencies. See Table 55.
3. The CLKIN_DIVIDE_BY_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the F_{MAX} (see Table 48 and Table 49 for BUFG and BUFIO2 limits). When used with CLK_FEEDBACK=2X, the input clock frequency matches the frequency for CLK2X, and is limited to CLKOUT_FREQ_2X.
4. CLKIN_FREQ_DLL input jitter beyond these limits can cause the DCM to lose LOCK, indicated by the LOCKED output deasserting. The user must then reset the DCM.
5. When using both DCMs in a CMT, both DCMs must be LOCKED.

Table 68: **Global Clock Input to Output Delay With DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.							
$T_{ICKOFDCM\_PLL}$	Global Clock and OUTFF with DCM and PLL	XC6SLX4	4.78	N/A	6.32	7.09	ns
		XC6SLX9	4.78	5.24	6.32	7.09	ns
		XC6SLX16	4.70	5.12	5.94	6.63	ns
		XC6SLX25	4.70	5.09	5.92	7.30	ns
		XC6SLX25T	4.70	5.09	5.92	N/A	ns
		XC6SLX45	4.63	4.98	5.83	7.26	ns
		XC6SLX45T	4.63	4.98	5.83	N/A	ns
		XC6SLX75	4.68	5.04	5.88	6.90	ns
		XC6SLX75T	4.68	5.04	5.88	N/A	ns
		XC6SLX100	4.72	5.07	5.92	7.77	ns
		XC6SLX100T	4.76	5.07	5.92	N/A	ns
		XC6SLX150	4.44	4.73	5.31	6.96	ns
		XC6SLX150T	4.44	4.73	5.31	N/A	ns
		XA6SLX4	5.07	N/A	6.18	N/A	ns
		XA6SLX9	5.07	N/A	6.18	N/A	ns
		XA6SLX16	5.22	N/A	5.77	N/A	ns
		XA6SLX25	5.01	N/A	5.80	N/A	ns
		XA6SLX25T	5.01	N/A	5.90	N/A	ns
		XA6SLX45	4.93	N/A	5.67	N/A	ns
		XA6SLX45T	4.93	N/A	5.67	N/A	ns
		XA6SLX75	4.94	N/A	5.70	N/A	ns
		XA6SLX75T	4.94	N/A	5.70	N/A	ns
		XA6SLX100	N/A	N/A	5.77	N/A	ns
		XQ6SLX75	N/A	N/A	5.70	6.90	ns
		XQ6SLX75T	4.94	N/A	5.70	N/A	ns
		XQ6SLX150	N/A	N/A	5.31	6.96	ns
		XQ6SLX150T	5.02	N/A	5.31	N/A	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 71: **Global Clock Setup and Hold Without DCM or PLL (Default Delay)**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSFD}/ T_{PHFD}	Default Delay(2) Global Clock and IFF(3) without DCM or PLL	XC6SLX4	0.66/1.17	N/A	1.05/0.79	2.09/1.05	ns
		XC6SLX9	0.66/1.17	0.75/1.17	1.05/1.17	2.09/1.05	ns
		XC6SLX16	0.87/1.16	0.93/1.16	0.96/1.16	1.86/1.06	ns
		XC6SLX25	0.68/0.77	0.81/0.81	0.87/0.82	2.21/1.33	ns
		XC6SLX25T	0.68/0.77	0.81/0.81	0.87/0.82	N/A	ns
		XC6SLX45	0.40/1.05	0.42/1.17	0.64/1.20	1.61/1.67	ns
		XC6SLX45T	0.40/1.05	0.42/1.17	0.64/1.20	N/A	ns
		XC6SLX75	0.41/1.11	0.41/1.13	0.80/1.14	1.23/1.82	ns
		XC6SLX75T	0.41/1.11	0.41/1.13	0.80/1.14	N/A	ns
		XC6SLX100	0.39/1.12	0.39/1.23	0.39/1.28	1.13/1.94	ns
		XC6SLX100T	0.39/1.12	0.39/1.23	0.39/1.28	N/A	ns
		XC6SLX150	0.23/1.54	0.23/1.62	0.23/1.62	1.14/2.05	ns
		XC6SLX150T	0.23/1.54	0.23/1.62	0.23/1.62	N/A	ns
		XA6SLX4	0.73/1.18	N/A	1.05/0.80	N/A	ns
		XA6SLX9	0.73/1.18	N/A	1.05/0.80	N/A	ns
		XA6SLX16	0.90/1.20	N/A	0.96/0.75	N/A	ns
		XA6SLX25	0.70/0.81	N/A	0.87/0.91	N/A	ns
		XA6SLX25T	0.76/0.81	N/A	1.03/0.91	N/A	ns
		XA6SLX45	0.40/1.06	N/A	0.64/1.20	N/A	ns
		XA6SLX45T	0.40/1.06	N/A	0.64/1.20	N/A	ns
		XA6SLX75	0.41/1.24	N/A	0.80/1.18	N/A	ns
		XA6SLX75T	0.41/1.24	N/A	0.80/1.18	N/A	ns
		XA6SLX100	N/A	N/A	0.86/1.55	N/A	ns
		XQ6SLX75	N/A	N/A	0.80/1.18	1.23/1.82	ns
		XQ6SLX75T	0.41/1.24	N/A	0.80/1.18	N/A	ns
		XQ6SLX150	N/A	N/A	0.28/1.57	1.14/2.05	ns
		XQ6SLX150T	0.28/1.78	N/A	0.28/1.57	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Default delay uses IODELAY2 tap 0.
3. IFF = Input Flip-Flop or Latch.

Table 74: **Global Clock Setup and Hold With PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSPLL}/ T_{PHPLL}	No Delay Global Clock and IFF(2) with PLL in System-Synchronous Mode	XC6SLX4	1.37/0.25	N/A	1.52/0.41	2.07/0.69	ns
		XC6SLX9	1.37/0.21	1.48/0.21	1.52/0.26	2.07/0.69	ns
		XC6SLX16	1.33/–0.03	1.53/–0.02	1.60/–0.02	1.57/0.48	ns
		XC6SLX25	1.65/0.28	1.71/0.28	1.91/0.28	2.44/0.76	ns
		XC6SLX25T	1.65/0.28	1.71/0.28	1.91/0.28	N/A	ns
		XC6SLX45	1.55/0.18	1.64/0.18	1.75/0.18	2.02/0.90	ns
		XC6SLX45T	1.55/0.18	1.64/0.18	1.75/0.18	N/A	ns
		XC6SLX75	1.77/0.21	1.89/0.21	2.13/0.21	2.46/0.53	ns
		XC6SLX75T	1.77/0.21	1.89/0.21	2.13/0.21	N/A	ns
		XC6SLX100	1.44/0.32	1.52/0.32	1.70/0.32	1.78/0.86	ns
		XC6SLX100T	1.44/0.32	1.52/0.32	1.70/0.32	N/A	ns
		XC6SLX150	1.39/0.49	1.48/0.49	1.67/0.49	1.94/0.94	ns
		XC6SLX150T	1.39/0.49	1.48/0.49	1.67/0.49	N/A	ns
		XA6SLX4	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX9	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX16	1.89/–0.08	N/A	1.72/–0.08	N/A	ns
		XA6SLX25	1.85/0.16	N/A	2.08/0.16	N/A	ns
		XA6SLX25T	1.85/0.16	N/A	2.17/0.16	N/A	ns
		XA6SLX45	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX45T	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX75	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX100	N/A	N/A	2.34/0.14	N/A	ns
		XQ6SLX75	N/A	N/A	2.25/0.06	2.46/0.53	ns
		XQ6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XQ6SLX150	N/A	N/A	1.79/0.37	1.94/0.94	ns
		XQ6SLX150T	1.43/0.37	N/A	1.79/0.37	N/A	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 79: **Package Skew *(Cont'd)***

Symbol	Description	Device	Package[2]	Value	Units
$T_{PKGSKEW}$	Package Skew[1]	LX45	CSG324	70	ps
			CS(G)484	99	ps
			FG(G)484	109	ps
			FG(G)676	138	ps
		LX45T	CSG324	75	ps
			CS(G)484	100	ps
			FG(G)484	95	ps
		LX75	CS(G)484	101	ps
			FG(G)484	107	ps
			FG(G)676	161	ps
		LX75T	CS(G)484	107	ps
			FG(G)484	110	ps
			FG(G)676	134	ps
		LX100	CS(G)484	95	ps
			FG(G)484	155	ps
			FG(G)676	144	ps
		LX100T	CS(G)484	88	ps
			FG(G)484	111	ps
			FG(G)676	147	ps
			FG(G)900	134	ps
		LX150	CS(G)484	84	ps
			FG(G)484	103	ps
			FG(G)676	115	ps
			FG(G)900	121	ps
		LX150T	CS(G)484	83	ps
			FG(G)484	88	ps
			FG(G)676	141	ps
			FG(G)900	120	ps

Notes:
1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from Pad to Ball.
2. Some of the devices are available in both Pb and Pb-free (additional G) packages as standard ordering options. See DS160: *Spartan-6 Family Overview* for more information.

Table 80: **Sample Window**

Symbol	Description	Device[1]	Speed Grade				Units
			-3	-3N	-2	-1L	
T_{SAMP}	Sampling Error at Receiver Pins[2]	All	510	510	530	740	ps
T_{SAMP_BUFIO2}	Sampling Error at Receiver Pins using BUFIO2[3]	All	430	430	450	590	ps

Notes:
1. LXT devices are not available with a -1L speed grade.
2. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 DCM jitter
   - DCM accuracy (phase offset)
   - DCM phase shift resolution

   These measurements do not include package or clock tree skew.
3. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO2 clock network and IODELAY2 to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
08/26/09	1.1	Added V_{FS} to Table 1and Table 2. Added R_{FUSE} to Table 2. Added XC6SLX75 and XC6SLX75T to V_{BATT} and I_{BATT} in Table 1, Table 2, and Table 4. Corrected the quiescent supply current for the XC6SLX4 in Table 5. Updated Table 11. Removed DV_{PPIN} from Figure 2. Removed $F_{PCIECORE}$ from Table 24 and added values to $F_{PCIEUSER}$. Added more networking applications to Table 25. Updated values for $T_{SUSPENDLOW\_AWAKE}$, $T_{SUSPEND\_ENABLE}$, and T_{SCP_AWAKE} in Table 46. Numerous changes to Table 47, page 54 including the addition of new values to various specifications, revising the $T_{SMCKCSO}$ description, and changing the units of T_{POR}. Also, removed *Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK section* from Table 47 and updated all the notes. In Table 52, added to F_{INMAX}, revised F_{OUTMAX}, and removed PLL Maximum Output Frequency for BUFIO2. Revised values for DCM_DELAY_STEP in Table 54. Updated CLKIN_FREQ_FX values in Table 55.
01/04/10	1.2	Added -4 speed grade to entire document. Updated speed specification of -4, -3, -2 speed grades to version 1.03. Added -1L speed grade numbers per speed specification 1.00. Updated T_{SOL} in Table 1. Added -1L rows for LVCMOS12, LVCMOS15, and LVCMOS18 in Table 9. Revised much of the detail in GTP Transceiver Specifications in Table 12 through Table 23. Added -2 data to Table 25. Updated F_{MAX} in Table 44. Updated descriptions for $T_{DNACLKL}$ and $T_{DNACLKH}$ in Table 45 and revised values for all parameters. Removed $T_{INITADDR}$ from Table 47 and added new data. Updated values in Table 48 through Table 62. Added Table 51 (BUFPLL) and Table 57 (DCM_CLKGEN). Removed $T_{LOCKMAX}$ note from Table 52. Updated note 3 in Table 53. In Table 79: removed XC6SLX75CSG324 and XC6SLX75TCSG324; added XC6SLX75FG(G)484 and XC6SLX75FG(G)484.
02/22/10	1.3	Production release of XC6SLX16 -2 speed grade devices. The changes to Table 26 and Table 27 includes updating this data sheet to the data in ISE v11.5 software with speed specification v1.06. Updated maximum of V_{IN} and V_{TS} and note 2 in Table 1. In Table 2, changed V_{IN}, added I_{IN} and note 5, revised notes 1, 6, and 7, and added note 8 to R_{FUSE}. In Table 4, removed previous note 1 and added data to I_{RPU}, I_{RPD}, and I_{BATT}, changed C_{IN}, added R_{DT} and R_{IN_TERM}, and added note 2 and 3. Updated V_{CCO2} in Table 6. Added Table 7 and Table 8. Removed PCI66_3 from Table 9. Updated PCI33_3 and I2C in Table 9. Updated the description of Table 11. Completely updated Table 25. Updated Table 28 including adding values for PCI33_3. Updated V_{REF} value for HSTL_III_18 in Table 31. Updates missing V_{REF} values in Table 32. Added Simultaneously Switching Outputs, page 36. Removed T_{GSRQ} and T_{RPW} from Table 35 and Table 36. Also removed T_{DOQ} from Table 36. Removed T_{ISDO_DO} and note 1 from Table 37. Removed T_{OSCCK_S} and combinatorial section from Table 38. In Table 39, removed T_{IODDO_T} and added new tap parameters and note 2. In Table 40, Table 41, and Table 42, made typographical edits and removed notes. Removed clock CLK section in Table 41. Removed clock CLK section and T_{REG_MUX} and T_{REG_M31} in Table 42. Added block RAM F_{MAX} values to Table 43. Updated values and added note 2 to Table 45. Added values to Table 46 and removed note 1. Numerous changes to Table 47. Completely updated Table 57. Revised data in Table 62. Removed note 3 from Table 71. Added values to Table 79. Added data to Table 80 and Table 81.
03/10/10	1.4	Production release of XC6SLX45 -2 speed grade devices, which includes changes to Table 26 and Table 27 updating this data sheet to the data in ISE v11.5 software with speed specification v1.07. Fixed R_{IN_TERM} description in Table 4. Added PCI66_3 to Table 7 and replaced note 1. Corrected note 1 and the V, Max for TMDS_33 in Table 8. In Table 10, added note 1 to LVPECL_33 and TMDS_33. Also updated specifications for TMDS_33. Updated the GTP Transceiver Specifications section including adding values to Table 16, Table 17, and Table 20 through Table 23. Added PCI66_3 back into Table 9, Table 28, Table 31, Table 32, and Table 34. Updated note 3 on Table 32. In Table 34, corrected some typographical errors and fixed SSO limits for bank1/3 in FG(G)484 package. Corrected T_{OSCKC_OCE} in Table 38. In Table 57, updated CLKFX_FREEZE_VAR and CLKFX_FREEZE_TEMP_SLOPE and added typical values to $T_{CENTER\_LOW\_SPREAD}$ and $T_{CENTER\_HIGH\_SPREAD}$. Updated and added values to Table 63 through Table 78, and Table 81. In Table 79, revised the XC6SLX16-CSG324 and the XC6SLX45-CSG484 and FG(G)484 values.