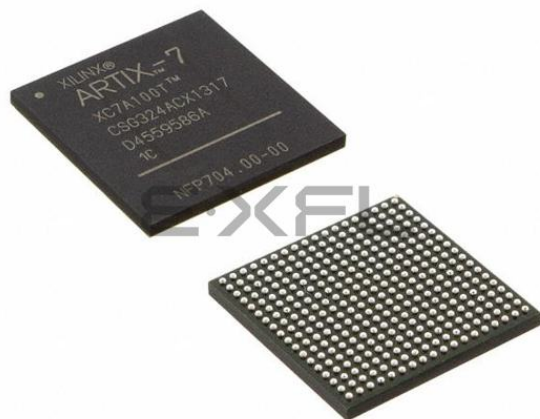




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	1879
Number of Logic Elements/Cells	24051
Total RAM Bits	958464
Number of I/O	226
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-LFBGA, CSPBGA
Supplier Device Package	324-CSPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx25-3csg324c

Table 5: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	LX4	2.5	2.5	2.5	2.5	mA
		LX9	2.5	2.5	2.5	2.5	mA
		LX16	3.0	3.0	3.0	3.0	mA
		LX25	4.0	4.0	4.0	4.0	mA
		LX25T	4.0	4.0	4.0	N/A	mA
		LX45	5.0	5.0	5.0	5.0	mA
		LX45T	5.0	5.0	5.0	N/A	mA
		LX75	7.0	7.0	7.0	7.0	mA
		LX75T	7.0	7.0	7.0	N/A	mA
		LX100	9.0	9.0	9.0	9.0	mA
		LX100T	9.0	9.0	9.0	N/A	mA
		LX150	12.0	12.0	12.0	12.0	mA
		LX150T	12.0	12.0	12.0	N/A	mA

Notes:

- Typical values are specified at nominal voltage, 25°C junction temperatures (T_j). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 25°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. Nominal V_{CCINT} is 1.20V; use the XPE tool to calculate 1.23V values for the nominal V_{CCINT} of the extended performance range.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- If differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 6: Power Supply Ramp Time

Symbol	Description	Speed Grade	Ramp Time	Units
V _{CCINTR}	Internal supply voltage ramp time	-3, -3N, -2	0.20 to 50.0	ms
		-1L	0.20 to 40.0	ms
V _{CCO2} ⁽¹⁾	Output drivers bank 2 supply voltage ramp time	All	0.20 to 50.0	ms
V _{CCAUXR}	Auxiliary supply voltage ramp time	All	0.20 to 50.0	ms

Notes:

- The minimum V_{CCO2} for power-on reset and configuration is 1.65V.
- Spartan-6 FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply. Use the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools to estimate current drain on these supplies. Spartan-6 devices do not have a required power-on sequence.

Table 10: Differential I/O Standard DC Input and Output Levels

I/O Standard	V _{ID}		V _{ICM}		V _{OD}		V _{OCM}		V _{OH}	V _{OL}
	mV, Min	mV, Max	V, Min	V, Max	mV, Min	mV, Max	V, Min	V, Max	V, Min	V, Max
LVDS_33 ⁽²⁾⁽³⁾	100	600	0.3	2.35	247	454	1.125	1.375	–	–
LVDS_25 ⁽²⁾⁽³⁾	100	600	0.3	2.35	247	454	1.125	1.375	–	–
BLVDS_25 ⁽²⁾⁽³⁾	100	–	0.3	2.35	240	460	Typical 50% V _{CCO}		–	–
MINI_LVDS_33	200	600	0.3	1.95	300	600	1.0	1.4	–	–
MINI_LVDS_25	200	600	0.3	1.95	300	600	1.0	1.4	–	–
LVPECL_33 ⁽²⁾⁽³⁾	100	1000	0.3	2.8 ⁽¹⁾	Inputs only					
LVPECL_25 ⁽²⁾⁽³⁾	100	1000	0.3	1.95	Inputs only					
RSDS_33 ⁽²⁾⁽³⁾	100	–	0.3	1.5	100	400	1.0	1.4	–	–
RSDS_25 ⁽²⁾⁽³⁾	100	–	0.3	1.5	100	400	1.0	1.4	–	–
TMDS_33	150	1200	2.7	3.23 ⁽¹⁾	400	800	V _{CCO} – 0.405	V _{CCO} – 0.190	–	–
PPDS_33 ⁽²⁾⁽³⁾	100	400	0.2	2.3	100	400	0.5	1.4	–	–
PPDS_25 ⁽²⁾⁽³⁾	100	400	0.2	2.3	100	400	0.5	1.4	–	–
DISPLAY_PORT	190	1260	0.3	2.35	–	–	Typical 50% V _{CCO}		–	–
DIFF_MOBILE_DDR	100	–	0.78	1.02	–	–	–	–	90% V _{CCO}	10% V _{CCO}
DIFF_HSTL_I	100	–	0.68	0.9	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_HSTL_II	100	–	0.68	0.9	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_HSTL_III	100	–	0.68	0.9	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_HSTL_I_18	100	–	0.8	1.1	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_HSTL_II_18	100	–	0.8	1.1	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_HSTL_III_18	100	–	0.8	1.1	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_SSTL3_I	100	–	1.0	1.9	–	–	–	–	V _{TT} + 0.6	V _{TT} – 0.6
DIFF_SSTL3_II	100	–	1.0	1.9	–	–	–	–	V _{TT} + 0.8	V _{TT} – 0.8
DIFF_SSTL2_I	100	–	1.0	1.5	–	–	–	–	V _{TT} + 0.61	V _{TT} – 0.61
DIFF_SSTL2_II	100	–	1.0	1.5	–	–	–	–	V _{TT} + 0.81	V _{TT} – 0.81
DIFF_SSTL18_I	100	–	0.7	1.1	–	–	–	–	V _{TT} + 0.47	V _{TT} – 0.47
DIFF_SSTL18_II	100	–	0.7	1.1	–	–	–	–	V _{TT} + 0.6	V _{TT} – 0.6
DIFF_SSTL15_II	100	–	0.55	0.95	–	–	–	–	V _{TT} + 0.4	V _{TT} – 0.4

Notes:

1. LVPECL_33 and TMDS_33 maximum V_{ICM} is the lower of V (maximum) or V_{CCAUX} – (V_{ID}/2)
2. When V_{CCAUX} = 3.3V, the DCD can be higher than 5% for V_{ICM} < 0.7V when using these I/O standards: LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, LVPECL_33, RSDS_25, RSDS_33, PPDS_25, and PPDS_33.
3. The -1L devices require V_{CCAUX} = 2.5V when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.20 for -3, -3N, and -2; and v1.08 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

The -1L speed grade refers to the lower-power Spartan-6 devices. The -3N speed grade refers to the Spartan-6 devices that do not support MCB functionality.

[Table 26](#) correlates the current status of each Spartan-6 device on a per speed grade basis.

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-6 devices.

Table 26: Spartan-6 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6SLX4 ⁽¹⁾			-3, -2, -1L
XC6SLX9			-3, -3N, -2, -1L
XC6SLX16			-3, -3N, -2, -1L
XC6SLX25			-3, -3N, -2, -1L
XC6SLX25T			-3, -3N, -2
XC6SLX45			-3, -3N, -2, -1L
XC6SLX45T			-3, -3N, -2
XC6SLX75			-3, -3N, -2, -1L
XC6SLX75T			-3, -3N, -2
XC6SLX100			-3, -3N, -2, -1L
XC6SLX100T			-3, -3N, -2
XC6SLX150			-3, -3N, -2, -1L
XC6SLX150T			-3, -3N, -2
XA6SLX4			-3, -2
XA6SLX9			-3, -2
XA6SLX16			-3, -2
XA6SLX25			-3, -2
XA6SLX25T			-3, -2
XA6SLX45			-3, -2
XA6SLX45T			-3, -2
XA6SLX75			-3, -2
XA6SLX75T			-3, -2
XA6SLX100			-2
XQ6SLX75			-2, -1L
XQ6SLX75T			-3, -2
XQ6SLX150			-2, -1L
XQ6SLX150T			-3, -2

Notes:

1. The XC6SLX4 is not available in the -3N speed grade.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. [Table 27](#) lists the production released Spartan-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE® software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 27: Spartan-6 Device Production Software and Speed Specification Release⁽¹⁾

Device	Speed Grade Designations ⁽²⁾			
	-3 ⁽³⁾	-3N	-2 ⁽⁴⁾	-1L
XC6SLX4	ISE 12.4 v1.15	N/A	ISE 12.3 v1.12 ⁽⁵⁾	ISE 13.2 v1.07
XC6SLX9	ISE 12.4 v1.15	ISE 13.1 Update v1.18 ⁽⁷⁾	ISE 12.3 v1.12 ⁽⁵⁾	ISE 13.2 v1.07
XC6SLX16	ISE 12.1 v1.08	ISE 13.1 Update v1.18 ⁽⁷⁾	ISE 11.5 v1.06	ISE 13.2 v1.07
XC6SLX25	ISE 12.2 v1.11 ⁽⁶⁾	ISE 13.1 Update v1.18 ⁽⁷⁾	ISE 12.2 v1.11 ⁽⁶⁾	ISE 13.2 v1.07
XC6SLX25T	ISE 12.2 v1.11 ⁽⁶⁾	ISE 13.1 Update v1.18 ⁽⁷⁾	ISE 12.2 v1.11 ⁽⁶⁾	N/A
XC6SLX45	ISE 12.1 v1.08	ISE 13.1 Update v1.18 ⁽⁷⁾	ISE 11.5 v1.07	ISE 13.1 v1.06
XC6SLX45T	ISE 12.1 v1.08	ISE 13.1 Update v1.18 ⁽⁷⁾	ISE 12.1 v1.08	N/A
XC6SLX75	ISE 12.2 v1.11 ⁽⁶⁾	ISE 13.1 Update v1.18 ⁽⁷⁾	ISE 12.2 v1.11 ⁽⁶⁾	ISE 13.2 v1.07
XC6SLX75T	ISE 12.2 v1.11 ⁽⁶⁾	ISE 13.1 Update v1.18 ⁽⁷⁾	ISE 12.2 v1.11 ⁽⁶⁾	N/A
XC6SLX100	ISE 12.2 v1.11 ⁽⁶⁾	ISE 13.1 Update v1.18 ⁽⁷⁾	ISE 12.2 v1.11 ⁽⁶⁾	ISE 13.1 v1.06
XC6SLX100T	ISE 12.2 v1.11 ⁽⁶⁾	ISE 13.1 Update v1.18 ⁽⁷⁾	ISE 12.2 v1.11 ⁽⁶⁾	N/A
XC6SLX150	ISE 12.2 v1.11 ⁽⁶⁾	ISE 13.1 Update v1.18 ⁽⁷⁾	ISE 12.2 v1.11 ⁽⁶⁾	ISE 13.1 v1.06
XC6SLX150T	ISE 12.2 v1.11 ⁽⁶⁾	ISE 13.1 Update v1.18 ⁽⁷⁾	ISE 12.2 v1.11 ⁽⁶⁾	N/A
XA6SLX4	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX9	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX16	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX25	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX25T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX45	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX45T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX75	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX75T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX100	N/A	N/A	ISE 13.3 v1.20	N/A

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVC MOS18, Slow, 24 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVC MOS18, Fast, 2 mA	1.18	1.30	1.43	2.04	3.59	3.73	3.93	4.53	3.59	3.73	3.93	4.53	ns
LVC MOS18, Fast, 4 mA	1.18	1.30	1.43	2.04	2.39	2.53	2.73	3.35	2.39	2.53	2.73	3.35	ns
LVC MOS18, Fast, 6 mA	1.18	1.30	1.43	2.04	1.88	2.02	2.22	2.84	1.88	2.02	2.22	2.84	ns
LVC MOS18, Fast, 8 mA	1.18	1.30	1.43	2.04	1.81	1.95	2.15	2.77	1.81	1.95	2.15	2.77	ns
LVC MOS18, Fast, 12 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVC MOS18, Fast, 16 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVC MOS18, Fast, 24 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVC MOS18_JEDEC, QUIETIO, 2 mA	0.94	1.06	1.19	1.41	5.91	6.05	6.25	6.79	5.91	6.05	6.25	6.79	ns
LVC MOS18_JEDEC, QUIETIO, 4 mA	0.94	1.06	1.19	1.41	4.75	4.89	5.09	5.64	4.75	4.89	5.09	5.64	ns
LVC MOS18_JEDEC, QUIETIO, 6 mA	0.94	1.06	1.19	1.41	4.04	4.18	4.38	4.96	4.04	4.18	4.38	4.96	ns
LVC MOS18_JEDEC, QUIETIO, 8 mA	0.94	1.06	1.19	1.41	3.71	3.85	4.05	4.62	3.71	3.85	4.05	4.62	ns
LVC MOS18_JEDEC, QUIETIO, 12 mA	0.94	1.06	1.19	1.41	3.35	3.49	3.69	4.28	3.35	3.49	3.69	4.28	ns
LVC MOS18_JEDEC, QUIETIO, 16 mA	0.94	1.06	1.19	1.41	3.20	3.34	3.54	4.13	3.20	3.34	3.54	4.13	ns
LVC MOS18_JEDEC, QUIETIO, 24 mA	0.94	1.06	1.19	1.41	2.96	3.10	3.30	3.98	2.96	3.10	3.30	3.98	ns
LVC MOS18_JEDEC, Slow, 2 mA	0.94	1.06	1.19	1.41	4.59	4.73	4.93	5.54	4.59	4.73	4.93	5.54	ns
LVC MOS18_JEDEC, Slow, 4 mA	0.94	1.06	1.19	1.41	3.69	3.83	4.03	4.60	3.69	3.83	4.03	4.60	ns
LVC MOS18_JEDEC, Slow, 6 mA	0.94	1.06	1.19	1.41	3.00	3.14	3.34	3.94	3.00	3.14	3.34	3.94	ns
LVC MOS18_JEDEC, Slow, 8 mA	0.94	1.06	1.19	1.41	2.19	2.33	2.53	3.18	2.19	2.33	2.53	3.18	ns
LVC MOS18_JEDEC, Slow, 12 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVC MOS18_JEDEC, Slow, 16 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVC MOS18_JEDEC, Slow, 24 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVC MOS18_JEDEC, Fast, 2 mA	0.94	1.06	1.19	1.41	3.57	3.71	3.91	4.52	3.57	3.71	3.91	4.52	ns
LVC MOS18_JEDEC, Fast, 4 mA	0.94	1.06	1.19	1.41	2.39	2.53	2.73	3.35	2.39	2.53	2.73	3.35	ns
LVC MOS18_JEDEC, Fast, 6 mA	0.94	1.06	1.19	1.41	1.88	2.02	2.22	2.84	1.88	2.02	2.22	2.84	ns
LVC MOS18_JEDEC, Fast, 8 mA	0.94	1.06	1.19	1.41	1.80	1.94	2.14	2.76	1.80	1.94	2.14	2.76	ns
LVC MOS18_JEDEC, Fast, 12 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVC MOS18_JEDEC, Fast, 16 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVC MOS18_JEDEC, Fast, 24 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVC MOS15, QUIETIO, 2 mA	0.98	1.10	1.23	1.79	5.47	5.61	5.81	6.38	5.47	5.61	5.81	6.38	ns
LVC MOS15, QUIETIO, 4 mA	0.98	1.10	1.23	1.79	4.61	4.75	4.95	5.51	4.61	4.75	4.95	5.51	ns
LVC MOS15, QUIETIO, 6 mA	0.98	1.10	1.23	1.79	4.07	4.21	4.41	4.97	4.07	4.21	4.41	4.97	ns
LVC MOS15, QUIETIO, 8 mA	0.98	1.10	1.23	1.79	3.91	4.05	4.25	4.81	3.91	4.05	4.25	4.81	ns
LVC MOS15, QUIETIO, 12 mA	0.98	1.10	1.23	1.79	3.53	3.67	3.87	4.51	3.53	3.67	3.87	4.51	ns
LVC MOS15, QUIETIO, 16 mA	0.98	1.10	1.23	1.79	3.32	3.46	3.66	4.31	3.32	3.46	3.66	4.31	ns
LVC MOS15, Slow, 2 mA	0.98	1.10	1.23	1.79	4.18	4.32	4.52	5.11	4.18	4.32	4.52	5.11	ns
LVC MOS15, Slow, 4 mA	0.98	1.10	1.23	1.79	3.42	3.56	3.76	4.34	3.42	3.56	3.76	4.34	ns
LVC MOS15, Slow, 6 mA	0.98	1.10	1.23	1.79	2.29	2.43	2.63	3.24	2.29	2.43	2.63	3.24	ns

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVC MOS15, Slow, 8 mA	0.98	1.10	1.23	1.79	2.30	2.44	2.64	3.25	2.30	2.44	2.64	3.25	ns
LVC MOS15, Slow, 12 mA	0.98	1.10	1.23	1.79	2.03	2.17	2.37	2.99	2.03	2.17	2.37	2.99	ns
LVC MOS15, Slow, 16 mA	0.98	1.10	1.23	1.79	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVC MOS15, Fast, 2 mA	0.98	1.10	1.23	1.79	3.29	3.43	3.63	4.24	3.29	3.43	3.63	4.24	ns
LVC MOS15, Fast, 4 mA	0.98	1.10	1.23	1.79	2.27	2.41	2.61	3.22	2.27	2.41	2.61	3.22	ns
LVC MOS15, Fast, 6 mA	0.98	1.10	1.23	1.79	1.78	1.92	2.12	2.74	1.78	1.92	2.12	2.74	ns
LVC MOS15, Fast, 8 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.69	1.73	1.87	2.07	2.69	ns
LVC MOS15, Fast, 12 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.64	1.73	1.87	2.07	2.64	ns
LVC MOS15, Fast, 16 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.64	1.73	1.87	2.07	2.64	ns
LVC MOS15_JEDEC, QUIETIO, 2 mA	1.03	1.15	1.28	1.49	5.49	5.63	5.83	6.37	5.49	5.63	5.83	6.37	ns
LVC MOS15_JEDEC, QUIETIO, 4 mA	1.03	1.15	1.28	1.49	4.61	4.75	4.95	5.51	4.61	4.75	4.95	5.51	ns
LVC MOS15_JEDEC, QUIETIO, 6 mA	1.03	1.15	1.28	1.49	4.07	4.21	4.41	4.97	4.07	4.21	4.41	4.97	ns
LVC MOS15_JEDEC, QUIETIO, 8 mA	1.03	1.15	1.28	1.49	3.92	4.06	4.26	4.81	3.92	4.06	4.26	4.81	ns
LVC MOS15_JEDEC, QUIETIO, 12 mA	1.03	1.15	1.28	1.49	3.54	3.68	3.88	4.51	3.54	3.68	3.88	4.51	ns
LVC MOS15_JEDEC, QUIETIO, 16 mA	1.03	1.15	1.28	1.49	3.33	3.47	3.67	4.31	3.33	3.47	3.67	4.31	ns
LVC MOS15_JEDEC, Slow, 2 mA	1.03	1.15	1.28	1.49	4.18	4.32	4.52	5.13	4.18	4.32	4.52	5.13	ns
LVC MOS15_JEDEC, Slow, 4 mA	1.03	1.15	1.28	1.49	3.42	3.56	3.76	4.35	3.42	3.56	3.76	4.35	ns
LVC MOS15_JEDEC, Slow, 6 mA	1.03	1.15	1.28	1.49	2.29	2.43	2.63	3.25	2.29	2.43	2.63	3.25	ns
LVC MOS15_JEDEC, Slow, 8 mA	1.03	1.15	1.28	1.49	2.30	2.44	2.64	3.26	2.30	2.44	2.64	3.26	ns
LVC MOS15_JEDEC, Slow, 12 mA	1.03	1.15	1.28	1.49	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVC MOS15_JEDEC, Slow, 16 mA	1.03	1.15	1.28	1.49	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVC MOS15_JEDEC, Fast, 2 mA	1.03	1.15	1.28	1.49	3.28	3.42	3.62	4.22	3.28	3.42	3.62	4.22	ns
LVC MOS15_JEDEC, Fast, 4 mA	1.03	1.15	1.28	1.49	2.27	2.41	2.61	3.23	2.27	2.41	2.61	3.23	ns
LVC MOS15_JEDEC, Fast, 6 mA	1.03	1.15	1.28	1.49	1.78	1.92	2.12	2.74	1.78	1.92	2.12	2.74	ns
LVC MOS15_JEDEC, Fast, 8 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.69	1.73	1.87	2.07	2.69	ns
LVC MOS15_JEDEC, Fast, 12 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.63	1.73	1.87	2.07	2.63	ns
LVC MOS15_JEDEC, Fast, 16 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.63	1.73	1.87	2.07	2.63	ns
LVC MOS12, QUIETIO, 2 mA	0.91	1.03	1.16	1.51	6.40	6.54	6.74	7.30	6.40	6.54	6.74	7.30	ns
LVC MOS12, QUIETIO, 4 mA	0.91	1.03	1.16	1.51	4.98	5.12	5.32	5.90	4.98	5.12	5.32	5.90	ns
LVC MOS12, QUIETIO, 6 mA	0.91	1.03	1.16	1.51	4.65	4.79	4.99	5.55	4.65	4.79	4.99	5.55	ns
LVC MOS12, QUIETIO, 8 mA	0.91	1.03	1.16	1.51	4.23	4.37	4.57	5.21	4.23	4.37	4.57	5.21	ns
LVC MOS12, QUIETIO, 12 mA	0.91	1.03	1.16	1.51	3.98	4.12	4.32	4.94	3.98	4.12	4.32	4.94	ns
LVC MOS12, Slow, 2 mA	0.91	1.03	1.16	1.51	4.98	5.12	5.32	5.91	4.98	5.12	5.32	5.91	ns
LVC MOS12, Slow, 4 mA	0.91	1.03	1.16	1.51	2.84	2.98	3.18	3.81	2.84	2.98	3.18	3.81	ns
LVC MOS12, Slow, 6 mA	0.91	1.03	1.16	1.51	2.77	2.91	3.11	3.72	2.77	2.91	3.11	3.72	ns
LVC MOS12, Slow, 8 mA	0.91	1.03	1.16	1.51	2.34	2.48	2.68	3.31	2.34	2.48	2.68	3.31	ns
LVC MOS12, Slow, 12 mA	0.91	1.03	1.16	1.51	2.08	2.22	2.42	3.06	2.08	2.22	2.42	3.06	ns

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
DIFF_SSTL3_I	1.26	1.44	1.95	2.15	1.95	2.15	ns
DIFF_SSTL3_II	1.26	1.44	1.94	2.14	1.94	2.14	ns
DIFF_SSTL2_I	1.09	1.27	1.94	2.14	1.94	2.14	ns
DIFF_SSTL2_II	1.09	1.27	1.90	2.10	1.90	2.10	ns
DIFF_SSTL18_I	1.04	1.22	1.86	2.06	1.86	2.06	ns
DIFF_SSTL18_II	1.05	1.23	1.82	2.02	1.82	2.02	ns
DIFF_SSTL15_II	1.01	1.19	1.81	2.01	1.81	2.01	ns
DIFF_MOBILE_DDR	1.04	1.22	1.89	2.09	1.89	2.09	ns
LVTTL, QUIETIO, 2 mA	1.42	1.60	5.64	5.84	5.64	5.84	ns
LVTTL, QUIETIO, 4 mA	1.42	1.60	4.46	4.66	4.46	4.66	ns
LVTTL, QUIETIO, 6 mA	1.42	1.60	3.92	4.12	3.92	4.12	ns
LVTTL, QUIETIO, 8 mA	1.42	1.60	3.37	3.57	3.37	3.57	ns
LVTTL, QUIETIO, 12 mA	1.42	1.60	3.42	3.62	3.42	3.62	ns
LVTTL, QUIETIO, 16 mA	1.42	1.60	3.09	3.29	3.09	3.29	ns
LVTTL, QUIETIO, 24 mA	1.42	1.60	2.83	3.03	2.83	3.03	ns
LVTTL, Slow, 2 mA	1.42	1.60	4.58	4.78	4.58	4.78	ns
LVTTL, Slow, 4 mA	1.42	1.60	3.38	3.58	3.38	3.58	ns
LVTTL, Slow, 6 mA	1.42	1.60	2.95	3.15	2.95	3.15	ns
LVTTL, Slow, 8 mA	1.42	1.60	2.73	2.93	2.73	2.93	ns
LVTTL, Slow, 12 mA	1.42	1.60	2.72	2.92	2.72	2.92	ns
LVTTL, Slow, 16 mA	1.42	1.60	2.53	2.73	2.53	2.73	ns
LVTTL, Slow, 24 mA	1.42	1.60	2.42	2.62	2.42	2.62	ns
LVTTL, Fast, 2 mA	1.42	1.60	4.04	4.24	4.04	4.24	ns
LVTTL, Fast, 4 mA	1.42	1.60	2.66	2.86	2.66	2.86	ns
LVTTL, Fast, 6 mA	1.42	1.60	2.58	2.78	2.58	2.78	ns
LVTTL, Fast, 8 mA	1.42	1.60	2.46	2.66	2.46	2.66	ns
LVTTL, Fast, 12 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns
LVTTL, Fast, 16 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns
LVTTL, Fast, 24 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns
LVC MOS33, QUIETIO, 2 mA	1.41	1.59	5.65	5.85	5.65	5.85	ns
LVC MOS33, QUIETIO, 4 mA	1.41	1.59	4.20	4.40	4.20	4.40	ns
LVC MOS33, QUIETIO, 6 mA	1.41	1.59	3.65	3.85	3.65	3.85	ns
LVC MOS33, QUIETIO, 8 mA	1.41	1.59	3.51	3.71	3.51	3.71	ns
LVC MOS33, QUIETIO, 12 mA	1.41	1.59	3.09	3.29	3.09	3.29	ns
LVC MOS33, QUIETIO, 16 mA	1.41	1.59	2.91	3.11	2.91	3.11	ns
LVC MOS33, QUIETIO, 24 mA	1.41	1.59	2.73	2.93	2.73	2.93	ns
LVC MOS33, Slow, 2 mA	1.41	1.59	4.59	4.79	4.59	4.79	ns
LVC MOS33, Slow, 4 mA	1.41	1.59	3.14	3.34	3.14	3.34	ns

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

V _{CCO}	I/O Standard	Drive	Slew	SSO Limit per V _{CCO} /GND Pair				
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324		
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5	
1.8V	LVCMOS18, LVCMOS18_JEDEC	2	Fast	39	46	39	47	
			Slow	65	75	65	74	
			QuietIO	80	80	80	85	
		4	Fast	22	25	22	25	
			Slow	38	36	38	29	
			QuietIO	45	40	45	35	
		6	Fast	16	18	16	17	
			Slow	27	25	27	19	
			QuietIO	30	28	30	23	
		8	Fast	13	15	13	14	
			Slow	16	18	16	16	
			QuietIO	25	22	25	18	
		12	Fast	5	7	5	5	
			Slow	7	8	7	6	
			QuietIO	11	10	11	8	
		16	Fast	4	5	4	4	
			Slow	7	8	7	5	
			QuietIO	11	10	11	8	
		24	Fast	N/A	5	N/A	3	
			Slow	N/A	8	N/A	8	
			QuietIO	N/A	10	N/A	8	
		HSTL_I_18			9	10	9	9
		HSTL_II_18			N/A	5	N/A	6
		HSTL_III_18			9	10	9	11
	DIFF_HSTL_I_18			27	30	27	27	
	DIFF_HSTL_II_18			N/A	15	N/A	18	
	DIFF_HSTL_III_18			27	30	27	33	
	MOBILE_DDR ⁽³⁾			12	14	12	14	
DIFF_MOBILE_DDR ⁽³⁾			36	42	36	42		
SSTL_18_I ⁽³⁾			9	10	9	10		
SSTL_18_II ⁽³⁾			N/A	5	N/A	4		
DIFF_SSTL_18_I ⁽³⁾			27	30	27	30		
DIFF_SSTL_18_II ⁽³⁾			N/A	15	N/A	12		

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

V _{CCO}	I/O Standard	Drive	Slew	SSO Limit per V _{CCO} /GND Pair				
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324		
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5	
3.3V	LVTTTL	2	Fast	53	65	53	62	
			Slow	70	80	70	73	
			QuietIO	79	89	79	91	
		4	Fast	23	30	23	27	
			Slow	34	41	34	37	
			QuietIO	44	49	44	46	
		6	Fast	16	21	16	20	
			Slow	21	28	21	25	
			QuietIO	34	39	34	34	
		8	Fast	12	16	12	15	
			Slow	16	22	16	19	
			QuietIO	27	28	27	24	
		12	Fast	1	3	1	1	
			Slow	2	5	2	4	
			QuietIO	2	10	2	8	
		16	Fast	1	3	1	1	
			Slow	1	7	1	2	
			QuietIO	3	11	3	8	
		24	Fast	1	2	1	1	
			Slow	2	5	2	2	
			QuietIO	8	9	8	8	
	PCI33_3				18	19	18	19
	PCI66_3				18	19	18	19
	SSTL_3_I				5	8	5	8
	SSTL_3_II				3	5	3	3
	DIFF_SSTL_3_I				15	24	15	24
	DIFF_SSTL_3_II				9	15	9	9
	SDIO				17	18	17	15

Input/Output Logic Switching Characteristics

Table 35: ILOGIC2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T _{ICE0CK} /T _{ICKCE0}	CE0 pin Setup/Hold with respect to CLK	0.56/ −0.30	0.56/ −0.25	0.79/ −0.22	1.21/ −0.52	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.74/ −0.23	0.74/ −0.22	0.98/ −0.20	1.31/ −0.45	ns
T _{IDOCK} /T _{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	1.19/ −0.83	1.36/ −0.83	1.73/ −0.83	2.18/ −1.77	ns
T _{IDOCKD} /T _{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	0.31/ 0.00	0.47/ 0.00	0.54/ 0.00	0.63/ −0.39	ns
Combinatorial						
T _{IDI}	D pin to O pin propagation delay, no Delay	0.95	1.28	1.53	2.25	ns
T _{IDID}	DDLY pin to O pin propagation delay (using IODELAY2)	0.23	0.39	0.44	0.74	ns
Sequential Delays						
T _{IDLO}	D pin to Q pin using flip-flop as a latch without Delay	1.56	1.86	2.39	3.49	ns
T _{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY2)	0.68	0.97	1.20	1.94	ns
T _{ICKQ}	CLK to Q outputs for XC devices	1.03	1.24	1.43	2.11	ns
	CLK to Q outputs for XA and XQ devices	1.38	N/A	1.78	2.11	ns
T _{RQ_ILOGIC2}	SR pin to Q outputs	1.81	1.81	2.50	3.05	ns

Table 36: OLOGIC2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T _{ODCK} /T _{OOCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.81/ −0.05	0.86/ −0.05	1.18/ 0.00	1.73/ −0.27	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.75/ −0.10	0.75/ −0.10	1.01/ −0.05	1.66/ −0.23	ns
T _{OSRCK} /T _{OCKSR}	SR pin Setup/Hold with respect to CLK	0.70/ −0.28	0.79/ −0.28	1.03/ −0.23	1.39/ −0.47	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.24/ −0.08	0.56/ −0.06	0.83/ −0.01	0.99/ −0.19	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.58/ −0.06	0.72/ −0.06	1.18/ −0.01	1.51/ −0.13	ns
Sequential Delays						
T _{OOCKQ}	CLK to OQ/TQ out for XC devices	0.48	0.51	0.74	0.74	ns
	CLK to OQ/TQ out for XA and XQ devices	0.85	N/A	1.16	0.74	ns
T _{RQ_OLOGIC2}	SR pin to OQ/TQ out	1.81	1.81	2.50	3.05	ns

Block RAM Switching Characteristics

Table 43: Block RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Block RAM Clock to Out Delays						
T _{RCKO_DO}	Clock CLK to DOUT output (without output register) ⁽¹⁾	1.85	2.10	2.10	3.50	ns, Max
T _{RCKO_DO_REG}	Clock CLK to DOUT output (with output register) ⁽²⁾	1.60	1.75	1.75	2.30	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{RCCK_ADDR} /T _{RCKC_ADDR}	ADDR inputs for XC devices ⁽³⁾	0.35/ 0.10	0.40/ 0.12	0.40/ 0.12	0.50/ 0.15	ns, Min
	ADDR inputs for XA and XQ devices ⁽³⁾	0.35/ 0.17	N/A	0.40/ 0.17	0.50/ 0.15	ns, Min
T _{RDCK_DI} /T _{RCKD_DI}	DIN inputs ⁽⁴⁾	0.30/ 0.10	0.30/ 0.10	0.30/ 0.10	0.40/ 0.15	ns, Min
T _{RCCK_EN} /T _{RCKC_EN}	Block RAM Enable (EN) input	0.22/ 0.05	0.25/ 0.06	0.25/ 0.06	0.44/ 0.10	ns, Min
T _{RCCK_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.20/ 0.10	0.20/ 0.10	0.20/ 0.10	0.28/ 0.15	ns, Min
T _{RCCK_WE} /T _{RCKC_WE}	Write Enable (WE) input	0.25/ 0.10	0.33/ 0.10	0.33/ 0.10	0.28/ 0.15	ns, Min
Maximum Frequency						
F _{MAX}	Block RAM in all modes	320	280	280	150	MHz

Notes:

- T_{RCKO_DO} includes T_{RCKO_DOA} and T_{RCKO_DOPA} as well as the B port equivalent timing parameters.
- $T_{RCKO_DO_REG}$ includes $T_{RCKO_DOA_REG}$ and $T_{RCKO_DOPA_REG}$ as well as the B port equivalent timing parameters.
- The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
- T_{RDCK_DI} includes both A and B inputs as well as the parity inputs of A and B.

Table 45: Device DNA Interface Port Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T _{DNASSU}	Setup time on SHIFT before the rising edge of CLK	7				ns, Min
T _{DNASH}	Hold time on SHIFT after the rising edge of CLK	1				ns, Min
T _{DNADSU}	Setup time on DIN before the rising edge of CLK	7				ns, Min
T _{DNADH}	Hold time on DIN after the rising edge of CLK	1				ns, Min
T _{DNARSU}	Setup time on READ before the rising edge of CLK	7				ns, Min
		1,000				ns, Max
T _{DNARH}	Hold time on READ after the rising edge of CLK	1				ns, Min
T _{DNADCKO}	Clock-to-output delay on DOUT after rising edge of CLK	0.5				ns, Min
		6				ns, Max
T _{DNACKF} ⁽²⁾	CLK frequency	2				MHz, Max
T _{DNACKL}	CLK Low time	50				ns, Min
T _{DNACKH}	CLK High time	50				ns, Min

Notes:

1. The minimum READ pulse width is 8 ns, the maximum READ pulse width is 1 μ s.
2. Also applies to TCK when reading DNA through the boundary-scan port.

Table 46: Suspend Mode Switching Characteristics

Symbol	Description	Min	Max	Units
Entering Suspend Mode				
T _{SUSPENDHIGH_AWAKE}	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter	2.5	14	ns
T _{SUSPENDFILTER}	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled	31	430	ns
T _{SUSPEND_GWE}	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior (without glitch filter)	–	15	ns
T _{SUSPEND_GTS}	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements (without glitch filter)	–	15	ns
T _{SUSPEND_DISABLE}	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled (without glitch filter)	–	1500	ns
Exiting Suspend Mode				
T _{SUSPENDLOW_AWAKE}	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM or PLL lock time.	7	75	μ s
T _{SUSPEND_ENABLE}	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	7	41	μ s
T _{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using sw_clk:InternalClock and sw_gwe_cycle:1 .	–	80	ns
T _{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using sw_clk:InternalClock and sw_gwe_cycle:512 .	–	20.5	μ s
T _{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using sw_clk:InternalClock and sw_gts_cycle:1 .	–	80	ns
T _{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using sw_clk:InternalClock and sw_gts_cycle:512 .	–	20.5	μ s
T _{SCP_AWAKE}	Rising edge of SCP pins to rising edge of AWAKE pin	7	75	μ s

Table 54: Switching Characteristics for the Delay-Locked Loop (DLL)⁽¹⁾

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges										
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs.	5	280	5	280	5	250	5	175	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs.	5	200	5	200	5	200	5	175	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs.	10	375	10	375	10	334	10	250	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output.	0.3125	186	0.3125	186	0.3125	166	0.3125	88.6	MHz
Output Clock Jitter ⁽²⁾⁽³⁾⁽⁴⁾										
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output.	–	±100	–	±100	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs.	Maximum = ±[0.5% of CLKIN period + 100]								ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division.	Maximum = ±[0.5% of CLKIN period + 100]								ps
Duty Cycle ⁽⁴⁾										
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion.	Typical = ±[1% of CLKIN period + 350]								ps
Phase Alignment ⁽⁴⁾										
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 1X).	–	±150	–	±150	–	±150	–	±250	ps
	Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 2X). ⁽⁶⁾	–	±250	–	±250	–	±250	–	±350	
CLKOUT_PHASE_DLL	Phase offset between DLL outputs for CLK0 to CLK2X (not CLK2X180).	Maximum = ±[1% of CLKIN period + 100]								ps
	Phase offset between DLL outputs for all others.	Maximum = ±[1% of CLKIN period + 150]						Maximum = ±[1% of CLKIN period + 200]		ps

Table 56: Switching Characteristics for the Digital Frequency Synthesizer (DFS) for DCM_SP⁽¹⁾

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz
Output Clock Jitter ⁽²⁾⁽³⁾										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN < 20 MHz	Use the Clocking Wizard								ps
	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN > 20 MHz	Typical = ±(1% of CLKFX period + 100)								ps
Duty Cycle ⁽⁴⁾⁽⁵⁾										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±(1% of CLKFX period + 350)								ps
Phase Alignment ⁽⁵⁾										
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used	–	±200	–	±200	–	±200	–	±250	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used	Maximum = ±(1% of CLKFX period + 200)								ps
LOCKED Time										
LOCK_FX ⁽²⁾	When FCLKIN < 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	–	5	–	5	–	5	–	5	ms
	When FCLKIN > 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	–	0.45	–	0.45	–	0.45	–	0.60	ms

Notes:

- The values in this table are based on the operating conditions described in Table 2 and Table 55.
- For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
- Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
- The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
- Some duty cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of $\pm(1\%$ of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is $\pm(100\text{ ps} + 200\text{ ps}) = \pm 300\text{ ps}$.

Table 68: Global Clock Input to Output Delay With DCM and PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.							
T _{ICKOFDCM_PLL}	Global Clock and OUTFF with DCM and PLL	XC6SLX4	4.78	N/A	6.32	7.09	ns
		XC6SLX9	4.78	5.24	6.32	7.09	ns
		XC6SLX16	4.70	5.12	5.94	6.63	ns
		XC6SLX25	4.70	5.09	5.92	7.30	ns
		XC6SLX25T	4.70	5.09	5.92	N/A	ns
		XC6SLX45	4.63	4.98	5.83	7.26	ns
		XC6SLX45T	4.63	4.98	5.83	N/A	ns
		XC6SLX75	4.68	5.04	5.88	6.90	ns
		XC6SLX75T	4.68	5.04	5.88	N/A	ns
		XC6SLX100	4.72	5.07	5.92	7.77	ns
		XC6SLX100T	4.76	5.07	5.92	N/A	ns
		XC6SLX150	4.44	4.73	5.31	6.96	ns
		XC6SLX150T	4.44	4.73	5.31	N/A	ns
		XA6SLX4	5.07	N/A	6.18	N/A	ns
		XA6SLX9	5.07	N/A	6.18	N/A	ns
		XA6SLX16	5.22	N/A	5.77	N/A	ns
		XA6SLX25	5.01	N/A	5.80	N/A	ns
		XA6SLX25T	5.01	N/A	5.90	N/A	ns
		XA6SLX45	4.93	N/A	5.67	N/A	ns
		XA6SLX45T	4.93	N/A	5.67	N/A	ns
		XA6SLX75	4.94	N/A	5.70	N/A	ns
		XA6SLX75T	4.94	N/A	5.70	N/A	ns
		XA6SLX100	N/A	N/A	5.77	N/A	ns
		XQ6SLX75	N/A	N/A	5.70	6.90	ns
		XQ6SLX75T	4.94	N/A	5.70	N/A	ns
		XQ6SLX150	N/A	N/A	5.31	6.96	ns
		XQ6SLX150T	5.02	N/A	5.31	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 69: Global Clock Input to Output Delay With DCM and PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode.							
T _{ICKOFDCM0_PLL}	Global Clock and OUTFF with DCM and PLL	XC6SLX4	5.58	N/A	7.42	8.54	ns
		XC6SLX9	5.58	6.19	7.42	8.54	ns
		XC6SLX16	5.50	6.06	7.05	8.24	ns
		XC6SLX25	5.57	6.04	7.02	8.33	ns
		XC6SLX25T	5.57	6.04	7.02	N/A	ns
		XC6SLX45	5.53	5.97	6.96	8.32	ns
		XC6SLX45T	5.53	5.97	6.96	N/A	ns
		XC6SLX75	5.55	6.00	6.99	8.54	ns
		XC6SLX75T	5.55	6.00	6.99	N/A	ns
		XC6SLX100	5.58	6.03	7.02	9.11	ns
		XC6SLX100T	5.62	6.03	7.02	N/A	ns
		XC6SLX150	5.32	5.70	6.41	8.26	ns
		XC6SLX150T	5.32	5.70	6.41	N/A	ns
		XA6SLX4	5.87	N/A	7.28	N/A	ns
		XA6SLX9	5.87	N/A	7.28	N/A	ns
		XA6SLX16	6.02	N/A	6.87	N/A	ns
		XA6SLX25	5.88	N/A	6.90	N/A	ns
		XA6SLX25T	5.88	N/A	7.00	N/A	ns
		XA6SLX45	5.82	N/A	6.81	N/A	ns
		XA6SLX45T	5.82	N/A	6.81	N/A	ns
		XA6SLX75	5.81	N/A	6.80	N/A	ns
		XA6SLX75T	5.81	N/A	6.80	N/A	ns
		XA6SLX100	N/A	N/A	6.88	N/A	ns
		XQ6SLX75	N/A	N/A	6.80	8.54	ns
		XQ6SLX75T	5.81	N/A	6.80	N/A	ns
		XQ6SLX150	N/A	N/A	6.41	8.26	ns
		XQ6SLX150T	5.90	N/A	6.41	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 74: Global Clock Setup and Hold With PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.(1)							
T _{PSPLL} / T _{PHPLL}	No Delay Global Clock and IFF(2) with PLL in System-Synchronous Mode	XC6SLX4	1.37/0.25	N/A	1.52/0.41	2.07/0.69	ns
		XC6SLX9	1.37/0.21	1.48/0.21	1.52/0.26	2.07/0.69	ns
		XC6SLX16	1.33/−0.03	1.53/−0.02	1.60/−0.02	1.57/0.48	ns
		XC6SLX25	1.65/0.28	1.71/0.28	1.91/0.28	2.44/0.76	ns
		XC6SLX25T	1.65/0.28	1.71/0.28	1.91/0.28	N/A	ns
		XC6SLX45	1.55/0.18	1.64/0.18	1.75/0.18	2.02/0.90	ns
		XC6SLX45T	1.55/0.18	1.64/0.18	1.75/0.18	N/A	ns
		XC6SLX75	1.77/0.21	1.89/0.21	2.13/0.21	2.46/0.53	ns
		XC6SLX75T	1.77/0.21	1.89/0.21	2.13/0.21	N/A	ns
		XC6SLX100	1.44/0.32	1.52/0.32	1.70/0.32	1.78/0.86	ns
		XC6SLX100T	1.44/0.32	1.52/0.32	1.70/0.32	N/A	ns
		XC6SLX150	1.39/0.49	1.48/0.49	1.67/0.49	1.94/0.94	ns
		XC6SLX150T	1.39/0.49	1.48/0.49	1.67/0.49	N/A	ns
		XA6SLX4	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX9	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX16	1.89/−0.08	N/A	1.72/−0.08	N/A	ns
		XA6SLX25	1.85/0.16	N/A	2.08/0.16	N/A	ns
		XA6SLX25T	1.85/0.16	N/A	2.17/0.16	N/A	ns
		XA6SLX45	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX45T	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX75	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX100	N/A	N/A	2.34/0.14	N/A	ns
		XQ6SLX75	N/A	N/A	2.25/0.06	2.46/0.53	ns
		XQ6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XQ6SLX150	N/A	N/A	1.79/0.37	1.94/0.94	ns
		XQ6SLX150T	1.43/0.37	N/A	1.79/0.37	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 75: Global Clock Setup and Hold With PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.(1)							
T _{PSPLL0} / T _{PHPLL0}	No Delay Global Clock and IFF(2) with PLL in Source-Synchronous Mode	XC6SLX4	0.47/1.08	N/A	0.47/1.60	1.15/1.68	ns
		XC6SLX9	0.47/1.08	0.47/1.35	0.47/1.60	1.15/1.68	ns
		XC6SLX16	0.37/0.75	0.37/0.82	0.51/0.94	0.57/1.31	ns
		XC6SLX25	0.69/1.06	0.69/1.06	0.69/1.06	1.86/1.67	ns
		XC6SLX25T	0.69/1.06	0.69/1.06	0.69/1.06	N/A	ns
		XC6SLX45	0.57/1.05	0.65/1.10	0.65/1.18	1.02/1.65	ns
		XC6SLX45T	0.57/1.06	0.65/1.10	0.65/1.18	N/A	ns
		XC6SLX75	0.86/1.04	0.87/1.04	0.90/1.04	1.34/1.55	ns
		XC6SLX75T	0.86/1.04	0.87/1.04	0.90/1.04	N/A	ns
		XC6SLX100	0.53/1.13	0.54/1.13	0.55/1.13	0.89/2.39	ns
		XC6SLX100T	0.53/1.13	0.54/1.13	0.55/1.13	N/A	ns
		XC6SLX150	0.50/1.31	0.51/1.31	0.52/1.31	1.02/1.72	ns
		XC6SLX150T	0.50/1.31	0.51/1.31	0.52/1.31	N/A	ns
		XA6SLX4	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX9	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX16	0.92/0.69	N/A	0.63/0.82	N/A	ns
		XA6SLX25	0.99/0.94	N/A	0.96/0.94	N/A	ns
		XA6SLX25T	0.99/0.94	N/A	1.04/0.94	N/A	ns
		XA6SLX45	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX45T	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX75	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX100	N/A	N/A	1.25/0.96	N/A	ns
		XQ6SLX75	N/A	N/A	1.02/0.89	1.34/1.55	ns
		XQ6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XQ6SLX150	N/A	N/A	0.63/1.19	1.02/1.72	ns
		XQ6SLX150T	0.60/1.19	N/A	0.63/1.19	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 79: Package Skew (Cont'd)

Symbol	Description	Device	Package ⁽²⁾	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	LX45	CSG324	70	ps
			CS(G)484	99	ps
			FG(G)484	109	ps
			FG(G)676	138	ps
		LX45T	CSG324	75	ps
			CS(G)484	100	ps
			FG(G)484	95	ps
		LX75	CS(G)484	101	ps
			FG(G)484	107	ps
			FG(G)676	161	ps
		LX75T	CS(G)484	107	ps
			FG(G)484	110	ps
			FG(G)676	134	ps
		LX100	CS(G)484	95	ps
			FG(G)484	155	ps
			FG(G)676	144	ps
		LX100T	CS(G)484	88	ps
			FG(G)484	111	ps
			FG(G)676	147	ps
			FG(G)900	134	ps
		LX150	CS(G)484	84	ps
			FG(G)484	103	ps
			FG(G)676	115	ps
			FG(G)900	121	ps
		LX150T	CS(G)484	83	ps
			FG(G)484	88	ps
			FG(G)676	141	ps
			FG(G)900	120	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from Pad to Ball.
- Some of the devices are available in both Pb and Pb-free (additional G) packages as standard ordering options. See [DS160: Spartan-6 Family Overview](#) for more information.

Table 80: Sample Window

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{SAMP}	Sampling Error at Receiver Pins ⁽²⁾	All	510	510	530	740	ps
T _{SAMP_BUFIO2}	Sampling Error at Receiver Pins using BUFIO2 ⁽³⁾	All	430	430	450	590	ps

Notes:

- LXT devices are not available with a -1L speed grade.
- This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 DCM jitter
 - DCM accuracy (phase offset)
 - DCM phase shift resolution
These measurements do not include package or clock tree skew.
- This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO2 clock network and IODELAY2 to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Date	Version	Description of Revisions
01/10/11	1.11	Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.4 software with speed specification v1.15 for the -4, -3, -3N, and -2 speed grades. Added note 3 to Table 27. Also updated the -1L speed grade requirements to ISE v12.4 software with speed specification v1.06. Revised -3N definition throughout the document. Added note 4 to Table 2 and updated note 5. Added information on V_{CCINT} to note 1 in Table 5. Updated Networking Applications -3 values in Table 25 to match improvements made in ISE v12.4. In Table 28, added note 1 and revised the T_{IOTP} values for LVDS_33, LVDS_25, MINI_LVDS_33, MINI_LVDS_25, RSDS_33, RSDS_25, TMDS_33, PPDS_33, and PPDS_25. Added note 3 to Table 55.
02/11/11	1.12	As described in XCEN11008: Product Discontinuation Notice For Spartan-6 LXT -4 Devices, the -4 speed specifications have been discontinued. As outlined in page 2 of the XCN, designers currently using -4 speed specifications should rerun timing analysis using the new -3 speed specifications before moving to a replacement device. Updated the networking applications section of Table 25. Updated -2 speed specifications throughout document and added note 3 to Table 27 advising designers to use the -2 speed specification update (v1.17) with the ISE 12.4 software patch. Added F_{CLKDIV} to Table 37 and Table 38. Updated note 2 in Table 39. Updated units for $T_{SMCKCSO}$ and T_{BPICCO} in Table 47. Updated -1L in Table 71. Removed Note 2: <i>Package delay information is available for these device/package combinations. This information can be used to deskew the package</i> from Table 79.
03/31/11	2.0	Production release of XC6SLX45 in the -1L speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. In Table 39, removed values in the -1L column and added note 3 as IODELAY2 only supports Tap0 for lower-power devices. Updated copyright page 1 and Notice of Disclaimer.
05/20/11	2.1	Production release of XC6SLX100 and XC6SLX150 in the specific speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. Updated Table 27 and Note 7 with changes per XCEN11012: Speed File Change for -3N Devices. Revised Switching Characteristics section for speed specifications: v1.18 for -3, -3N, and -2; including improvements in Table 73 through Table 77 and Table 81. Removed <i>Memory Controller Block</i> from the performance heading in Table 2 and revised Note 2. In Table 4, added Note 1 to C_{IN} and updated the description of R_{IN_TERM}. Updated Note 1 in Table 5. Updated Note 1 of Table 7. In Table 25, added and removed -1L specifications, increased the standard performance DDR3 specifications, removed the extended performance DDR3 row and updated Note 3 and Note 4. Clarified the introductory information for Table 28 and Table 30. In Table 32: Revised V_{MEAS} value for LVCMOS12; revised V_{REF} for LVDS_25, LVDS_33, BLVDS_25, MINI_LVDS_25, MINI_LVDS_33, RSDS_25, and RSDS_33; revised R_{REF} for BLVDS_25 and TMDS_33; and added Note 4 and Note 5. Updated Note 2 and Note 3 in Table 39. In Table 47, revised the values and description of T_{POR} including adding Note 3. Also in Table 47, augmented the description and added specifications for F_{RBCK} and removed XC6SLX4 from F_{MCCK} (maximum frequency, parallel mode (Master SelectMAP/BPI)). Added BUFGMUX to Table 48 title. Added Table 50. In Table 52, revised specifications for $T_{EXTFVAR}$ and $F_{INJITTER}$. In Table 54 removed the 5 MHz < CLKIN_FREQ_DLL parameter in the LOCK_DLL description. In both Table 56 and Table 57, removed the 5 MHz < F_{CLKIN} parameter in the LOCK_FX description. In Table 58, updated description for PSCLK_FREQ and PSCLK_PULSE. Revised title and symbol of Table 70, added new speed specifications for -1L, and added Note 2. Added Table 71.
07/11/11	2.2	Added the Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices to all appropriate tables while sometimes removing the XC6S nomenclature. Added expanded temperature range (Q) to all appropriate tables. Updated T_{SOL} packages in Table 1. Added R_{OUT_TERM} to Table 4. Updated Note 2 on Table 13. Production release of the XC6SLX4, XC6SLX9, XC6SLX16, XC6SLX25, XC6SLX75, XQ6SLX75, and XQ6SLX150 in Table 26 and Table 27 using ISE v13.2 software with -1L speed specification v1.07. Production release of the XA6SLX16, XA6SLX25T, XA6SLX45, XA6SLX45T, XQ6SLX75, XQ6SLX75T, XQ6SLX150, and XQ6SLX150T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices(1). Updated CS(G)484 from CSG484 throughout data sheet. Clarified Note 3 in Table 39.
08/08/11	2.3	Production release of the XA6SLX25, XA6SLX75, and XA6SLX75T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19.