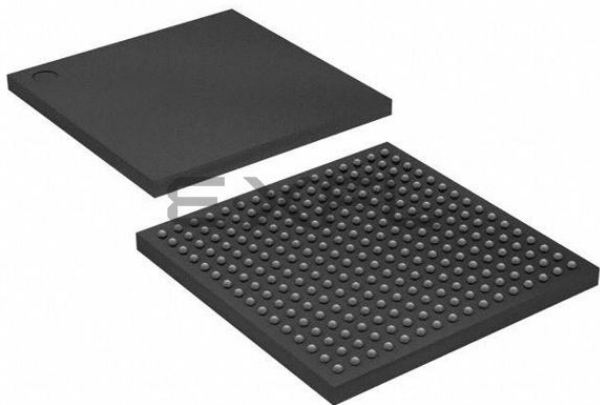




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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                         |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Active                                                                                                                                  |
| Number of LABs/CLBs            | 1879                                                                                                                                    |
| Number of Logic Elements/Cells | 24051                                                                                                                                   |
| Total RAM Bits                 | 958464                                                                                                                                  |
| Number of I/O                  | 186                                                                                                                                     |
| Number of Gates                | -                                                                                                                                       |
| Voltage - Supply               | 1.14V ~ 1.26V                                                                                                                           |
| Mounting Type                  | Surface Mount                                                                                                                           |
| Operating Temperature          | -40°C ~ 100°C (TJ)                                                                                                                      |
| Package / Case                 | 256-LBGA                                                                                                                                |
| Supplier Device Package        | 256-FTBGA (17x17)                                                                                                                       |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/xilinx/xc6slx25-3ft256i">https://www.e-xfl.com/product-detail/xilinx/xc6slx25-3ft256i</a> |

Table 1: Absolute Maximum Ratings<sup>(1)</sup> (Cont'd)

| Symbol                               | Description                                                                                          |                                        |              |                                       |               | Units |
|--------------------------------------|------------------------------------------------------------------------------------------------------|----------------------------------------|--------------|---------------------------------------|---------------|-------|
| $V_{IN}$ and $V_{TS}$ <sup>(3)</sup> | I/O input voltage or voltage applied to 3-state output, relative to GND <sup>(4)</sup>               | All user and dedicated I/Os            | Commercial   | DC                                    | –0.60 to 4.10 | V     |
|                                      |                                                                                                      |                                        |              | 20% overshoot duration                | –0.75 to 4.25 | V     |
|                                      |                                                                                                      |                                        |              | 8% overshoot duration <sup>(5)</sup>  | –0.75 to 4.40 | V     |
|                                      |                                                                                                      |                                        | Industrial   | DC                                    | –0.60 to 3.95 | V     |
|                                      |                                                                                                      |                                        |              | 20% overshoot duration                | –0.75 to 4.15 | V     |
|                                      |                                                                                                      |                                        |              | 4% overshoot duration <sup>(5)</sup>  | –0.75 to 4.40 | V     |
|                                      |                                                                                                      |                                        | Expanded (Q) | DC                                    | –0.60 to 3.95 | V     |
|                                      |                                                                                                      |                                        |              | 20% overshoot duration                | –0.75 to 4.15 | V     |
|                                      |                                                                                                      |                                        |              | 4% overshoot duration <sup>(5)</sup>  | –0.75 to 4.40 | V     |
|                                      |                                                                                                      | Restricted to maximum of 100 user I/Os | Commercial   | 20% overshoot duration                | –0.75 to 4.35 | V     |
|                                      |                                                                                                      |                                        |              | 15% overshoot duration <sup>(5)</sup> | –0.75 to 4.40 | V     |
|                                      |                                                                                                      |                                        |              | 10% overshoot duration                | –0.75 to 4.45 | V     |
|                                      |                                                                                                      |                                        | Industrial   | 20% overshoot duration                | –0.75 to 4.25 | V     |
|                                      |                                                                                                      |                                        |              | 10% overshoot duration                | –0.75 to 4.35 | V     |
|                                      |                                                                                                      |                                        |              | 8% overshoot duration <sup>(5)</sup>  | –0.75 to 4.40 | V     |
|                                      |                                                                                                      |                                        | Expanded (Q) | 20% overshoot duration                | –0.75 to 4.25 | V     |
|                                      |                                                                                                      |                                        |              | 10% overshoot duration                | –0.75 to 4.35 | V     |
|                                      |                                                                                                      |                                        |              | 8% overshoot duration <sup>(5)</sup>  | –0.75 to 4.40 | V     |
| $T_{STG}$                            | Storage temperature (ambient)                                                                        |                                        |              |                                       | –65 to 150    | °C    |
| $T_{SOL}$                            | Maximum soldering temperature <sup>(6)</sup><br>(TQG144, CPG196, CSG225, CSG324, CSG484, and FTG256) |                                        |              |                                       | +260          | °C    |
|                                      | Maximum soldering temperature <sup>(6)</sup> (Pb-free packages: FGG484, FGG676, and FGG900)          |                                        |              |                                       | +250          | °C    |
|                                      | Maximum soldering temperature <sup>(6)</sup> (Pb packages: CS484, FT256, FG484, FG676, and FG900)    |                                        |              |                                       | +220          | °C    |
| $T_j$                                | Maximum junction temperature <sup>(6)</sup>                                                          |                                        |              |                                       | +125          | °C    |

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- When programming eFUSE,  $V_{FS} \leq V_{CCAUX}$ . Requires up to 40 mA current. For read mode,  $V_{FS}$  can be between GND and 3.45 V.
- I/O absolute maximum limit applied to DC and AC signals. Overshoot duration is the percentage of a data period that the I/O is stressed beyond 3.45V.
- For I/O operation, refer to [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.
- Maximum percent overshoot duration to meet 4.40V maximum.
- For soldering guidelines and thermal considerations, see [UG385](#): *Spartan-6 FPGA Packaging and Pinout Specification*.

Table 5: Typical Quiescent Supply Current (Cont'd)

| Symbol              | Description                                 | Device | Speed Grade |      |      |      | Units |
|---------------------|---------------------------------------------|--------|-------------|------|------|------|-------|
|                     |                                             |        | -3          | -3N  | -2   | -1L  |       |
| I <sub>CCAUXQ</sub> | Quiescent V <sub>CCAUX</sub> supply current | LX4    | 2.5         | 2.5  | 2.5  | 2.5  | mA    |
|                     |                                             | LX9    | 2.5         | 2.5  | 2.5  | 2.5  | mA    |
|                     |                                             | LX16   | 3.0         | 3.0  | 3.0  | 3.0  | mA    |
|                     |                                             | LX25   | 4.0         | 4.0  | 4.0  | 4.0  | mA    |
|                     |                                             | LX25T  | 4.0         | 4.0  | 4.0  | N/A  | mA    |
|                     |                                             | LX45   | 5.0         | 5.0  | 5.0  | 5.0  | mA    |
|                     |                                             | LX45T  | 5.0         | 5.0  | 5.0  | N/A  | mA    |
|                     |                                             | LX75   | 7.0         | 7.0  | 7.0  | 7.0  | mA    |
|                     |                                             | LX75T  | 7.0         | 7.0  | 7.0  | N/A  | mA    |
|                     |                                             | LX100  | 9.0         | 9.0  | 9.0  | 9.0  | mA    |
|                     |                                             | LX100T | 9.0         | 9.0  | 9.0  | N/A  | mA    |
|                     |                                             | LX150  | 12.0        | 12.0 | 12.0 | 12.0 | mA    |
|                     |                                             | LX150T | 12.0        | 12.0 | 12.0 | N/A  | mA    |

**Notes:**

- Typical values are specified at nominal voltage, 25°C junction temperatures (T<sub>j</sub>). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 25°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. Nominal V<sub>CCINT</sub> is 1.20V; use the XPE tool to calculate 1.23V values for the nominal V<sub>CCINT</sub> of the extended performance range.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- If differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 6: Power Supply Ramp Time

| Symbol                           | Description                                    | Speed Grade | Ramp Time    | Units |
|----------------------------------|------------------------------------------------|-------------|--------------|-------|
| V <sub>CCINTR</sub>              | Internal supply voltage ramp time              | -3, -3N, -2 | 0.20 to 50.0 | ms    |
|                                  |                                                | -1L         | 0.20 to 40.0 | ms    |
| V <sub>CCO2</sub> <sup>(1)</sup> | Output drivers bank 2 supply voltage ramp time | All         | 0.20 to 50.0 | ms    |
| V <sub>CCAUXR</sub>              | Auxiliary supply voltage ramp time             | All         | 0.20 to 50.0 | ms    |

**Notes:**

- The minimum V<sub>CCO2</sub> for power-on reset and configuration is 1.65V.
- Spartan-6 FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply. Use the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools to estimate current drain on these supplies. Spartan-6 devices do not have a required power-on sequence.

In Table 9 and Table 10, values for  $V_{IL}$  and  $V_{IH}$  are recommended input voltages. Values for  $I_{OL}$  and  $I_{OH}$  are guaranteed over the recommended operating conditions at the  $V_{OL}$  and  $V_{OH}$  test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum  $V_{CCO}$  with the respective  $V_{OL}$  and  $V_{OH}$  voltage levels shown. Other standards are sample tested.

Table 9: Single-Ended I/O Standard DC Input and Output Levels

| I/O Standard    | $V_{IL}$ |                   | $V_{IH}$          |                 | $V_{OL}$        | $V_{OH}$         | $I_{OL}$ | $I_{OH}$ |
|-----------------|----------|-------------------|-------------------|-----------------|-----------------|------------------|----------|----------|
|                 | V, Min   | V, Max            | V, Min            | V, Max          | V, Max          | V, Min           | mA       | mA       |
| LVTTTL          | −0.5     | 0.8               | 2.0               | 4.1             | 0.4             | 2.4              | Note 2   | Note 2   |
| LVC MOS33       | −0.5     | 0.8               | 2.0               | 4.1             | 0.4             | $V_{CCO} - 0.4$  | Note 2   | Note 2   |
| LVC MOS25       | −0.5     | 0.7               | 1.7               | 4.1             | 0.4             | $V_{CCO} - 0.4$  | Note 2   | Note 2   |
| LVC MOS18       | −0.5     | 0.38              | 0.8               | 4.1             | 0.45            | $V_{CCO} - 0.45$ | Note 2   | Note 2   |
| LVC MOS18 (−1L) | −0.5     | 0.33              | 0.71              | 4.1             | 0.45            | $V_{CCO} - 0.45$ | Note 2   | Note 2   |
| LVC MOS18_JEDEC | −0.5     | 35% $V_{CCO}$     | 65% $V_{CCO}$     | 4.1             | 0.45            | $V_{CCO} - 0.45$ | Note 2   | Note 2   |
| LVC MOS15       | −0.5     | 0.38              | 0.8               | 4.1             | 25% $V_{CCO}$   | 75% $V_{CCO}$    | Note 3   | Note 3   |
| LVC MOS15 (−1L) | −0.5     | 0.33              | 0.71              | 4.1             | 25% $V_{CCO}$   | 75% $V_{CCO}$    | Note 3   | Note 3   |
| LVC MOS15_JEDEC | −0.5     | 35% $V_{CCO}$     | 65% $V_{CCO}$     | 4.1             | 25% $V_{CCO}$   | 75% $V_{CCO}$    | Note 3   | Note 3   |
| LVC MOS12       | −0.5     | 0.38              | 0.8               | 4.1             | 0.4             | $V_{CCO} - 0.4$  | Note 4   | Note 4   |
| LVC MOS12 (−1L) | −0.5     | 0.33              | 0.71              | 4.1             | 0.4             | $V_{CCO} - 0.4$  | Note 4   | Note 4   |
| LVC MOS12_JEDEC | −0.5     | 35% $V_{CCO}$     | 65% $V_{CCO}$     | 4.1             | 0.4             | $V_{CCO} - 0.4$  | Note 4   | Note 4   |
| PCI33_3         | −0.5     | 30% $V_{CCO}$     | 50% $V_{CCO}$     | $V_{CCO} + 0.5$ | 10% $V_{CCO}$   | 90% $V_{CCO}$    | 1.5      | −0.5     |
| PCI66_3         | −0.5     | 30% $V_{CCO}$     | 50% $V_{CCO}$     | $V_{CCO} + 0.5$ | 10% $V_{CCO}$   | 90% $V_{CCO}$    | 1.5      | −0.5     |
| I2C             | −0.5     | 25% $V_{CCO}$     | 70% $V_{CCO}$     | 4.1             | 20% $V_{CCO}$   | —                | 3        | —        |
| SMBUS           | −0.5     | 0.8               | 2.1               | 4.1             | 0.4             | —                | 4        | —        |
| SDIO            | −0.5     | 12.5% $V_{CCO}$   | 75% $V_{CCO}$     | 4.1             | 12.5% $V_{CCO}$ | 75% $V_{CCO}$    | 0.1      | −0.1     |
| MOBILE_DDR      | −0.5     | 20% $V_{CCO}$     | 80% $V_{CCO}$     | 4.1             | 10% $V_{CCO}$   | 90% $V_{CCO}$    | 0.1      | −0.1     |
| HSTL_I          | −0.5     | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | 4.1             | 0.4             | $V_{CCO} - 0.4$  | 8        | −8       |
| HSTL_II         | −0.5     | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | 4.1             | 0.4             | $V_{CCO} - 0.4$  | 16       | −16      |
| HSTL_III        | −0.5     | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | 4.1             | 0.4             | $V_{CCO} - 0.4$  | 24       | −8       |
| HSTL_I_18       | −0.5     | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | 4.1             | 0.4             | $V_{CCO} - 0.4$  | 11       | −11      |
| HSTL_II_18      | −0.5     | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | 4.1             | 0.4             | $V_{CCO} - 0.4$  | 22       | −22      |
| HSTL_III_18     | −0.5     | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | 4.1             | 0.4             | $V_{CCO} - 0.4$  | 30       | −11      |
| SSTL3_I         | −0.5     | $V_{REF} - 0.2$   | $V_{REF} + 0.2$   | 4.1             | $V_{TT} - 0.6$  | $V_{TT} + 0.6$   | 8        | −8       |
| SSTL3_II        | −0.5     | $V_{REF} - 0.2$   | $V_{REF} + 0.2$   | 4.1             | $V_{TT} - 0.8$  | $V_{TT} + 0.8$   | 16       | −16      |
| SSTL2_I         | −0.5     | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | 4.1             | $V_{TT} - 0.61$ | $V_{TT} + 0.61$  | 8.1      | −8.1     |
| SSTL2_II        | −0.5     | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | 4.1             | $V_{TT} - 0.81$ | $V_{TT} + 0.81$  | 16.2     | −16.2    |
| SSTL18_I        | −0.5     | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | 4.1             | $V_{TT} - 0.47$ | $V_{TT} + 0.47$  | 6.7      | −6.7     |
| SSTL18_II       | −0.5     | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | 4.1             | $V_{TT} - 0.60$ | $V_{TT} + 0.60$  | 13.4     | −13.4    |
| SSTL15_II       | −0.5     | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | 4.1             | $V_{TT} - 0.4$  | $V_{TT} + 0.4$   | 13.4     | −13.4    |

**Notes:**

1. Tested according to relevant specifications.
2. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
3. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
4. Using drive strengths of 2, 4, 6, 8, or 12 mA.
5. For more information, refer to [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.

## GTP Transceiver DC Input and Output Levels

Table 16 summarizes the DC output specifications of the GTP transceivers in Spartan-6 FPGAs. Figure 1 shows the single-ended output voltage swing. Figure 2 shows the peak-to-peak differential output voltage.

Consult [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#) for further details.

Table 16: GTP Transceiver DC Specifications

| Symbol        | DC Parameter                                              | Conditions                                         | Min                       | Typ              | Max       | Units    |
|---------------|-----------------------------------------------------------|----------------------------------------------------|---------------------------|------------------|-----------|----------|
| $DV_{PPIN}$   | Differential peak-to-peak input voltage                   | External AC coupled                                | 140                       | –                | 2000      | mV       |
| $V_{IN}$      | Absolute input voltage                                    | DC coupled<br>MGTAVTTRX = 1.2V                     | –400                      | –                | MGTAVTTRX | mV       |
| $V_{CMIN}$    | Common mode input voltage                                 | DC coupled<br>MGTAVTTRX = 1.2V                     | –                         | 3/4<br>MGTAVTTRX | –         | mV       |
| $DV_{PPOUT}$  | Differential peak-to-peak output voltage <sup>(1)</sup>   | Transmitter output swing is set to maximum setting | –                         | –                | 1000      | mV       |
| $V_{SEOUT}$   | Single-ended output voltage swing <sup>(1)</sup>          |                                                    | –                         | –                | 500       | mV       |
| $V_{CMOUTDC}$ | Common mode output voltage                                | Equation based                                     | $MGTAVTTTX - V_{SEOUT}/2$ |                  |           | mV       |
| $R_{IN}$      | Differential input resistance                             |                                                    | 80                        | 100              | 130       | $\Omega$ |
| $R_{OUT}$     | Differential output resistance                            |                                                    | 80                        | 100              | 130       | $\Omega$ |
| $T_{OSKEW}$   | Transmitter output skew                                   |                                                    | –                         | –                | 15        | ps       |
| $C_{EXT}$     | Recommended external AC coupling capacitor <sup>(2)</sup> |                                                    | 75                        | 100              | 200       | nF       |

### Notes:

- The output swing and preemphasis levels are programmable using the attributes discussed in [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#) and can result in values lower than reported in this table.
- Other values can be used as appropriate to conform to specific protocols and standards.

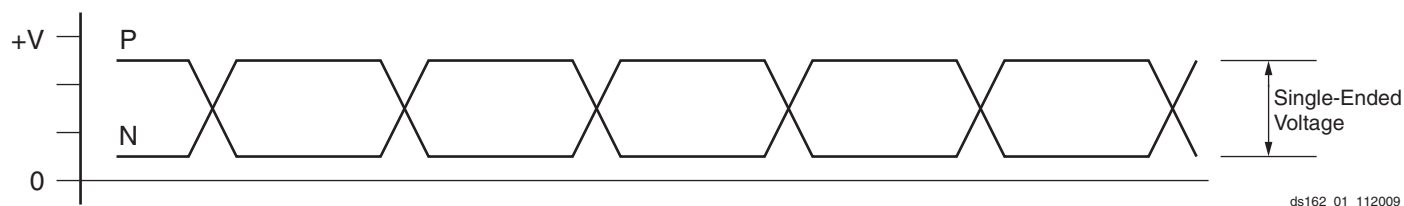


Figure 1: Single-Ended Peak-to-Peak Voltage

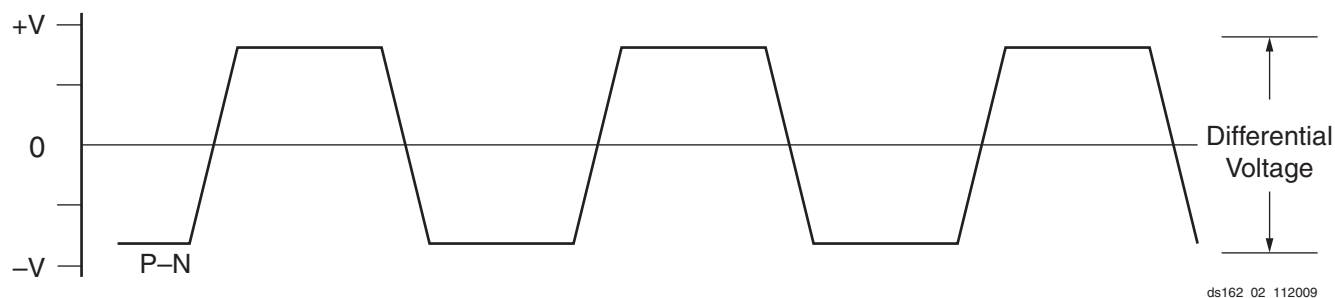


Figure 2: Differential Peak-to-Peak Voltage

Table 17 summarizes the DC specifications of the clock input of the GTP transceiver. Consult [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#) for further details.

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [Switching Characteristics, page 19](#).

Table 25: Interface Performances

| Description                                                                                     | I/O Resource             | Clock Buffer | Data Width | Speed Grade |        |     |     | Units |
|-------------------------------------------------------------------------------------------------|--------------------------|--------------|------------|-------------|--------|-----|-----|-------|
|                                                                                                 |                          |              |            | -3          | -3N    | -2  | -1L |       |
| Networking Applications <sup>(1)</sup>                                                          |                          |              |            |             |        |     |     |       |
| SDR LVDS transmitter or receiver                                                                | IOB SDR register         | BUFG         | –          | 400         | 400    | 375 | 250 | Mb/s  |
| DDR LVDS transmitter or receiver                                                                | ODDR2/IDDR2 register     | 2 BUFGs      | –          | 800         | 800    | 750 | 500 | Mb/s  |
| SDR LVDS transmitter                                                                            | OSERDES2                 | BUFPLL       | 2          | 500         | 500    | 500 | 250 | Mb/s  |
|                                                                                                 |                          |              | 3          | 750         | 750    | 750 | 375 | Mb/s  |
|                                                                                                 |                          |              | 4-8        | 1080        | 1050   | 950 | 500 | Mb/s  |
| DDR LVDS transmitter                                                                            | OSERDES2                 | 2 BUFIO2s    | 2          | 500         | 500    | 500 | 250 | Mb/s  |
|                                                                                                 |                          |              | 3          | 750         | 750    | 750 | 375 | Mb/s  |
|                                                                                                 |                          |              | 4-8        | 1080        | 1050   | 950 | 500 | Mb/s  |
| SDR LVDS receiver                                                                               | ISERDES2 in RETIMED mode | BUFPLL       | 2          | 500         | 500    | 500 | —   | Mb/s  |
|                                                                                                 |                          |              | 3          | 750         | 750    | 750 | —   | Mb/s  |
|                                                                                                 |                          |              | 4-8        | 1080        | 1050   | 950 | —   | Mb/s  |
| DDR LVDS receiver                                                                               | ISERDES2 in RETIMED mode | 2 BUFIO2s    | 2          | 500         | 500    | 500 | —   | Mb/s  |
|                                                                                                 |                          |              | 3          | 750         | 750    | 750 | —   | Mb/s  |
|                                                                                                 |                          |              | 4-8        | 1080        | 1050   | 950 | —   | Mb/s  |
| Memory Interfaces (Implemented using the Spartan-6 FPGA Memory Controller Block) <sup>(2)</sup> |                          |              |            |             |        |     |     |       |
| Standard Performance (Standard V <sub>CCINT</sub> )                                             |                          |              |            |             |        |     |     |       |
| DDR                                                                                             |                          |              |            | 400         | Note 4 | 400 | 350 | Mb/s  |
| DDR2                                                                                            |                          |              |            | 667         | Note 4 | 625 | 400 | Mb/s  |
| DDR3                                                                                            |                          |              |            | 800         | Note 4 | 667 | —   | Mb/s  |
| LPDDR (Mobile_DDR)                                                                              |                          |              |            | 400         | Note 4 | 400 | 350 | Mb/s  |
| Extended Performance (Requires Extended Performance V <sub>CCINT</sub> ) <sup>(3)</sup>         |                          |              |            |             |        |     |     |       |
| DDR2                                                                                            |                          |              |            | 800         | Note 4 | 667 | —   | Mb/s  |

### Notes:

1. Refer to [XAPP1064](#), *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)* and [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.
2. Refer to [UG388](#), *Spartan-6 FPGA Memory Controller User Guide*.
3. Extended Memory Controller block performance for DDR2 can be achieved using the extended performance  $V_{CCINT}$  range from [Table 2](#).
4. The LX4 device, all devices in the TQG144 and CPG196 packages, and the -3N speed grade do not support a Memory Controller Block.

## Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. [Table 27](#) lists the production released Spartan-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE® software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

**Table 27: Spartan-6 Device Production Software and Speed Specification Release<sup>(1)</sup>**

| Device     | Speed Grade Designations <sup>(2)</sup> |                                      |                               |                |
|------------|-----------------------------------------|--------------------------------------|-------------------------------|----------------|
|            | -3 <sup>(3)</sup>                       | -3N                                  | -2 <sup>(4)</sup>             | -1L            |
| XC6SLX4    | ISE 12.4 v1.15                          | N/A                                  | ISE 12.3 v1.12 <sup>(5)</sup> | ISE 13.2 v1.07 |
| XC6SLX9    | ISE 12.4 v1.15                          | ISE 13.1 Update v1.18 <sup>(7)</sup> | ISE 12.3 v1.12 <sup>(5)</sup> | ISE 13.2 v1.07 |
| XC6SLX16   | ISE 12.1 v1.08                          | ISE 13.1 Update v1.18 <sup>(7)</sup> | ISE 11.5 v1.06                | ISE 13.2 v1.07 |
| XC6SLX25   | ISE 12.2 v1.11 <sup>(6)</sup>           | ISE 13.1 Update v1.18 <sup>(7)</sup> | ISE 12.2 v1.11 <sup>(6)</sup> | ISE 13.2 v1.07 |
| XC6SLX25T  | ISE 12.2 v1.11 <sup>(6)</sup>           | ISE 13.1 Update v1.18 <sup>(7)</sup> | ISE 12.2 v1.11 <sup>(6)</sup> | N/A            |
| XC6SLX45   | ISE 12.1 v1.08                          | ISE 13.1 Update v1.18 <sup>(7)</sup> | ISE 11.5 v1.07                | ISE 13.1 v1.06 |
| XC6SLX45T  | ISE 12.1 v1.08                          | ISE 13.1 Update v1.18 <sup>(7)</sup> | ISE 12.1 v1.08                | N/A            |
| XC6SLX75   | ISE 12.2 v1.11 <sup>(6)</sup>           | ISE 13.1 Update v1.18 <sup>(7)</sup> | ISE 12.2 v1.11 <sup>(6)</sup> | ISE 13.2 v1.07 |
| XC6SLX75T  | ISE 12.2 v1.11 <sup>(6)</sup>           | ISE 13.1 Update v1.18 <sup>(7)</sup> | ISE 12.2 v1.11 <sup>(6)</sup> | N/A            |
| XC6SLX100  | ISE 12.2 v1.11 <sup>(6)</sup>           | ISE 13.1 Update v1.18 <sup>(7)</sup> | ISE 12.2 v1.11 <sup>(6)</sup> | ISE 13.1 v1.06 |
| XC6SLX100T | ISE 12.2 v1.11 <sup>(6)</sup>           | ISE 13.1 Update v1.18 <sup>(7)</sup> | ISE 12.2 v1.11 <sup>(6)</sup> | N/A            |
| XC6SLX150  | ISE 12.2 v1.11 <sup>(6)</sup>           | ISE 13.1 Update v1.18 <sup>(7)</sup> | ISE 12.2 v1.11 <sup>(6)</sup> | ISE 13.1 v1.06 |
| XC6SLX150T | ISE 12.2 v1.11 <sup>(6)</sup>           | ISE 13.1 Update v1.18 <sup>(7)</sup> | ISE 12.2 v1.11 <sup>(6)</sup> | N/A            |
| XA6SLX4    | ISE 13.2 v1.19                          | N/A                                  | ISE 13.2 v1.19                | N/A            |
| XA6SLX9    | ISE 13.2 v1.19                          | N/A                                  | ISE 13.2 v1.19                | N/A            |
| XA6SLX16   | ISE 13.2 v1.19                          | N/A                                  | ISE 13.2 v1.19                | N/A            |
| XA6SLX25   | ISE 13.2 v1.19                          | N/A                                  | ISE 13.2 v1.19                | N/A            |
| XA6SLX25T  | ISE 13.2 v1.19                          | N/A                                  | ISE 13.2 v1.19                | N/A            |
| XA6SLX45   | ISE 13.2 v1.19                          | N/A                                  | ISE 13.2 v1.19                | N/A            |
| XA6SLX45T  | ISE 13.2 v1.19                          | N/A                                  | ISE 13.2 v1.19                | N/A            |
| XA6SLX75   | ISE 13.2 v1.19                          | N/A                                  | ISE 13.2 v1.19                | N/A            |
| XA6SLX75T  | ISE 13.2 v1.19                          | N/A                                  | ISE 13.2 v1.19                | N/A            |
| XA6SLX100  | N/A                                     | N/A                                  | ISE 13.3 v1.20                | N/A            |

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices<sup>(1)</sup>

| I/O Standard             | T <sub>IOPI</sub> |      | T <sub>IOOP</sub> |       | T <sub>IOTP</sub> |       | Units |
|--------------------------|-------------------|------|-------------------|-------|-------------------|-------|-------|
|                          | Speed Grade       |      | Speed Grade       |       | Speed Grade       |       |       |
|                          | -3                | -2   | -3                | -2    | -3                | -2    |       |
| LVDS_33                  | 1.24              | 1.42 | 1.69              | 1.89  | 3000              | 3000  | ns    |
| LVDS_25                  | 1.08              | 1.26 | 1.79              | 1.99  | 3000              | 3000  | ns    |
| BLVDS_25                 | 1.09              | 1.27 | 1.86              | 2.06  | 1.86              | 2.06  | ns    |
| MINI_LVDS_33             | 1.25              | 1.43 | 1.71              | 1.91  | 3000              | 3000  | ns    |
| MINI_LVDS_25             | 1.08              | 1.26 | 1.79              | 1.99  | 3000              | 3000  | ns    |
| LVPECL_33                | 1.25              | 1.43 | N/A               | N/A   | N/A               | N/A   | ns    |
| LVPECL_25                | 1.09              | 1.27 | N/A               | N/A   | N/A               | N/A   | ns    |
| RSDS_33 (point to point) | 1.24              | 1.42 | 1.71              | 1.91  | 3000              | 3000  | ns    |
| RSDS_25 (point to point) | 1.08              | 1.26 | 1.79              | 1.99  | 3000              | 3000  | ns    |
| TMDS_33                  | 1.29              | 1.47 | 1.68              | 1.88  | 3000              | 3000  | ns    |
| PPDS_33                  | 1.25              | 1.43 | 1.71              | 1.91  | 3000              | 3000  | ns    |
| PPDS_25                  | 1.08              | 1.26 | 1.82              | 2.02  | 3000              | 3000  | ns    |
| PCI33_3                  | 1.14              | 1.32 | 3.81              | 4.01  | 3.81              | 4.01  | ns    |
| PCI66_3                  | 1.14              | 1.32 | 3.81              | 4.01  | 3.81              | 4.01  | ns    |
| DISPLAY_PORT             | 1.09              | 1.27 | 3.29              | 3.49  | 3.29              | 3.49  | ns    |
| I2C                      | 1.40              | 1.58 | 11.70             | 11.90 | 11.70             | 11.90 | ns    |
| SMBUS                    | 1.40              | 1.58 | 11.70             | 11.90 | 11.70             | 11.90 | ns    |
| SDIO                     | 1.43              | 1.61 | 2.78              | 2.98  | 2.78              | 2.98  | ns    |
| MOBILE_DDR               | 1.01              | 1.19 | 2.50              | 2.70  | 2.50              | 2.70  | ns    |
| HSTL_I                   | 1.01              | 1.19 | 1.80              | 2.00  | 1.80              | 2.00  | ns    |
| HSTL_II                  | 1.01              | 1.19 | 1.86              | 2.06  | 1.86              | 2.06  | ns    |
| HSTL_III                 | 1.07              | 1.25 | 1.81              | 2.01  | 1.81              | 2.01  | ns    |
| HSTL_I_18                | 1.05              | 1.23 | 1.91              | 2.11  | 1.91              | 2.11  | ns    |
| HSTL_II_18               | 1.05              | 1.23 | 1.99              | 2.19  | 1.99              | 2.19  | ns    |
| HSTL_III_18              | 1.13              | 1.31 | 1.93              | 2.13  | 1.93              | 2.13  | ns    |
| SSTL3_I                  | 1.65              | 1.83 | 1.97              | 2.17  | 1.97              | 2.17  | ns    |
| SSTL3_II                 | 1.65              | 1.83 | 2.15              | 2.35  | 2.15              | 2.35  | ns    |
| SSTL2_I                  | 1.37              | 1.55 | 1.91              | 2.11  | 1.91              | 2.11  | ns    |
| SSTL2_II                 | 1.37              | 1.55 | 2.00              | 2.20  | 2.00              | 2.20  | ns    |
| SSTL18_I                 | 0.99              | 1.17 | 1.77              | 1.97  | 1.77              | 1.97  | ns    |
| SSTL18_II                | 1.00              | 1.18 | 1.80              | 2.00  | 1.80              | 2.00  | ns    |
| SSTL15_II                | 1.00              | 1.18 | 1.81              | 2.01  | 1.81              | 2.01  | ns    |
| DIFF_HSTL_I              | 1.01              | 1.19 | 1.91              | 2.11  | 1.91              | 2.11  | ns    |
| DIFF_HSTL_II             | 1.00              | 1.18 | 1.86              | 2.06  | 1.86              | 2.06  | ns    |
| DIFF_HSTL_III            | 1.00              | 1.18 | 1.83              | 2.03  | 1.83              | 2.03  | ns    |
| DIFF_HSTL_I_18           | 1.04              | 1.22 | 1.93              | 2.13  | 1.93              | 2.13  | ns    |
| DIFF_HSTL_II_18          | 1.04              | 1.22 | 1.83              | 2.03  | 1.83              | 2.03  | ns    |
| DIFF_HSTL_III_18         | 1.04              | 1.22 | 1.83              | 2.03  | 1.83              | 2.03  | ns    |



Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices<sup>(1)</sup> (Cont'd)

| I/O Standard                    | T <sub>IOPI</sub> |      | T <sub>IOOP</sub> |      | T <sub>IOTP</sub> |      | Units |
|---------------------------------|-------------------|------|-------------------|------|-------------------|------|-------|
|                                 | Speed Grade       |      | Speed Grade       |      | Speed Grade       |      |       |
|                                 | -3                | -2   | -3                | -2   | -3                | -2   |       |
| LVC MOS15, QUIETIO, 2 mA        | 1.05              | 1.23 | 5.63              | 5.83 | 5.63              | 5.83 | ns    |
| LVC MOS15, QUIETIO, 4 mA        | 1.05              | 1.23 | 4.75              | 4.95 | 4.75              | 4.95 | ns    |
| LVC MOS15, QUIETIO, 6 mA        | 1.05              | 1.23 | 4.21              | 4.41 | 4.21              | 4.41 | ns    |
| LVC MOS15, QUIETIO, 8 mA        | 1.05              | 1.23 | 4.05              | 4.25 | 4.05              | 4.25 | ns    |
| LVC MOS15, QUIETIO, 12 mA       | 1.05              | 1.23 | 3.74              | 3.94 | 3.74              | 3.94 | ns    |
| LVC MOS15, QUIETIO, 16 mA       | 1.05              | 1.23 | 3.52              | 3.72 | 3.52              | 3.72 | ns    |
| LVC MOS15, Slow, 2 mA           | 1.05              | 1.23 | 4.32              | 4.52 | 4.32              | 4.52 | ns    |
| LVC MOS15, Slow, 4 mA           | 1.05              | 1.23 | 3.58              | 3.78 | 3.58              | 3.78 | ns    |
| LVC MOS15, Slow, 6 mA           | 1.05              | 1.23 | 2.45              | 2.65 | 2.45              | 2.65 | ns    |
| LVC MOS15, Slow, 8 mA           | 1.05              | 1.23 | 2.46              | 2.66 | 2.46              | 2.66 | ns    |
| LVC MOS15, Slow, 12 mA          | 1.05              | 1.23 | 2.17              | 2.37 | 2.17              | 2.37 | ns    |
| LVC MOS15, Slow, 16 mA          | 1.05              | 1.23 | 2.15              | 2.35 | 2.15              | 2.35 | ns    |
| LVC MOS15, Fast, 2 mA           | 1.05              | 1.23 | 3.43              | 3.63 | 3.43              | 3.63 | ns    |
| LVC MOS15, Fast, 4 mA           | 1.05              | 1.23 | 2.42              | 2.62 | 2.42              | 2.62 | ns    |
| LVC MOS15, Fast, 6 mA           | 1.05              | 1.23 | 1.92              | 2.12 | 1.92              | 2.12 | ns    |
| LVC MOS15, Fast, 8 mA           | 1.05              | 1.23 | 1.87              | 2.07 | 1.87              | 2.07 | ns    |
| LVC MOS15, Fast, 12 mA          | 1.05              | 1.23 | 1.87              | 2.07 | 1.87              | 2.07 | ns    |
| LVC MOS15, Fast, 16 mA          | 1.05              | 1.23 | 1.87              | 2.07 | 1.87              | 2.07 | ns    |
| LVC MOS15_JEDEC, QUIETIO, 2 mA  | 1.10              | 1.28 | 5.64              | 5.84 | 5.64              | 5.84 | ns    |
| LVC MOS15_JEDEC, QUIETIO, 4 mA  | 1.10              | 1.28 | 4.75              | 4.95 | 4.75              | 4.95 | ns    |
| LVC MOS15_JEDEC, QUIETIO, 6 mA  | 1.10              | 1.28 | 4.21              | 4.41 | 4.21              | 4.41 | ns    |
| LVC MOS15_JEDEC, QUIETIO, 8 mA  | 1.10              | 1.28 | 4.06              | 4.26 | 4.06              | 4.26 | ns    |
| LVC MOS15_JEDEC, QUIETIO, 12 mA | 1.10              | 1.28 | 3.75              | 3.95 | 3.75              | 3.95 | ns    |
| LVC MOS15_JEDEC, QUIETIO, 16 mA | 1.10              | 1.28 | 3.53              | 3.73 | 3.53              | 3.73 | ns    |
| LVC MOS15_JEDEC, Slow, 2 mA     | 1.10              | 1.28 | 4.32              | 4.52 | 4.32              | 4.52 | ns    |
| LVC MOS15_JEDEC, Slow, 4 mA     | 1.10              | 1.28 | 3.56              | 3.76 | 3.56              | 3.76 | ns    |
| LVC MOS15_JEDEC, Slow, 6 mA     | 1.10              | 1.28 | 2.44              | 2.64 | 2.44              | 2.64 | ns    |
| LVC MOS15_JEDEC, Slow, 8 mA     | 1.10              | 1.28 | 2.47              | 2.67 | 2.47              | 2.67 | ns    |
| LVC MOS15_JEDEC, Slow, 12 mA    | 1.10              | 1.28 | 2.15              | 2.35 | 2.15              | 2.35 | ns    |
| LVC MOS15_JEDEC, Slow, 16 mA    | 1.10              | 1.28 | 2.15              | 2.35 | 2.15              | 2.35 | ns    |
| LVC MOS15_JEDEC, Fast, 2 mA     | 1.10              | 1.28 | 3.43              | 3.63 | 3.43              | 3.63 | ns    |
| LVC MOS15_JEDEC, Fast, 4 mA     | 1.10              | 1.28 | 2.42              | 2.62 | 2.42              | 2.62 | ns    |
| LVC MOS15_JEDEC, Fast, 6 mA     | 1.10              | 1.28 | 1.92              | 2.12 | 1.92              | 2.12 | ns    |
| LVC MOS15_JEDEC, Fast, 8 mA     | 1.10              | 1.28 | 1.87              | 2.07 | 1.87              | 2.07 | ns    |
| LVC MOS15_JEDEC, Fast, 12 mA    | 1.10              | 1.28 | 1.87              | 2.07 | 1.87              | 2.07 | ns    |
| LVC MOS15_JEDEC, Fast, 16 mA    | 1.10              | 1.28 | 1.87              | 2.07 | 1.87              | 2.07 | ns    |
| LVC MOS12, QUIETIO, 2 mA        | 0.98              | 1.16 | 6.54              | 6.74 | 6.54              | 6.74 | ns    |
| LVC MOS12, QUIETIO, 4 mA        | 0.98              | 1.16 | 5.12              | 5.32 | 5.12              | 5.32 | ns    |

Table 34: SSO Limit per  $V_{CCO}/GND$  Pair

| $V_{CCO}$ | I/O Standard             | Drive | Slew    | SSO Limit per $V_{CCO}/GND$ Pair                               |          |                                                                       |              |
|-----------|--------------------------|-------|---------|----------------------------------------------------------------|----------|-----------------------------------------------------------------------|--------------|
|           |                          |       |         | All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324 |          | All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324 |              |
|           |                          |       |         | Bank 0/2                                                       | Bank 1/3 | Bank 0/2                                                              | Bank 1/3/4/5 |
| 1.2V      | LVCMOS12, LVCMOS12_JEDEC | 2     | Fast    | 30 <sup>(1)</sup>                                              | 35       | 30                                                                    | 35           |
|           |                          |       | Slow    | 51                                                             | 55       | 51                                                                    | 52           |
|           |                          |       | QuietIO | 71                                                             | 58       | 71                                                                    | 70           |
|           |                          | 4     | Fast    | 17                                                             | 17       | 17                                                                    | 19           |
|           |                          |       | Slow    | 23                                                             | 25       | 23                                                                    | 22           |
|           |                          |       | QuietIO | 35                                                             | 32       | 35                                                                    | 32           |
|           |                          | 6     | Fast    | 13                                                             | 15       | 13                                                                    | 14           |
|           |                          |       | Slow    | 19                                                             | 20       | 19                                                                    | 17           |
|           |                          |       | QuietIO | 26                                                             | 24       | 26                                                                    | 24           |
|           |                          | 8     | Fast    | N/A                                                            | 12       | N/A                                                                   | 12           |
|           |                          |       | Slow    | N/A                                                            | 15       | N/A                                                                   | 13           |
|           |                          |       | QuietIO | N/A                                                            | 20       | N/A                                                                   | 19           |
|           |                          | 12    | Fast    | N/A                                                            | 5        | N/A                                                                   | 4            |
|           |                          |       | Slow    | N/A                                                            | 8        | N/A                                                                   | 5            |
|           |                          |       | QuietIO | N/A                                                            | 11       | N/A                                                                   | 10           |

## DSP48A1 Switching Characteristics

Table 44: DSP48A1 Switching Characteristics

| Symbol                                                                         | Description                                               | Pre-adder | Multiplier | Post-adder | Speed Grade    |                |                |                 | Units |
|--------------------------------------------------------------------------------|-----------------------------------------------------------|-----------|------------|------------|----------------|----------------|----------------|-----------------|-------|
|                                                                                |                                                           |           |            |            | -3             | -3N            | -2             | -1L             |       |
| Setup and Hold Times of Data/Control Pins to the Input Register Clock          |                                                           |           |            |            |                |                |                |                 |       |
| T <sub>DSPDCK_A_A1REG</sub> /<br>T <sub>DSPCKD_A_A1REG</sub>                   | A input to A1 register CLK                                | N/A       | N/A        | N/A        | 0.15/<br>0.09  | 0.17/<br>0.09  | 0.17/<br>0.09  | 0.32/<br>0.09   | ns    |
| T <sub>DSPDCK_D_B1REG</sub> /<br>T <sub>DSPCKD_D_B1REG</sub>                   | D input to B1 register CLK                                | Yes       | N/A        | N/A        | 1.90/<br>−0.07 | 1.95/<br>−0.07 | 1.95/<br>−0.07 | 2.82/<br>−0.07  | ns    |
| T <sub>DSPDCK_C_CREG</sub> /<br>T <sub>DSPCKD_C_CREG</sub>                     | C input to C register CLK for XC devices                  | N/A       | N/A        | N/A        | 0.11/<br>0.15  | 0.13/<br>0.15  | 0.13/<br>0.15  | 0.24/<br>0.09   | ns    |
|                                                                                | C input to C register CLK for XA and XQ devices           |           |            |            | 0.11/<br>0.19  | N/A            | 0.13/<br>0.23  | 0.24/<br>0.09   |       |
| T <sub>DSPDCK_D_DREG</sub> /<br>T <sub>DSPCKD_D_DREG</sub>                     | D input to D register CLK for XC devices                  | N/A       | N/A        | N/A        | 0.09/<br>0.15  | 0.10/<br>0.15  | 0.10/<br>0.15  | 0.19/<br>0.12   | ns    |
|                                                                                | D input to D register CLK for XA and XQ devices           |           |            |            | 0.09/<br>0.23  | N/A            | 0.10/<br>0.27  | 0.19/<br>0.12   |       |
| T <sub>DSPDCK_OPMODE_B1REG</sub> /<br>T <sub>DSPCKD_OPMODE_B1REG</sub>         | OPMODE input to B1 register CLK                           | Yes       | N/A        | N/A        | 1.97/<br>0.01  | 2.00/<br>0.01  | 2.00/<br>0.01  | 2.85/<br>0.01   | ns    |
| T <sub>DSPDCK_OPMODE_OPMODEREG</sub> /<br>T <sub>DSPCKD_OPMODE_OPMODEREG</sub> | OPMODE input to OPMODE register CLK for XC devices        | N/A       | N/A        | N/A        | 0.18/<br>0.12  | 0.21/<br>0.12  | 0.21/<br>0.12  | 0.40/<br>0.12   | ns    |
|                                                                                | OPMODE input to OPMODE register CLK for XA and XQ devices |           |            |            | 0.18/<br>0.16  | N/A            | 0.21/<br>0.22  | 0.40/<br>0.12   |       |
| Setup and Hold Times of Data Pins to the Pipeline Register Clock               |                                                           |           |            |            |                |                |                |                 |       |
| T <sub>DSPDCK_A_MREG</sub> /<br>T <sub>DSPCKD_A_MREG</sub>                     | A input to M register CLK                                 | N/A       | Yes        | N/A        | 3.06/<br>−0.40 | 3.51/<br>−0.40 | 3.51/<br>−0.40 | 3.97/<br>−0.40  | ns    |
| T <sub>DSPDCK_B_MREG</sub> /<br>T <sub>DSPCKD_B_MREG</sub>                     | B input to M register CLK                                 | Yes       | Yes        | N/A        | 3.96/<br>−0.68 | 4.58/<br>−0.68 | 4.58/<br>−0.68 | 7.00/<br>−0.68  | ns    |
| T <sub>DSPDCK_D_MREG</sub> /<br>T <sub>DSPCKD_D_MREG</sub>                     | D input to M register CLK                                 | Yes       | Yes        | N/A        | 4.23/<br>−0.56 | 4.80/<br>−0.56 | 4.80/<br>−0.56 | 6.84/<br>−0.56  | ns    |
| T <sub>DSPDCK_OPMODE_MREG</sub> /<br>T <sub>DSPCKD_OPMODE_MREG</sub>           | OPMODE to M register CLK                                  | Yes       | Yes        | N/A        | 4.18/<br>−0.48 | 4.80/<br>−0.48 | 4.80/<br>−0.48 | 6.88/<br>−0.48  | ns    |
|                                                                                |                                                           | No        | Yes        | N/A        | 2.37/<br>−0.48 | 2.70/<br>−0.48 | 2.70/<br>−0.48 | 4.28/<br>−0.48  | ns    |
| Setup and Hold Times of Data/Control Pins to the Output Register Clock         |                                                           |           |            |            |                |                |                |                 |       |
| T <sub>DSPDCK_A_PREG</sub> /<br>T <sub>DSPCKD_A_PREG</sub>                     | A input to P register CLK                                 | N/A       | Yes        | Yes        | 4.32/<br>−0.76 | 5.06/<br>−0.76 | 5.06/<br>−0.76 | 7.52/<br>−0.76  | ns    |
| T <sub>DSPDCK_B_PREG</sub> /<br>T <sub>DSPCKD_B_PREG</sub>                     | B input to P register CLK                                 | Yes       | Yes        | Yes        | 5.87/<br>−0.59 | 6.87/<br>−0.59 | 6.87/<br>−0.59 | 10.55/<br>−0.59 | ns    |
|                                                                                |                                                           | No        | Yes        | Yes        | 4.14/<br>−0.93 | 4.68/<br>−0.93 | 4.68/<br>−0.93 | 8.12/<br>−0.93  | ns    |
| T <sub>DSPDCK_C_PREG</sub> /<br>T <sub>DSPCKD_C_PREG</sub>                     | C input to P register CLK                                 | N/A       | N/A        | Yes        | 2.20/<br>−0.23 | 2.25/<br>−0.23 | 2.25/<br>−0.23 | 3.27/<br>−0.23  | ns    |
| T <sub>DSPDCK_D_PREG</sub> /<br>T <sub>DSPCKD_D_PREG</sub>                     | D input to P register CLK                                 | Yes       | Yes        | Yes        | 5.90/<br>−0.92 | 6.91/<br>−0.92 | 6.91/<br>−0.92 | 10.39/<br>−0.92 | ns    |

## DCM Switching Characteristics

Table 53: Operating Frequency Ranges and Conditions for the Delay-Locked Loop (DLL)<sup>(1)</sup>

| Symbol                                                               | Description                                                                                | Speed Grade      |                    |                  |                    |                  |                    |                  |                    | Units |  |
|----------------------------------------------------------------------|--------------------------------------------------------------------------------------------|------------------|--------------------|------------------|--------------------|------------------|--------------------|------------------|--------------------|-------|--|
|                                                                      |                                                                                            | -3               |                    | -3N              |                    | -2               |                    | -1L              |                    |       |  |
|                                                                      |                                                                                            | Min              | Max                | Min              | Max                | Min              | Max                | Min              | Max                |       |  |
| Input Frequency Ranges                                               |                                                                                            |                  |                    |                  |                    |                  |                    |                  |                    |       |  |
| CLKIN_FREQ_DLL                                                       | Frequency of the CLKIN clock input when the CLKDV output is not used.                      | 5 <sup>(2)</sup> | 280 <sup>(3)</sup> | 5 <sup>(2)</sup> | 280 <sup>(3)</sup> | 5 <sup>(2)</sup> | 250 <sup>(3)</sup> | 5 <sup>(2)</sup> | 175 <sup>(3)</sup> | MHz   |  |
|                                                                      | Frequency of the CLKIN clock input when using the CLKDV output.                            | 5 <sup>(2)</sup> | 280 <sup>(3)</sup> | 5 <sup>(2)</sup> | 280 <sup>(3)</sup> | 5 <sup>(2)</sup> | 250 <sup>(3)</sup> | 5 <sup>(2)</sup> | 133 <sup>(3)</sup> | MHz   |  |
| Input Pulse Requirements                                             |                                                                                            |                  |                    |                  |                    |                  |                    |                  |                    |       |  |
| CLKIN_PULSE                                                          | CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL < 150 MHz         | 40               | 60                 | 40               | 60                 | 40               | 60                 | 40               | 60                 | %     |  |
|                                                                      | CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL > 150 MHz         | 45               | 55                 | 45               | 55                 | 45               | 55                 | 45               | 55                 | %     |  |
| Input Clock Jitter Tolerance and Delay Path Variation <sup>(4)</sup> |                                                                                            |                  |                    |                  |                    |                  |                    |                  |                    |       |  |
| CLKIN_CYC_JITT_DLL_LF                                                | Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL < 150 MHz                      | –                | ±300               | –                | ±300               | –                | ±300               | –                | ±300               | ps    |  |
| CLKIN_CYC_JITT_DLL_HF                                                | Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL > 150 MHz.                     | –                | ±150               | –                | ±150               | –                | ±150               | –                | ±150               | ps    |  |
| CLKIN_PER_JITT_DLL                                                   | Period jitter at the CLKIN input.                                                          | –                | ±1                 | –                | ±1                 | –                | ±1                 | –                | ±1                 | ns    |  |
| CLKFB_DELAY_VAR_EXT                                                  | Allowable variation of the off-chip feedback delay from the DCM output to the CLKFB input. | –                | ±1                 | –                | ±1                 | –                | ±1                 | –                | ±1                 | ns    |  |

**Notes:**

- DLL specifications apply when using any of the DLL outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV.
- When operating independently of the DLL, the DFS supports lower CLKIN\_FREQ\_DLL frequencies. See Table 55.
- The CLKIN\_DIVIDE\_BY\_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the F<sub>MAX</sub> (see Table 48 and Table 49 for BUFG and BUFGIO2 limits). When used with CLK\_FEEDBACK=2X, the input clock frequency matches the frequency for CLK2X, and is limited to CLKOUT\_FREQ\_2X.
- CLKIN\_FREQ\_DLL input jitter beyond these limits can cause the DCM to lose LOCK, indicated by the LOCKED output deasserting. The user must then reset the DCM.
- When using both DCMs in a CMT, both DCMs must be LOCKED.

Table 57: Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM\_CLKGEN)<sup>(1)</sup> (Cont'd)

| Symbol                                                | Description                                                                                                              | Speed Grade                                                   |     |     |     |     |     |     |     | Units |
|-------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------|-----|-----|-----|-----|-----|-----|-----|-------|
|                                                       |                                                                                                                          | -3                                                            |     | -3N |     | -2  |     | -1L |     |       |
|                                                       |                                                                                                                          | Min                                                           | Max | Min | Max | Min | Max | Min | Max |       |
| Spread Spectrum                                       |                                                                                                                          |                                                               |     |     |     |     |     |     |     |       |
| F <sub>CLKIN_FIXED_SPREAD_SPECTRUM</sub>              | Frequency of the CLKIN input for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD/ CENTER_HIGH_SPREAD)         | 30                                                            | 200 | 30  | 200 | 30  | 200 | 30  | 200 | MHz   |
| T <sub>CENTER_LOW_SPREAD</sub> <sup>(6)</sup>         | Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD)                               | Typical = $\frac{100}{\text{CLKFX\_DIVIDE}}$<br>Maximum = 250 |     |     |     |     |     |     |     | ps    |
| T <sub>CENTER_HIGH_SPREAD</sub> <sup>(6)</sup>        | Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM= CENTER_HIGH_SPREAD)                               | Typical = $\frac{240}{\text{CLKFX\_DIVIDE}}$<br>Maximum = 400 |     |     |     |     |     |     |     | ps    |
| F <sub>MOD_FIXED_SPREAD_SPECTRUM</sub> <sup>(6)</sup> | Average modulation frequency when using fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD / CENTER_HIGH_SPREAD) | Typical = F <sub>IN</sub> /1024                               |     |     |     |     |     |     |     | MHz   |

**Notes:**

- The values in this table are based on the operating conditions described in Table 2 and Table 55.
- For optimal jitter tolerance and a faster LOCK time, use the CLKIN\_PERIOD attribute.
- Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
- The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
- Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of  $\pm(1\% \text{ of CLKFX period} + 200 \text{ ps})$ . Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is  $\pm(100 \text{ ps} + 200 \text{ ps}) = \pm 300 \text{ ps}$ .
- When using CENTER\_LOW\_SPREAD, CENTER\_HIGH\_SPREAD, the valid values for CLKFX\_MULTIPLY are limited to 2 through 32, and the valid values for CLKFX\_DIVIDE are limited to 1 through 4.

Table 58: Recommended Operating Conditions for the Phase-Shift Clock in Variable Phase Mode (DCM\_SP) or Dynamic Frequency Synthesis (DCM\_CLKGEN)

| Symbol                     | Description                                                                             | Speed Grade |     |     |     |     |     |     |     | Units |
|----------------------------|-----------------------------------------------------------------------------------------|-------------|-----|-----|-----|-----|-----|-----|-----|-------|
|                            |                                                                                         | -3          |     | -3N |     | -2  |     | -1L |     |       |
|                            |                                                                                         | Min         | Max | Min | Max | Min | Max | Min | Max |       |
| Operating Frequency Ranges |                                                                                         |             |     |     |     |     |     |     |     |       |
| PSCLK_FREQ                 | Frequency for the PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) input.                         | 1           | 167 | 1   | 167 | 1   | 167 | 1   | 100 | MHz   |
| Input Pulse Requirements   |                                                                                         |             |     |     |     |     |     |     |     |       |
| PSCLK_PULSE                | PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) pulse width as a percentage of the clock period. | 40          | 60  | 40  | 60  | 40  | 60  | 40  | 60  | %     |

Table 64: Global Clock Input to Output Delay With DCM in System-Synchronous Mode

| Symbol                                                                                                                                | Description                            | Device     | Speed Grade |      |      |      | Units |
|---------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|------------|-------------|------|------|------|-------|
|                                                                                                                                       |                                        |            | -3          | -3N  | -2   | -1L  |       |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in System-Synchronous Mode. |                                        |            |             |      |      |      |       |
| T <sub>ICKOFDCM</sub>                                                                                                                 | Global Clock and OUTFF <i>with</i> DCM | XC6SLX4    | 4.23        | N/A  | 6.11 | 6.60 | ns    |
|                                                                                                                                       |                                        | XC6SLX9    | 4.23        | 5.17 | 6.11 | 6.60 | ns    |
|                                                                                                                                       |                                        | XC6SLX16   | 4.28        | 4.57 | 5.34 | 6.36 | ns    |
|                                                                                                                                       |                                        | XC6SLX25   | 3.95        | 4.18 | 4.59 | 6.91 | ns    |
|                                                                                                                                       |                                        | XC6SLX25T  | 3.95        | 4.18 | 4.59 | N/A  | ns    |
|                                                                                                                                       |                                        | XC6SLX45   | 4.37        | 4.70 | 5.50 | 6.85 | ns    |
|                                                                                                                                       |                                        | XC6SLX45T  | 4.37        | 4.70 | 5.50 | N/A  | ns    |
|                                                                                                                                       |                                        | XC6SLX75   | 3.90        | 4.23 | 4.77 | 6.31 | ns    |
|                                                                                                                                       |                                        | XC6SLX75T  | 3.90        | 4.23 | 4.77 | N/A  | ns    |
|                                                                                                                                       |                                        | XC6SLX100  | 3.86        | 4.16 | 4.66 | 7.25 | ns    |
|                                                                                                                                       |                                        | XC6SLX100T | 3.90        | 4.16 | 4.66 | N/A  | ns    |
|                                                                                                                                       |                                        | XC6SLX150  | 4.03        | 4.33 | 4.83 | 6.63 | ns    |
|                                                                                                                                       |                                        | XC6SLX150T | 4.03        | 4.33 | 4.83 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX4    | 4.55        | N/A  | 6.11 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX9    | 4.55        | N/A  | 6.11 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX16   | 4.62        | N/A  | 5.33 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX25   | 4.27        | N/A  | 4.59 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX25T  | 4.27        | N/A  | 4.69 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX45   | 4.69        | N/A  | 5.50 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX45T  | 4.69        | N/A  | 5.50 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX75   | 4.22        | N/A  | 4.77 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX75T  | 4.22        | N/A  | 4.77 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX100  | N/A         | N/A  | 5.34 | N/A  | ns    |
|                                                                                                                                       |                                        | XQ6SLX75   | N/A         | N/A  | 4.77 | 6.31 | ns    |
|                                                                                                                                       |                                        | XQ6SLX75T  | 4.22        | N/A  | 4.77 | N/A  | ns    |
|                                                                                                                                       |                                        | XQ6SLX150  | N/A         | N/A  | 4.96 | 6.63 | ns    |
|                                                                                                                                       |                                        | XQ6SLX150T | 4.62        | N/A  | 4.96 | N/A  | ns    |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 66: Global Clock Input to Output Delay With PLL in System-Synchronous Mode

| Symbol                                                                                                                                | Description                            | Device     | Speed Grade |      |      |      | Units |
|---------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|------------|-------------|------|------|------|-------|
|                                                                                                                                       |                                        |            | -3          | -3N  | -2   | -1L  |       |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> PLL in System-Synchronous Mode. |                                        |            |             |      |      |      |       |
| T <sub>ICKOFFPLL</sub>                                                                                                                | Global Clock and OUTFF <i>with</i> PLL | XC6SLX4    | 4.57        | N/A  | 6.25 | 7.34 | ns    |
|                                                                                                                                       |                                        | XC6SLX9    | 4.57        | 5.25 | 6.25 | 7.34 | ns    |
|                                                                                                                                       |                                        | XC6SLX16   | 4.41        | 4.64 | 5.39 | 6.92 | ns    |
|                                                                                                                                       |                                        | XC6SLX25   | 4.03        | 4.32 | 4.91 | 7.64 | ns    |
|                                                                                                                                       |                                        | XC6SLX25T  | 4.03        | 4.32 | 4.91 | N/A  | ns    |
|                                                                                                                                       |                                        | XC6SLX45   | 4.63        | 4.96 | 5.75 | 7.36 | ns    |
|                                                                                                                                       |                                        | XC6SLX45T  | 4.63        | 4.96 | 5.75 | N/A  | ns    |
|                                                                                                                                       |                                        | XC6SLX75   | 4.01        | 4.30 | 4.88 | 7.15 | ns    |
|                                                                                                                                       |                                        | XC6SLX75T  | 4.01        | 4.30 | 4.88 | N/A  | ns    |
|                                                                                                                                       |                                        | XC6SLX100  | 4.02        | 4.33 | 4.90 | 7.37 | ns    |
|                                                                                                                                       |                                        | XC6SLX100T | 4.06        | 4.33 | 4.90 | N/A  | ns    |
|                                                                                                                                       |                                        | XC6SLX150  | 3.65        | 3.98 | 4.58 | 6.94 | ns    |
|                                                                                                                                       |                                        | XC6SLX150T | 3.65        | 3.98 | 4.58 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX4    | 4.88        | N/A  | 6.13 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX9    | 4.88        | N/A  | 6.13 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX16   | 4.74        | N/A  | 5.27 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX25   | 4.43        | N/A  | 4.78 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX25T  | 4.43        | N/A  | 4.88 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX45   | 4.94        | N/A  | 5.62 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX45T  | 4.94        | N/A  | 5.62 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX75   | 4.32        | N/A  | 4.77 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX75T  | 4.32        | N/A  | 4.77 | N/A  | ns    |
|                                                                                                                                       |                                        | XA6SLX100  | N/A         | N/A  | 5.41 | N/A  | ns    |
|                                                                                                                                       |                                        | XQ6SLX75   | N/A         | N/A  | 4.77 | 7.15 | ns    |
|                                                                                                                                       |                                        | XQ6SLX75T  | 4.32        | N/A  | 4.77 | N/A  | ns    |
|                                                                                                                                       |                                        | XQ6SLX150  | N/A         | N/A  | 4.60 | 6.94 | ns    |
|                                                                                                                                       |                                        | XQ6SLX150T | 4.35        | N/A  | 4.60 | N/A  | ns    |

**Notes:**

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
- PLL output jitter is included in the timing calculation.

Table 73: Global Clock Setup and Hold With DCM in Source-Synchronous Mode

| Symbol                                                                                     | Description                                                             | Device     | Speed Grade |           |           |           | Units |
|--------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|------------|-------------|-----------|-----------|-----------|-------|
|                                                                                            |                                                                         |            | -3          | -3N       | -2        | -1L       |       |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.(1) |                                                                         |            |             |           |           |           |       |
| T <sub>PSDCM0</sub> / T <sub>PHDCM0</sub>                                                  | No Delay Global Clock and IFF(2)<br>with DCM in Source-Synchronous Mode | XC6SLX4    | 0.71/0.65   | N/A       | 0.72/1.22 | 1.58/1.18 | ns    |
|                                                                                            |                                                                         | XC6SLX9    | 0.71/0.69   | 0.71/1.19 | 0.72/1.36 | 1.58/1.18 | ns    |
|                                                                                            |                                                                         | XC6SLX16   | 0.86/0.52   | 0.92/0.57 | 1.04/0.60 | 1.02/1.06 | ns    |
|                                                                                            |                                                                         | XC6SLX25   | 0.84/0.58   | 0.90/0.59 | 1.01/0.59 | 1.58/1.07 | ns    |
|                                                                                            |                                                                         | XC6SLX25T  | 0.84/0.58   | 0.90/0.59 | 1.01/0.59 | N/A       | ns    |
|                                                                                            |                                                                         | XC6SLX45   | 0.85/0.70   | 0.90/0.76 | 0.98/0.79 | 1.34/1.34 | ns    |
|                                                                                            |                                                                         | XC6SLX45T  | 0.85/0.70   | 0.90/0.76 | 0.98/0.79 | N/A       | ns    |
|                                                                                            |                                                                         | XC6SLX75   | 1.00/0.62   | 1.06/0.63 | 1.15/0.63 | 1.65/1.46 | ns    |
|                                                                                            |                                                                         | XC6SLX75T  | 1.00/0.71   | 1.06/0.72 | 1.15/0.72 | N/A       | ns    |
|                                                                                            |                                                                         | XC6SLX100  | 0.81/0.68   | 0.81/0.69 | 0.94/0.69 | 1.42/2.07 | ns    |
|                                                                                            |                                                                         | XC6SLX100T | 0.81/0.68   | 0.81/0.69 | 0.94/0.69 | N/A       | ns    |
|                                                                                            |                                                                         | XC6SLX150  | 0.68/0.98   | 0.69/0.99 | 0.79/0.99 | 1.45/1.60 | ns    |
|                                                                                            |                                                                         | XC6SLX150T | 0.68/0.98   | 0.69/0.99 | 0.79/0.99 | N/A       | ns    |
|                                                                                            |                                                                         | XA6SLX4    | 0.81/0.74   | N/A       | 0.72/1.36 | N/A       | ns    |
|                                                                                            |                                                                         | XA6SLX9    | 0.81/0.74   | N/A       | 0.72/1.36 | N/A       | ns    |
|                                                                                            |                                                                         | XA6SLX16   | 1.01/0.56   | N/A       | 1.04/0.60 | N/A       | ns    |
|                                                                                            |                                                                         | XA6SLX25   | 0.94/0.76   | N/A       | 1.06/0.77 | N/A       | ns    |
|                                                                                            |                                                                         | XA6SLX25T  | 0.94/0.76   | N/A       | 1.14/0.77 | N/A       | ns    |
|                                                                                            |                                                                         | XA6SLX45   | 0.86/0.74   | N/A       | 0.98/0.78 | N/A       | ns    |
|                                                                                            |                                                                         | XA6SLX45T  | 0.86/0.74   | N/A       | 0.98/0.78 | N/A       | ns    |
|                                                                                            |                                                                         | XA6SLX75   | 1.02/0.71   | N/A       | 1.15/0.72 | N/A       | ns    |
|                                                                                            |                                                                         | XA6SLX75T  | 1.02/0.71   | N/A       | 1.15/0.72 | N/A       | ns    |
|                                                                                            |                                                                         | XA6SLX100  | N/A         | N/A       | 1.37/0.75 | N/A       | ns    |
|                                                                                            |                                                                         | XQ6SLX75   | N/A         | N/A       | 1.15/0.72 | 1.65/1.46 | ns    |
|                                                                                            |                                                                         | XQ6SLX75T  | 1.02/0.71   | N/A       | 1.15/0.72 | N/A       | ns    |
|                                                                                            |                                                                         | XQ6SLX150  | N/A         | N/A       | 0.79/1.15 | 1.45/1.60 | ns    |
|                                                                                            |                                                                         | XQ6SLX150T | 0.73/1.15   | N/A       | 0.79/1.15 | N/A       | ns    |

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.



Table 74: Global Clock Setup and Hold With PLL in System-Synchronous Mode

| Symbol                                                                                                | Description                                                                      | Device     | Speed Grade |            |            |           | Units |
|-------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|------------|-------------|------------|------------|-----------|-------|
|                                                                                                       |                                                                                  |            | -3          | -3N        | -2         | -1L       |       |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. <sup>(1)</sup> |                                                                                  |            |             |            |            |           |       |
| T <sub>PSPLL</sub> / T <sub>PHPLL</sub>                                                               | No Delay Global Clock and IFF <sup>(2)</sup> with PLL in System-Synchronous Mode | XC6SLX4    | 1.37/0.25   | N/A        | 1.52/0.41  | 2.07/0.69 | ns    |
|                                                                                                       |                                                                                  | XC6SLX9    | 1.37/0.21   | 1.48/0.21  | 1.52/0.26  | 2.07/0.69 | ns    |
|                                                                                                       |                                                                                  | XC6SLX16   | 1.33/−0.03  | 1.53/−0.02 | 1.60/−0.02 | 1.57/0.48 | ns    |
|                                                                                                       |                                                                                  | XC6SLX25   | 1.65/0.28   | 1.71/0.28  | 1.91/0.28  | 2.44/0.76 | ns    |
|                                                                                                       |                                                                                  | XC6SLX25T  | 1.65/0.28   | 1.71/0.28  | 1.91/0.28  | N/A       | ns    |
|                                                                                                       |                                                                                  | XC6SLX45   | 1.55/0.18   | 1.64/0.18  | 1.75/0.18  | 2.02/0.90 | ns    |
|                                                                                                       |                                                                                  | XC6SLX45T  | 1.55/0.18   | 1.64/0.18  | 1.75/0.18  | N/A       | ns    |
|                                                                                                       |                                                                                  | XC6SLX75   | 1.77/0.21   | 1.89/0.21  | 2.13/0.21  | 2.46/0.53 | ns    |
|                                                                                                       |                                                                                  | XC6SLX75T  | 1.77/0.21   | 1.89/0.21  | 2.13/0.21  | N/A       | ns    |
|                                                                                                       |                                                                                  | XC6SLX100  | 1.44/0.32   | 1.52/0.32  | 1.70/0.32  | 1.78/0.86 | ns    |
|                                                                                                       |                                                                                  | XC6SLX100T | 1.44/0.32   | 1.52/0.32  | 1.70/0.32  | N/A       | ns    |
|                                                                                                       |                                                                                  | XC6SLX150  | 1.39/0.49   | 1.48/0.49  | 1.67/0.49  | 1.94/0.94 | ns    |
|                                                                                                       |                                                                                  | XC6SLX150T | 1.39/0.49   | 1.48/0.49  | 1.67/0.49  | N/A       | ns    |
|                                                                                                       |                                                                                  | XA6SLX4    | 1.61/0.10   | N/A        | 1.64/0.28  | N/A       | ns    |
|                                                                                                       |                                                                                  | XA6SLX9    | 1.61/0.10   | N/A        | 1.64/0.28  | N/A       | ns    |
|                                                                                                       |                                                                                  | XA6SLX16   | 1.89/−0.08  | N/A        | 1.72/−0.08 | N/A       | ns    |
|                                                                                                       |                                                                                  | XA6SLX25   | 1.85/0.16   | N/A        | 2.08/0.16  | N/A       | ns    |
|                                                                                                       |                                                                                  | XA6SLX25T  | 1.85/0.16   | N/A        | 2.17/0.16  | N/A       | ns    |
|                                                                                                       |                                                                                  | XA6SLX45   | 1.58/0.07   | N/A        | 1.87/0.03  | N/A       | ns    |
|                                                                                                       |                                                                                  | XA6SLX45T  | 1.58/0.07   | N/A        | 1.87/0.03  | N/A       | ns    |
|                                                                                                       |                                                                                  | XA6SLX75   | 1.80/0.06   | N/A        | 2.25/0.06  | N/A       | ns    |
|                                                                                                       |                                                                                  | XA6SLX75T  | 1.80/0.06   | N/A        | 2.25/0.06  | N/A       | ns    |
|                                                                                                       |                                                                                  | XA6SLX100  | N/A         | N/A        | 2.34/0.14  | N/A       | ns    |
|                                                                                                       |                                                                                  | XQ6SLX75   | N/A         | N/A        | 2.25/0.06  | 2.46/0.53 | ns    |
|                                                                                                       |                                                                                  | XQ6SLX75T  | 1.80/0.06   | N/A        | 2.25/0.06  | N/A       | ns    |
|                                                                                                       |                                                                                  | XQ6SLX150  | N/A         | N/A        | 1.79/0.37  | 1.94/0.94 | ns    |
|                                                                                                       |                                                                                  | XQ6SLX150T | 1.43/0.37   | N/A        | 1.79/0.37  | N/A       | ns    |

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 81: Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out Using BUFIO2 (Cont'd)

| Symbol                               | Description                         | Device     | Speed Grade |      |      |      | Units |
|--------------------------------------|-------------------------------------|------------|-------------|------|------|------|-------|
|                                      |                                     |            | -3          | -3N  | -2   | -1L  |       |
| Pin-to-Pin Clock-to-Out Using BUFIO2 |                                     |            |             |      |      |      |       |
| T <sub>ICKO</sub> FCS                | OFF clock-to-out using BUFIO2 clock | XC6SLX4    | 5.51        | N/A  | 6.95 | 8.45 | ns    |
|                                      |                                     | XC6SLX9    | 5.51        | 5.89 | 6.95 | 8.45 | ns    |
|                                      |                                     | XC6SLX16   | 5.31        | 5.70 | 6.67 | 8.21 | ns    |
|                                      |                                     | XC6SLX25   | 5.53        | 6.00 | 7.02 | 8.72 | ns    |
|                                      |                                     | XC6SLX25T  | 5.53        | 6.00 | 7.02 | N/A  | ns    |
|                                      |                                     | XC6SLX45   | 5.76        | 6.18 | 7.22 | 8.77 | ns    |
|                                      |                                     | XC6SLX45T  | 5.76        | 6.18 | 7.22 | N/A  | ns    |
|                                      |                                     | XC6SLX75   | 5.94        | 6.46 | 7.57 | 9.72 | ns    |
|                                      |                                     | XC6SLX75T  | 5.94        | 6.46 | 7.57 | N/A  | ns    |
|                                      |                                     | XC6SLX100  | 6.09        | 6.53 | 7.60 | 9.66 | ns    |
|                                      |                                     | XC6SLX100T | 6.09        | 6.53 | 7.60 | N/A  | ns    |
|                                      |                                     | XC6SLX150  | 6.29        | 6.69 | 7.81 | 9.94 | ns    |
|                                      |                                     | XC6SLX150T | 6.29        | 6.69 | 7.81 | N/A  | ns    |
|                                      |                                     | XA6SLX4    | 5.83        | N/A  | 6.95 | N/A  | ns    |
|                                      |                                     | XA6SLX9    | 5.83        | N/A  | 6.95 | N/A  | ns    |
|                                      |                                     | XA6SLX16   | 5.65        | N/A  | 6.68 | N/A  | ns    |
|                                      |                                     | XA6SLX25   | 5.85        | N/A  | 7.03 | N/A  | ns    |
|                                      |                                     | XA6SLX25T  | 5.85        | N/A  | 7.03 | N/A  | ns    |
|                                      |                                     | XA6SLX45   | 6.07        | N/A  | 7.25 | N/A  | ns    |
|                                      |                                     | XA6SLX45T  | 6.07        | N/A  | 7.25 | N/A  | ns    |
|                                      |                                     | XA6SLX75   | 6.26        | N/A  | 7.57 | N/A  | ns    |
|                                      |                                     | XA6SLX75T  | 6.26        | N/A  | 7.57 | N/A  | ns    |
|                                      |                                     | XA6SLX100  | N/A         | N/A  | 7.48 | N/A  | ns    |
|                                      |                                     | XQ6SLX75   | N/A         | N/A  | 7.57 | 9.72 | ns    |
|                                      |                                     | XQ6SLX75T  | 6.26        | N/A  | 7.57 | N/A  | ns    |
|                                      |                                     | XQ6SLX150  | N/A         | N/A  | 7.81 | 9.94 | ns    |
|                                      |                                     | XQ6SLX150T | 6.62        | N/A  | 7.81 | N/A  | ns    |

## Revision History

The following table shows the revision history for this document.

| Date     | Version | Description of Revisions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 06/24/09 | 1.0     | Initial Xilinx release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 08/26/09 | 1.1     | Added $V_{FS}$ to <a href="#">Table 1</a> and <a href="#">Table 2</a> . Added $R_{FUSE}$ to <a href="#">Table 2</a> . Added XC6SLX75 and XC6SLX75T to $V_{BATT}$ and $I_{BATT}$ in <a href="#">Table 1</a> , <a href="#">Table 2</a> , and <a href="#">Table 4</a> . Corrected the quiescent supply current for the XC6SLX4 in <a href="#">Table 5</a> . Updated <a href="#">Table 11</a> . Removed $DV_{PPIN}$ from <a href="#">Figure 2</a> . Removed $F_{PCIECORE}$ from <a href="#">Table 24</a> and added values to $F_{PCIEUSER}$ . Added more networking applications to <a href="#">Table 25</a> . Updated values for $T_{SUSPENDLOW\_AWAKE}$ , $T_{SUSPEND\_ENABLE}$ , and $T_{SCP\_AWAKE}$ in <a href="#">Table 46</a> . Numerous changes to <a href="#">Table 47</a> , <a href="#">page 54</a> including the addition of new values to various specifications, revising the $T_{SMCKCSO}$ description, and changing the units of $T_{POR}$ . Also, removed <i>Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK</i> section from <a href="#">Table 47</a> and updated all the notes. In <a href="#">Table 52</a> , added to $F_{INMAX}$ , revised $F_{OUTMAX}$ , and removed PLL Maximum Output Frequency for BUFIO2. Revised values for DCM_DELAY_STEP in <a href="#">Table 54</a> . Updated CLKIN_FREQ_FX values in <a href="#">Table 55</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 01/04/10 | 1.2     | Added -4 speed grade to entire document. Updated speed specification of -4, -3, -2 speed grades to version 1.03. Added -1L speed grade numbers per speed specification 1.00. Updated $T_{SOL}$ in <a href="#">Table 1</a> . Added -1L rows for LVCMOS12, LVCMOS15, and LVCMOS18 in <a href="#">Table 9</a> . Revised much of the detail in <a href="#">GTP Transceiver Specifications</a> in <a href="#">Table 12</a> through <a href="#">Table 23</a> . Added -2 data to <a href="#">Table 25</a> . Updated $F_{MAX}$ in <a href="#">Table 44</a> . Updated descriptions for $T_{DNACKL}$ and $T_{DNACKH}$ in <a href="#">Table 45</a> and revised values for all parameters. Removed $T_{INITADDR}$ from <a href="#">Table 47</a> and added new data. Updated values in <a href="#">Table 48</a> through <a href="#">Table 62</a> . Added <a href="#">Table 51</a> (BUFPLL) and <a href="#">Table 57</a> (DCM_CLKGEN). Removed $T_{LOCKMAX}$ note from <a href="#">Table 52</a> . Updated note 3 in <a href="#">Table 53</a> . In <a href="#">Table 79</a> : removed XC6SLX75CSG324 and XC6SLX75TCSG324; added XC6SLX75FG(G)484 and XC6SLX75FG(G)484.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 02/22/10 | 1.3     | Production release of XC6SLX16 -2 speed grade devices. The changes to <a href="#">Table 26</a> and <a href="#">Table 27</a> includes updating this data sheet to the data in ISE v11.5 software with speed specification v1.06. Updated maximum of $V_{IN}$ and $V_{TS}$ and note 2 in <a href="#">Table 1</a> . In <a href="#">Table 2</a> , changed $V_{IN}$ , added $I_{IN}$ and note 5, revised notes 1, 6, and 7, and added note 8 to $R_{FUSE}$ . In <a href="#">Table 4</a> , removed previous note 1 and added data to $I_{RPU}$ , $I_{RPD}$ , and $I_{BATT}$ , changed $C_{IN}$ , added $R_{DT}$ and $R_{IN\_TERM}$ , and added note 2 and 3. Updated $V_{CCO2}$ in <a href="#">Table 6</a> . Added <a href="#">Table 7</a> and <a href="#">Table 8</a> . Removed PCI66_3 from <a href="#">Table 9</a> . Updated PCI33_3 and I2C in <a href="#">Table 9</a> . Updated the description of <a href="#">Table 11</a> . Completely updated <a href="#">Table 25</a> . Updated <a href="#">Table 28</a> including adding values for PCI33_3. Updated $V_{REF}$ value for HSTL_III_18 in <a href="#">Table 31</a> . Updates missing $V_{REF}$ values in <a href="#">Table 32</a> . Added <a href="#">Simultaneously Switching Outputs</a> , <a href="#">page 36</a> . Removed $T_{GSRQ}$ and $T_{RPW}$ from <a href="#">Table 35</a> and <a href="#">Table 36</a> . Also removed $T_{DOQ}$ from <a href="#">Table 36</a> . Removed $T_{ISDO\_DO}$ and note 1 from <a href="#">Table 37</a> . Removed $T_{OSCK\_S}$ and combinatorial section from <a href="#">Table 38</a> . In <a href="#">Table 39</a> , removed $T_{IODDO\_T}$ and added new tap parameters and note 2. In <a href="#">Table 40</a> , <a href="#">Table 41</a> , and <a href="#">Table 42</a> , made typographical edits and removed notes. Removed clock CLK section in <a href="#">Table 41</a> . Removed clock CLK section and $T_{REG\_MUX}$ and $T_{REG\_M31}$ in <a href="#">Table 42</a> . Added block RAM $F_{MAX}$ values to <a href="#">Table 43</a> . Updated values and added note 2 to <a href="#">Table 45</a> . Added values to <a href="#">Table 46</a> and removed note 1. Numerous changes to <a href="#">Table 47</a> . Completely updated <a href="#">Table 57</a> . Revised data in <a href="#">Table 62</a> . Removed note 3 from <a href="#">Table 71</a> . Added values to <a href="#">Table 79</a> . Added data to <a href="#">Table 80</a> and <a href="#">Table 81</a> . |
| 03/10/10 | 1.4     | Production release of XC6SLX45 -2 speed grade devices, which includes changes to <a href="#">Table 26</a> and <a href="#">Table 27</a> updating this data sheet to the data in ISE v11.5 software with speed specification v1.07. Fixed $R_{IN\_TERM}$ description in <a href="#">Table 4</a> . Added PCI66_3 to <a href="#">Table 7</a> and replaced note 1. Corrected note 1 and the V, Max for TMDS_33 in <a href="#">Table 8</a> . In <a href="#">Table 10</a> , added note 1 to LVPECL_33 and TMDS_33. Also updated specifications for TMDS_33. Updated the <a href="#">GTP Transceiver Specifications</a> section including adding values to <a href="#">Table 16</a> , <a href="#">Table 17</a> , and <a href="#">Table 20</a> through <a href="#">Table 23</a> . Added PCI66_3 back into <a href="#">Table 9</a> , <a href="#">Table 28</a> , <a href="#">Table 31</a> , <a href="#">Table 32</a> , and <a href="#">Table 34</a> . Updated note 3 on <a href="#">Table 32</a> . In <a href="#">Table 34</a> , corrected some typographical errors and fixed SSO limits for bank1/3 in FG(G)484 package. Corrected $T_{OSCK\_OCE}$ in <a href="#">Table 38</a> . In <a href="#">Table 57</a> , updated CLKFX_FREEZE_VAR and CLKFX_FREEZE_TEMP_SLOPE and added typical values to $T_{CENTER\_LOW\_SPREAD}$ and $T_{CENTER\_HIGH\_SPREAD}$ . Updated and added values to <a href="#">Table 63</a> through <a href="#">Table 78</a> , and <a href="#">Table 81</a> . In <a href="#">Table 79</a> , revised the XC6SLX16-CSG324 and the XC6SLX45-CSG484 and FG(G)484 values.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

| Date     | Version | Description of Revisions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 06/14/10 | 1.5     | <p>In <a href="#">Table 2</a>, added note 5 and added temperature range to <math>V_{FS}</math> and <math>R_{FUSE}</math>. Removed speed grade delineation, revised <math>I_{RPD}</math> description, and updated note 2 in <a href="#">Table 4</a>. Added note 2 to <a href="#">Table 7</a>. Added <math>DIFF\_MOBILE\_DDR</math> to <a href="#">Table 8</a> and <a href="#">Table 10</a>. Added note 4 to <a href="#">Table 15</a>. Changed minimum <math>DV_{PPIN}</math> in <a href="#">Table 16</a>. Updated <math>F_{GTPDRCLK}</math> in <a href="#">Table 19</a>. Increased maximum <math>T_{LLSKEW}</math> in <a href="#">Table 22</a>. Updated descriptions and added data to <a href="#">Table 23</a>. Removed note 1 and added new data to the Networking Applications section in <a href="#">Table 25</a>. Updated <a href="#">Table 26</a> and <a href="#">Table 27</a> to the data in ISE v12.1 software with speed specification v1.08. In <a href="#">Table 28</a>, added <math>DIFF\_MOBILE\_DDR</math> and updated -4 speed grade data. Updated the maximum I/O pairs per bank in <a href="#">Table 33</a>. Updated note 2 on <a href="#">Table 39</a>. Revised the <math>F_{MAX}</math> in <a href="#">Table 44</a>. In <a href="#">Table 47</a>, updated description for <math>T_{SMCKCSO}</math>, revised values for <math>T_{POR}</math> and added Min value, added <math>T_{BPIICCK}</math> and <math>T_{SPIICCK}</math>. Also in <a href="#">Table 47</a>, added device dependencies to <math>F_{SMCKCK}</math> and <math>F_{RBCKCK}</math>. Updated and added data to <a href="#">Table 63</a> through <a href="#">Table 78</a>, and <a href="#">Table 81</a>. In <a href="#">Table 79</a>, added data on the XC6SLX45-FG(G)676 and revised the XC6SLX45T and XC6SLX150T values.</p> <p>The following changes to this specification are addressed in the product change notice <a href="#">XC6SLX45-FG(G)676</a>, <i>MCB Performance and JTAG Revision Code for Spartan-6 LX16 and LX45 FPGAs</i>. In <a href="#">Table 2</a>, revised the <math>V_{CCINT}</math> to add the memory controller block extended performance specifications. In <a href="#">Table 25</a>, changed the standard specifications and added extended performance specifications for the memory controller block and note 2. Added note 4 and updated values in <a href="#">Table 34</a>.</p> |
| 06/24/10 | 1.6     | <p>Production release of XC6SLX45T (-2 and -3 speed grades), XC6SLX16 and XC6SLX45 (-3 speed grade) devices which includes changes to <a href="#">Table 26</a> and <a href="#">Table 27</a> (ISE v12.1 software with speed specification v1.08).</p> <p>Added the -3N speed grade, which designates Spartan-6 devices that do not support MCB functionality. This includes changes to <a href="#">Table 2</a> (note 2), <a href="#">Table 25</a> (note 4), and <a href="#">Switching Characteristics</a> (<a href="#">Table 26</a>).</p> <p>Updated <a href="#">Simultaneously Switching Outputs</a> discussion. Added -3 speed grade values for <math>T_{TAP}</math> and <math>F_{MINCAL}</math> values in <a href="#">Table 39</a>. In <a href="#">Table 40</a>, updated <math>T_{RPW}</math> (-2 and -3 speed grade) values and <math>F_{TOG}</math> (-3 speed grade) values. In <a href="#">Table 48</a>, updated <math>T_{GIO}</math> (-2 and -3 speed grade) values. Updated -3 values in spread spectrum section of <a href="#">Table 57</a>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 07/16/10 | 1.7     | <p>Production release of specific devices listed in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v12.2 software with speed specification v1.11. Added note 4 advising designers of the patch which contains v1.11. Also updated the -1L speed specification to v1.04. Updated numerous -4 and -1L values. Added -4 <math>T_{TAP}</math> values and <math>F_{MINCAL}</math> to <a href="#">Table 39</a>. Revised <math>T_{CINCK}/T_{CKCIN}</math> in <a href="#">Table 40</a>. In <a href="#">Table 41</a>, revised <math>T_{SHCKO}</math>. In <a href="#">Table 42</a>, revised <math>T_{REQ}</math>. Added new -1L values to <a href="#">Table 47</a>. Added and updated values in <a href="#">Table 79</a>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 07/26/10 | 1.8     | <p>Production release of XC6SLX25, XC6SLX25T, XC6SLX100 and XC6SLX100T in the specific speed grades listed in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v12.2 software with speed specification v1.11. Added note 7 to <a href="#">Table 2</a> and moved <math>V_{FS}</math> and <math>R_{FUSE}</math> to a new <a href="#">Table 3</a>. Added <math>I_{HS}</math> and note 4 to <a href="#">Table 4</a>. Added note 1 to <a href="#">Table 28</a>. Added and updated SSO limits per <math>V_{CCO}/GND</math> pairs in <a href="#">Table 34</a>. Added note 3 to <a href="#">Table 47</a>. In <a href="#">Table 54</a>, removed -1L specifications for <math>CLKOUT\_PER\_JITT\_DV1/2</math> and revised <math>CLKIN\_CLKFB\_PHASE</math> and <math>CLKOUT\_PHASE\_DLL</math> values. Updated note 3 in both <a href="#">Table 56</a> and <a href="#">Table 57</a>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 08/23/10 | 1.9     | <p>Updated values for <math>F_{GTPRANGE1}</math>, <math>F_{GTPRANGE2}</math>, and <math>F_{GPLLMIN}</math> in <a href="#">Table 18</a>. Revised -3 and -4 values in <a href="#">Table 21</a>. Removed the -1L speed grade readback support restriction and note 3 in <a href="#">Table 47</a>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 11/05/10 | 1.10    | <p>Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v12.3 software with speed specification v1.12 for the -2 speed grade available in the 12.3 <i>Speed Files Patch</i>. Added note 3 advising designers of the patch which contains v1.12.</p> <p>In <a href="#">Table 2</a>, added note 4. In <a href="#">Table 4</a>, added note 2. In <a href="#">Table 10</a>, added notes 2 and 3. In <a href="#">Table 44</a>, added note 2. In <a href="#">Table 47</a>, updated symbol for <math>T_{SMWCKCK}/T_{SMCKCKW}</math>, changed -1L values for <math>T_{USERCCLKH}</math> and <math>T_{USERCCLKL}</math>, and added and revised the modes for <math>F_{MCKCK}</math> and <math>F_{SMCKCK}</math>. In <a href="#">Table 53</a>, redefined and expanded description for <math>CLKIN\_FREQ\_DLL</math> and rewrote note 3. Updated title of <a href="#">Table 58</a>. Also in <a href="#">Table 78</a>, revised <math>T_{DCD\_CLK}</math> for XC6SLX150 and XC6SLX150T. Changed description of <math>T_{PSFD}/T_{PHFD}</math> in <a href="#">Table 71</a>.</p> <p>For the -1L speed grade, updated data sheet to ISE 12.3 software with speed specification v1.05 which revised the values in the following tables: <a href="#">Table 25</a>, <a href="#">Table 28</a>, <a href="#">Table 35</a>, <a href="#">Table 36</a>, <a href="#">Table 37</a>, <a href="#">Table 40</a> through <a href="#">Table 43</a>, <a href="#">Table 48</a> through <a href="#">Table 56</a>, <a href="#">Table 62</a> through <a href="#">Table 78</a>, <a href="#">Table 80</a>, and <a href="#">Table 81</a>. Updated <a href="#">Notice of Disclaimer</a>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

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