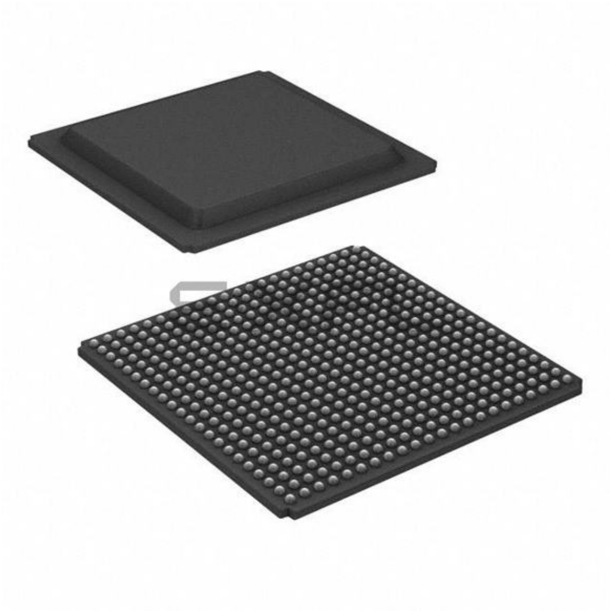
AMD Xilinx - XC6SLX25T-2FG484I Datasheet



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Details	
Product Status	Active
Number of LABs/CLBs	1879
Number of Logic Elements/Cells	24051
Total RAM Bits	958464
Number of I/O	250
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx25t-2fg484i

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In Table 9 and Table 10, values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: **Single-Ended I/O Standard DC Input and Output Levels**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL	–0.5	0.8	2.0	4.1	0.4	2.4	Note 2	Note 2
LVCMOS33	–0.5	0.8	2.0	4.1	0.4	V_{CCO} – 0.4	Note 2	Note 2
LVCMOS25	–0.5	0.7	1.7	4.1	0.4	V_{CCO} – 0.4	Note 2	Note 2
LVCMOS18	–0.5	0.38	0.8	4.1	0.45	V_{CCO} – 0.45	Note 2	Note 2
LVCMOS18 (-1L)	–0.5	0.33	0.71	4.1	0.45	V_{CCO} – 0.45	Note 2	Note 2
LVCMOS18_JEDEC	–0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.45	V_{CCO} – 0.45	Note 2	Note 2
LVCMOS15	–0.5	0.38	0.8	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVCMOS15 (-1L)	–0.5	0.33	0.71	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVCMOS15_JEDEC	–0.5	35% V_{CCO}	65% V_{CCO}	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVCMOS12	–0.5	0.38	0.8	4.1	0.4	V_{CCO} – 0.4	Note 4	Note 4
LVCMOS12 (-1L)	–0.5	0.33	0.71	4.1	0.4	V_{CCO} – 0.4	Note 4	Note 4
LVCMOS12_JEDEC	–0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.4	V_{CCO} – 0.4	Note 4	Note 4
PCI33_3	–0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
PCI66_3	–0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
I2C	–0.5	25% V_{CCO}	70% V_{CCO}	4.1	20% V_{CCO}	–	3	–
SMBUS	–0.5	0.8	2.1	4.1	0.4	–	4	–
SDIO	–0.5	12.5% V_{CCO}	75% V_{CCO}	4.1	12.5% V_{CCO}	75% V_{CCO}	0.1	–0.1
MOBILE_DDR	–0.5	20% V_{CCO}	80% V_{CCO}	4.1	10% V_{CCO}	90% V_{CCO}	0.1	–0.1
HSTL_I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	8	–8
HSTL_II	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	16	–16
HSTL_III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	24	–8
HSTL_I_18	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	11	–11
HSTL_II_18	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	22	–22
HSTL_III_18	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	30	–11
SSTL3_I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	4.1	V_{TT} – 0.6	V_{TT} + 0.6	8	–8
SSTL3_II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	4.1	V_{TT} – 0.8	V_{TT} + 0.8	16	–16
SSTL2_I	–0.5	V_{REF} – 0.15	V_{REF} + 0.15	4.1	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2_II	–0.5	V_{REF} – 0.15	V_{REF} + 0.15	4.1	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL18_I	–0.5	V_{REF} – 0.125	V_{REF} + 0.125	4.1	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18_II	–0.5	V_{REF} – 0.125	V_{REF} + 0.125	4.1	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
SSTL15_II	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	V_{TT} – 0.4	V_{TT} + 0.4	13.4	–13.4

Notes:

1. Tested according to relevant specifications.
2. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
3. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
4. Using drive strengths of 2, 4, 6, 8, or 12 mA.
5. For more information, refer to UG381: *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 14: **GTP Transceiver Current Supply (per Lane)**

Symbol	Description	Typ(1)	Max	Units
$I_{MGTAVCC}$	GTP transceiver internal analog supply current	40.4	Note 2	mA
$I_{MGTAVTTTX}$	GTP transmitter termination supply current	27.4		mA
$I_{MGTAVTTRX}$	GTP receiver termination supply current	13.6		mA
$I_{MGTAVCCPLL}$	GTP transmitter and receiver PLL supply current	28.7		mA
$R_{MGTRREF}$	Precision reference resistor for internal calibration termination	50.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 2.5 Gb/s line rate, with a shared PLL use mode.
2. Values for currents of other transceiver configurations and conditions can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 15: **GTP Transceiver Quiescent Supply Current (per Lane)(1)(2)(3)(4)**

Symbol	Description	Typ(5)	Max	Units
$I_{MGTAVCCQ}$	Quiescent MGTAVCC supply current	1.7	Note 2	mA
$I_{MGTAVTTTXQ}$	Quiescent MGTAVTTTX supply current	0.1		mA
$I_{MGTAVTTRXQ}$	Quiescent MGTAVTTRX supply current	1.2		mA
$I_{MGTAVCCPLLQ}$	Quiescent MGTAVCCPLL supply current	1.0		mA

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
3. GTP transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTP transceivers.
4. Does not include power-up MGTAVTTRCAL supply current during device configuration.
5. Typical values are specified at nominal voltage, 25°C.

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.20 for -3, -3N, and -2; and v1.08 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

The -1L speed grade refers to the lower-power Spartan-6 devices. The -3N speed grade refers to the Spartan-6 devices that do not support MCB functionality.

Table 26 correlates the current status of each Spartan-6 device on a per speed grade basis.

Table 26: **Spartan-6 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	**Preliminary**	**Production**
XC6SLX4[1]			-3, -2, -1L
XC6SLX9			-3, -3N, -2, -1L
XC6SLX16			-3, -3N, -2, -1L
XC6SLX25			-3, -3N, -2, -1L
XC6SLX25T			-3, -3N, -2
XC6SLX45			-3, -3N, -2, -1L
XC6SLX45T			-3, -3N, -2
XC6SLX75			-3, -3N, -2, -1L
XC6SLX75T			-3, -3N, -2
XC6SLX100			-3, -3N, -2, -1L
XC6SLX100T			-3, -3N, -2
XC6SLX150			-3, -3N, -2, -1L
XC6SLX150T			-3, -3N, -2
XA6SLX4			-3, -2
XA6SLX9			-3, -2
XA6SLX16			-3, -2
XA6SLX25			-3, -2
XA6SLX25T			-3, -2
XA6SLX45			-3, -2
XA6SLX45T			-3, -2
XA6SLX75			-3, -2
XA6SLX75T			-3, -2
XA6SLX100			-2
XQ6SLX75			-2, -1L
XQ6SLX75T			-3, -2
XQ6SLX150			-2, -1L
XQ6SLX150T			-3, -2

Notes:

1. The XC6SLX4 is not available in the -3N speed grade.

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-6 devices.

Table 29: **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices[1]** ***(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVCMOS33, Slow, 6 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVCMOS33, Slow, 8 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVCMOS33, Slow, 12 mA	1.41	1.59	2.53	2.73	2.53	2.73	ns
LVCMOS33, Slow, 16 mA	1.41	1.59	2.45	2.65	2.45	2.65	ns
LVCMOS33, Slow, 24 mA	1.41	1.59	2.42	2.62	2.42	2.62	ns
LVCMOS33, Fast, 2 mA	1.41	1.59	4.05	4.25	4.05	4.25	ns
LVCMOS33, Fast, 4 mA	1.41	1.59	2.66	2.86	2.66	2.86	ns
LVCMOS33, Fast, 6 mA	1.41	1.59	2.46	2.66	2.46	2.66	ns
LVCMOS33, Fast, 8 mA	1.41	1.59	2.21	2.41	2.21	2.41	ns
LVCMOS33, Fast, 12 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVCMOS33, Fast, 16 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVCMOS33, Fast, 24 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVCMOS25, QUIETIO, 2 mA	0.89	1.07	5.00	5.20	5.00	5.20	ns
LVCMOS25, QUIETIO, 4 mA	0.89	1.07	3.85	4.05	3.85	4.05	ns
LVCMOS25, QUIETIO, 6 mA	0.89	1.07	3.60	3.80	3.60	3.80	ns
LVCMOS25, QUIETIO, 8 mA	0.89	1.07	3.34	3.54	3.34	3.54	ns
LVCMOS25, QUIETIO, 12 mA	0.89	1.07	2.98	3.18	2.98	3.18	ns
LVCMOS25, QUIETIO, 16 mA	0.89	1.07	2.79	2.99	2.79	2.99	ns
LVCMOS25, QUIETIO, 24 mA	0.89	1.07	2.64	2.84	2.64	2.84	ns
LVCMOS25, Slow, 2 mA	0.89	1.07	3.96	4.16	3.96	4.16	ns
LVCMOS25, Slow, 4 mA	0.89	1.07	2.96	3.16	2.96	3.16	ns
LVCMOS25, Slow, 6 mA	0.89	1.07	2.88	3.08	2.88	3.08	ns
LVCMOS25, Slow, 8 mA	0.89	1.07	2.63	2.83	2.63	2.83	ns
LVCMOS25, Slow, 12 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVCMOS25, Slow, 16 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVCMOS25, Slow, 24 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVCMOS25, Fast, 2 mA	0.89	1.07	3.52	3.72	3.52	3.72	ns
LVCMOS25, Fast, 4 mA	0.89	1.07	2.43	2.63	2.43	2.63	ns
LVCMOS25, Fast, 6 mA	0.89	1.07	2.23	2.43	2.23	2.43	ns
LVCMOS25, Fast, 8 mA	0.89	1.07	2.16	2.36	2.16	2.36	ns
LVCMOS25, Fast, 12 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVCMOS25, Fast, 16 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVCMOS25, Fast, 24 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVCMOS18, QUIETIO, 2 mA	1.25	1.43	6.11	6.31	6.11	6.31	ns
LVCMOS18, QUIETIO, 4 mA	1.25	1.43	4.88	5.08	4.88	5.08	ns
LVCMOS18, QUIETIO, 6 mA	1.25	1.43	4.20	4.40	4.20	4.40	ns
LVCMOS18, QUIETIO, 8 mA	1.25	1.43	3.86	4.06	3.86	4.06	ns
LVCMOS18, QUIETIO, 12 mA	1.25	1.43	3.49	3.69	3.49	3.69	ns

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 4 and Figure 5.

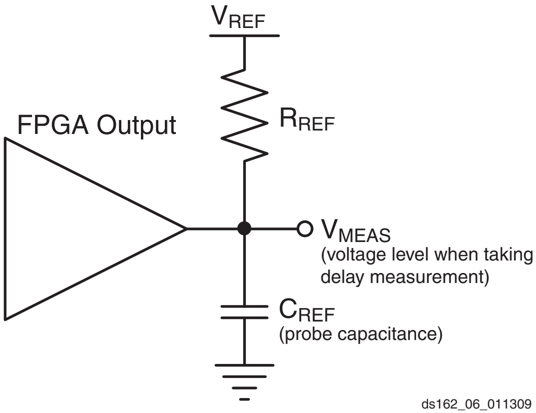

Figure 4: **Single-Ended Test Setup**

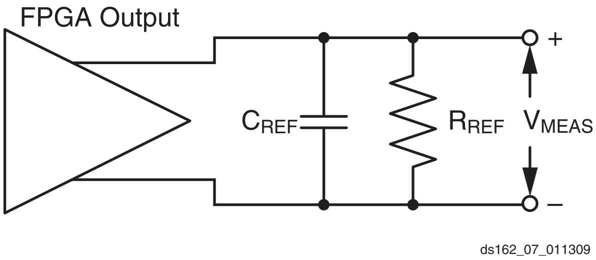

Figure 5: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 32.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 32: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[(1)] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.4	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
PCI (Peripheral Component Interface) 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3 (rising edge)	25	10[(2)]	0.94	0
	PCI33_3, PCI66_3 (falling edge)	25	10[(2)]	2.03	3.3
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25

Table 32: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
SSTL, Class II, 1.5V	SSTL15_II	25	0	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	100	0	0(3)	–
BLVDS (Bus LVDS), 2.5V	BLVDS_25	Note 4	0	0(3)	–
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	100	0	0(3)	–
RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RSDS_25, RSDS_33	100	0	0(3)	–
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	Note 5	0	0(3)	–
PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V	PPDS_25, PPDS_33	100	0	0(3)	–

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. The value given is the differential output voltage.
4. See the *BLVDS Output Termination* section in UG381, *Spartan-6 FPGA SelectIO Resources User Guide.*
5. See the *TMDS_33 Termination* section in UG381, *Spartan-6 FPGA SelectIO Resources User Guide.*

Simultaneously Switching Outputs

Due to package electrical parasitics, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. Table 33 and Table 34 provide guidelines for the recommended maximum allowable number of SSOs. These guidelines describe the maximum number of user I/O pins of an output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise for that particular signal standard. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of GND and power bounce.

For each device/package combination, Table 33 provides the number of equivalent V_{CCO}/GND pairs per bank. For each output signal standard and drive strength, Table 34 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines are categorized by package style, slew rate, and output drive current. The number of SSOs are also specified by I/O bank. Multiply the appropriate numbers from each table to calculate the maximum number of SSOs allowed within an I/O bank. The guidelines assume that all pins within a bank use the same I/O standard. Exceeding these SSO guidelines can result in increased power or GND bounce, degraded signal integrity, or increased system jitter. For a given I/O standard, if the SSO limit per pair in Table 34 is greater than the maximum I/O per pair in Table 33, then there is no SSO limit for the exclusive use of that I/O standard.

The recommended maximum SSO values assume that the FPGA is soldered on a printed circuit board and that the board uses sound design practices. Due to the additional inductance introduced by the socket, the SSO values do not apply for FPGAs mounted in sockets. The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics. For more detail, see UG381: *Spartan-6 FPGA SelectIO Resources User Guide.*

Table 33: **Spartan-6 FPGA V_{CCO}/GND Pairs per Bank**

Package	Devices	Description	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5
TQG144	LX	V_{CCO}/GND Pairs	3	3	2	3	N/A	N/A
		Maximum I/O per Pair	8	8	13	8	N/A	N/A
CPG196	LX	VCCO/GND Pairs	4	6	4	6	N/A	N/A
		Maximum I/O per Pair	6	4	7	4	N/A	N/A
CSG225	LX	V_{CCO}/GND Pairs	4	4	4	4	N/A	N/A
		Maximum I/O per Pair	10	10	9	10	N/A	N/A
FT(G)256	LX	V_{CCO}/GND Pairs	5	6	4	5	N/A	N/A
		Maximum I/O per Pair	8	9	9	10	N/A	N/A
CSG324	LX	V_{CCO}/GND Pairs	6	6	6	6	N/A	N/A
		Maximum I/O per Pair	10	9	10	9	N/A	N/A
	LXT	V_{CCO}/GND Pairs	4	6	6	6	N/A	N/A
		Maximum I/O per Pair	4	9	10	9	N/A	N/A
CS(G)484	LX	V_{CCO}/GND Pairs	8	13	8	13	N/A	N/A
		Maximum I/O per Pair	7	8	7	8	N/A	N/A
	LXT	V_{CCO}/GND Pairs	7	12	8	13	N/A	N/A
		Maximum I/O per Pair	5	8	6	8	N/A	N/A
FG(G)484	LX	V_{CCO}/GND Pairs	10	10	11	11	N/A	N/A
		Maximum I/O per Pair	6	8	9	8	N/A	N/A
	LXT	V_{CCO}/GND Pairs	6	10	11	10	N/A	N/A
		Maximum I/O per Pair	7	8	7	8	N/A	N/A
FG(G)676	LX45	V_{CCO}/GND Pairs	12	15	10	16	N/A	N/A
		Maximum I/O per Pair	3	7	8	7	N/A	N/A
	LX75, LX100, LX150	V_{CCO}/GND Pairs	12	9	10	10	6	6
		Maximum I/O per Pair	9	10	9	9	8	9
	LXT	V_{CCO}/GND Pairs	10	8	10	8	7	7
		Maximum I/O per Pair	8	7	8	8	7	7
FG(G)900	LX	V_{CCO}/GND Pairs	17	14	17	14	7	8
		Maximum I/O per Pair	7	6	7	8	7	6
	LXT	V_{CCO}/GND Pairs	15	14	13	14	7	8
		Maximum I/O per Pair	7	6	8	8	7	6

Table 34: **SSO Limit per V_{CCO}/GND Pair** ***(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
3.3V	LVCMOS33	2	Fast	42	46	42	44
			Slow	50	55	50	49
			QuietIO	60	68	60	60
		4	Fast	21	27	21	25
			Slow	32	37	32	32
			QuietIO	39	42	39	37
		6	Fast	14	19	14	17
			Slow	19	25	19	22
			QuietIO	29	30	29	25
		8	Fast	11	15	11	14
			Slow	15	20	15	18
			QuietIO	25	24	25	20
		12	Fast	1	3	1	1
			Slow	2	5	2	2
			QuietIO	4	9	4	7
		16	Fast	1	2	1	1
			Slow	1	5	1	1
			QuietIO	3	10	3	8
		24	Fast	1	2	1	1
			Slow	2	5	2	1
			QuietIO	7	9	7	7

Table 44: **DSP48A1 Switching Characteristics *(Cont'd)***

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-3	-3N	-2	-1L	
$T_{DSPDCK\_OPMODE\_PREG}$/ $T_{DSPCKD\_OPMODE\_PREG}$	OPMODE input to P register CLK	Yes	Yes	Yes	6.21/ –0.84	7.27/ –0.84	7.27/ –0.84	10.43/ –0.84	ns
		No	Yes	Yes	1.69/ –0.87	1.98/ –0.87	1.98/ –0.87	3.62/ –0.87	ns
		No	No	Yes	2.09/ –0.22	2.30/ –0.22	2.30/ –0.22	3.79/ –0.22	ns
Clock to Out from Output Register Clock to Output Pin									
$T_{DSPCKO\_P\_PREG}$	CLK (PREG) to P output	N/A	N/A	N/A	1.20	1.34	1.34	1.90	ns
Clock to Out from Pipeline Register Clock to Output Pins									
$T_{DSPCKO\_P\_MREG}$	CLK (MREG) to P output	N/A	N/A	Yes	3.38	3.95	3.95	5.83	ns
Clock to Out from Input Register Clock to Output Pins									
$T_{DSPCKO\_P\_A1REG}$	CLK (A1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.65	ns
$T_{DSPCKO\_P\_B1REG}$	CLK (B1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.63	ns
$T_{DSPCKO\_P\_CREG}$	CLK (CREG) to P output	N/A	N/A	Yes	3.12	3.64	3.64	5.24	ns
$T_{DSPCKO\_P\_DREG}$	CLK (DREG) to P output	Yes	Yes	Yes	6.77	7.92	7.92	12.53	ns
Combinatorial Delays from Input Pins to Output Pins									
$T_{DSPDO\_A\_P}$	A input to P output	N/A	No	Yes	2.85	3.33	3.33	4.73	ns
		N/A	Yes	No(2)	3.35	3.93	3.93	6.74	ns
		N/A	Yes	Yes	4.56	5.22	5.22	8.94	ns
$T_{DSPDO\_B\_P}$	B input to P output	Yes	No	No(2)	3.22	3.76	3.76	5.55	ns
		Yes	Yes	No(2)	6.01	6.54	6.54	9.76	ns
		Yes	Yes	Yes	6.27	7.34	7.34	11.96	ns
$T_{DSPDO\_C\_P}$	C input to P output	N/A	N/A	Yes	2.69	3.15	3.15	4.68	ns
$T_{DSPDO\_D\_P}$	D input to P output	Yes	Yes	Yes	6.31	7.38	7.38	11.81	ns
$T_{DSPDO\_OPMODE\_P}$	OPMODE input to P output	Yes	Yes	Yes	6.43	7.52	7.52	11.84	ns
		No	Yes	Yes	4.84	5.66	5.66	9.25	ns
		No	No	Yes	3.11	3.49	3.49	5.03	ns
Maximum Frequency									
F_{MAX}	All registers used	Yes	Yes	Yes	390	333	333	213	MHz

Notes:

1. A Yes signifies that the component is in the path. A No signifies that the component is being bypassed. N/A signifies not applicable because no path exists.
2. Implemented in the post-adder by adding to zero.

Clock Buffers and Networks

Table 48: **Global Clock Switching Characteristics (BUFGMUX)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T_{GSI}	S pin Setup to I0/I1 inputs	LX devices	0.25	0.31	0.48	0.48	ns
		LXT devices	0.25	0.31	0.48	N/A	ns
T_{GIO}	BUFGMUX delay from I0/I1 to O	LX devices	0.21	0.21	0.21	0.21	ns
		LXT devices	0.21	0.21	0.21	N/A	ns
Maximum Frequency							
F_{MAX}	Global clock tree (BUFGMUX)	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 49: **Input/Output Clock Switching Characteristics (BUFIO2)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T_{BUFCKO_O}	Clock to out delay from I to O	LX devices	0.67	0.82	1.09	1.50	ns
		LXT devices	0.67	0.82	1.09	N/A	ns
Maximum Frequency							
F_{MAX}	I/O clock tree (BUFIO2)	LX devices	540	525	500	300	MHz
		LXT devices	540	525	500	N/A	MHz

Table 50: **Input/Output Clock Switching Characteristics (BUFIO2FB)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
Maximum Frequency							
F_{MAX}	I/O clock tree (BUFIO2FB)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

Table 51: **Input/Output Clock Switching Characteristics (BUFPLL)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
Maximum Frequency							
F_{MAX}	BUFPLL clock tree (BUFPLL)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

PLL Switching Characteristics

Table 52: **PLL Specification**

Symbol	Description	Device(1)	Speed Grade				Units
			-3	-3N	-2	-1L	
F_{INMAX}	Maximum Input Clock Frequency from I/O Clock	LX devices	540	525	450	300	MHz
		LXT devices	540	525	450	N/A	MHz
	Maximum Input Clock Frequency from Global Clock	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 52: **PLL Specification *(Cont'd)***

Symbol	Description	Device(1)	Speed Grade				Units
			-3	-3N	-2	-1L	
F_{INMIN}	Minimum Input Clock Frequency	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter: 19–200 MHz	All	1 ns Maximum				
	Maximum Input Clock Period Jitter: > 200 MHz	All	<20% of clock input period Maximum				
F_{INDUTY}	Allowable Input Duty Cycle: 19—199 MHz	All	25/75				%
	Allowable Input Duty Cycle: 200—299 MHz	All	35/65				%
	Allowable Input Duty Cycle: > 300 MHz	All	45/55				%
F_{VCOMIN}	Minimum PLL VCO Frequency	LX devices	400	400	400	400	MHz
		LXT devices	400	400	400	N/A	MHz
F_{VCOMAX}	Maximum PLL VCO Frequency	LX devices	1080	1050	1000	1000	MHz
		LXT devices	1080	1050	1000	N/A	MHz
$F_{BANDWIDTH}$	Low PLL Bandwidth at Typical(3)	All	1	1	1	1	MHz
	High PLL Bandwidth at Typical(3)	All	4	4	4	4	MHz
$T_{STAPHAOFFSET}$	Static Phase Offset of the PLL Outputs	All	0.12	0.12	0.12	0.15	ns
$T_{OUTJITTER}$	PLL Output Jitter(3)	All	Note 2				
$T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision(4)	All	0.15	0.15	0.20	0.25	ns
$T_{LOCKMAX}$	PLL Maximum Lock Time	All	100	100	100	100	µs
F_{OUTMAX}	PLL Maximum Output Frequency for BUFGMUX	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz
	PLL Maximum Output Frequency for BUFPLL	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz
F_{OUTMIN}	PLL Minimum Output Frequency(5)	All	3.125	3.125	3.125	3.125	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation: 19–200 MHz	All	1 ns Maximum				
	External Clock Feedback Variation: > 200 MHz	All	< 20% of clock input period Maximum				
$RST_{MINPULSE}$	Minimum Reset Pulse Width	All	5	5	5	5	ns
F_{PFDMAX}(5)	Maximum Frequency at the Phase Frequency Detector	LX devices	500	500	400	300	MHz
		LXT devices	500	500	400	N/A	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	All	3 ns Max or one CLKIN cycle				

Notes:

1. LXT devices are not available with a -1L speed grade.
2. Values for this parameter are available in the Clocking Wizard.
3. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When using CLK_FEEDBACK = CLKOUT0 with BUFIO2 feedback, the feedback frequency will be higher than the phase frequency detector frequency. $F_{PFDMAX} = F_{CLKFB}$ / CLKFBOUT_MULT

Table 54: Switching Characteristics for the Delay-Locked Loop (DLL)[1] *(Cont'd)*

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
LOCK_DLL[3]	When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. CLKIN_FREQ_DLL < 50 MHz.	–	5	–	5	–	5	–	5	ms
	When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. CLKIN_FREQ_DLL > 50 MHz	–	0.60	–	0.60	–	0.60	–	0.60	ms
Delay Lines										
DCM_DELAY_STEP[5]	Finest delay resolution, averaged over all steps.	10	40	10	40	10	40	10	40	ps

Notes:

1. The values in this table are based on the operating conditions described in Table 2 and Table 53.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster LOCK time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, this data sheet specifies a maximum jitter of ±(1% of CLKIN period + 150 ps). Assuming that the CLKIN frequency is 100 MHz, the equivalent CLKIN period is 10 ns. Since 1% of 10 ns is 0.1 ns or 100 ps, the maximum jitter is ±(100 ps + 150 ps) = ±250 ps.
5. A typical delay step size is 23 ps.
6. The timing analysis tools use the CLK_FEEDBACK = 1X condition for the CLKIN_CLKFB_PHASE value (reported as phase error). When using CLK_FEEDBACK = 2X, add 100 ps to the phase error for the CLKIN_CLKFB_PHASE value (as shown in this table).

Table 55: Recommended Operating Conditions for the Digital Frequency Synthesizer (DFS)[1]

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Input Frequency Ranges[2]										
CLKIN_FREQ_FX	Frequency for the CLKIN input. Also described as F_{CLKIN}.	0.5	375[3]	0.5	375[3]	0.5	333[3]	0.5	200[3]	MHz
Input Clock Jitter Tolerance[4]										
CLKIN_CYC_JITT_FX_LF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: FCLKFX < 150 MHz.	–	±300	–	±300	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: FCLKFX > 150 MHz.	–	±150	–	±150	–	±150	–	±150	ps
CLKIN_PER_JITT_FX	Period jitter at the CLKIN input.	–	±1	–	±1	–	±1	–	±1	ns

Notes:

1. DFS specifications apply when using either of the DFS outputs (CLKFX or CLKFX180).
2. When using both DFS and DLL outputs on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 53.
3. The CLKIN_DIVIDE_BY_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the F_{MAX} (see Table 48 and Table 49 for BUFG and BUFIO2 limits).
4. CLKIN input jitter beyond these limits can cause the DCM to lose LOCK.

Table 64: **Global Clock Input to Output Delay With DCM in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in System-Synchronous Mode.							
$T_{ICKOFDCM}$	Global Clock and OUTFF *with* DCM	XC6SLX4	4.23	N/A	6.11	6.60	ns
		XC6SLX9	4.23	5.17	6.11	6.60	ns
		XC6SLX16	4.28	4.57	5.34	6.36	ns
		XC6SLX25	3.95	4.18	4.59	6.91	ns
		XC6SLX25T	3.95	4.18	4.59	N/A	ns
		XC6SLX45	4.37	4.70	5.50	6.85	ns
		XC6SLX45T	4.37	4.70	5.50	N/A	ns
		XC6SLX75	3.90	4.23	4.77	6.31	ns
		XC6SLX75T	3.90	4.23	4.77	N/A	ns
		XC6SLX100	3.86	4.16	4.66	7.25	ns
		XC6SLX100T	3.90	4.16	4.66	N/A	ns
		XC6SLX150	4.03	4.33	4.83	6.63	ns
		XC6SLX150T	4.03	4.33	4.83	N/A	ns
		XA6SLX4	4.55	N/A	6.11	N/A	ns
		XA6SLX9	4.55	N/A	6.11	N/A	ns
		XA6SLX16	4.62	N/A	5.33	N/A	ns
		XA6SLX25	4.27	N/A	4.59	N/A	ns
		XA6SLX25T	4.27	N/A	4.69	N/A	ns
		XA6SLX45	4.69	N/A	5.50	N/A	ns
		XA6SLX45T	4.69	N/A	5.50	N/A	ns
		XA6SLX75	4.22	N/A	4.77	N/A	ns
		XA6SLX75T	4.22	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.34	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	6.31	ns
		XQ6SLX75T	4.22	N/A	4.77	N/A	ns
		XQ6SLX150	N/A	N/A	4.96	6.63	ns
		XQ6SLX150T	4.62	N/A	4.96	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Spartan-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 70 through Table 77. Values are expressed in nanoseconds unless otherwise noted.

Table 70: **Global Clock Setup and Hold Without DCM or PLL (No Delay)**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSND}/ T_{PHND}	No Delay Global Clock and IFF(3) without DCM or PLL	XC6SLX4	0.10/1.56	N/A	0.10/1.83	0.07/2.54	ns
		XC6SLX9	0.10/1.56	0.10/1.57	0.10/1.84	0.07/2.54	ns
		XC6SLX16	0.12/1.42	0.12/1.48	0.12/1.64	0.13/2.19	ns
		XC6SLX25	0.18/1.64	0.18/1.75	0.18/1.99	0.11/2.57	ns
		XC6SLX25T	0.18/1.64	0.18/1.75	0.18/1.99	N/A	ns
		XC6SLX45	–0.08/1.80	–0.08/1.95	–0.08/2.27	–0.17/2.74	ns
		XC6SLX45T	–0.08/1.80	–0.08/1.95	–0.08/2.27	N/A	ns
		XC6SLX75	0.13/1.81	0.13/2.06	0.13/2.27	–0.12/3.30	ns
		XC6SLX75T	0.13/1.81	0.13/2.06	0.13/2.27	N/A	ns
		XC6SLX100	–0.14/2.03	–0.14/2.24	–0.14/2.56	–0.17/3.44	ns
		XC6SLX100T	–0.14/2.03	–0.14/2.24	–0.14/2.56	N/A	ns
		XC6SLX150	–0.24/2.42	–0.24/2.74	–0.24/2.95	–0.60/3.75	ns
		XC6SLX150T	–0.24/2.42	–0.24/2.74	–0.24/2.95	N/A	ns
		XA6SLX4	0.10/1.57	N/A	0.10/1.84	N/A	ns
		XA6SLX9	0.10/1.57	N/A	0.10/1.84	N/A	ns
		XA6SLX16	0.12/1.43	N/A	0.12/1.64	N/A	ns
		XA6SLX25	0.18/1.65	N/A	0.18/1.99	N/A	ns
		XA6SLX25T	0.18/1.65	N/A	0.18/1.99	N/A	ns
		XA6SLX45	–0.08/1.82	N/A	–0.08/2.27	N/A	ns
		XA6SLX45T	–0.08/1.82	N/A	–0.08/2.27	N/A	ns
		XA6SLX75	0.13/2.02	N/A	0.13/2.32	N/A	ns
		XA6SLX75T	0.13/2.02	N/A	0.13/2.32	N/A	ns
		XA6SLX100	N/A	N/A	0.10/2.51	N/A	ns
		XQ6SLX75	N/A	N/A	0.13/2.32	–0.12/3.30	ns
		XQ6SLX75T	0.13/2.02	N/A	0.13/2.32	N/A	ns
		XQ6SLX150	N/A	N/A	–0.24/2.95	–0.60/3.75	ns
		XQ6SLX150T	–0.24/2.74	N/A	–0.24/2.95	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.

Table 71: **Global Clock Setup and Hold Without DCM or PLL (Default Delay)**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSFD}/ T_{PHFD}	Default Delay(2) Global Clock and IFF(3) without DCM or PLL	XC6SLX4	0.66/1.17	N/A	1.05/0.79	2.09/1.05	ns
		XC6SLX9	0.66/1.17	0.75/1.17	1.05/1.17	2.09/1.05	ns
		XC6SLX16	0.87/1.16	0.93/1.16	0.96/1.16	1.86/1.06	ns
		XC6SLX25	0.68/0.77	0.81/0.81	0.87/0.82	2.21/1.33	ns
		XC6SLX25T	0.68/0.77	0.81/0.81	0.87/0.82	N/A	ns
		XC6SLX45	0.40/1.05	0.42/1.17	0.64/1.20	1.61/1.67	ns
		XC6SLX45T	0.40/1.05	0.42/1.17	0.64/1.20	N/A	ns
		XC6SLX75	0.41/1.11	0.41/1.13	0.80/1.14	1.23/1.82	ns
		XC6SLX75T	0.41/1.11	0.41/1.13	0.80/1.14	N/A	ns
		XC6SLX100	0.39/1.12	0.39/1.23	0.39/1.28	1.13/1.94	ns
		XC6SLX100T	0.39/1.12	0.39/1.23	0.39/1.28	N/A	ns
		XC6SLX150	0.23/1.54	0.23/1.62	0.23/1.62	1.14/2.05	ns
		XC6SLX150T	0.23/1.54	0.23/1.62	0.23/1.62	N/A	ns
		XA6SLX4	0.73/1.18	N/A	1.05/0.80	N/A	ns
		XA6SLX9	0.73/1.18	N/A	1.05/0.80	N/A	ns
		XA6SLX16	0.90/1.20	N/A	0.96/0.75	N/A	ns
		XA6SLX25	0.70/0.81	N/A	0.87/0.91	N/A	ns
		XA6SLX25T	0.76/0.81	N/A	1.03/0.91	N/A	ns
		XA6SLX45	0.40/1.06	N/A	0.64/1.20	N/A	ns
		XA6SLX45T	0.40/1.06	N/A	0.64/1.20	N/A	ns
		XA6SLX75	0.41/1.24	N/A	0.80/1.18	N/A	ns
		XA6SLX75T	0.41/1.24	N/A	0.80/1.18	N/A	ns
		XA6SLX100	N/A	N/A	0.86/1.55	N/A	ns
		XQ6SLX75	N/A	N/A	0.80/1.18	1.23/1.82	ns
		XQ6SLX75T	0.41/1.24	N/A	0.80/1.18	N/A	ns
		XQ6SLX150	N/A	N/A	0.28/1.57	1.14/2.05	ns
		XQ6SLX150T	0.28/1.78	N/A	0.28/1.57	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Default delay uses IODELAY2 tap 0.
3. IFF = Input Flip-Flop or Latch.

Table 74: **Global Clock Setup and Hold With PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.[1]							
T_{PSPLL}/ T_{PHPLL}	No Delay Global Clock and IFF[2] with PLL in System-Synchronous Mode	XC6SLX4	1.37/0.25	N/A	1.52/0.41	2.07/0.69	ns
		XC6SLX9	1.37/0.21	1.48/0.21	1.52/0.26	2.07/0.69	ns
		XC6SLX16	1.33/–0.03	1.53/–0.02	1.60/–0.02	1.57/0.48	ns
		XC6SLX25	1.65/0.28	1.71/0.28	1.91/0.28	2.44/0.76	ns
		XC6SLX25T	1.65/0.28	1.71/0.28	1.91/0.28	N/A	ns
		XC6SLX45	1.55/0.18	1.64/0.18	1.75/0.18	2.02/0.90	ns
		XC6SLX45T	1.55/0.18	1.64/0.18	1.75/0.18	N/A	ns
		XC6SLX75	1.77/0.21	1.89/0.21	2.13/0.21	2.46/0.53	ns
		XC6SLX75T	1.77/0.21	1.89/0.21	2.13/0.21	N/A	ns
		XC6SLX100	1.44/0.32	1.52/0.32	1.70/0.32	1.78/0.86	ns
		XC6SLX100T	1.44/0.32	1.52/0.32	1.70/0.32	N/A	ns
		XC6SLX150	1.39/0.49	1.48/0.49	1.67/0.49	1.94/0.94	ns
		XC6SLX150T	1.39/0.49	1.48/0.49	1.67/0.49	N/A	ns
		XA6SLX4	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX9	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX16	1.89/–0.08	N/A	1.72/–0.08	N/A	ns
		XA6SLX25	1.85/0.16	N/A	2.08/0.16	N/A	ns
		XA6SLX25T	1.85/0.16	N/A	2.17/0.16	N/A	ns
		XA6SLX45	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX45T	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX75	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX100	N/A	N/A	2.34/0.14	N/A	ns
		XQ6SLX75	N/A	N/A	2.25/0.06	2.46/0.53	ns
		XQ6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XQ6SLX150	N/A	N/A	1.79/0.37	1.94/0.94	ns
		XQ6SLX150T	1.43/0.37	N/A	1.79/0.37	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 76: **Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.[1]							
$T_{PSDCMPLL}$/ $T_{PHDCMPLL}$	No Delay Global Clock and IFF[2] with DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.	XC6SLX4	1.16/0.49	N/A	1.39/0.49	2.36/0.59	ns
		XC6SLX9	1.16/0.44	1.37/0.44	1.39/0.44	2.36/0.59	ns
		XC6SLX16	1.44/–0.08	1.49/–0.04	1.62/–0.04	2.06/0.55	ns
		XC6SLX25	1.52/0.42	1.65/0.42	1.83/0.42	2.52/0.43	ns
		XC6SLX25T	1.52/0.42	1.65/0.42	1.83/0.42	N/A	ns
		XC6SLX45	1.54/0.39	1.59/0.39	1.75/0.39	2.48/0.76	ns
		XC6SLX45T	1.54/0.39	1.59/0.39	1.75/0.39	N/A	ns
		XC6SLX75	1.72/0.41	1.80/0.41	1.99/0.41	2.60/0.75	ns
		XC6SLX75T	1.72/0.41	1.80/0.41	1.99/0.41	N/A	ns
		XC6SLX100	1.34/0.51	1.46/0.51	1.64/0.51	2.12/0.90	ns
		XC6SLX100T	1.34/0.51	1.46/0.51	1.64/0.51	N/A	ns
		XC6SLX150	1.30/0.60	1.40/0.60	1.55/0.60	2.57/0.97	ns
		XC6SLX150T	1.30/0.60	1.40/0.60	1.55/0.60	N/A	ns
		XA6SLX4	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX9	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX16	2.67/0.35	N/A	2.67/0.17	N/A	ns
		XA6SLX25	1.74/0.27	N/A	1.95/0.27	N/A	ns
		XA6SLX25T	1.74/0.27	N/A	2.03/0.27	N/A	ns
		XA6SLX45	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX45T	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX75	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX100	N/A	N/A	2.64/0.82	N/A	ns
		XQ6SLX75	N/A	N/A	2.11/0.24	2.60/0.75	ns
		XQ6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XQ6SLX150	N/A	N/A	1.67/0.70	2.57/0.97	ns
		XQ6SLX150T	1.50/0.70	N/A	1.67/0.70	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Date	Version	Description of Revisions
01/10/11	1.11	Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.4 software with speed specification v1.15 for the -4, -3, -3N, and -2 speed grades. Added note 3 to Table 27. Also updated the -1L speed grade requirements to ISE v12.4 software with speed specification v1.06. Revised -3N definition throughout the document. Added note 4 to Table 2 and updated note 5. Added information on V_{CCINT} to note 1 in Table 5. Updated Networking Applications -3 values in Table 25 to match improvements made in ISE v12.4. In Table 28, added note 1 and revised the T_{IOTP} values for LVDS_33, LVDS_25, MINI_LVDS_33, MINI_LVDS_25, RSDS_33, RSDS_25, TMDS_33. PPDS_33, and PPDS_25. Added note 3 to Table 55.
02/11/11	1.12	As described in XCN11008: *Product Discontinuation Notice For Spartan-6 LXT -4 Devices*, the -4 speed specifications have been discontinued. As outlined in page 2 of the XCN, designers currently using -4 speed specifications should rerun timing analysis using the new -3 speed specifications before moving to a replacement device. Updated the networking applications section of Table 25. Updated -2 speed specifications throughout document and added note 3 to Table 27 advising designers to use the -2 speed specification update (v1.17) with the ISE 12.4 software patch. Added F_{CLKDIV} to Table 37 and Table 38. Updated note 2 in Table 39. Updated units for $T_{SMCKCSO}$ and T_{BPICCO} in Table 47. Updated -1L in Table 71. Removed Note 2: *Package delay information is available for these device/package combinations. This information can be used to deskew the package* from Table 79.
03/31/11	2.0	Production release of XC6SLX45 in the -1L speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. In Table 39, removed values in the -1L column and added note 3 as IODELAY2 only supports Tap0 for lower-power devices. Updated copyright page 1 and Notice of Disclaimer.
05/20/11	2.1	Production release of XC6SLX100 and XC6SLX150 in the specific speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. Updated Table 27 and Note 7 with changes per XCN11012: *Speed File Change for -3N Devices*. Revised Switching Characteristics section for speed specifications: v1.18 for -3, -3N, and -2; including improvements in Table 73 through Table 77 and Table 81. Removed *Memory Controller Block* from the performance heading in Table 2 and revised Note 2. In Table 4, added Note 1 to C_{IN} and updated the description of R_{IN_TERM}. Updated Note 1 in Table 5. Updated Note 1 of Table 7. In Table 25, added and removed -1L specifications, increased the standard performance DDR3 specifications, removed the extended performance DDR3 row and updated Note 3 and Note 4. Clarified the introductory information for Table 28 and Table 30. In Table 32: Revised V_{MEAS} value for LVCMOS12; revised V_{REF} for LVDS_25, LVDS_33, BLVDS_25,MINI_LVDS_25, MINI_LVDS_33, RSDS_25, and RSDS_33; revised R_{REF} for BLVDS_25 and TMDS_33; and added Note 4 and Note 5. Updated Note 2 and Note 3 in Table 39. In Table 47, revised the values and description of T_{POR} including adding Note 3. Also in Table 47, augmented the description and added specifications for F_{RBCCK} and removed XC6SLX4 from F_{MCCK} (maximum frequency, parallel mode (Master SelectMAP/BPI). Added BUFGMUX to Table 48 title. Added Table 50. In Table 52, revised specifications for $T_{EXTFDVAR}$ and $F_{INJITTER}$. In Table 54 removed the 5 MHz < CLKIN_FREQ_DLL parameter in the LOCK_DLL description. In both Table 56 and Table 57, removed the 5 MHz < F_{CLKIN} parameter in the LOCK_FX description. In Table 58, updated description for PSCLK_FREQ and PSCLK_PULSE. Revised title and symbol of Table 70, added new speed specifications for -1L, and added Note 2. Added Table 71.
07/11/11	2.2	Added the Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices to all appropriate tables while sometimes removing the XC6S nomenclature. Added expanded temperature range (Q) to all appropriate tables. Updated T_{SOL} packages in Table 1. Added R_{OUT_TERM} to Table 4. Updated Note 2 on Table 13. Production release of the XC6SLX4, XC6SLX9, XC6SLX16, XC6SLX25, XC6SLX75, XQ6SLX75, and XQ6SLX150 in Table 26 and Table 27 using ISE v13.2 software with -1L speed specification v1.07. Production release of the XA6SLX16, XA6SLX25T, XA6SLX45, XA6SLX45T, XQ6SLX75, XQ6SLX75T, XQ6SLX150, and XQ6SLX150T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices(1). Updated CS(G)484 from CSG484 throughout data sheet. Clarified Note 3 in Table 39.
08/08/11	2.3	Production release of the XA6SLX25, XA6SLX75, and XA6SLX75T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19.

Date	Version	Description of Revisions
09/14/11	2.4	Production release of the XA6SLX4 and XA6SLX9 devices in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added production released version of the XA6SLX100 to Table 26 and Table 27 using ISE v13.3 software with -2 speed specification v1.20. Updated R_{OUT_TERM} description in Table 4. Fixed the LVPECL V_H error in Table 31. Updated introduction in Simultaneously Switching Outputs. Added the XA6SLX100 to Table 63 through Table 78, and Table 81. Added Note 4 to Table 78 because the T_{CKSKEW} for the XC6SLX100 is not the same as the T_{CKSKEW} for the XA6SLX100. Revised the revision history for version 1.6 dated 06/24/10. Removed the parenthetical statement about the -3N speed grade: (specifications are identical to the -3 speed grade).
10/17/11	3.0	Changed the data sheet from Preliminary Product Specification to Product Specification. Updated the Switching Characteristics, page 19 speed specification version ISE v13.3 software to -2 and -3 speed specification v1.20 and -1L speed specification of v1.08. Also updated Note 1 in Table 27. In Table 43, *Block RAM Switching Characteristics*, the F_{MAX} value for the -2 speed grade has been changed from 260 MHz to 280 MHz. In Table 54, *Switching Characteristics for the DLL*, a Note 6 was added and linked to CLKIN_CLKFB_PHASE.

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