



Welcome to [E-XFL.COM](http://E-XFL.COM)

### Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	1879
Number of Logic Elements/Cells	24051
Total RAM Bits	958464
Number of I/O	190
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-LFBGA, CSPBGA
Supplier Device Package	324-CSPBGA (15x15)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xc6slx25t-3csg324c">https://www.e-xfl.com/product-detail/xilinx/xc6slx25t-3csg324c</a>

Table 2: Recommended Operating Conditions<sup>(1)</sup>

Symbol	Description		Min	Typ	Max	Units	
V <sub>CCINT</sub>	Internal supply voltage relative to GND	-3, -3N, -2	Standard performance <sup>(2)</sup>	1.14	1.2	1.26	V
		-3, -2	Extended performance <sup>(2)</sup>	1.2	1.23	1.26	V
		-1L	Standard performance <sup>(2)</sup>	0.95	1.0	1.05	V
V <sub>CCAUX</sub> <sup>(3)(4)</sup>	Auxiliary supply voltage relative to GND	V <sub>CCAUX</sub> = 2.5V <sup>(5)</sup>		2.375	2.5	2.625	V
		V <sub>CCAUX</sub> = 3.3V		3.15	3.3	3.45	V
V <sub>CCO</sub> <sup>(6)(7)(8)</sup>	Output supply voltage relative to GND		1.1	–	3.45	V	
V <sub>IN</sub>	Input voltage relative to GND	All I/O standards (except PCI)	Commercial temperature (C)	–0.5	–	4.0	V
			Industrial temperature (I)	–0.5	–	3.95	V
			Expanded (Q) temperature	–0.5	–	3.95	V
		PCI I/O standard <sup>(9)</sup>		–0.5	–	V <sub>CCO</sub> + 0.5	V
I <sub>IN</sub> <sup>(10)</sup>	Maximum current through pin using PCI I/O standard when forward biasing the clamp diode. <sup>(9)</sup>	Commercial (C) and Industrial temperature (I)		–	–	10	mA
		Expanded (Q) temperature		–	–	7	mA
V <sub>BATT</sub> <sup>(11)</sup>	Battery voltage relative to GND, T <sub>j</sub> = 0°C to +85°C (LX75, LX75T, LX100, LX100T, LX150, and LX150T only)		1.0	–	3.6	V	
T <sub>j</sub>	Junction temperature operating range	Commercial (C) range		0	–	85	°C
		Industrial temperature (I) range		–40	–	100	°C
		Expanded (Q) temperature range		–40	–	125	°C

**Notes:**

- All voltages are relative to ground.
- See *Interface Performances for Memory Interfaces* in Table 25. The extended performance range is specified for designs not using the standard V<sub>CCINT</sub> voltage range. The standard V<sub>CCINT</sub> voltage range is used for:
  - Designs that do not use an MCB
  - LX4 devices
  - Devices in the TQG144 or CPG196 packages
  - Devices with the -3N speed grade
- Recommended maximum voltage droop for V<sub>CCAUX</sub> is 10 mV/ms.
- During configuration, if V<sub>CCO\_2</sub> is 1.8V, then V<sub>CCAUX</sub> must be 2.5V.
- The -1L devices require V<sub>CCAUX</sub> = 2.5V when using the LVDS\_25, LVDS\_33, BLVDS\_25, LVPECL\_25, RSDS\_25, RSDS\_33, PPDS\_25, and PPDS\_33 I/O standards on inputs. LVPECL\_33 is not supported in the -1L devices.
- Configuration data is retained even if V<sub>CCO</sub> drops to 0V.
- Includes V<sub>CCO</sub> of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
- For PCI systems, the transmitter and receiver should have common supplies for V<sub>CCO</sub>.
- Devices with a -1L speed grade do not support Xilinx PCI IP.
- Do not exceed a total of 100 mA per bank.
- V<sub>BATT</sub> is required to maintain the battery backed RAM (BBR) AES key when V<sub>CCAUX</sub> is not applied. Once V<sub>CCAUX</sub> is applied, V<sub>BATT</sub> can be unconnected. When BBR is not used, Xilinx recommends connecting to V<sub>CCAUX</sub> or GND. However, V<sub>BATT</sub> can be unconnected.

Table 4: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
$V_{DRINT}$	Data retention $V_{CCINT}$ voltage (below which configuration data might be lost)	0.8	–	–	V
$V_{DRAUX}$	Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost)	2.0	–	–	V
$I_{REF}$	$V_{REF}$ leakage current per pin for commercial (C) and industrial (I) devices	–10	–	10	$\mu$ A
	$V_{REF}$ leakage current per pin for expanded (Q) devices	–15	–	15	$\mu$ A
$I_L$	Input or output leakage current per pin (sample-tested) for commercial (C) and industrial (I) devices	–10	–	10	$\mu$ A
	Input or output leakage current per pin (sample-tested) for expanded (Q) devices	–15	–	15	$\mu$ A
$I_{HS}$	Leakage current on pins during hot socketing with FPGA unpowered	–20	–	20	$\mu$ A
	All pins except PROGRAM_B, DONE, and JTAG pins when HSWAPEN = 1 PROGRAM_B, DONE, and JTAG pins, or other pins when HSWAPEN = 0	$I_{HS} + I_{RPU}$			$\mu$ A
$C_{IN}^{(1)}$	Die input capacitance at the pad	–	–	10	pF
$I_{RPU}$	Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 3.3V$ or $V_{CCAUX} = 3.3V$	200	–	500	$\mu$ A
	Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 2.5V$ or $V_{CCAUX} = 2.5V$	120	–	350	$\mu$ A
	Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 1.8V$	60	–	200	$\mu$ A
	Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 1.5V$	40	–	150	$\mu$ A
	Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 1.2V$	12	–	100	$\mu$ A
$I_{RPD}$	Pad pull-down (when selected) @ $V_{IN} = V_{CCO}$ , $V_{CCAUX} = 3.3V$	200	–	550	$\mu$ A
	Pad pull-down (when selected) @ $V_{IN} = V_{CCO}$ , $V_{CCAUX} = 2.5V$	140	–	400	$\mu$ A
$I_{BATT}^{(2)}$	Battery supply current	–	–	150	nA
$R_{DT}^{(3)}$	Resistance of optional input differential termination circuit, $V_{CCAUX} = 3.3V$	–	100	–	$\Omega$
$R_{IN\_TERM}^{(5)}$	Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_25) for commercial (C) and industrial (I) devices	23	25	55	$\Omega$
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_25) for expanded (Q) devices	20	25	55	$\Omega$
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_50) for commercial (C) and industrial (I) devices	39	50	72	$\Omega$
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_50) for expanded (Q) devices	32	50	74	$\Omega$
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_75) for commercial (C) and industrial (I) devices	56	75	109	$\Omega$
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_75) for expanded (Q) devices	47	75	115	$\Omega$
$R_{OUT\_TERM}$	Thevenin equivalent resistance of programmable output termination (UNTUNED_25)	11	25	52	$\Omega$
	Thevenin equivalent resistance of programmable output termination (UNTUNED_50)	21	50	96	$\Omega$
	Thevenin equivalent resistance of programmable output termination (UNTUNED_75)	29	75	145	$\Omega$

**Notes:**

1. The  $C_{IN}$  measurement represents the die capacitance at the pad, not including the package.
2. Maximum value specified for worst case process at 25°C. LX75, LX75T, LX100, LX100T, LX150, and LX150T only.
3. Refer to IBIS models for  $R_{DT}$  variation and for values at  $V_{CCAUX} = 2.5V$ . IBIS values for  $R_{DT}$  are valid for all temperature ranges.
4.  $V_{CCO2}$  is not required for data retention. The minimum  $V_{CCO2}$  for power-on reset and configuration is 1.65V.
5. Termination resistance to a  $V_{CCO}/2$  level.

**Table 5: Typical Quiescent Supply Current (Cont'd)**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
I <sub>CCAUXQ</sub>	Quiescent V <sub>CCAUX</sub> supply current	LX4	2.5	2.5	2.5	2.5	mA
		LX9	2.5	2.5	2.5	2.5	mA
		LX16	3.0	3.0	3.0	3.0	mA
		LX25	4.0	4.0	4.0	4.0	mA
		LX25T	4.0	4.0	4.0	N/A	mA
		LX45	5.0	5.0	5.0	5.0	mA
		LX45T	5.0	5.0	5.0	N/A	mA
		LX75	7.0	7.0	7.0	7.0	mA
		LX75T	7.0	7.0	7.0	N/A	mA
		LX100	9.0	9.0	9.0	9.0	mA
		LX100T	9.0	9.0	9.0	N/A	mA
		LX150	12.0	12.0	12.0	12.0	mA
		LX150T	12.0	12.0	12.0	N/A	mA

**Notes:**

1. Typical values are specified at nominal voltage, 25°C junction temperatures (T<sub>j</sub>). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 25°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. Nominal V<sub>CCINT</sub> is 1.20V; use the XPE tool to calculate 1.23V values for the nominal V<sub>CCINT</sub> of the extended performance range.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

**Table 6: Power Supply Ramp Time**

Symbol	Description	Speed Grade	Ramp Time	Units
V <sub>CCINTR</sub>	Internal supply voltage ramp time	-3, -3N, -2	0.20 to 50.0	ms
		-1L	0.20 to 40.0	ms
V <sub>CCO2</sub> <sup>(1)</sup>	Output drivers bank 2 supply voltage ramp time	All	0.20 to 50.0	ms
V <sub>CCAUXR</sub>	Auxiliary supply voltage ramp time	All	0.20 to 50.0	ms

**Notes:**

1. The minimum V<sub>CCO2</sub> for power-on reset and configuration is 1.65V.
2. Spartan-6 FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply. Use the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools to estimate current drain on these supplies. Spartan-6 devices do not have a required power-on sequence.

Table 8: Recommended Operating Conditions for User I/Os Using Differential Signal Standards

I/O Standard	V <sub>CCO</sub> for Drivers		
	V, Min	V, Nom	V, Max
LVDS_33	3.0	3.3	3.45
LVDS_25	2.25	2.5	2.75
BLVDS_25	2.25	2.5	2.75
MINI_LVDS_33	3.0	3.3	3.45
MINI_LVDS_25	2.25	2.5	2.75
LVPECL_33 <sup>(1)</sup>	N/A—Inputs Only		
LVPECL_25	N/A—Inputs Only		
RSDS_33	3.0	3.3	3.45
RSDS_25	2.25	2.5	2.75
TMDS_33 <sup>(1)</sup>	3.14	3.3	3.45
PPDS_33	3.0	3.3	3.45
PPDS_25	2.25	2.5	2.75
DISPLAY_PORT	2.3	2.5	2.7
DIFF_MOBILE_DDR	1.7	1.8	1.9
DIFF_HSTL_I	1.4	1.5	1.6
DIFF_HSTL_II	1.4	1.5	1.6
DIFF_HSTL_III	1.4	1.5	1.6
DIFF_HSTL_I_18	1.7	1.8	1.9
DIFF_HSTL_II_18	1.7	1.8	1.9
DIFF_HSTL_III_18	1.7	1.8	1.9
DIFF_SSTL3_I	3.0	3.3	3.45
DIFF_SSTL3_II	3.0	3.3	3.45
DIFF_SSTL2_I	2.3	2.5	2.7
DIFF_SSTL2_II	2.3	2.5	2.7
DIFF_SSTL18_I	1.7	1.8	1.9
DIFF_SSTL18_II	1.7	1.8	1.9
DIFF_SSTL15_II	1.425	1.5	1.575

**Notes:**

1. LVPECL\_33 and TMDS\_33 inputs require V<sub>CCAUX</sub> = 3.3V nominal.

Table 10: Differential I/O Standard DC Input and Output Levels

I/O Standard	V <sub>ID</sub>		V <sub>ICM</sub>		V <sub>OD</sub>		V <sub>OCM</sub>		V <sub>OH</sub>	V <sub>OL</sub>
	mV, Min	mV, Max	V, Min	V, Max	mV, Min	mV, Max	V, Min	V, Max	V, Min	V, Max
LVDS_33 <sup>(2)(3)</sup>	100	600	0.3	2.35	247	454	1.125	1.375	–	–
LVDS_25 <sup>(2)(3)</sup>	100	600	0.3	2.35	247	454	1.125	1.375	–	–
BLVDS_25 <sup>(2)(3)</sup>	100	–	0.3	2.35	240	460	Typical 50% V <sub>CCO</sub>		–	–
MINI_LVDS_33	200	600	0.3	1.95	300	600	1.0	1.4	–	–
MINI_LVDS_25	200	600	0.3	1.95	300	600	1.0	1.4	–	–
LVPECL_33 <sup>(2)(3)</sup>	100	1000	0.3	2.8 <sup>(1)</sup>	Inputs only					
LVPECL_25 <sup>(2)(3)</sup>	100	1000	0.3	1.95	Inputs only					
RSDS_33 <sup>(2)(3)</sup>	100	–	0.3	1.5	100	400	1.0	1.4	–	–
RSDS_25 <sup>(2)(3)</sup>	100	–	0.3	1.5	100	400	1.0	1.4	–	–
TMDS_33	150	1200	2.7	3.23 <sup>(1)</sup>	400	800	V <sub>CCO</sub> – 0.405	V <sub>CCO</sub> – 0.190	–	–
PPDS_33 <sup>(2)(3)</sup>	100	400	0.2	2.3	100	400	0.5	1.4	–	–
PPDS_25 <sup>(2)(3)</sup>	100	400	0.2	2.3	100	400	0.5	1.4	–	–
DISPLAY_PORT	190	1260	0.3	2.35	–	–	Typical 50% V <sub>CCO</sub>		–	–
DIFF_MOBILE_DDR	100	–	0.78	1.02	–	–	–	–	90% V <sub>CCO</sub>	10% V <sub>CCO</sub>
DIFF_HSTL_I	100	–	0.68	0.9	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_HSTL_II	100	–	0.68	0.9	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_HSTL_III	100	–	0.68	0.9	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_HSTL_I_18	100	–	0.8	1.1	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_HSTL_II_18	100	–	0.8	1.1	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_HSTL_III_18	100	–	0.8	1.1	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_SSTL3_I	100	–	1.0	1.9	–	–	–	–	V <sub>TT</sub> + 0.6	V <sub>TT</sub> – 0.6
DIFF_SSTL3_II	100	–	1.0	1.9	–	–	–	–	V <sub>TT</sub> + 0.8	V <sub>TT</sub> – 0.8
DIFF_SSTL2_I	100	–	1.0	1.5	–	–	–	–	V <sub>TT</sub> + 0.61	V <sub>TT</sub> – 0.61
DIFF_SSTL2_II	100	–	1.0	1.5	–	–	–	–	V <sub>TT</sub> + 0.81	V <sub>TT</sub> – 0.81
DIFF_SSTL18_I	100	–	0.7	1.1	–	–	–	–	V <sub>TT</sub> + 0.47	V <sub>TT</sub> – 0.47
DIFF_SSTL18_II	100	–	0.7	1.1	–	–	–	–	V <sub>TT</sub> + 0.6	V <sub>TT</sub> – 0.6
DIFF_SSTL15_II	100	–	0.55	0.95	–	–	–	–	V <sub>TT</sub> + 0.4	V <sub>TT</sub> – 0.4

**Notes:**

1. LVPECL\_33 and TMDS\_33 maximum V<sub>ICM</sub> is the lower of V (maximum) or V<sub>CCAUX</sub> – (V<sub>ID</sub>/2)
2. When V<sub>CCAUX</sub> = 3.3V, the DCD can be higher than 5% for V<sub>ICM</sub> < 0.7V when using these I/O standards: LVDS\_25, LVDS\_33, BLVDS\_25, LVPECL\_25, LVPECL\_33, RSDS\_25, RSDS\_33, PPDS\_25, and PPDS\_33.
3. The -1L devices require V<sub>CCAUX</sub> = 2.5V when using the LVDS\_25, LVDS\_33, BLVDS\_25, LVPECL\_25, RSDS\_25, RSDS\_33, PPDS\_25, and PPDS\_33 I/O standards on inputs. LVPECL\_33 is not supported in the -1L devices.

## eFUSE Read Endurance

Table 11 lists the minimum guaranteed number of read cycle operations for Device DNA and for the AES eFUSE key. For more information, see [UG380: Spartan-6 FPGA Configuration User Guide](#).

Table 11: eFUSE Read Endurance

Symbol	Description	Speed Grade				Units (Min)
		-3	-3N	-2	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

## GTP Transceiver Specifications

GTP transceivers are available in the Spartan-6 LXT devices. See [DS160: Spartan-6 Family Overview](#) for more information.

### GTP Transceiver DC Characteristics

Table 12: Absolute Maximum Ratings for GTP Transceivers<sup>(1)</sup>

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	-0.5	1.32	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	-0.5	1.32	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	-0.5	1.32	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	-0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	-0.5	1.32	V
V <sub>IN</sub>	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	-0.5	1.32	V
V <sub>MGTREFCLK</sub>	Reference clock absolute input voltage	-0.5	1.32	V

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 13: Recommended Operating Conditions for GTP Transceivers<sup>(1)(2)(3)</sup>

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	1.14	1.20	1.26	V

**Notes:**

- Each voltage listed requires the filter circuit described in [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#).
- Voltages are specified for the temperature range of T<sub>j</sub> = -40°C to +125°C.
- The voltage level of MGTAVCCPLL must not exceed the voltage level of MGTAVCC +10mV. The voltage level of MGTAVCC must not exceed the voltage level of MGTAVCCPLL.

Table 14: GTP Transceiver Current Supply (per Lane)

Symbol	Description	Typ <sup>(1)</sup>	Max	Units
I <sub>MGTAVCC</sub>	GTP transceiver internal analog supply current	40.4	Note 2	mA
I <sub>MGTAVTTTX</sub>	GTP transmitter termination supply current	27.4		mA
I <sub>MGTAVTTRX</sub>	GTP receiver termination supply current	13.6		mA
I <sub>MGTAVCCPLL</sub>	GTP transmitter and receiver PLL supply current	28.7		mA
R <sub>MGTRREF</sub>	Precision reference resistor for internal calibration termination	50.0 ± 1% tolerance		Ω

**Notes:**

- Typical values are specified at nominal voltage, 25°C, with a 2.5 Gb/s line rate, with a shared PLL use mode.
- Values for currents of other transceiver configurations and conditions can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

 Table 15: GTP Transceiver Quiescent Supply Current (per Lane)<sup>(1)(2)(3)(4)</sup>

Symbol	Description	Typ <sup>(5)</sup>	Max	Units
I <sub>MGTAVCCQ</sub>	Quiescent MGTAVCC supply current	1.7	Note 2	mA
I <sub>MGTAVTTTXQ</sub>	Quiescent MGTAVTTTX supply current	0.1		mA
I <sub>MGTAVTTRXQ</sub>	Quiescent MGTAVTTRX supply current	1.2		mA
I <sub>MGTAVCCPLLQ</sub>	Quiescent MGTAVCCPLL supply current	1.0		mA

**Notes:**

- Device powered and unconfigured.
- Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
- GTP transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTP transceivers.
- Does not include power-up MGTAVTTRCAL supply current during device configuration.
- Typical values are specified at nominal voltage, 25°C.



## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [Switching Characteristics, page 19](#).

Table 25: Interface Performances

Description	I/O Resource	Clock Buffer	Data Width	Speed Grade				Units
				-3	-3N	-2	-1L	
<b>Networking Applications<sup>(1)</sup></b>								
SDR LVDS transmitter or receiver	IOB SDR register	BUFG	–	400	400	375	250	Mb/s
DDR LVDS transmitter or receiver	ODDR2/IDDR2 register	2 BUFGs	–	800	800	750	500	Mb/s
SDR LVDS transmitter	OSERDES2	BUFPLL	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
DDR LVDS transmitter	OSERDES2	2 BUFIO2s	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
SDR LVDS receiver	ISERDES2 in RETIMED mode	BUFPLL	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
DDR LVDS receiver	ISERDES2 in RETIMED mode	2 BUFIO2s	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
<b>Memory Interfaces (Implemented using the Spartan-6 FPGA Memory Controller Block)<sup>(2)</sup></b>								
<b>Standard Performance (Standard V<sub>CCINT</sub>)</b>								
DDR				400	<a href="#">Note 4</a>	400	350	Mb/s
DDR2				667	<a href="#">Note 4</a>	625	400	Mb/s
DDR3				800	<a href="#">Note 4</a>	667	—	Mb/s
LPDDR (Mobile_DDR)				400	<a href="#">Note 4</a>	400	350	Mb/s
<b>Extended Performance (Requires Extended Performance V<sub>CCINT</sub>)<sup>(3)</sup></b>								
DDR2				800	<a href="#">Note 4</a>	667	—	Mb/s

**Notes:**

1. Refer to [XAPP1064](#), *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)* and [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.
2. Refer to [UG388](#), *Spartan-6 FPGA Memory Controller User Guide*.
3. Extended Memory Controller block performance for DDR2 can be achieved using the extended performance V<sub>CCINT</sub> range from [Table 2](#).
4. The LX4 device, all devices in the TQG144 and CPG196 packages, and the -3N speed grade do not support a Memory Controller Block.

## Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.20 for -3, -3N, and -2; and v1.08 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

### Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

The -1L speed grade refers to the lower-power Spartan-6 devices. The -3N speed grade refers to the Spartan-6 devices that do not support MCB functionality.

[Table 26](#) correlates the current status of each Spartan-6 device on a per speed grade basis.

## Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-6 devices.

Table 26: Spartan-6 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6SLX4 <sup>(1)</sup>			-3, -2, -1L
XC6SLX9			-3, -3N, -2, -1L
XC6SLX16			-3, -3N, -2, -1L
XC6SLX25			-3, -3N, -2, -1L
XC6SLX25T			-3, -3N, -2
XC6SLX45			-3, -3N, -2, -1L
XC6SLX45T			-3, -3N, -2
XC6SLX75			-3, -3N, -2, -1L
XC6SLX75T			-3, -3N, -2
XC6SLX100			-3, -3N, -2, -1L
XC6SLX100T			-3, -3N, -2
XC6SLX150			-3, -3N, -2, -1L
XC6SLX150T			-3, -3N, -2
XA6SLX4			-3, -2
XA6SLX9			-3, -2
XA6SLX16			-3, -2
XA6SLX25			-3, -2
XA6SLX25T			-3, -2
XA6SLX45			-3, -2
XA6SLX45T			-3, -2
XA6SLX75			-3, -2
XA6SLX75T			-3, -2
XA6SLX100			-2
XQ6SLX75			-2, -1L
XQ6SLX75T			-3, -2
XQ6SLX150			-2, -1L
XQ6SLX150T			-3, -2

### Notes:

1. The XC6SLX4 is not available in the -3N speed grade.

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T <sub>IOPI</sub>				T <sub>IOOP</sub>				T <sub>IOTP</sub>				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	
LVTTTL, QUIETIO, 2 mA	1.35	1.47	1.60	1.82	5.39	5.53	5.73	6.37	5.39	5.53	5.73	6.37	ns
LVTTTL, QUIETIO, 4 mA	1.35	1.47	1.60	1.82	4.29	4.43	4.63	5.22	4.29	4.43	4.63	5.22	ns
LVTTTL, QUIETIO, 6 mA	1.35	1.47	1.60	1.82	3.75	3.89	4.09	4.69	3.75	3.89	4.09	4.69	ns
LVTTTL, QUIETIO, 8 mA	1.35	1.47	1.60	1.82	3.23	3.37	3.57	4.20	3.23	3.37	3.57	4.20	ns
LVTTTL, QUIETIO, 12 mA	1.35	1.47	1.60	1.82	3.28	3.42	3.62	4.22	3.28	3.42	3.62	4.22	ns
LVTTTL, QUIETIO, 16 mA	1.35	1.47	1.60	1.82	2.94	3.08	3.28	3.92	2.94	3.08	3.28	3.92	ns
LVTTTL, QUIETIO, 24 mA	1.35	1.47	1.60	1.82	2.69	2.83	3.03	3.67	2.69	2.83	3.03	3.67	ns
LVTTTL, Slow, 2 mA	1.35	1.47	1.60	1.82	4.36	4.50	4.70	5.30	4.36	4.50	4.70	5.30	ns
LVTTTL, Slow, 4 mA	1.35	1.47	1.60	1.82	3.17	3.31	3.51	4.16	3.17	3.31	3.51	4.16	ns
LVTTTL, Slow, 6 mA	1.35	1.47	1.60	1.82	2.76	2.90	3.10	3.75	2.76	2.90	3.10	3.75	ns
LVTTTL, Slow, 8 mA	1.35	1.47	1.60	1.82	2.59	2.73	2.93	3.55	2.59	2.73	2.93	3.55	ns
LVTTTL, Slow, 12 mA	1.35	1.47	1.60	1.82	2.58	2.72	2.92	3.54	2.58	2.72	2.92	3.54	ns
LVTTTL, Slow, 16 mA	1.35	1.47	1.60	1.82	2.39	2.53	2.73	3.40	2.39	2.53	2.73	3.40	ns
LVTTTL, Slow, 24 mA	1.35	1.47	1.60	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVTTTL, Fast, 2 mA	1.35	1.47	1.60	1.82	3.78	3.92	4.12	4.74	3.78	3.92	4.12	4.74	ns
LVTTTL, Fast, 4 mA	1.35	1.47	1.60	1.82	2.49	2.63	2.83	3.45	2.49	2.63	2.83	3.45	ns
LVTTTL, Fast, 6 mA	1.35	1.47	1.60	1.82	2.44	2.58	2.78	3.40	2.44	2.58	2.78	3.40	ns
LVTTTL, Fast, 8 mA	1.35	1.47	1.60	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns
LVTTTL, Fast, 12 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTTL, Fast, 16 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTTL, Fast, 24 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVC MOS33, QUIETIO, 2 mA	1.34	1.46	1.59	1.82	5.40	5.54	5.74	6.37	5.40	5.54	5.74	6.37	ns
LVC MOS33, QUIETIO, 4 mA	1.34	1.46	1.59	1.82	4.03	4.17	4.37	5.01	4.03	4.17	4.37	5.01	ns
LVC MOS33, QUIETIO, 6 mA	1.34	1.46	1.59	1.82	3.51	3.65	3.85	4.47	3.51	3.65	3.85	4.47	ns
LVC MOS33, QUIETIO, 8 mA	1.34	1.46	1.59	1.82	3.37	3.51	3.71	4.33	3.37	3.51	3.71	4.33	ns
LVC MOS33, QUIETIO, 12 mA	1.34	1.46	1.59	1.82	2.94	3.08	3.28	3.93	2.94	3.08	3.28	3.93	ns
LVC MOS33, QUIETIO, 16 mA	1.34	1.46	1.59	1.82	2.77	2.91	3.11	3.78	2.77	2.91	3.11	3.78	ns
LVC MOS33, QUIETIO, 24 mA	1.34	1.46	1.59	1.82	2.59	2.73	2.93	3.58	2.59	2.73	2.93	3.58	ns
LVC MOS33, Slow, 2 mA	1.34	1.46	1.59	1.82	4.37	4.51	4.71	5.28	4.37	4.51	4.71	5.28	ns
LVC MOS33, Slow, 4 mA	1.34	1.46	1.59	1.82	2.98	3.12	3.32	3.94	2.98	3.12	3.32	3.94	ns
LVC MOS33, Slow, 6 mA	1.34	1.46	1.59	1.82	2.58	2.72	2.92	3.61	2.58	2.72	2.92	3.61	ns
LVC MOS33, Slow, 8 mA	1.34	1.46	1.59	1.82	2.65	2.79	2.99	3.61	2.65	2.79	2.99	3.61	ns
LVC MOS33, Slow, 12 mA	1.34	1.46	1.59	1.82	2.39	2.53	2.73	3.31	2.39	2.53	2.73	3.31	ns
LVC MOS33, Slow, 16 mA	1.34	1.46	1.59	1.82	2.31	2.45	2.65	3.27	2.31	2.45	2.65	3.27	ns
LVC MOS33, Slow, 24 mA	1.34	1.46	1.59	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVC MOS33, Fast, 2 mA	1.34	1.46	1.59	1.82	3.76	3.90	4.10	4.70	3.76	3.90	4.10	4.70	ns
LVC MOS33, Fast, 4 mA	1.34	1.46	1.59	1.82	2.48	2.62	2.82	3.44	2.48	2.62	2.82	3.44	ns
LVC MOS33, Fast, 6 mA	1.34	1.46	1.59	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T <sub>IOPI</sub>				T <sub>IOOP</sub>				T <sub>IOTP</sub>				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	
LVC MOS18, Slow, 24 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVC MOS18, Fast, 2 mA	1.18	1.30	1.43	2.04	3.59	3.73	3.93	4.53	3.59	3.73	3.93	4.53	ns
LVC MOS18, Fast, 4 mA	1.18	1.30	1.43	2.04	2.39	2.53	2.73	3.35	2.39	2.53	2.73	3.35	ns
LVC MOS18, Fast, 6 mA	1.18	1.30	1.43	2.04	1.88	2.02	2.22	2.84	1.88	2.02	2.22	2.84	ns
LVC MOS18, Fast, 8 mA	1.18	1.30	1.43	2.04	1.81	1.95	2.15	2.77	1.81	1.95	2.15	2.77	ns
LVC MOS18, Fast, 12 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVC MOS18, Fast, 16 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVC MOS18, Fast, 24 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVC MOS18_JEDEC, QUIETIO, 2 mA	0.94	1.06	1.19	1.41	5.91	6.05	6.25	6.79	5.91	6.05	6.25	6.79	ns
LVC MOS18_JEDEC, QUIETIO, 4 mA	0.94	1.06	1.19	1.41	4.75	4.89	5.09	5.64	4.75	4.89	5.09	5.64	ns
LVC MOS18_JEDEC, QUIETIO, 6 mA	0.94	1.06	1.19	1.41	4.04	4.18	4.38	4.96	4.04	4.18	4.38	4.96	ns
LVC MOS18_JEDEC, QUIETIO, 8 mA	0.94	1.06	1.19	1.41	3.71	3.85	4.05	4.62	3.71	3.85	4.05	4.62	ns
LVC MOS18_JEDEC, QUIETIO, 12 mA	0.94	1.06	1.19	1.41	3.35	3.49	3.69	4.28	3.35	3.49	3.69	4.28	ns
LVC MOS18_JEDEC, QUIETIO, 16 mA	0.94	1.06	1.19	1.41	3.20	3.34	3.54	4.13	3.20	3.34	3.54	4.13	ns
LVC MOS18_JEDEC, QUIETIO, 24 mA	0.94	1.06	1.19	1.41	2.96	3.10	3.30	3.98	2.96	3.10	3.30	3.98	ns
LVC MOS18_JEDEC, Slow, 2 mA	0.94	1.06	1.19	1.41	4.59	4.73	4.93	5.54	4.59	4.73	4.93	5.54	ns
LVC MOS18_JEDEC, Slow, 4 mA	0.94	1.06	1.19	1.41	3.69	3.83	4.03	4.60	3.69	3.83	4.03	4.60	ns
LVC MOS18_JEDEC, Slow, 6 mA	0.94	1.06	1.19	1.41	3.00	3.14	3.34	3.94	3.00	3.14	3.34	3.94	ns
LVC MOS18_JEDEC, Slow, 8 mA	0.94	1.06	1.19	1.41	2.19	2.33	2.53	3.18	2.19	2.33	2.53	3.18	ns
LVC MOS18_JEDEC, Slow, 12 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVC MOS18_JEDEC, Slow, 16 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVC MOS18_JEDEC, Slow, 24 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVC MOS18_JEDEC, Fast, 2 mA	0.94	1.06	1.19	1.41	3.57	3.71	3.91	4.52	3.57	3.71	3.91	4.52	ns
LVC MOS18_JEDEC, Fast, 4 mA	0.94	1.06	1.19	1.41	2.39	2.53	2.73	3.35	2.39	2.53	2.73	3.35	ns
LVC MOS18_JEDEC, Fast, 6 mA	0.94	1.06	1.19	1.41	1.88	2.02	2.22	2.84	1.88	2.02	2.22	2.84	ns
LVC MOS18_JEDEC, Fast, 8 mA	0.94	1.06	1.19	1.41	1.80	1.94	2.14	2.76	1.80	1.94	2.14	2.76	ns
LVC MOS18_JEDEC, Fast, 12 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVC MOS18_JEDEC, Fast, 16 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVC MOS18_JEDEC, Fast, 24 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVC MOS15, QUIETIO, 2 mA	0.98	1.10	1.23	1.79	5.47	5.61	5.81	6.38	5.47	5.61	5.81	6.38	ns
LVC MOS15, QUIETIO, 4 mA	0.98	1.10	1.23	1.79	4.61	4.75	4.95	5.51	4.61	4.75	4.95	5.51	ns
LVC MOS15, QUIETIO, 6 mA	0.98	1.10	1.23	1.79	4.07	4.21	4.41	4.97	4.07	4.21	4.41	4.97	ns
LVC MOS15, QUIETIO, 8 mA	0.98	1.10	1.23	1.79	3.91	4.05	4.25	4.81	3.91	4.05	4.25	4.81	ns
LVC MOS15, QUIETIO, 12 mA	0.98	1.10	1.23	1.79	3.53	3.67	3.87	4.51	3.53	3.67	3.87	4.51	ns
LVC MOS15, QUIETIO, 16 mA	0.98	1.10	1.23	1.79	3.32	3.46	3.66	4.31	3.32	3.46	3.66	4.31	ns
LVC MOS15, Slow, 2 mA	0.98	1.10	1.23	1.79	4.18	4.32	4.52	5.11	4.18	4.32	4.52	5.11	ns
LVC MOS15, Slow, 4 mA	0.98	1.10	1.23	1.79	3.42	3.56	3.76	4.34	3.42	3.56	3.76	4.34	ns
LVC MOS15, Slow, 6 mA	0.98	1.10	1.23	1.79	2.29	2.43	2.63	3.24	2.29	2.43	2.63	3.24	ns

**Table 33: Spartan-6 FPGA V<sub>CCO</sub>/GND Pairs per Bank**

Package	Devices	Description	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5
TQG144	LX	V <sub>CCO</sub> /GND Pairs	3	3	2	3	N/A	N/A
		Maximum I/O per Pair	8	8	13	8	N/A	N/A
CPG196	LX	V <sub>CCO</sub> /GND Pairs	4	6	4	6	N/A	N/A
		Maximum I/O per Pair	6	4	7	4	N/A	N/A
CSG225	LX	V <sub>CCO</sub> /GND Pairs	4	4	4	4	N/A	N/A
		Maximum I/O per Pair	10	10	9	10	N/A	N/A
FT(G)256	LX	V <sub>CCO</sub> /GND Pairs	5	6	4	5	N/A	N/A
		Maximum I/O per Pair	8	9	9	10	N/A	N/A
CSG324	LX	V <sub>CCO</sub> /GND Pairs	6	6	6	6	N/A	N/A
		Maximum I/O per Pair	10	9	10	9	N/A	N/A
	LXT	V <sub>CCO</sub> /GND Pairs	4	6	6	6	N/A	N/A
		Maximum I/O per Pair	4	9	10	9	N/A	N/A
CS(G)484	LX	V <sub>CCO</sub> /GND Pairs	8	13	8	13	N/A	N/A
		Maximum I/O per Pair	7	8	7	8	N/A	N/A
	LXT	V <sub>CCO</sub> /GND Pairs	7	12	8	13	N/A	N/A
		Maximum I/O per Pair	5	8	6	8	N/A	N/A
FG(G)484	LX	V <sub>CCO</sub> /GND Pairs	10	10	11	11	N/A	N/A
		Maximum I/O per Pair	6	8	9	8	N/A	N/A
	LXT	V <sub>CCO</sub> /GND Pairs	6	10	11	10	N/A	N/A
		Maximum I/O per Pair	7	8	7	8	N/A	N/A
FG(G)676	LX45	V <sub>CCO</sub> /GND Pairs	12	15	10	16	N/A	N/A
		Maximum I/O per Pair	3	7	8	7	N/A	N/A
	LX75, LX100, LX150	V <sub>CCO</sub> /GND Pairs	12	9	10	10	6	6
		Maximum I/O per Pair	9	10	9	9	8	9
	LXT	V <sub>CCO</sub> /GND Pairs	10	8	10	8	7	7
		Maximum I/O per Pair	8	7	8	8	7	7
FG(G)900	LX	V <sub>CCO</sub> /GND Pairs	17	14	17	14	7	8
		Maximum I/O per Pair	7	6	7	8	7	6
	LXT	V <sub>CCO</sub> /GND Pairs	15	14	13	14	7	8
		Maximum I/O per Pair	7	6	8	8	7	6

Table 34: SSO Limit per V<sub>CCO</sub>/GND Pair (Cont'd)

V <sub>CCO</sub>	I/O Standard	Drive	Slew	SSO Limit per V <sub>CCO</sub> /GND Pair					
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324			
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5		
3.3V	LVTTTL	2	Fast	53	65	53	62		
			Slow	70	80	70	73		
			QuietIO	79	89	79	91		
		4	Fast	23	30	23	27		
			Slow	34	41	34	37		
			QuietIO	44	49	44	46		
		6	Fast	16	21	16	20		
			Slow	21	28	21	25		
			QuietIO	34	39	34	34		
		8	Fast	12	16	12	15		
			Slow	16	22	16	19		
			QuietIO	27	28	27	24		
		12	Fast	1	3	1	1		
			Slow	2	5	2	4		
			QuietIO	2	10	2	8		
		16	Fast	1	3	1	1		
			Slow	1	7	1	2		
			QuietIO	3	11	3	8		
		24	Fast	1	2	1	1		
			Slow	2	5	2	2		
			QuietIO	8	9	8	8		
			PCI33_3			18	19	18	19
			PCI66_3			18	19	18	19
			SSTL_3_I			5	8	5	8
			SSTL_3_II			3	5	3	3
			DIFF_SSTL_3_I			15	24	15	24
			DIFF_SSTL_3_II			9	15	9	9
	SDIO			17	18	17	15		

## Input/Output Delay Switching Characteristics

Table 39: IODELAY2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L <sup>(3)</sup>	
$T_{\text{IODCCK\_CAL}} / T_{\text{IODCKC\_CAL}}$	CAL pin Setup/Hold with respect to CK	0.28/ -0.13	0.33/ -0.13	0.48/ -0.13	N/A	ns
$T_{\text{IODCCK\_CE}} / T_{\text{IODCKC\_CE}}$	CE pin Setup/Hold with respect to CK	0.17/ -0.03	0.17/ -0.03	0.25/ -0.02	N/A	ns
$T_{\text{IODCCK\_INC}} / T_{\text{IODCKC\_INC}}$	INC pin Setup/Hold with respect to CK	0.10/ 0.02	0.12/ 0.03	0.18/ 0.06	N/A	ns
$T_{\text{IODCCK\_RST}} / T_{\text{IODCKC\_RST}}$	RST pin Setup/Hold with respect to CK	0.12/ -0.02	0.15/ -0.02	0.22/ -0.01	N/A	ns
$T_{\text{TAP1}}^{(2)}$	Maximum tap 1 delay	8	14	16	N/A	ps
$T_{\text{TAP2}}$	Maximum tap 2 delay	40	66	77	N/A	ps
$T_{\text{TAP3}}$	Maximum tap 3 delay	95	120	140	N/A	ps
$T_{\text{TAP4}}$	Maximum tap 4 delay	108	141	166	N/A	ps
$T_{\text{TAP5}}$	Maximum tap 5 delay	171	194	231	N/A	ps
$T_{\text{TAP6}}$	Maximum tap 6 delay	207	249	292	N/A	ps
$T_{\text{TAP7}}$	Maximum tap 7 delay	212	276	343	N/A	ps
$T_{\text{TAP8}}$	Maximum tap 8 delay	322	341	424	N/A	ps
$F_{\text{MINCAL}}$	Minimum allowed bit rate for calibration in variable mode: VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX, and DIFF_PHASE_DETECTOR.	188	188	188	N/A	Mb/s
$T_{\text{IODDO\_IDATAIN}}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	–
$T_{\text{IODDO\_ODATAIN}}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	–

### Notes:

- Delay depends on IODELAY2 tap setting. See TRACE report for actual values.
- Maximum delay = integer (number of taps/8)  $\times$   $T_{\text{TAP8}}$  +  $T_{\text{TAPn}}$  (where n equals the remainder). For minimum delay consult the TRACE setup and hold report. Minimum delay is typically greater than 30% of the maximum delay. Tap delays can vary by device and overall conditions. See TRACE report for actual values.
- Spartan-6 -1L devices only support tap 0. See TRACE report for actual values.

## DSP48A1 Switching Characteristics

Table 44: DSP48A1 Switching Characteristics

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-3	-3N	-2	-1L	
<b>Setup and Hold Times of Data/Control Pins to the Input Register Clock</b>									
$T_{DSPDCK\_A\_A1REG}/$ $T_{DSPCKD\_A\_A1REG}$	A input to A1 register CLK	N/A	N/A	N/A	0.15/ 0.09	0.17/ 0.09	0.17/ 0.09	0.32/ 0.09	ns
$T_{DSPDCK\_D\_B1REG}/$ $T_{DSPCKD\_D\_B1REG}$	D input to B1 register CLK	Yes	N/A	N/A	1.90/ -0.07	1.95/ -0.07	1.95/ -0.07	2.82/ -0.07	ns
$T_{DSPDCK\_C\_CREG}/$ $T_{DSPCKD\_C\_CREG}$	C input to C register CLK for XC devices	N/A	N/A	N/A	0.11/ 0.15	0.13/ 0.15	0.13/ 0.15	0.24/ 0.09	ns
	C input to C register CLK for XA and XQ devices				0.11/ 0.19	N/A	0.13/ 0.23	0.24/ 0.09	
$T_{DSPDCK\_D\_DREG}/$ $T_{DSPCKD\_D\_DREG}$	D input to D register CLK for XC devices	N/A	N/A	N/A	0.09/ 0.15	0.10/ 0.15	0.10/ 0.15	0.19/ 0.12	ns
	D input to D register CLK for XA and XQ devices				0.09/ 0.23	N/A	0.10/ 0.27	0.19/ 0.12	
$T_{DSPDCK\_OPMODE\_B1REG}/$ $T_{DSPCKD\_OPMODE\_B1REG}$	OPMODE input to B1 register CLK	Yes	N/A	N/A	1.97/ 0.01	2.00/ 0.01	2.00/ 0.01	2.85/ 0.01	ns
$T_{DSPDCK\_OPMODE\_OPMODEREG}/$ $T_{DSPCKD\_OPMODE\_OPMODEREG}$	OPMODE input to OPMODE register CLK for XC devices	N/A	N/A	N/A	0.18/ 0.12	0.21/ 0.12	0.21/ 0.12	0.40/ 0.12	ns
	OPMODE input to OPMODE register CLK for XA and XQ devices				0.18/ 0.16	N/A	0.21/ 0.22	0.40/ 0.12	
<b>Setup and Hold Times of Data Pins to the Pipeline Register Clock</b>									
$T_{DSPDCK\_A\_MREG}/$ $T_{DSPCKD\_A\_MREG}$	A input to M register CLK	N/A	Yes	N/A	3.06/ -0.40	3.51/ -0.40	3.51/ -0.40	3.97/ -0.40	ns
$T_{DSPDCK\_B\_MREG}/$ $T_{DSPCKD\_B\_MREG}$	B input to M register CLK	Yes	Yes	N/A	3.96/ -0.68	4.58/ -0.68	4.58/ -0.68	7.00/ -0.68	ns
$T_{DSPDCK\_D\_MREG}/$ $T_{DSPCKD\_D\_MREG}$	D input to M register CLK	Yes	Yes	N/A	4.23/ -0.56	4.80/ -0.56	4.80/ -0.56	6.84/ -0.56	ns
$T_{DSPDCK\_OPMODE\_MREG}/$ $T_{DSPCKD\_OPMODE\_MREG}$	OPMODE to M register CLK	Yes	Yes	N/A	4.18/ -0.48	4.80/ -0.48	4.80/ -0.48	6.88/ -0.48	ns
		No	Yes	N/A	2.37/ -0.48	2.70/ -0.48	2.70/ -0.48	4.28/ -0.48	ns
<b>Setup and Hold Times of Data/Control Pins to the Output Register Clock</b>									
$T_{DSPDCK\_A\_PREG}/$ $T_{DSPCKD\_A\_PREG}$	A input to P register CLK	N/A	Yes	Yes	4.32/ -0.76	5.06/ -0.76	5.06/ -0.76	7.52/ -0.76	ns
$T_{DSPDCK\_B\_PREG}/$ $T_{DSPCKD\_B\_PREG}$	B input to P register CLK	Yes	Yes	Yes	5.87/ -0.59	6.87/ -0.59	6.87/ -0.59	10.55/ -0.59	ns
		No	Yes	Yes	4.14/ -0.93	4.68/ -0.93	4.68/ -0.93	8.12/ -0.93	ns
$T_{DSPDCK\_C\_PREG}/$ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK	N/A	N/A	Yes	2.20/ -0.23	2.25/ -0.23	2.25/ -0.23	3.27/ -0.23	ns
$T_{DSPDCK\_D\_PREG}/$ $T_{DSPCKD\_D\_PREG}$	D input to P register CLK	Yes	Yes	Yes	5.90/ -0.92	6.91/ -0.92	6.91/ -0.92	10.39/ -0.92	ns



Table 44: DSP48A1 Switching Characteristics (Cont'd)

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-3	-3N	-2	-1L	
T <sub>DSPDCK_OPMODE_PREG</sub> / T <sub>DSPCKD_OPMODE_PREG</sub>	OPMODE input to P register CLK	Yes	Yes	Yes	6.21/ -0.84	7.27/ -0.84	7.27/ -0.84	10.43/ -0.84	ns
		No	Yes	Yes	1.69/ -0.87	1.98/ -0.87	1.98/ -0.87	3.62/ -0.87	ns
		No	No	Yes	2.09/ -0.22	2.30/ -0.22	2.30/ -0.22	3.79/ -0.22	ns
<b>Clock to Out from Output Register Clock to Output Pin</b>									
T <sub>DSPCKO_P_PREG</sub>	CLK (PREG) to P output	N/A	N/A	N/A	1.20	1.34	1.34	1.90	ns
<b>Clock to Out from Pipeline Register Clock to Output Pins</b>									
T <sub>DSPCKO_P_MREG</sub>	CLK (MREG) to P output	N/A	N/A	Yes	3.38	3.95	3.95	5.83	ns
<b>Clock to Out from Input Register Clock to Output Pins</b>									
T <sub>DSPCKO_P_A1REG</sub>	CLK (A1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.65	ns
T <sub>DSPCKO_P_B1REG</sub>	CLK (B1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.63	ns
T <sub>DSPCKO_P_CREG</sub>	CLK (CREG) to P output	N/A	N/A	Yes	3.12	3.64	3.64	5.24	ns
T <sub>DSPCKO_P_DREG</sub>	CLK (DREG) to P output	Yes	Yes	Yes	6.77	7.92	7.92	12.53	ns
<b>Combinatorial Delays from Input Pins to Output Pins</b>									
T <sub>DSPDO_A_P</sub>	A input to P output	N/A	No	Yes	2.85	3.33	3.33	4.73	ns
		N/A	Yes	No <sup>(2)</sup>	3.35	3.93	3.93	6.74	ns
		N/A	Yes	Yes	4.56	5.22	5.22	8.94	ns
T <sub>DSPDO_B_P</sub>	B input to P output	Yes	No	No <sup>(2)</sup>	3.22	3.76	3.76	5.55	ns
		Yes	Yes	No <sup>(2)</sup>	6.01	6.54	6.54	9.76	ns
		Yes	Yes	Yes	6.27	7.34	7.34	11.96	ns
T <sub>DSPDO_C_P</sub>	C input to P output	N/A	N/A	Yes	2.69	3.15	3.15	4.68	ns
T <sub>DSPDO_D_P</sub>	D input to P output	Yes	Yes	Yes	6.31	7.38	7.38	11.81	ns
T <sub>DSPDO_OPMODE_P</sub>	OPMODE input to P output	Yes	Yes	Yes	6.43	7.52	7.52	11.84	ns
		No	Yes	Yes	4.84	5.66	5.66	9.25	ns
		No	No	Yes	3.11	3.49	3.49	5.03	ns
<b>Maximum Frequency</b>									
F <sub>MAX</sub>	All registers used	Yes	Yes	Yes	390	333	333	213	MHz

**Notes:**

1. A Yes signifies that the component is in the path. A No signifies that the component is being bypassed. N/A signifies not applicable because no path exists.
2. Implemented in the post-adder by adding to zero.

## Configuration Switching Characteristics

Table 47: Configuration Switching Characteristics<sup>(1)</sup>

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
<b>Power-up Timing Characteristics</b>						
T <sub>PL</sub> <sup>(2)</sup>	PROGRAM_B Latency	4	4	4	5	ms, Max
T <sub>POR</sub> <sup>(2)</sup>	Power-on reset (50 ms ramp time) <sup>(3)</sup>	5/30	5/34	5/40	5/40	ms, Min/Max
	Power-on reset (10 ms ramp time)	5/25	5/29	5/35	5/40	ms, Min/Max
T <sub>PROGRAM</sub>	PROGRAM_B Pulse Width	500	500	500	500	ns, Min
<b>Slave Serial Mode Programming Switching</b>						
T <sub>DCCK</sub> /T <sub>CCKD</sub>	DIN Setup/Hold, slave mode	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T <sub>CCO</sub>	CCLK to DOUT	12	12	12	17	ns, Max
F <sub>SCCK</sub>	Slave mode external CCLK	80	80	80	50	MHz, Max
<b>Slave SelectMAP Mode Programming Switching</b>						
T <sub>SMDCCK</sub> /T <sub>SMCCKD</sub>	SelectMAP Data Setup/Hold	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T <sub>SMCSCCK</sub> /T <sub>SMCCKCS</sub>	CSI_B Setup/Hold	7.0/0.0	7.0/0.0	7.0/0.0	9.0/2.0	ns, Min
T <sub>SMWCCK</sub> /T <sub>SMCCKW</sub>	RDWR_B Setup/Hold	17.0/1.0	17.0/1.0	17.0/1.0	27.0/2.0	ns, Min
T <sub>SMCKCSO</sub>	CSO_B clock to out	16	16	16	26	ns, Max
T <sub>SMCO</sub>	CCLK to DATA out in readback	13	13	13	25	ns, Max
T <sub>SMCKBY</sub>	CCLK to BUSY out in readback	12	12	12	17	ns, Max
F <sub>SMCCK</sub>	Maximum CCLK frequency (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	25	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x8 mode, LX150, and LX150T only)	40	40	40	20	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x16 mode only)	35	35	35	20	MHz, Max
F <sub>RBCK</sub>	Maximum Readback CCLK frequency, including block RAM (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	20	20	20	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	30	MHz, Max
	Maximum Readback CCLK frequency, including block RAM (LX100, LX100T, LX150, and LX150T only)	12	12	12	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX100, LX100T, LX150, and LX150T only)	35	35	35	20	MHz, Max
<b>Boundary-Scan Port Timing Specifications</b>						
T <sub>TAPTCK</sub>	TMS and TDI Setup time before TCK	10	10	10	17	ns, Min
T <sub>TCKTAP</sub>	TMS and TDI Hold time after TCK	5.5	5.5	5.5	5.5	ns, Min
T <sub>TCKTDO</sub>	TCK falling edge to TDO output valid	6.5	6.5	6.5	8	ns, Max
T <sub>TCKH</sub>	TCK clock minimum High time	12	12	12	21	ns, Min
T <sub>TCKL</sub>	TCK clock minimum Low time	12	12	12	21	ns, Min
F <sub>TCK</sub>	Maximum configuration TCK clock frequency	33	33	33	18	MHz, Max
F <sub>TCKB</sub>	Maximum boundary-scan TCK clock frequency	33	33	33	18	MHz, Max
F <sub>TCKAES</sub>	Maximum AES key TCK clock frequency	2	2	2	2	MHz, Max

## Clock Buffers and Networks

Table 48: Global Clock Switching Characteristics (BUFGMUX)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T <sub>GSI</sub>	S pin Setup to I0/I1 inputs	LX devices	0.25	0.31	0.48	0.48	ns
		LXT devices	0.25	0.31	0.48	N/A	ns
T <sub>GIO</sub>	BUFGMUX delay from I0/I1 to O	LX devices	0.21	0.21	0.21	0.21	ns
		LXT devices	0.21	0.21	0.21	N/A	ns
<b>Maximum Frequency</b>							
F <sub>MAX</sub>	Global clock tree (BUFGMUX)	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 49: Input/Output Clock Switching Characteristics (BUFIO2)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T <sub>BUFCO_O</sub>	Clock to out delay from I to O	LX devices	0.67	0.82	1.09	1.50	ns
		LXT devices	0.67	0.82	1.09	N/A	ns
<b>Maximum Frequency</b>							
F <sub>MAX</sub>	I/O clock tree (BUFIO2)	LX devices	540	525	500	300	MHz
		LXT devices	540	525	500	N/A	MHz

Table 50: Input/Output Clock Switching Characteristics (BUFIO2FB)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
<b>Maximum Frequency</b>							
F <sub>MAX</sub>	I/O clock tree (BUFIO2FB)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

Table 51: Input/Output Clock Switching Characteristics (BUFPLL)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
<b>Maximum Frequency</b>							
F <sub>MAX</sub>	BUFPLL clock tree (BUFPLL)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

## PLL Switching Characteristics

Table 52: PLL Specification

Symbol	Description	Device <sup>(1)</sup>	Speed Grade				Units
			-3	-3N	-2	-1L	
F <sub>INMAX</sub>	Maximum Input Clock Frequency from I/O Clock	LX devices	540	525	450	300	MHz
		LXT devices	540	525	450	N/A	MHz
	Maximum Input Clock Frequency from Global Clock	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 56: Switching Characteristics for the Digital Frequency Synthesizer (DFS) for DCM\_SP<sup>(1)</sup>

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
<b>Output Frequency Ranges</b>										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz
<b>Output Clock Jitter<sup>(2)(3)</sup></b>										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN < 20 MHz	Use the Clocking Wizard								ps
	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN > 20 MHz	Typical = ±(1% of CLKFX period + 100)								ps
<b>Duty Cycle<sup>(4)(5)</sup></b>										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±(1% of CLKFX period + 350)								ps
<b>Phase Alignment<sup>(5)</sup></b>										
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used	-	±200	-	±200	-	±200	-	±250	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used	Maximum = ±(1% of CLKFX period + 200)								ps
<b>LOCKED Time</b>										
LOCK_FX <sup>(2)</sup>	When FCLKIN < 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	-	5	-	5	-	5	-	5	ms
	When FCLKIN > 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	-	0.45	-	0.45	-	0.45	-	0.60	ms

**Notes:**

1. The values in this table are based on the operating conditions described in Table 2 and Table 55.
2. For optimal jitter tolerance and a faster LOCK time, use the CLKIN\_PERIOD attribute.
3. Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
5. Some duty cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.

Date	Version	Description of Revisions
01/10/11	1.11	<p>Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v12.4 software with speed specification v1.15 for the -4, -3, -3N, and -2 speed grades. Added note 3 to <a href="#">Table 27</a>. Also updated the -1L speed grade requirements to ISE v12.4 software with speed specification v1.06. Revised -3N definition throughout the document.</p> <p>Added note 4 to <a href="#">Table 2</a> and updated note 5. Added information on <math>V_{CCINT}</math> to note 1 in <a href="#">Table 5</a>. Updated Networking Applications -3 values in <a href="#">Table 25</a> to match improvements made in ISE v12.4. In <a href="#">Table 28</a>, added note 1 and revised the <math>T_{IOTP}</math> values for LVDS_33, LVDS_25, MINI_LVDS_33, MINI_LVDS_25, RSDS_33, RSDS_25, TMDS_33, PPDS_33, and PPDS_25. Added note 3 to <a href="#">Table 55</a>.</p>
02/11/11	1.12	<p>As described in <a href="#">XCN11008: Product Discontinuation Notice For Spartan-6 LXT -4 Devices</a>, the -4 speed specifications have been discontinued. As outlined in page 2 of the XCN, designers currently using -4 speed specifications should rerun timing analysis using the new -3 speed specifications before moving to a replacement device.</p> <p>Updated the networking applications section of <a href="#">Table 25</a>. Updated -2 speed specifications throughout document and added note 3 to <a href="#">Table 27</a> advising designers to use the -2 speed specification update (v1.17) with the ISE 12.4 software patch. Added <math>F_{CLKDIV}</math> to <a href="#">Table 37</a> and <a href="#">Table 38</a>. Updated note 2 in <a href="#">Table 39</a>. Updated units for <math>T_{SMCKCSO}</math> and <math>T_{BPICCO}</math> in <a href="#">Table 47</a>. Updated -1L in <a href="#">Table 71</a>. Removed Note 2: <i>Package delay information is available for these device/package combinations. This information can be used to deskew the package</i> from <a href="#">Table 79</a>.</p>
03/31/11	2.0	<p>Production release of XC6SLX45 in the -1L speed grades listed in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v13.1 software with -1L speed specification v1.06.</p> <p>In <a href="#">Table 39</a>, removed values in the -1L column and added note 3 as IODELAY2 only supports Tap0 for lower-power devices. Updated copyright <a href="#">page 1</a> and <a href="#">Notice of Disclaimer</a>.</p>
05/20/11	2.1	<p>Production release of XC6SLX100 and XC6SLX150 in the specific speed grades listed in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v13.1 software with -1L speed specification v1.06. Updated <a href="#">Table 27</a> and <a href="#">Note 7</a> with changes per <a href="#">XCN11012: Speed File Change for -3N Devices</a>. Revised <a href="#">Switching Characteristics</a> section for speed specifications: v1.18 for -3, -3N, and -2; including improvements in <a href="#">Table 73</a> through <a href="#">Table 77</a> and <a href="#">Table 81</a>.</p> <p>Removed <i>Memory Controller Block</i> from the performance heading in <a href="#">Table 2</a> and revised <a href="#">Note 2</a>. In <a href="#">Table 4</a>, added <a href="#">Note 1</a> to <math>C_{IN}</math> and updated the description of <math>R_{IN\_TERM}</math>. Updated <a href="#">Note 1</a> in <a href="#">Table 5</a>. Updated <a href="#">Note 1</a> of <a href="#">Table 7</a>. In <a href="#">Table 25</a>, added and removed -1L specifications, increased the standard performance DDR3 specifications, removed the extended performance DDR3 row and updated <a href="#">Note 3</a> and <a href="#">Note 4</a>. Clarified the introductory information for <a href="#">Table 28</a> and <a href="#">Table 30</a>.</p> <p>In <a href="#">Table 32</a>: Revised <math>V_{MEAS}</math> value for LVCMOS12; revised <math>V_{REF}</math> for LVDS_25, LVDS_33, BLVDS_25, MINI_LVDS_25, MINI_LVDS_33, RSDS_25, and RSDS_33; revised <math>R_{REF}</math> for BLVDS_25 and TMDS_33; and added <a href="#">Note 4</a> and <a href="#">Note 5</a>. Updated <a href="#">Note 2</a> and <a href="#">Note 3</a> in <a href="#">Table 39</a>.</p> <p>In <a href="#">Table 47</a>, revised the values and description of <math>T_{POR}</math> including adding <a href="#">Note 3</a>. Also in <a href="#">Table 47</a>, augmented the description and added specifications for <math>F_{RBCK}</math> and removed XC6SLX4 from <math>F_{MCCK}</math> (maximum frequency, parallel mode (Master SelectMAP/BPI)). Added BUFGMUX to <a href="#">Table 48</a> title. Added <a href="#">Table 50</a>.</p> <p>In <a href="#">Table 52</a>, revised specifications for <math>T_{EXTFVAR}</math> and <math>F_{INJITTER}</math>. In <a href="#">Table 54</a> removed the 5 MHz &lt; <math>CLKIN\_FREQ\_DLL</math> parameter in the LOCK_DLL description. In both <a href="#">Table 56</a> and <a href="#">Table 57</a>, removed the 5 MHz &lt; <math>F_{CLKIN}</math> parameter in the LOCK_FX description. In <a href="#">Table 58</a>, updated description for PSCLK_FREQ and PSCLK_PULSE.</p> <p>Revised title and symbol of <a href="#">Table 70</a>, added new speed specifications for -1L, and added <a href="#">Note 2</a>. Added <a href="#">Table 71</a>.</p>
07/11/11	2.2	<p>Added the Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices to all appropriate tables while sometimes removing the XC6S nomenclature. Added expanded temperature range (Q) to all appropriate tables. Updated <math>T_{SOL}</math> packages in <a href="#">Table 1</a>. Added <math>R_{OUT\_TERM}</math> to <a href="#">Table 4</a>. Updated <a href="#">Note 2</a> on <a href="#">Table 13</a>.</p> <p>Production release of the XC6SLX4, XC6SLX9, XC6SLX16, XC6SLX25, XC6SLX75, XQ6SLX75, and XQ6SLX150 in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v13.2 software with -1L speed specification v1.07.</p> <p>Production release of the XA6SLX16, XA6SLX25T, XA6SLX45, XA6SLX45T, XQ6SLX75, XQ6SLX75T, XQ6SLX150, and XQ6SLX150T in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v13.2 software with -2 and -3 speed specification v1.19.</p> <p>Added <a href="#">Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices(1)</a>. Updated CS(G)484 from CSG484 throughout data sheet. Clarified <a href="#">Note 3</a> in <a href="#">Table 39</a>.</p>
08/08/11	2.3	<p>Production release of the XA6SLX25, XA6SLX75, and XA6SLX75T in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v13.2 software with -2 and -3 speed specification v1.19.</p>