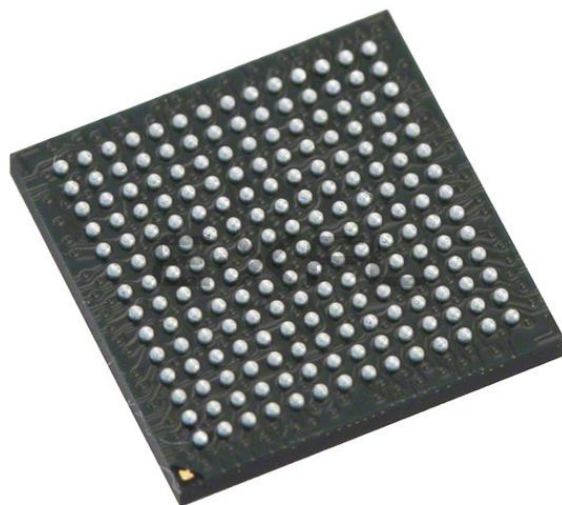




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	300
Number of Logic Elements/Cells	3840
Total RAM Bits	221184
Number of I/O	106
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	196-TFBGA, CSBGA
Supplier Device Package	196-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx4-3cpg196c

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description					Units
V_{IN} and V_{TS} ⁽³⁾	I/O input voltage or voltage applied to 3-state output, relative to GND ⁽⁴⁾	All user and dedicated I/Os	Commercial	DC	–0.60 to 4.10	V
				20% overshoot duration	–0.75 to 4.25	V
				8% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
			Industrial	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
			Expanded (Q)	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
		Restricted to maximum of 100 user I/Os	Commercial	20% overshoot duration	–0.75 to 4.35	V
				15% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
				10% overshoot duration	–0.75 to 4.45	V
			Industrial	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
			Expanded (Q)	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
T_{STG}	Storage temperature (ambient)				–65 to 150	°C
T_{SOL}	Maximum soldering temperature ⁽⁶⁾ (TQG144, CPG196, CSG225, CSG324, CSG484, and FTG256)				+260	°C
	Maximum soldering temperature ⁽⁶⁾ (Pb-free packages: FGG484, FGG676, and FGG900)				+250	°C
	Maximum soldering temperature ⁽⁶⁾ (Pb packages: CS484, FT256, FG484, FG676, and FG900)				+220	°C
T_j	Maximum junction temperature ⁽⁶⁾				+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- When programming eFUSE, $V_{FS} \leq V_{CCAUX}$. Requires up to 40 mA current. For read mode, V_{FS} can be between GND and 3.45 V.
- I/O absolute maximum limit applied to DC and AC signals. Overshoot duration is the percentage of a data period that the I/O is stressed beyond 3.45V.
- For I/O operation, refer to [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.
- Maximum percent overshoot duration to meet 4.40V maximum.
- For soldering guidelines and thermal considerations, see [UG385](#): *Spartan-6 FPGA Packaging and Pinout Specification*.

Table 3: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
V_{FS} ⁽²⁾	External voltage supply	3.2	3.3	3.4	V
I_{FS}	V_{FS} supply current	–	–	40	mA
V_{CCAUX}	Auxiliary supply voltage relative to GND	3.2	3.3	3.45	V
R_{FUSE} ⁽³⁾	External resistor from R_{FUSE} pin to GND	1129	1140	1151	Ω
V_{CCINT}	Internal supply voltage relative to GND	1.14	1.2	1.26	V
t_j	Temperature range	15	–	85	°C

Notes:

- These specifications apply during programming of the eFUSE AES key. Programming is only supported through JTAG. The AES key is only supported in the following devices: LX75, LX75T, LX100, LX100T, LX150, and LX150T.
- When programming eFUSE, V_{FS} must be less than or equal to V_{CCAUX} . When not programming or when eFUSE is not used, Xilinx recommends connecting V_{FS} to GND. However, V_{FS} can be between GND and 3.45 V.
- An R_{FUSE} resistor is required when programming the eFUSE AES key. When not programming or when eFUSE is not used, Xilinx recommends connecting the R_{FUSE} pin to V_{CCAUX} or GND. However, R_{FUSE} can be unconnected.

SelectIO™ Interface DC Input and Output Levels

Table 7: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

I/O Standard	V _{CCO} for Drivers ⁽¹⁾			V _{REF} for Inputs		
	V, Min	V, Nom	V, Max	V, Min	V, Nom	V, Max
LVTTTL	3.0	3.3	3.45	V _{REF} is not used for these I/O standards		
LVC MOS33	3.0	3.3	3.45			
LVC MOS25	2.3	2.5	2.7			
LVC MOS18	1.65	1.8	1.95			
LVC MOS18_JEDEC	1.65	1.8	1.95			
LVC MOS15	1.4	1.5	1.6			
LVC MOS15_JEDEC	1.4	1.5	1.6			
LVC MOS12	1.1	1.2	1.3			
LVC MOS12_JEDEC	1.1	1.2	1.3			
PCI33_3 ⁽²⁾	3.0	3.3	3.45			
PCI66_3 ⁽²⁾	3.0	3.3	3.45			
I2C	2.7	3.0	3.45			
SMBUS	2.7	3.0	3.45			
SDIO	3.0	3.3	3.45			
MOBILE_DDR	1.7	1.8	1.9			
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_II	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_III	1.4	1.5	1.6	–	0.9	–
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–
HSTL_III_18	1.7	1.8	1.9	–	1.1	–
SSTL3_I	3.0	3.3	3.45	1.3	1.5	1.7
SSTL3_II	3.0	3.3	3.45	1.3	1.5	1.7
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38
SSTL18_I	1.7	1.8	1.9	0.833	0.9	0.969
SSTL18_II	1.7	1.8	1.9	0.833	0.9	0.969
SSTL15_II	1.425	1.5	1.575	0.69	0.75	0.81

Notes:

1. V_{CCO} range required when using I/O standard for an output. Also required for MOBILE_DDR, PCI33_3, LVC MOS18_JEDEC, LVC MOS15_JEDEC, and LVC MOS12_JEDEC inputs, and for LVC MOS25 inputs when V_{CCAUX} = 3.3V.
2. For PCI systems, the transmitter and receiver should have common supplies for V_{CCO}.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [Switching Characteristics, page 19](#).

Table 25: Interface Performances

Description	I/O Resource	Clock Buffer	Data Width	Speed Grade				Units
				-3	-3N	-2	-1L	
Networking Applications ⁽¹⁾								
SDR LVDS transmitter or receiver	IOB SDR register	BUFG	–	400	400	375	250	Mb/s
DDR LVDS transmitter or receiver	ODDR2/IDDR2 register	2 BUFPGs	–	800	800	750	500	Mb/s
SDR LVDS transmitter	OSERDES2	BUFPLL	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
DDR LVDS transmitter	OSERDES2	2 BUFIO2s	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
SDR LVDS receiver	ISERDES2 in RETIMED mode	BUFPLL	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
DDR LVDS receiver	ISERDES2 in RETIMED mode	2 BUFIO2s	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
Memory Interfaces (Implemented using the Spartan-6 FPGA Memory Controller Block) ⁽²⁾								
Standard Performance (Standard V _{CCINT})								
DDR				400	Note 4	400	350	Mb/s
DDR2				667	Note 4	625	400	Mb/s
DDR3				800	Note 4	667	—	Mb/s
LPDDR (Mobile_DDR)				400	Note 4	400	350	Mb/s
Extended Performance (Requires Extended Performance V _{CCINT}) ⁽³⁾								
DDR2				800	Note 4	667	—	Mb/s

Notes:

1. Refer to [XAPP1064](#), *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)* and [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.
2. Refer to [UG388](#), *Spartan-6 FPGA Memory Controller User Guide*.
3. Extended Memory Controller block performance for DDR2 can be achieved using the extended performance V_{CCINT} range from [Table 2](#).
4. The LX4 device, all devices in the TQG144 and CPG196 packages, and the -3N speed grade do not support a Memory Controller Block.

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVTTL, QUIETIO, 2 mA	1.35	1.47	1.60	1.82	5.39	5.53	5.73	6.37	5.39	5.53	5.73	6.37	ns
LVTTL, QUIETIO, 4 mA	1.35	1.47	1.60	1.82	4.29	4.43	4.63	5.22	4.29	4.43	4.63	5.22	ns
LVTTL, QUIETIO, 6 mA	1.35	1.47	1.60	1.82	3.75	3.89	4.09	4.69	3.75	3.89	4.09	4.69	ns
LVTTL, QUIETIO, 8 mA	1.35	1.47	1.60	1.82	3.23	3.37	3.57	4.20	3.23	3.37	3.57	4.20	ns
LVTTL, QUIETIO, 12 mA	1.35	1.47	1.60	1.82	3.28	3.42	3.62	4.22	3.28	3.42	3.62	4.22	ns
LVTTL, QUIETIO, 16 mA	1.35	1.47	1.60	1.82	2.94	3.08	3.28	3.92	2.94	3.08	3.28	3.92	ns
LVTTL, QUIETIO, 24 mA	1.35	1.47	1.60	1.82	2.69	2.83	3.03	3.67	2.69	2.83	3.03	3.67	ns
LVTTL, Slow, 2 mA	1.35	1.47	1.60	1.82	4.36	4.50	4.70	5.30	4.36	4.50	4.70	5.30	ns
LVTTL, Slow, 4 mA	1.35	1.47	1.60	1.82	3.17	3.31	3.51	4.16	3.17	3.31	3.51	4.16	ns
LVTTL, Slow, 6 mA	1.35	1.47	1.60	1.82	2.76	2.90	3.10	3.75	2.76	2.90	3.10	3.75	ns
LVTTL, Slow, 8 mA	1.35	1.47	1.60	1.82	2.59	2.73	2.93	3.55	2.59	2.73	2.93	3.55	ns
LVTTL, Slow, 12 mA	1.35	1.47	1.60	1.82	2.58	2.72	2.92	3.54	2.58	2.72	2.92	3.54	ns
LVTTL, Slow, 16 mA	1.35	1.47	1.60	1.82	2.39	2.53	2.73	3.40	2.39	2.53	2.73	3.40	ns
LVTTL, Slow, 24 mA	1.35	1.47	1.60	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVTTL, Fast, 2 mA	1.35	1.47	1.60	1.82	3.78	3.92	4.12	4.74	3.78	3.92	4.12	4.74	ns
LVTTL, Fast, 4 mA	1.35	1.47	1.60	1.82	2.49	2.63	2.83	3.45	2.49	2.63	2.83	3.45	ns
LVTTL, Fast, 6 mA	1.35	1.47	1.60	1.82	2.44	2.58	2.78	3.40	2.44	2.58	2.78	3.40	ns
LVTTL, Fast, 8 mA	1.35	1.47	1.60	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns
LVTTL, Fast, 12 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTL, Fast, 16 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTL, Fast, 24 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVC MOS33, QUIETIO, 2 mA	1.34	1.46	1.59	1.82	5.40	5.54	5.74	6.37	5.40	5.54	5.74	6.37	ns
LVC MOS33, QUIETIO, 4 mA	1.34	1.46	1.59	1.82	4.03	4.17	4.37	5.01	4.03	4.17	4.37	5.01	ns
LVC MOS33, QUIETIO, 6 mA	1.34	1.46	1.59	1.82	3.51	3.65	3.85	4.47	3.51	3.65	3.85	4.47	ns
LVC MOS33, QUIETIO, 8 mA	1.34	1.46	1.59	1.82	3.37	3.51	3.71	4.33	3.37	3.51	3.71	4.33	ns
LVC MOS33, QUIETIO, 12 mA	1.34	1.46	1.59	1.82	2.94	3.08	3.28	3.93	2.94	3.08	3.28	3.93	ns
LVC MOS33, QUIETIO, 16 mA	1.34	1.46	1.59	1.82	2.77	2.91	3.11	3.78	2.77	2.91	3.11	3.78	ns
LVC MOS33, QUIETIO, 24 mA	1.34	1.46	1.59	1.82	2.59	2.73	2.93	3.58	2.59	2.73	2.93	3.58	ns
LVC MOS33, Slow, 2 mA	1.34	1.46	1.59	1.82	4.37	4.51	4.71	5.28	4.37	4.51	4.71	5.28	ns
LVC MOS33, Slow, 4 mA	1.34	1.46	1.59	1.82	2.98	3.12	3.32	3.94	2.98	3.12	3.32	3.94	ns
LVC MOS33, Slow, 6 mA	1.34	1.46	1.59	1.82	2.58	2.72	2.92	3.61	2.58	2.72	2.92	3.61	ns
LVC MOS33, Slow, 8 mA	1.34	1.46	1.59	1.82	2.65	2.79	2.99	3.61	2.65	2.79	2.99	3.61	ns
LVC MOS33, Slow, 12 mA	1.34	1.46	1.59	1.82	2.39	2.53	2.73	3.31	2.39	2.53	2.73	3.31	ns
LVC MOS33, Slow, 16 mA	1.34	1.46	1.59	1.82	2.31	2.45	2.65	3.27	2.31	2.45	2.65	3.27	ns
LVC MOS33, Slow, 24 mA	1.34	1.46	1.59	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVC MOS33, Fast, 2 mA	1.34	1.46	1.59	1.82	3.76	3.90	4.10	4.70	3.76	3.90	4.10	4.70	ns
LVC MOS33, Fast, 4 mA	1.34	1.46	1.59	1.82	2.48	2.62	2.82	3.44	2.48	2.62	2.82	3.44	ns
LVC MOS33, Fast, 6 mA	1.34	1.46	1.59	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVC MOS12, Fast, 2 mA	0.91	1.03	1.16	1.51	3.46	3.60	3.80	4.44	3.46	3.60	3.80	4.44	ns
LVC MOS12, Fast, 4 mA	0.91	1.03	1.16	1.51	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVC MOS12, Fast, 6 mA	0.91	1.03	1.16	1.51	1.79	1.93	2.13	2.75	1.79	1.93	2.13	2.75	ns
LVC MOS12, Fast, 8 mA	0.91	1.03	1.16	1.51	1.68	1.82	2.02	2.64	1.68	1.82	2.02	2.64	ns
LVC MOS12, Fast, 12 mA	0.91	1.03	1.16	1.51	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
LVC MOS12_JEDEC, QUIETIO, 2 mA	1.50	1.62	1.75	1.88	6.39	6.53	6.73	7.31	6.39	6.53	6.73	7.31	ns
LVC MOS12_JEDEC, QUIETIO, 4 mA	1.50	1.62	1.75	1.88	4.98	5.12	5.32	5.88	4.98	5.12	5.32	5.88	ns
LVC MOS12_JEDEC, QUIETIO, 6 mA	1.50	1.62	1.75	1.88	4.67	4.81	5.01	5.54	4.67	4.81	5.01	5.54	ns
LVC MOS12_JEDEC, QUIETIO, 8 mA	1.50	1.62	1.75	1.88	4.23	4.37	4.57	5.22	4.23	4.37	4.57	5.22	ns
LVC MOS12_JEDEC, QUIETIO, 12 mA	1.50	1.62	1.75	1.88	3.99	4.13	4.33	4.94	3.99	4.13	4.33	4.94	ns
LVC MOS12_JEDEC, Slow, 2 mA	1.50	1.62	1.75	1.88	5.00	5.14	5.34	5.90	5.00	5.14	5.34	5.90	ns
LVC MOS12_JEDEC, Slow, 4 mA	1.50	1.62	1.75	1.88	2.85	2.99	3.19	3.80	2.85	2.99	3.19	3.80	ns
LVC MOS12_JEDEC, Slow, 6 mA	1.50	1.62	1.75	1.88	2.76	2.90	3.10	3.72	2.76	2.90	3.10	3.72	ns
LVC MOS12_JEDEC, Slow, 8 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVC MOS12_JEDEC, Slow, 12 mA	1.50	1.62	1.75	1.88	2.09	2.23	2.43	3.05	2.09	2.23	2.43	3.05	ns
LVC MOS12_JEDEC, Fast, 2 mA	1.50	1.62	1.75	1.88	3.46	3.60	3.80	4.42	3.46	3.60	3.80	4.42	ns
LVC MOS12_JEDEC, Fast, 4 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns
LVC MOS12_JEDEC, Fast, 6 mA	1.50	1.62	1.75	1.88	1.79	1.93	2.13	2.76	1.79	1.93	2.13	2.76	ns
LVC MOS12_JEDEC, Fast, 8 mA	1.50	1.62	1.75	1.88	1.69	1.83	2.03	2.65	1.69	1.83	2.03	2.65	ns
LVC MOS12_JEDEC, Fast, 12 mA	1.50	1.62	1.75	1.88	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns

Notes:

1. The -1L values listed in this table are also applicable to the Spartan-6Q devices.
2. Devices with a -1L speed grade do not support Xilinx PCI IP.

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
DIFF_SSTL3_I	1.26	1.44	1.95	2.15	1.95	2.15	ns
DIFF_SSTL3_II	1.26	1.44	1.94	2.14	1.94	2.14	ns
DIFF_SSTL2_I	1.09	1.27	1.94	2.14	1.94	2.14	ns
DIFF_SSTL2_II	1.09	1.27	1.90	2.10	1.90	2.10	ns
DIFF_SSTL18_I	1.04	1.22	1.86	2.06	1.86	2.06	ns
DIFF_SSTL18_II	1.05	1.23	1.82	2.02	1.82	2.02	ns
DIFF_SSTL15_II	1.01	1.19	1.81	2.01	1.81	2.01	ns
DIFF_MOBILE_DDR	1.04	1.22	1.89	2.09	1.89	2.09	ns
LVTTL, QUIETIO, 2 mA	1.42	1.60	5.64	5.84	5.64	5.84	ns
LVTTL, QUIETIO, 4 mA	1.42	1.60	4.46	4.66	4.46	4.66	ns
LVTTL, QUIETIO, 6 mA	1.42	1.60	3.92	4.12	3.92	4.12	ns
LVTTL, QUIETIO, 8 mA	1.42	1.60	3.37	3.57	3.37	3.57	ns
LVTTL, QUIETIO, 12 mA	1.42	1.60	3.42	3.62	3.42	3.62	ns
LVTTL, QUIETIO, 16 mA	1.42	1.60	3.09	3.29	3.09	3.29	ns
LVTTL, QUIETIO, 24 mA	1.42	1.60	2.83	3.03	2.83	3.03	ns
LVTTL, Slow, 2 mA	1.42	1.60	4.58	4.78	4.58	4.78	ns
LVTTL, Slow, 4 mA	1.42	1.60	3.38	3.58	3.38	3.58	ns
LVTTL, Slow, 6 mA	1.42	1.60	2.95	3.15	2.95	3.15	ns
LVTTL, Slow, 8 mA	1.42	1.60	2.73	2.93	2.73	2.93	ns
LVTTL, Slow, 12 mA	1.42	1.60	2.72	2.92	2.72	2.92	ns
LVTTL, Slow, 16 mA	1.42	1.60	2.53	2.73	2.53	2.73	ns
LVTTL, Slow, 24 mA	1.42	1.60	2.42	2.62	2.42	2.62	ns
LVTTL, Fast, 2 mA	1.42	1.60	4.04	4.24	4.04	4.24	ns
LVTTL, Fast, 4 mA	1.42	1.60	2.66	2.86	2.66	2.86	ns
LVTTL, Fast, 6 mA	1.42	1.60	2.58	2.78	2.58	2.78	ns
LVTTL, Fast, 8 mA	1.42	1.60	2.46	2.66	2.46	2.66	ns
LVTTL, Fast, 12 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns
LVTTL, Fast, 16 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns
LVTTL, Fast, 24 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns
LVC MOS33, QUIETIO, 2 mA	1.41	1.59	5.65	5.85	5.65	5.85	ns
LVC MOS33, QUIETIO, 4 mA	1.41	1.59	4.20	4.40	4.20	4.40	ns
LVC MOS33, QUIETIO, 6 mA	1.41	1.59	3.65	3.85	3.65	3.85	ns
LVC MOS33, QUIETIO, 8 mA	1.41	1.59	3.51	3.71	3.51	3.71	ns
LVC MOS33, QUIETIO, 12 mA	1.41	1.59	3.09	3.29	3.09	3.29	ns
LVC MOS33, QUIETIO, 16 mA	1.41	1.59	2.91	3.11	2.91	3.11	ns
LVC MOS33, QUIETIO, 24 mA	1.41	1.59	2.73	2.93	2.73	2.93	ns
LVC MOS33, Slow, 2 mA	1.41	1.59	4.59	4.79	4.59	4.79	ns
LVC MOS33, Slow, 4 mA	1.41	1.59	3.14	3.34	3.14	3.34	ns

I/O Standard Measurement Methodology

Input Delay Measurements

Table 31 shows the test setup parameters used for measuring input delay.

Table 31: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)}$	$V_H^{(1)}$	$V_{MEAS}^{(3)(4)}$	$V_{REF}^{(2)(4)}$
LVTTTL (Low-Voltage Transistor-Transistor Logic)	LVTTTL	0	3.0	1.4	—
LVC MOS (Low-Voltage CMOS), 3.3V	LVC MOS33	0	3.3	1.65	—
LVC MOS, 2.5V	LVC MOS25	0	2.5	1.25	—
LVC MOS, 1.8V	LVC MOS18	0	1.8	0.9	—
LVC MOS, 1.5V	LVC MOS15	0	1.5	0.75	—
LVC MOS, 1.2V	LVC MOS12	0	1.2	0.6	—
PCI (Peripheral Component Interface), 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3	Per PCI Specification			—
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III	HSTL_III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	1.1
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
SSTL, Class II, 1.5V	SSTL15_II	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	$1.25 - 0.125$	$1.25 + 0.125$	0 ⁽⁵⁾	—
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V & 3.3V	LVPECL_25, LVPECL_33	$1.2 - 0.3$	$1.2 + 0.3$	0 ⁽⁵⁾	—
BLVDS (Bus LVDS), 2.5V	BLVDS_25	$1.3 - 0.125$	$1.3 + 0.125$	0 ⁽⁵⁾	—
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	$1.2 - 0.125$	$1.2 + 0.125$	0 ⁽⁵⁾	—
RS DS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RS DS_25, RS DS_33	$1.2 - 0.1$	$1.2 + 0.1$	0 ⁽⁵⁾	—
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	$3.0 - 0.1$	$3.0 + 0.1$	0 ⁽⁵⁾	—
PPDS (Point-to-Point Differential Signaling), 2.5V & 3.3V	PPDS_25, PPDS_33	$1.25 - 0.1$	$1.25 + 0.1$	0 ⁽⁵⁾	—

Notes:

1. Input waveform switches between V_L and V_H .
2. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 4.
5. The value given is the differential input voltage.

Input Serializer/Deserializer Switching Characteristics

Table 37: ISERDES2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold for Control Lines						
T _{ISCKC_BITSIP} / T _{ISCKC_BITSIP}	BITSIP pin Setup/Hold with respect to CLKDIV	0.16/ −0.09	0.20/ −0.09	0.31/ −0.09	0.34/ −0.14	ns
T _{ISCKC_CE} / T _{ISCKC_CE}	CE pin Setup/Hold with respect to CLK	0.71/ −0.47	0.71/ −0.42	0.97/ −0.42	1.39/ −0.71	ns
Setup/Hold for Data Lines						
T _{ISDCK_D} / T _{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.24/ −0.15	0.25/ −0.05	0.29/ −0.05	0.09/ −0.05	ns
T _{ISDCK_DDLY} / T _{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	−0.25/ 0.30	−0.25/ 0.42	−0.25/ 0.56	−0.54/ 0.67	ns
T _{ISDCK_D_DDR} / T _{ISCKD_D_DDR}	D pin Setup/Hold with respect to CLK at DDR mode	−0.03/ 0.04	−0.03/ 0.16	−0.03/ 0.18	−0.05/ 0.12	ns
T _{ISDCK_DDLY_DDR} / T _{ISCKD_DDLY_DDR}	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY2)	−0.40/ 0.48	−0.40/ 0.53	−0.40/ 0.71	−0.71/ 0.86	ns
Sequential Delays						
T _{ISCKO_Q}	CLKDIV to out at Q pin	1.30	1.44	2.02	2.22	ns
F _{CLKDIV}	CLKDIV maximum frequency	270	262.5	250	125	MHz

Output Serializer/Deserializer Switching Characteristics

Table 38: OSERDES2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T _{OSDCK_D} /T _{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	−0.03/ 1.02	−0.03/ 1.17	−0.03/ 1.27	−0.02/ 0.23	ns
T _{OSDCK_T} /T _{OSCKD_T} ⁽¹⁾	T input Setup/Hold with respect to CLK	−0.05/ 1.03	−0.05/ 1.13	−0.05/ 1.23	−0.05/ 0.24	ns
T _{OSCK_OCE} /T _{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.12/ −0.03	0.15/ −0.03	0.24/ −0.03	0.28/ −0.17	ns
T _{OSCK_TCE} /T _{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.14/ −0.08	0.17/ −0.08	0.27/ −0.08	0.31/ −0.16	ns
Sequential Delays						
T _{OSCKO_OQ}	Clock to out from CLK to OQ	0.94	1.11	1.51	1.89	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ	0.94	1.11	1.51	1.91	ns
F _{CLKDIV}	CLKDIV maximum frequency	270	262.5	250	125	MHz

Notes:

- $T_{OSDCK_T2} / T_{OSCKD_T2}$ (T input setup/hold with respect to CLKDIV) are reported as $T_{OSDCK_T} / T_{OSCKD_T}$ in TRACE report.

CLB Switching Characteristics (SLICEM Only)

Table 40: CLB Switching Characteristics (SLICEM Only)

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT inputs to A to D outputs	0.21	0.26	0.26	0.46	ns, Max
	An – Dn LUT inputs through F7AMUX/F7BMUX to AMUX/CMUX output	0.37	0.43	0.43	0.77	ns, Max
T _{OPAB}	An – Dn LUT inputs through F7AMUX or F7BMUX and F8MUX to BMUX output	0.37	0.46	0.46	0.84	ns, Max
T _{ITO}	An – Dn LUT inputs through latch to AQ – DQ outputs	0.82	0.95	0.95	1.64	ns, Max
T _{TITO_LOGIC}	An – Dn LUT inputs to AQ – DQ outputs (latch as logic)	0.82	0.95	0.95	1.64	ns, Max
T _{OPCYA}	An LUT inputs to COUT output	0.38	0.48	0.48	0.69	ns, Max
T _{OPCYB}	Bn LUT inputs to COUT output	0.38	0.49	0.49	0.71	ns, Max
T _{OPCYC}	Cn LUT inputs to COUT output	0.28	0.33	0.33	0.55	ns, Max
T _{OPCYD}	Dn LUT inputs to COUT output	0.28	0.35	0.35	0.52	ns, Max
T _{AXCY}	AX input to COUT output	0.21	0.26	0.26	0.36	ns, Max
T _{BXCy}	BX input to COUT output	0.13	0.16	0.16	0.18	ns, Max
T _{CXCy}	CX input to COUT output	0.10	0.12	0.12	0.09	ns, Max
T _{DXCy}	DX input to COUT output	0.09	0.11	0.11	0.09	ns, Max
T _{BYP}	CIN input to COUT output	0.08	0.10	0.10	0.06	ns, Max
T _{CINA}	CIN input to AMUX output	0.21	0.22	0.22	0.47	ns, Max
T _{CINB}	CIN input to BMUX output	0.30	0.31	0.31	0.57	ns, Max
T _{CINC}	CIN input to CMUX output	0.29	0.31	0.31	0.58	ns, Max
T _{CIND}	CIN input to DMUX output	0.31	0.32	0.32	0.68	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.45	0.53	0.53	0.74	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{DICK} /T _{CKDI}	AX – DX input to CLK on A – D flip-flops	0.42/ 0.28	0.47/ 0.39	0.47/ 0.39	0.90/ 0.56	ns, Min
T _{CECK} /T _{CKCE}	CE input to CLK on A – D flip-flops	0.31/ –0.07	0.37/ –0.07	0.37/ –0.07	0.59/ –0.27	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D flip-flops for XC devices	0.41/ 0.02	0.42/ 0.02	0.42/ 0.02	0.68/ –0.29	ns, Min
	SR input to CLK on A – D flip-flops for XA and XQ devices	0.41/ 0.02	N/A	0.44/ 0.02	0.68/ –0.29	ns, Min
T _{CINCK} /T _{CKCIN}	CIN input to CLK on A – D flip-flops	0.31/ –0.17	0.31/ –0.13	0.31/ –0.13	0.81/ –0.42	ns, Min
Set/Reset						
T _{RPW}	SR input minimum pulse width	0.41	0.48	0.48	1.37	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.60	0.70	0.70	0.88	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.60	0.65	0.65	0.90	ns, Max
F _{TOG}	Toggle frequency (for export control)	862	806	667	500	MHz

Block RAM Switching Characteristics

Table 43: Block RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Block RAM Clock to Out Delays						
T _{RCKO_DO}	Clock CLK to DOUT output (without output register) ⁽¹⁾	1.85	2.10	2.10	3.50	ns, Max
T _{RCKO_DO_REG}	Clock CLK to DOUT output (with output register) ⁽²⁾	1.60	1.75	1.75	2.30	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{RCCK_ADDR} /T _{RCKC_ADDR}	ADDR inputs for XC devices ⁽³⁾	0.35/ 0.10	0.40/ 0.12	0.40/ 0.12	0.50/ 0.15	ns, Min
	ADDR inputs for XA and XQ devices ⁽³⁾	0.35/ 0.17	N/A	0.40/ 0.17	0.50/ 0.15	ns, Min
T _{RDCK_DI} /T _{RCKD_DI}	DIN inputs ⁽⁴⁾	0.30/ 0.10	0.30/ 0.10	0.30/ 0.10	0.40/ 0.15	ns, Min
T _{RCCK_EN} /T _{RCKC_EN}	Block RAM Enable (EN) input	0.22/ 0.05	0.25/ 0.06	0.25/ 0.06	0.44/ 0.10	ns, Min
T _{RCCK_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.20/ 0.10	0.20/ 0.10	0.20/ 0.10	0.28/ 0.15	ns, Min
T _{RCCK_WE} /T _{RCKC_WE}	Write Enable (WE) input	0.25/ 0.10	0.33/ 0.10	0.33/ 0.10	0.28/ 0.15	ns, Min
Maximum Frequency						
F _{MAX}	Block RAM in all modes	320	280	280	150	MHz

Notes:

1. T_{RCKO_DO} includes T_{RCKO_DOA} and T_{RCKO_DOPA} as well as the B port equivalent timing parameters.
2. $T_{RCKO_DO_REG}$ includes $T_{RCKO_DOA_REG}$ and $T_{RCKO_DOPA_REG}$ as well as the B port equivalent timing parameters.
3. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
4. T_{RDCK_DI} includes both A and B inputs as well as the parity inputs of A and B.

Table 45: Device DNA Interface Port Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T _{DNASSU}	Setup time on SHIFT before the rising edge of CLK	7				ns, Min
T _{DNASH}	Hold time on SHIFT after the rising edge of CLK	1				ns, Min
T _{DNADSU}	Setup time on DIN before the rising edge of CLK	7				ns, Min
T _{DNADH}	Hold time on DIN after the rising edge of CLK	1				ns, Min
T _{DNARSU}	Setup time on READ before the rising edge of CLK	7				ns, Min
		1,000				ns, Max
T _{DNARH}	Hold time on READ after the rising edge of CLK	1				ns, Min
T _{DNADCKO}	Clock-to-output delay on DOUT after rising edge of CLK	0.5				ns, Min
		6				ns, Max
T _{DNACKF} ⁽²⁾	CLK frequency	2				MHz, Max
T _{DNACKL}	CLK Low time	50				ns, Min
T _{DNACKH}	CLK High time	50				ns, Min

Notes:

1. The minimum READ pulse width is 8 ns, the maximum READ pulse width is 1 μ s.
2. Also applies to TCK when reading DNA through the boundary-scan port.

Table 46: Suspend Mode Switching Characteristics

Symbol	Description	Min	Max	Units
Entering Suspend Mode				
T _{SUSPENDHIGH_AWAKE}	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter	2.5	14	ns
T _{SUSPENDFILTER}	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled	31	430	ns
T _{SUSPEND_GWE}	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior (without glitch filter)	–	15	ns
T _{SUSPEND_GTS}	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements (without glitch filter)	–	15	ns
T _{SUSPEND_DISABLE}	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled (without glitch filter)	–	1500	ns
Exiting Suspend Mode				
T _{SUSPENDLOW_AWAKE}	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM or PLL lock time.	7	75	μ s
T _{SUSPEND_ENABLE}	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	7	41	μ s
T _{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using sw_clk:InternalClock and sw_gwe_cycle:1 .	–	80	ns
T _{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using sw_clk:InternalClock and sw_gwe_cycle:512 .	–	20.5	μ s
T _{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using sw_clk:InternalClock and sw_gts_cycle:1 .	–	80	ns
T _{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using sw_clk:InternalClock and sw_gts_cycle:512 .	–	20.5	μ s
T _{SCP_AWAKE}	Rising edge of SCP pins to rising edge of AWAKE pin	7	75	μ s

Configuration Switching Characteristics

Table 47: Configuration Switching Characteristics⁽¹⁾

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Power-up Timing Characteristics						
T _{PL} ⁽²⁾	PROGRAM_B Latency	4	4	4	5	ms, Max
T _{POR} ⁽²⁾	Power-on reset (50 ms ramp time) ⁽³⁾	5/30	5/34	5/40	5/40	ms, Min/Max
	Power-on reset (10 ms ramp time)	5/25	5/29	5/35	5/40	ms, Min/Max
T _{PROGRAM}	PROGRAM_B Pulse Width	500	500	500	500	ns, Min
Slave Serial Mode Programming Switching						
T _{DCCK} /T _{CCKD}	DIN Setup/Hold, slave mode	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T _{CCO}	CCLK to DOUT	12	12	12	17	ns, Max
F _{SCCK}	Slave mode external CCLK	80	80	80	50	MHz, Max
Slave SelectMAP Mode Programming Switching						
T _{SMDCK} /T _{SMCCKD}	SelectMAP Data Setup/Hold	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T _{SMCSCCK} /T _{SMCCKCS}	CSI_B Setup/Hold	7.0/0.0	7.0/0.0	7.0/0.0	9.0/2.0	ns, Min
T _{SMWCCK} /T _{SMCKKW}	RDWR_B Setup/Hold	17.0/1.0	17.0/1.0	17.0/1.0	27.0/2.0	ns, Min
T _{SMCKCSO}	CSO_B clock to out	16	16	16	26	ns, Max
T _{SMCO}	CCLK to DATA out in readback	13	13	13	25	ns, Max
T _{SMCKBY}	CCLK to BUSY out in readback	12	12	12	17	ns, Max
F _{SMCK}	Maximum CCLK frequency (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	25	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x8 mode, LX150, and LX150T only)	40	40	40	20	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x16 mode only)	35	35	35	20	MHz, Max
F _{RBCK}	Maximum Readback CCLK frequency, including block RAM (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	20	20	20	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	30	MHz, Max
	Maximum Readback CCLK frequency, including block RAM (LX100, LX100T, LX150, and LX150T only)	12	12	12	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX100, LX100T, LX150, and LX150T only)	35	35	35	20	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK}	TMS and TDI Setup time before TCK	10	10	10	17	ns, Min
T _{TCKTAP}	TMS and TDI Hold time after TCK	5.5	5.5	5.5	5.5	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output valid	6.5	6.5	6.5	8	ns, Max
T _{TCKH}	TCK clock minimum High time	12	12	12	21	ns, Min
T _{TCKL}	TCK clock minimum Low time	12	12	12	21	ns, Min
F _{TCK}	Maximum configuration TCK clock frequency	33	33	33	18	MHz, Max
F _{TCKB}	Maximum boundary-scan TCK clock frequency	33	33	33	18	MHz, Max
F _{TCKAES}	Maximum AES key TCK clock frequency	2	2	2	2	MHz, Max

DCM Switching Characteristics

Table 53: Operating Frequency Ranges and Conditions for the Delay-Locked Loop (DLL)⁽¹⁾

Symbol	Description	Speed Grade								Units	
		-3		-3N		-2		-1L			
		Min	Max	Min	Max	Min	Max	Min	Max		
Input Frequency Ranges											
CLKIN_FREQ_DLL	Frequency of the CLKIN clock input when the CLKDV output is not used.	5 ⁽²⁾	280 ⁽³⁾	5 ⁽²⁾	280 ⁽³⁾	5 ⁽²⁾	250 ⁽³⁾	5 ⁽²⁾	175 ⁽³⁾	MHz	
	Frequency of the CLKIN clock input when using the CLKDV output.	5 ⁽²⁾	280 ⁽³⁾	5 ⁽²⁾	280 ⁽³⁾	5 ⁽²⁾	250 ⁽³⁾	5 ⁽²⁾	133 ⁽³⁾	MHz	
Input Pulse Requirements											
CLKIN_PULSE	CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL < 150 MHz	40	60	40	60	40	60	40	60	%	
	CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL > 150 MHz	45	55	45	55	45	55	45	55	%	
Input Clock Jitter Tolerance and Delay Path Variation ⁽⁴⁾											
CLKIN_CYC_JITT_DLL_LF	Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL < 150 MHz	–	±300	–	±300	–	±300	–	±300	ps	
CLKIN_CYC_JITT_DLL_HF	Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL > 150 MHz.	–	±150	–	±150	–	±150	–	±150	ps	
CLKIN_PER_JITT_DLL	Period jitter at the CLKIN input.	–	±1	–	±1	–	±1	–	±1	ns	
CLKFB_DELAY_VAR_EXT	Allowable variation of the off-chip feedback delay from the DCM output to the CLKFB input.	–	±1	–	±1	–	±1	–	±1	ns	

Notes:

- DLL specifications apply when using any of the DLL outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV.
- When operating independently of the DLL, the DFS supports lower CLKIN_FREQ_DLL frequencies. See Table 55.
- The CLKIN_DIVIDE_BY_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the F_{MAX} (see Table 48 and Table 49 for BUFG and BUFGIO2 limits). When used with CLK_FEEDBACK=2X, the input clock frequency matches the frequency for CLK2X, and is limited to CLKOUT_FREQ_2X.
- CLKIN_FREQ_DLL input jitter beyond these limits can cause the DCM to lose LOCK, indicated by the LOCKED output deasserting. The user must then reset the DCM.
- When using both DCMs in a CMT, both DCMs must be LOCKED.

Table 57: Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)⁽¹⁾

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges (DCM_CLKGEN)										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz
CLKOUT_FREQ_FXDV	Frequency for the CLKFXDV output	0.15625	187.5	0.15625	187.5	0.15625	166.5	0.15625	100	MHz
Output Clock Jitter ⁽²⁾⁽³⁾										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKOUT_PER_JITT_FXDV	Period jitter at the CLKFXDV output.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKFX_FREEZE_VAR	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX > 50 MHz	Maximum = ±3% of CLKFX period								ps
	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX < 50 MHz	Maximum = ±5% of CLKFX period								ps
CLKFX_FREEZE_TEMP_SLOPE	CLKFX period will change in free_oscillator mode over temperature. Add to CLKFX_FREEZE_VAR to determine total CLKFX period change. Percentage change for CLKFX period over 1°C.	Maximum = 0.1								%/°C
Duty Cycle ⁽⁴⁾⁽⁵⁾										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
CLKOUT_DUTY_CYCLE_FXDV	Duty cycle precision for the CLKFXDV outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
Lock Time										
LOCK_FX ⁽²⁾	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX, CLKFX180, and CLKFXDV signals are valid. Lock time requires CLKFX_DIVIDE < F _{IN} /(0.50 MHz) when: F _{CLKIN} < 50 MHz	—	50	—	50	—	50	—	50	ms
	when: F _{CLKIN} > 50 MHz	—	5	—	5	—	5	—	5	ms

Table 67: Global Clock Input to Output Delay With PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> PLL in Source-Synchronous Mode.							
T _{ICKOFFLL_0}	Global Clock and OUTFF <i>with</i> PLL	XC6SLX4	5.49	N/A	7.44	8.55	ns
		XC6SLX9	5.49	6.29	7.44	8.55	ns
		XC6SLX16	5.23	5.77	6.79	8.21	ns
		XC6SLX25	5.00	5.35	6.10	8.54	ns
		XC6SLX25T	5.00	5.35	6.10	N/A	ns
		XC6SLX45	5.59	6.03	7.02	8.39	ns
		XC6SLX45T	5.59	6.03	7.02	N/A	ns
		XC6SLX75	4.96	5.41	6.22	8.32	ns
		XC6SLX75T	4.96	5.41	6.22	N/A	ns
		XC6SLX100	4.97	5.42	6.21	9.08	ns
		XC6SLX100T	5.01	5.42	6.21	N/A	ns
		XC6SLX150	4.59	5.06	5.86	8.13	ns
		XC6SLX150T	4.59	5.06	5.86	N/A	ns
		XA6SLX4	5.79	N/A	7.32	N/A	ns
		XA6SLX9	5.79	N/A	7.32	N/A	ns
		XA6SLX16	5.56	N/A	6.66	N/A	ns
		XA6SLX25	5.40	N/A	5.97	N/A	ns
		XA6SLX25T	5.40	N/A	6.07	N/A	ns
		XA6SLX45	5.89	N/A	6.90	N/A	ns
		XA6SLX45T	5.89	N/A	6.90	N/A	ns
		XA6SLX75	5.27	N/A	6.12	N/A	ns
		XA6SLX75T	5.27	N/A	6.12	N/A	ns
		XA6SLX100	N/A	N/A	6.80	N/A	ns
		XQ6SLX75	N/A	N/A	6.12	8.32	ns
		XQ6SLX75T	5.27	N/A	6.12	N/A	ns
		XQ6SLX150	N/A	N/A	5.88	8.13	ns
		XQ6SLX150T	5.21	N/A	5.88	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 75: Global Clock Setup and Hold With PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.(1)							
T _{PSPLL0} / T _{PHPLL0}	No Delay Global Clock and IFF(2) with PLL in Source-Synchronous Mode	XC6SLX4	0.47/1.08	N/A	0.47/1.60	1.15/1.68	ns
		XC6SLX9	0.47/1.08	0.47/1.35	0.47/1.60	1.15/1.68	ns
		XC6SLX16	0.37/0.75	0.37/0.82	0.51/0.94	0.57/1.31	ns
		XC6SLX25	0.69/1.06	0.69/1.06	0.69/1.06	1.86/1.67	ns
		XC6SLX25T	0.69/1.06	0.69/1.06	0.69/1.06	N/A	ns
		XC6SLX45	0.57/1.05	0.65/1.10	0.65/1.18	1.02/1.65	ns
		XC6SLX45T	0.57/1.06	0.65/1.10	0.65/1.18	N/A	ns
		XC6SLX75	0.86/1.04	0.87/1.04	0.90/1.04	1.34/1.55	ns
		XC6SLX75T	0.86/1.04	0.87/1.04	0.90/1.04	N/A	ns
		XC6SLX100	0.53/1.13	0.54/1.13	0.55/1.13	0.89/2.39	ns
		XC6SLX100T	0.53/1.13	0.54/1.13	0.55/1.13	N/A	ns
		XC6SLX150	0.50/1.31	0.51/1.31	0.52/1.31	1.02/1.72	ns
		XC6SLX150T	0.50/1.31	0.51/1.31	0.52/1.31	N/A	ns
		XA6SLX4	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX9	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX16	0.92/0.69	N/A	0.63/0.82	N/A	ns
		XA6SLX25	0.99/0.94	N/A	0.96/0.94	N/A	ns
		XA6SLX25T	0.99/0.94	N/A	1.04/0.94	N/A	ns
		XA6SLX45	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX45T	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX75	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX100	N/A	N/A	1.25/0.96	N/A	ns
		XQ6SLX75	N/A	N/A	1.02/0.89	1.34/1.55	ns
		XQ6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XQ6SLX150	N/A	N/A	0.63/1.19	1.02/1.72	ns
		XQ6SLX150T	0.60/1.19	N/A	0.63/1.19	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 76: Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾							
T _{PSDCMPLL} / T _{PHDCMPLL}	No Delay Global Clock and IFF ⁽²⁾ with DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.	XC6SLX4	1.16/0.49	N/A	1.39/0.49	2.36/0.59	ns
		XC6SLX9	1.16/0.44	1.37/0.44	1.39/0.44	2.36/0.59	ns
		XC6SLX16	1.44/−0.08	1.49/−0.04	1.62/−0.04	2.06/0.55	ns
		XC6SLX25	1.52/0.42	1.65/0.42	1.83/0.42	2.52/0.43	ns
		XC6SLX25T	1.52/0.42	1.65/0.42	1.83/0.42	N/A	ns
		XC6SLX45	1.54/0.39	1.59/0.39	1.75/0.39	2.48/0.76	ns
		XC6SLX45T	1.54/0.39	1.59/0.39	1.75/0.39	N/A	ns
		XC6SLX75	1.72/0.41	1.80/0.41	1.99/0.41	2.60/0.75	ns
		XC6SLX75T	1.72/0.41	1.80/0.41	1.99/0.41	N/A	ns
		XC6SLX100	1.34/0.51	1.46/0.51	1.64/0.51	2.12/0.90	ns
		XC6SLX100T	1.34/0.51	1.46/0.51	1.64/0.51	N/A	ns
		XC6SLX150	1.30/0.60	1.40/0.60	1.55/0.60	2.57/0.97	ns
		XC6SLX150T	1.30/0.60	1.40/0.60	1.55/0.60	N/A	ns
		XA6SLX4	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX9	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX16	2.67/0.35	N/A	2.67/0.17	N/A	ns
		XA6SLX25	1.74/0.27	N/A	1.95/0.27	N/A	ns
		XA6SLX25T	1.74/0.27	N/A	2.03/0.27	N/A	ns
		XA6SLX45	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX45T	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX75	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX100	N/A	N/A	2.64/0.82	N/A	ns
		XQ6SLX75	N/A	N/A	2.11/0.24	2.60/0.75	ns
		XQ6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XQ6SLX150	N/A	N/A	1.67/0.70	2.57/0.97	ns
		XQ6SLX150T	1.50/0.70	N/A	1.67/0.70	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 78: Duty Cycle Distortion and Clock-Tree Skew (Cont'd)

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{BUFIOSKEW}	I/O clock tree skew across one clock region	LX4	0.06	N/A	0.06	0.07	ns
		LX9	0.06	0.06	0.06	0.07	ns
		LX16	0.06	0.06	0.06	0.07	ns
		LX25	0.06	0.06	0.06	0.07	ns
		LX25T	0.06	0.06	0.06	N/A	ns
		LX45	0.06	0.06	0.06	0.07	ns
		LX45T	0.06	0.06	0.06	N/A	ns
		LX75	0.06	0.06	0.06	0.07	ns
		LX75T	0.06	0.06	0.06	N/A	ns
		LX100	0.06	0.06	0.06	0.07	ns
		LX100T	0.06	0.06	0.06	N/A	ns
		LX150	0.06	0.06	0.06	0.07	ns
		LX150T	0.06	0.06	0.06	N/A	ns

Notes:

1. LXT devices are not available with a -1L speed grade. The LX4 is not available in -3N speed grade.
2. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
3. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
4. The T_{CKSKEW} is 0.43 ns for the XA6SLX100 device using a -2 speed grade and 0.22 ns for the XC6SLX100 devices using the -2 speed grade.

Table 79: Package Skew

Symbol	Description	Device	Package ⁽²⁾	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	LX4	TQG144	N/A	ps
			CPG196	23	ps
			CSG225	58	ps
		LX9	TQG144	N/A	ps
			CPG196	23	ps
			CSG225	58	ps
			FT(G)256	88	ps
			CSG324	64	ps
		LX16	CPG196	19	ps
			CSG225	70	ps
			FT(G)256	71	ps
			CSG324	54	ps
		LX25	FT(G)256	90	ps
			CSG324	61	ps
			FG(G)484	84	ps
		LX25T	CSG324	48	ps
			FG(G)484	112	ps

Table 81: Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out Using BUFIO2 (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Pin-to-Pin Clock-to-Out Using BUFIO2							
T _{ICKO} FCS	OFF clock-to-out using BUFIO2 clock	XC6SLX4	5.51	N/A	6.95	8.45	ns
		XC6SLX9	5.51	5.89	6.95	8.45	ns
		XC6SLX16	5.31	5.70	6.67	8.21	ns
		XC6SLX25	5.53	6.00	7.02	8.72	ns
		XC6SLX25T	5.53	6.00	7.02	N/A	ns
		XC6SLX45	5.76	6.18	7.22	8.77	ns
		XC6SLX45T	5.76	6.18	7.22	N/A	ns
		XC6SLX75	5.94	6.46	7.57	9.72	ns
		XC6SLX75T	5.94	6.46	7.57	N/A	ns
		XC6SLX100	6.09	6.53	7.60	9.66	ns
		XC6SLX100T	6.09	6.53	7.60	N/A	ns
		XC6SLX150	6.29	6.69	7.81	9.94	ns
		XC6SLX150T	6.29	6.69	7.81	N/A	ns
		XA6SLX4	5.83	N/A	6.95	N/A	ns
		XA6SLX9	5.83	N/A	6.95	N/A	ns
		XA6SLX16	5.65	N/A	6.68	N/A	ns
		XA6SLX25	5.85	N/A	7.03	N/A	ns
		XA6SLX25T	5.85	N/A	7.03	N/A	ns
		XA6SLX45	6.07	N/A	7.25	N/A	ns
		XA6SLX45T	6.07	N/A	7.25	N/A	ns
		XA6SLX75	6.26	N/A	7.57	N/A	ns
		XA6SLX75T	6.26	N/A	7.57	N/A	ns
		XA6SLX100	N/A	N/A	7.48	N/A	ns
		XQ6SLX75	N/A	N/A	7.57	9.72	ns
		XQ6SLX75T	6.26	N/A	7.57	N/A	ns
		XQ6SLX150	N/A	N/A	7.81	9.94	ns
		XQ6SLX150T	6.62	N/A	7.81	N/A	ns