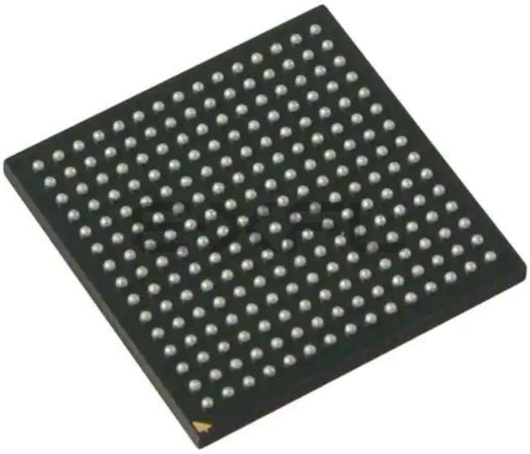
AMD Xilinx - XC6SLX4-L1CSG225I Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	300
Number of Logic Elements/Cells	3840
Total RAM Bits	221184
Number of I/O	132
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	225-LFBGA, CSPBGA
Supplier Device Package	225-CSPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx4-l1csg225i

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Table 1: **Absolute Maximum Ratings(1)** ***(Cont'd)***

Symbol	Description					Units
V_{IN} and V_{TS}(3)	I/O input voltage or voltage applied to 3-state output, relative to GND(4)	All user and dedicated I/Os	Commercial	DC	–0.60 to 4.10	V
				20% overshoot duration	–0.75 to 4.25	V
				8% overshoot duration(5)	–0.75 to 4.40	V
			Industrial	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration(5)	–0.75 to 4.40	V
			Expanded (Q)	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration(5)	–0.75 to 4.40	V
		Restricted to maximum of 100 user I/Os	Commercial	20% overshoot duration	–0.75 to 4.35	V
				15% overshoot duration(5)	–0.75 to 4.40	V
				10% overshoot duration	–0.75 to 4.45	V
			Industrial	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration(5)	–0.75 to 4.40	V
			Expanded (Q)	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration(5)	–0.75 to 4.40	V
T_{STG}	Storage temperature (ambient)				–65 to 150	°C
T_{SOL}	Maximum soldering temperature(6) (TQG144, CPG196, CSG225, CSG324, CSG484, and FTG256)				+260	°C
	Maximum soldering temperature(6) (Pb-free packages: FGG484, FGG676, and FGG900)				+250	°C
	Maximum soldering temperature(6) (Pb packages: CS484, FT256, FG484, FG676, and FG900)				+220	°C
T_j	Maximum junction temperature(6)				+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When programming eFUSE, $V_{FS} \leq V_{CCAUX}$. Requires up to 40 mA current. For read mode, V_{FS} can be between GND and 3.45 V.
3. I/O absolute maximum limit applied to DC and AC signals. Overshoot duration is the percentage of a data period that the I/O is stressed beyond 3.45V.
4. For I/O operation, refer to UG381: *Spartan-6 FPGA SelectIO Resources User Guide*.
5. Maximum percent overshoot duration to meet 4.40V maximum.
6. For soldering guidelines and thermal considerations, see UG385: *Spartan-6 FPGA Packaging and Pinout Specification*.

Table 3: **eFUSE Programming Conditions**(1)

Symbol	Description	Min	Typ	Max	Units
V_{FS}(2)	External voltage supply	3.2	3.3	3.4	V
I_{FS}	V_{FS} supply current	–	–	40	mA
V_{CCAUX}	Auxiliary supply voltage relative to GND	3.2	3.3	3.45	V
R_{FUSE}(3)	External resistor from R_{FUSE} pin to GND	1129	1140	1151	Ω
V_{CCINT}	Internal supply voltage relative to GND	1.14	1.2	1.26	V
t_j	Temperature range	15	–	85	°C

Notes:

1. These specifications apply during programming of the eFUSE AES key. Programming is only supported through JTAG.The AES key is only supported in the following devices: LX75, LX75T, LX100, LX100T, LX150, and LX150T.
2. When programming eFUSE, V_{FS} must be less than or equal to V_{CCAUX}. When not programming or when eFUSE is not used, Xilinx recommends connecting V_{FS} to GND. However, V_{FS} can be between GND and 3.45 V.
3. An R_{FUSE} resistor is required when programming the eFUSE AES key. When not programming or when eFUSE is not used, Xilinx recommends connecting the R_{FUSE} pin to V_{CCAUX} or GND. However, R_{FUSE} can be unconnected.

Table 4: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.8	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin for commercial (C) and industrial (I) devices	–10	–	10	µA
	V_{REF} leakage current per pin for expanded (Q) devices	–15	–	15	µA
I_L	Input or output leakage current per pin (sample-tested) for commercial (C) and industrial (I) devices	–10	–	10	µA
	Input or output leakage current per pin (sample-tested) for expanded (Q) devices	–15	–	15	µA
I_{HS}	Leakage current on pins during hot socketing with FPGA unpowered All pins except PROGRAM_B, DONE, and JTAG pins when HSWAPEN = 1	–20	–	20	µA
	PROGRAM_B, DONE, and JTAG pins, or other pins when HSWAPEN = 0	$I_{HS} + I_{RPU}$			µA
C_{IN}[1]	Die input capacitance at the pad	–	–	10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V or V_{CCAUX} = 3.3V	200	–	500	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V or V_{CCAUX} = 2.5V	120	–	350	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	60	–	200	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	40	–	150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	12	–	100	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = V_{CCO}, V_{CCAUX} = 3.3V	200	–	550	µA
	Pad pull-down (when selected) @ V_{IN} = V_{CCO}, V_{CCAUX} = 2.5V	140	–	400	µA
I_{BATT}[2]	Battery supply current	–	–	150	nA
R_{DT}[3]	Resistance of optional input differential termination circuit, V_{CCAUX} = 3.3V	–	100	–	Ω
R_{IN_TERM}[5]	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for commercial (C) and industrial (I) devices	23	25	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for expanded (Q) devices	20	25	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for commercial (C) and industrial (I) devices	39	50	72	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for expanded (Q) devices	32	50	74	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for commercial (C) and industrial (I) devices	56	75	109	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for expanded (Q) devices	47	75	115	Ω
R_{OUT_TERM}	Thevenin equivalent resistance of programmable output termination (UNTUNED_25)	11	25	52	Ω
	Thevenin equivalent resistance of programmable output termination (UNTUNED_50)	21	50	96	Ω
	Thevenin equivalent resistance of programmable output termination (UNTUNED_75)	29	75	145	Ω

Notes:

1. The C_{IN} measurement represents the die capacitance at the pad, not including the package.
2. Maximum value specified for worst case process at 25°C. LX75, LX75T, LX100, LX100T, LX150, and LX150T only.
3. Refer to IBIS models for R_{DT} variation and for values at V_{CCAUX} = 2.5V. IBIS values for R_{DT} are valid for all temperature ranges.
4. V_{CCO2} is not required for data retention. The minimum V_{CCO2} for power-on reset and configuration is 1.65V.
5. Termination resistance to a $V_{CCO}/2$ level.

In Table 9 and Table 10, values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: **Single-Ended I/O Standard DC Input and Output Levels**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL	–0.5	0.8	2.0	4.1	0.4	2.4	Note 2	Note 2
LVCMOS33	–0.5	0.8	2.0	4.1	0.4	V_{CCO} – 0.4	Note 2	Note 2
LVCMOS25	–0.5	0.7	1.7	4.1	0.4	V_{CCO} – 0.4	Note 2	Note 2
LVCMOS18	–0.5	0.38	0.8	4.1	0.45	V_{CCO} – 0.45	Note 2	Note 2
LVCMOS18 (-1L)	–0.5	0.33	0.71	4.1	0.45	V_{CCO} – 0.45	Note 2	Note 2
LVCMOS18_JEDEC	–0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.45	V_{CCO} – 0.45	Note 2	Note 2
LVCMOS15	–0.5	0.38	0.8	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVCMOS15 (-1L)	–0.5	0.33	0.71	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVCMOS15_JEDEC	–0.5	35% V_{CCO}	65% V_{CCO}	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVCMOS12	–0.5	0.38	0.8	4.1	0.4	V_{CCO} – 0.4	Note 4	Note 4
LVCMOS12 (-1L)	–0.5	0.33	0.71	4.1	0.4	V_{CCO} – 0.4	Note 4	Note 4
LVCMOS12_JEDEC	–0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.4	V_{CCO} – 0.4	Note 4	Note 4
PCI33_3	–0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
PCI66_3	–0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
I2C	–0.5	25% V_{CCO}	70% V_{CCO}	4.1	20% V_{CCO}	–	3	–
SMBUS	–0.5	0.8	2.1	4.1	0.4	–	4	–
SDIO	–0.5	12.5% V_{CCO}	75% V_{CCO}	4.1	12.5% V_{CCO}	75% V_{CCO}	0.1	–0.1
MOBILE_DDR	–0.5	20% V_{CCO}	80% V_{CCO}	4.1	10% V_{CCO}	90% V_{CCO}	0.1	–0.1
HSTL_I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	8	–8
HSTL_II	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	16	–16
HSTL_III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	24	–8
HSTL_I_18	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	11	–11
HSTL_II_18	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	22	–22
HSTL_III_18	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	30	–11
SSTL3_I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	4.1	V_{TT} – 0.6	V_{TT} + 0.6	8	–8
SSTL3_II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	4.1	V_{TT} – 0.8	V_{TT} + 0.8	16	–16
SSTL2_I	–0.5	V_{REF} – 0.15	V_{REF} + 0.15	4.1	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2_II	–0.5	V_{REF} – 0.15	V_{REF} + 0.15	4.1	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL18_I	–0.5	V_{REF} – 0.125	V_{REF} + 0.125	4.1	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18_II	–0.5	V_{REF} – 0.125	V_{REF} + 0.125	4.1	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
SSTL15_II	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	V_{TT} – 0.4	V_{TT} + 0.4	13.4	–13.4

Notes:

1. Tested according to relevant specifications.
2. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
3. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
4. Using drive strengths of 2, 4, 6, 8, or 12 mA.
5. For more information, refer to UG381: *Spartan-6 FPGA SelectIO Resources User Guide*.

eFUSE Read Endurance

Table 11 lists the minimum guaranteed number of read cycle operations for Device DNA and for the AES eFUSE key. For more information, see UG380: *Spartan-6 FPGA Configuration User Guide*.

Table 11: **eFUSE Read Endurance**

Symbol	Description	Speed Grade				Units (Min)
		-3	-3N	-2	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTP Transceiver Specifications

GTP transceivers are available in the Spartan-6 LXT devices. See DS160: *Spartan-6 Family Overview* for more information.

GTP Transceiver DC Characteristics

Table 12: **Absolute Maximum Ratings for GTP Transceivers(1)**

Symbol	Description	MIn	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	–0.5	1.32	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	–0.5	1.32	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	–0.5	1.32	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 13: **Recommended Operating Conditions for GTP Transceivers(1)(2)(3)**

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	1.14	1.20	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in UG386: *Spartan-6 FPGA GTP Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +125°C.
3. The voltage level of MGTAVCCPLL must not exceed the voltage level of MGTAVCC +10mV. The voltage level of MGTAVCC must not exceed the voltage level of MGTAVCCPLL.

GTP Transceiver DC Input and Output Levels

Table 16 summarizes the DC output specifications of the GTP transceivers in Spartan-6 FPGAs. Figure 1 shows the single-ended output voltage swing. Figure 2 shows the peak-to-peak differential output voltage.

Consult UG386: *Spartan-6 FPGA GTP Transceivers User Guide* for further details.

Table 16: **GTP Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled	140	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTTRX = 1.2V	–400	–	MGTAVTTRX	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTTRX = 1.2V	–	3/4 MGTAVTTRX	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	–	–	1000	mV
V_{SEOUT}	Single-ended output voltage swing(1)		–	–	500	mV
$V_{CMOUTDC}$	Common mode output voltage	Equation based	MGTAVTTTX – V_{SEOUT}/2			mV
R_{IN}	Differential input resistance		80	100	130	Ω
R_{OUT}	Differential output resistance		80	100	130	Ω
T_{OSKEW}	Transmitter output skew		–	–	15	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		75	100	200	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG386: *Spartan-6 FPGA GTP Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

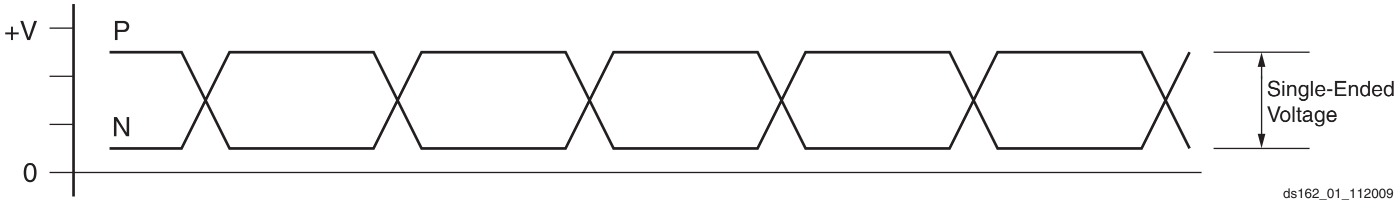

Figure 1: **Single-Ended Peak-to-Peak Voltage**

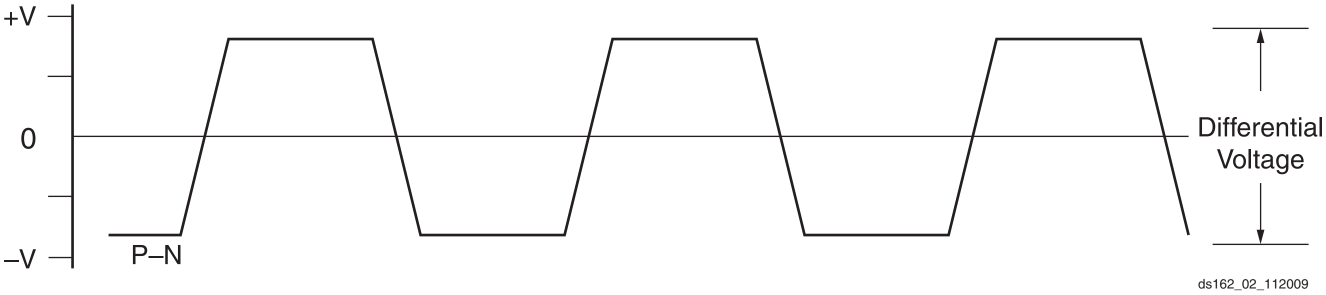

Figure 2: **Differential Peak-to-Peak Voltage**

Table 17 summarizes the DC specifications of the clock input of the GTP transceiver. Consult UG386: *Spartan-6 FPGA GTP Transceivers User Guide* for further details.

Table 21: GTP Transceiver User Clock Switching Characteristics(1)

Symbol	Description	Conditions	Speed Grade				Units
			-3	-3N	-2	-1L	
F_{TXOUT}	TXOUTCLK maximum frequency		320	320	270	N/A	MHz
F_{RXREC}	RXRECCLK maximum frequency		320	320	270	N/A	MHz
T_{RX}	RXUSRCLK maximum frequency		320	320	270	N/A	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz
T_{TX}	TXUSRCLK maximum frequency		320	320	270	N/A	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz

Notes:

1. Clocking must be implemented as described in UG386: *Spartan-6 FPGA GTP Transceivers User Guide*.

Table 22: GTP Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
T_{RTX}	TX Rise time	20%–80%	–	140	–	ps
T_{FTX}	TX Fall time	80%–20%	–	120	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	400	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	20	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	50	ns
$T_{J3.125}$	Total Jitter(2)	3.125 Gb/s	–	–	0.35	UI
$D_{J3.125}$	Deterministic Jitter(2)		–	–	0.15	UI
$T_{J2.5}$	Total Jitter(2)	2.5 Gb/s	–	–	0.33	UI
$D_{J2.5}$	Deterministic Jitter(2)		–	–	0.15	UI
$T_{J1.62}$	Total Jitter(2)	1.62 Gb/s	–	–	0.20	UI
$D_{J1.62}$	Deterministic Jitter(2)		–	–	0.10	UI
$T_{J1.25}$	Total Jitter(2)	1.25 Gb/s	–	–	0.20	UI
$D_{J1.25}$	Deterministic Jitter(2)		–	–	0.10	UI
T_{J614}	Total Jitter(2)	614 Mb/s	–	–	0.10	UI
D_{J614}	Deterministic Jitter(2)		–	–	0.05	UI

Notes:

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP transceiver sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.

Table 23: **GTP Transceiver Receiver Switching Characteristics**

Symbol	Description			Min	Typ	Max	Units
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data			–	75	–	ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak			60	–	150	mV
R_{XSST}	Receiver spread-spectrum tracking[1]		Modulated @ 33 KHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)	Internal AC capacitor bypassed		–	–	150	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	CDR 2^{nd}-order loop disabled		–200	–	200	ppm
		CDR 2^{nd}-order loop enabled	PLL_RXDIVSEL_OUT = 1	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 2	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 4	–1000	–	1000	ppm
SJ Jitter Tolerance[2]							
$JT\_SJ_{3.125}$	Sinusoidal Jitter[3]		3.125 Gb/s	0.4	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter[3]		2.5 Gb/s	0.4	–	–	UI
$JT\_SJ_{1.62}$	Sinusoidal Jitter[3]		1.62 Gb/s	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter[3]		1.25 Gb/s	0.5	–	–	UI
JT_SJ_{614}	Sinusoidal Jitter[3]		614 Mb/s	0.5	–	–	UI
SJ Jitter Tolerance with Stressed Eye[2][5]							
$JT\_TJSE_{3.125}$	Total Jitter with stressed eye[4]		3.125 Gb/s	0.65	–	–	UI
$JT\_SJSE_{3.125}$	Sinusoidal Jitter with stressed eye		3.125 Gb/s	0.1	–	–	UI
$JT\_TJSE_{2.7}$	Total Jitter with stressed eye[4]		2.7 Gb/s	0.65	–	–	UI
$JT\_SJSE_{2.7}$	Sinusoidal Jitter with stressed eye		2.7 Gb/s	0.1	–	–	UI

Notes:

1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a Bit Error Ratio of 1e^{-12}.
3. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
4. Composed of 0.37 UI DJ in the form of ISI and 0.18 UI RJ.
5. Measured using PRBS7 data pattern.

Endpoint Block for PCI Express Designs Switching Characteristics

The Endpoint block for PCI Express is available in the Spartan-6 LXT devices. Consult the Spartan-6 FPGA Integrated Endpoint Block for PCI Express for further information.

Table 24: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
$F_{PCIEUSER}$	User clock maximum frequency	62.5	62.5	62.5	N/A	MHz

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.20 for -3, -3N, and -2; and v1.08 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

The -1L speed grade refers to the lower-power Spartan-6 devices. The -3N speed grade refers to the Spartan-6 devices that do not support MCB functionality.

Table 26 correlates the current status of each Spartan-6 device on a per speed grade basis.

Table 26: **Spartan-6 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6SLX4(1)			-3, -2, -1L
XC6SLX9			-3, -3N, -2, -1L
XC6SLX16			-3, -3N, -2, -1L
XC6SLX25			-3, -3N, -2, -1L
XC6SLX25T			-3, -3N, -2
XC6SLX45			-3, -3N, -2, -1L
XC6SLX45T			-3, -3N, -2
XC6SLX75			-3, -3N, -2, -1L
XC6SLX75T			-3, -3N, -2
XC6SLX100			-3, -3N, -2, -1L
XC6SLX100T			-3, -3N, -2
XC6SLX150			-3, -3N, -2, -1L
XC6SLX150T			-3, -3N, -2
XA6SLX4			-3, -2
XA6SLX9			-3, -2
XA6SLX16			-3, -2
XA6SLX25			-3, -2
XA6SLX25T			-3, -2
XA6SLX45			-3, -2
XA6SLX45T			-3, -2
XA6SLX75			-3, -2
XA6SLX75T			-3, -2
XA6SLX100			-2
XQ6SLX75			-2, -1L
XQ6SLX75T			-3, -2
XQ6SLX150			-2, -1L
XQ6SLX150T			-3, -2

Notes:

1. The XC6SLX4 is not available in the -3N speed grade.

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-6 devices.

Table 29: **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices[1]** ***(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
DIFF_SSTL3_I	1.26	1.44	1.95	2.15	1.95	2.15	ns
DIFF_SSTL3_II	1.26	1.44	1.94	2.14	1.94	2.14	ns
DIFF_SSTL2_I	1.09	1.27	1.94	2.14	1.94	2.14	ns
DIFF_SSTL2_II	1.09	1.27	1.90	2.10	1.90	2.10	ns
DIFF_SSTL18_I	1.04	1.22	1.86	2.06	1.86	2.06	ns
DIFF_SSTL18_II	1.05	1.23	1.82	2.02	1.82	2.02	ns
DIFF_SSTL15_II	1.01	1.19	1.81	2.01	1.81	2.01	ns
DIFF_MOBILE_DDR	1.04	1.22	1.89	2.09	1.89	2.09	ns
LVTTL, QUIETIO, 2 mA	1.42	1.60	5.64	5.84	5.64	5.84	ns
LVTTL, QUIETIO, 4 mA	1.42	1.60	4.46	4.66	4.46	4.66	ns
LVTTL, QUIETIO, 6 mA	1.42	1.60	3.92	4.12	3.92	4.12	ns
LVTTL, QUIETIO, 8 mA	1.42	1.60	3.37	3.57	3.37	3.57	ns
LVTTL, QUIETIO, 12 mA	1.42	1.60	3.42	3.62	3.42	3.62	ns
LVTTL, QUIETIO, 16 mA	1.42	1.60	3.09	3.29	3.09	3.29	ns
LVTTL, QUIETIO, 24 mA	1.42	1.60	2.83	3.03	2.83	3.03	ns
LVTTL, Slow, 2 mA	1.42	1.60	4.58	4.78	4.58	4.78	ns
LVTTL, Slow, 4 mA	1.42	1.60	3.38	3.58	3.38	3.58	ns
LVTTL, Slow, 6 mA	1.42	1.60	2.95	3.15	2.95	3.15	ns
LVTTL, Slow, 8 mA	1.42	1.60	2.73	2.93	2.73	2.93	ns
LVTTL, Slow, 12 mA	1.42	1.60	2.72	2.92	2.72	2.92	ns
LVTTL, Slow, 16 mA	1.42	1.60	2.53	2.73	2.53	2.73	ns
LVTTL, Slow, 24 mA	1.42	1.60	2.42	2.62	2.42	2.62	ns
LVTTL, Fast, 2 mA	1.42	1.60	4.04	4.24	4.04	4.24	ns
LVTTL, Fast, 4 mA	1.42	1.60	2.66	2.86	2.66	2.86	ns
LVTTL, Fast, 6 mA	1.42	1.60	2.58	2.78	2.58	2.78	ns
LVTTL, Fast, 8 mA	1.42	1.60	2.46	2.66	2.46	2.66	ns
LVTTL, Fast, 12 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns
LVTTL, Fast, 16 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns
LVTTL, Fast, 24 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns
LVCMOS33, QUIETIO, 2 mA	1.41	1.59	5.65	5.85	5.65	5.85	ns
LVCMOS33, QUIETIO, 4 mA	1.41	1.59	4.20	4.40	4.20	4.40	ns
LVCMOS33, QUIETIO, 6 mA	1.41	1.59	3.65	3.85	3.65	3.85	ns
LVCMOS33, QUIETIO, 8 mA	1.41	1.59	3.51	3.71	3.51	3.71	ns
LVCMOS33, QUIETIO, 12 mA	1.41	1.59	3.09	3.29	3.09	3.29	ns
LVCMOS33, QUIETIO, 16 mA	1.41	1.59	2.91	3.11	2.91	3.11	ns
LVCMOS33, QUIETIO, 24 mA	1.41	1.59	2.73	2.93	2.73	2.93	ns
LVCMOS33, Slow, 2 mA	1.41	1.59	4.59	4.79	4.59	4.79	ns
LVCMOS33, Slow, 4 mA	1.41	1.59	3.14	3.34	3.14	3.34	ns

Table 34: **SSO Limit per V_{CCO}/GND Pair**

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
1.2V	LVCMOS12, LVCMOS12_JEDEC	2	Fast	30 (1)	35	30	35
			Slow	51	55	51	52
			QuietIO	71	58	71	70
		4	Fast	17	17	17	19
			Slow	23	25	23	22
			QuietIO	35	32	35	32
		6	Fast	13	15	13	14
			Slow	19	20	19	17
			QuietIO	26	24	26	24
		8	Fast	N/A	12	N/A	12
			Slow	N/A	15	N/A	13
			QuietIO	N/A	20	N/A	19
		12	Fast	N/A	5	N/A	4
			Slow	N/A	8	N/A	5
			QuietIO	N/A	11	N/A	10

Table 34: **SSO Limit per V_{CCO}/GND Pair *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
1.5V	LVCMOS15, LVCMOS15_JEDEC	2	Fast	33	40	33	41
			Slow	57	62	57	56
			QuietIO	70	67	70	66
		4	Fast	19	21	19	21
			Slow	30	30	30	24
			QuietIO	38	33	38	30
		6	Fast	14	16	14	16
			Slow	18	19	18	17
			QuietIO	27	24	27	21
		8	Fast	11	13	11	12
			Slow	16	16	16	14
			QuietIO	23	20	23	17
		12	Fast	N/A	5	N/A	4
			Slow	N/A	8	N/A	5
			QuietIO	N/A	10	N/A	9
		16	Fast	N/A	5	N/A	4
			Slow	N/A	8	N/A	8
			QuietIO	N/A	10	N/A	9
	HSTL_I			9	10	9	10
	HSTL_II			N/A	5	N/A	6
	HSTL_III			7	9	7	9
	DIFF_HSTL_I			27	30	27	30
	DIFF_HSTL_II			N/A	15	N/A	18
	DIFF_HSTL_III			21	27	21	27
	SSTL_15_II (3)			N/A	5	N/A	4
	DIFF_SSTL_15_II (3)			N/A	15	N/A	12

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 41: **CLB Distributed RAM Switching Characteristics (SLICEM Only)**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Sequential Delays						
T_{SHCKO}	Clock to A – D outputs	1.26	1.55	1.55	2.35	ns, Max
	Clock to A – D outputs (direct output path)	0.96	1.20	1.20	1.87	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS}/T_{DH}	AX – DX or AI – DI inputs to CLK	0.59/ 0.17	0.73/ 0.22	0.73/ 0.22	1.17/ 0.33	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock for XC devices	0.28/ 0.35	0.32/ 0.42	0.32/ 0.42	0.26/ 0.71	ns, Min
	Address An inputs to clock for XA and XQ devices	0.28/ 0.51	N/A	0.32/ 0.51	0.26/ 0.71	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.31/ –0.08	0.37/ –0.08	0.37/ –0.08	0.59/ –0.27	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.31/ –0.08	0.37/ –0.08	0.37/ –0.08	0.59/ –0.27	ns, Min

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 42: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	1.35	1.78	1.78	2.74	ns, Max
	Clock to A – D outputs (direct output path)	1.24	1.65	1.65	2.48	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS}/T_{WH}	WE input to CLK	0.20/ –0.07	0.24/ –0.07	0.24/ –0.07	0.29/ –0.27	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK for XC devices	0.30/ 0.30	0.30/ 0.38	0.30/ 0.38	0.82/ –0.41	ns, Min
	CE input to CLK for XA and XQ devices	0.32/ 0.30	N/A	0.40/ 0.38	0.82/ –0.41	ns, Min
T_{DS}/T_{DH}	AX – DX or AI – DI inputs to CLK	0.07/ 0.11	0.09/ 0.14	0.09/ 0.14	0.11/ 0.23	ns, Min

Block RAM Switching Characteristics

Table 43: **Block RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Block RAM Clock to Out Delays						
T_{RCKO_DO}	Clock CLK to DOUT output (without output register)(1)	1.85	2.10	2.10	3.50	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register)(2)	1.60	1.75	1.75	2.30	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs for XC devices(3)	0.35/ 0.10	0.40/ 0.12	0.40/ 0.12	0.50/ 0.15	ns, Min
	ADDR inputs for XA and XQ devices(3)	0.35/ 0.17	N/A	0.40/ 0.17	0.50/ 0.15	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs(4)	0.30/ 0.10	0.30/ 0.10	0.30/ 0.10	0.40/ 0.15	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.22/ 0.05	0.25/ 0.06	0.25/ 0.06	0.44/ 0.10	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.20/ 0.10	0.20/ 0.10	0.20/ 0.10	0.28/ 0.15	ns, Min
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input	0.25/ 0.10	0.33/ 0.10	0.33/ 0.10	0.28/ 0.15	ns, Min
Maximum Frequency						
F_{MAX}	Block RAM in all modes	320	280	280	150	MHz

Notes:

1. T_{RCKO_DO} includes T_{RCKO_DOA} and T_{RCKO_DOPA} as well as the B port equivalent timing parameters.
2. $T_{RCKO\_DO\_REG}$ includes $T_{RCKO\_DOA\_REG}$ and $T_{RCKO\_DOPA\_REG}$ as well as the B port equivalent timing parameters.
3. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
4. T_{RDCK_DI} includes both A and B inputs as well as the parity inputs of A and B.

Table 54: **Switching Characteristics for the Delay-Locked Loop (DLL)(1)**

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges										
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs.	5	280	5	280	5	250	5	175	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs.	5	200	5	200	5	200	5	175	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs.	10	375	10	375	10	334	10	250	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output.	0.3125	186	0.3125	186	0.3125	166	0.3125	88.6	MHz
Output Clock Jitter(2)(3)(4)										
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output.	–	±100	–	±100	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs.	Maximum = ±[0.5% of CLKIN period + 100]								ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division.	Maximum = ±[0.5% of CLKIN period + 100]								ps
Duty Cycle(4)										
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion.	Typical = ±[1% of CLKIN period + 350]								ps
Phase Alignment(4)										
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 1X).	–	±150	–	±150	–	±150	–	±250	ps
	Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 2X).(6)	–	±250	–	±250	–	±250	–	±350	
CLKOUT_PHASE_DLL	Phase offset between DLL outputs for CLK0 to CLK2X (not CLK2X180).	Maximum = ±[1% of CLKIN period + 100]								ps
	Phase offset between DLL outputs for all others.	Maximum = ±[1% of CLKIN period + 150]						Maximum = ±[1% of CLKIN period + 200]		ps

Table 57: **Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)[1]**

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges (DCM_CLKGEN)										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz
CLKOUT_FREQ_FXDV	Frequency for the CLKFXDV output	0.15625	187.5	0.15625	187.5	0.15625	166.5	0.15625	100	MHz
Output Clock Jitter[2][3]										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKOUT_PER_JITT_FXDV	Period jitter at the CLKFXDV output.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKFX_FREEZE_VAR	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX > 50 MHz	Maximum = ±3% of CLKFX period								ps
	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX < 50 MHz	Maximum = ±5% of CLKFX period								ps
CLKFX_FREEZE_TEMP_SLOPE	CLKFX period will change in free_oscillator mode over temperature. Add to CLKFX_FREEZE_VAR to determine total CLKFX period change. Percentage change for CLKFX period over 1°C.	Maximum = 0.1								%/°C
Duty Cycle[4][5]										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
CLKOUT_DUTY_CYCLE_FXDV	Duty cycle precision for the CLKFXDV outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
Lock Time										
LOCK_FX[2]	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX, CLKFX180, and CLKFXDV signals are valid. Lock time requires CLKFX_DIVIDE < F_{IN}/(0.50 MHz) when: F_{CLKIN} < 50 MHz	–	50	–	50	–	50	–	50	ms
	when: F_{CLKIN} > 50 MHz	–	5	–	5	–	5	–	5	ms

Table 77: **Global Clock Setup and Hold With DCM and PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Example Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin,(1) Using DCM, PLL, and Global Clock Buffer for the LVCMOS25 standard.							
$T_{PSDCMPLL\_0}$/ $T_{PHDCMPLL\_0}$	No Delay Global Clock and IFF(2) with DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode.	XC6SLX4	0.43/1.07	N/A	0.43/1.43	1.10/1.67	ns
		XC6SLX9	0.43/1.03	0.45/1.14	0.45/1.43	1.10/1.67	ns
		XC6SLX16	0.74/0.93	0.74/1.12	0.74/1.21	0.77/1.35	ns
		XC6SLX25	0.67/1.02	0.76/1.11	0.84/1.18	1.23/1.46	ns
		XC6SLX25T	0.67/1.02	0.76/1.11	0.84/1.18	N/A	ns
		XC6SLX45	0.65/0.99	0.65/1.04	0.71/1.12	1.18/1.58	ns
		XC6SLX45T	0.65/1.00	0.65/1.04	0.71/1.12	N/A	ns
		XC6SLX75	0.86/1.01	0.88/1.06	0.94/1.14	1.29/1.67	ns
		XC6SLX75T	0.86/1.01	0.88/1.06	0.94/1.14	N/A	ns
		XC6SLX100	0.50/1.10	0.56/1.10	0.61/1.17	0.84/2.24	ns
		XC6SLX100T	0.50/1.10	0.56/1.10	0.61/1.17	N/A	ns
		XC6SLX150	0.45/1.28	0.47/1.28	0.52/1.28	1.27/1.56	ns
		XC6SLX150T	0.45/1.28	0.47/1.28	0.52/1.28	N/A	ns
		XA6SLX4	0.74/1.00	N/A	0.74/1.43	N/A	ns
		XA6SLX9	0.74/1.00	N/A	0.74/1.43	N/A	ns
		XA6SLX16	1.81/1.15	N/A	1.81/1.03	N/A	ns
		XA6SLX25	0.89/1.01	N/A	0.96/1.05	N/A	ns
		XA6SLX25T	0.89/1.01	N/A	1.04/1.15	N/A	ns
		XA6SLX45	0.69/0.95	N/A	0.83/0.96	N/A	ns
		XA6SLX45T	0.69/0.95	N/A	0.83/0.96	N/A	ns
		XA6SLX75	0.88/0.94	N/A	1.06/0.96	N/A	ns
		XA6SLX75T	0.88/0.94	N/A	1.06/0.96	N/A	ns
		XA6SLX100	N/A	N/A	1.55/1.33	N/A	ns
		XQ6SLX75	N/A	N/A	1.06/0.96	1.29/1.67	ns
		XQ6SLX75T	0.88/0.94	N/A	1.06/0.96	N/A	ns
		XQ6SLX150	N/A	N/A	0.64/1.30	1.27/1.56	ns
		XQ6SLX150T	0.58/1.30	N/A	0.64/1.30	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG. Package skew is not included in these measurements.
2. IFF = Input Flip-Flop

Table 81: **Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out Using BUFIO2**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO2							
T_{PSCS}/T_{PHCS}	IFF setup/hold using BUFIO2 clock	XC6SLX4	0.57/0.94	N/A	0.95/1.12	0.27/1.56	ns
		XC6SLX9	0.40/0.95	0.50/0.96	0.60/1.12	0.27/1.56	ns
		XC6SLX16	0.48/0.74	0.55/0.75	0.69/0.83	1.27/1.31	ns
		XC6SLX25	0.28/1.02	0.28/1.12	0.28/1.24	0.15/1.78	ns
		XC6SLX25T	0.28/1.02	0.28/1.12	0.28/1.24	N/A	ns
		XC6SLX45	0.42/1.19	0.44/1.29	0.50/1.40	0.12/1.83	ns
		XC6SLX45T	0.42/1.19	0.44/1.29	0.50/1.40	N/A	ns
		XC6SLX75	0.38/1.48	0.38/1.63	0.38/1.84	0.05/2.78	ns
		XC6SLX75T	0.38/1.48	0.38/1.63	0.38/1.84	N/A	ns
		XC6SLX100	0.06/1.48	0.06/1.63	0.06/1.87	–0.03/2.72	ns
		XC6SLX100T	0.06/1.48	0.06/1.63	0.06/1.87	N/A	ns
		XC6SLX150	0.04/1.73	0.04/1.75	0.04/1.98	–0.08/3.07	ns
		XC6SLX150T	0.04/1.73	0.04/1.75	0.04/1.98	N/A	ns
		XA6SLX4	0.64/0.96	N/A	0.97/1.12	N/A	ns
		XA6SLX9	0.44/0.99	N/A	0.62/1.16	N/A	ns
		XA6SLX16	0.50/0.78	N/A	0.69/0.83	N/A	ns
		XA6SLX25	0.28/1.04	N/A	0.28/1.25	N/A	ns
		XA6SLX25T	0.28/1.04	N/A	0.28/1.25	N/A	ns
		XA6SLX45	0.43/1.21	N/A	0.50/1.40	N/A	ns
		XA6SLX45T	0.43/1.21	N/A	0.50/1.40	N/A	ns
		XA6SLX75	0.38/1.49	N/A	0.38/1.84	N/A	ns
		XA6SLX75T	0.38/1.49	N/A	0.38/1.84	N/A	ns
		XA6SLX100	N/A	N/A	1.01/1.63	N/A	ns
		XQ6SLX75	N/A	N/A	0.38/1.84	0.05/2.78	ns
		XQ6SLX75T	0.38/1.49	N/A	0.38/1.84	N/A	ns
		XQ6SLX150	N/A	N/A	0.04/1.98	–0.08/3.07	ns
		XQ6SLX150T	0.04/1.75	N/A	0.04/1.98	N/A	ns

Table 81: **Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out Using BUFIO2** ***(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Pin-to-Pin Clock-to-Out Using BUFIO2							
$T_{ICKOFCS}$	OFF clock-to-out using BUFIO2 clock	XC6SLX4	5.51	N/A	6.95	8.45	ns
		XC6SLX9	5.51	5.89	6.95	8.45	ns
		XC6SLX16	5.31	5.70	6.67	8.21	ns
		XC6SLX25	5.53	6.00	7.02	8.72	ns
		XC6SLX25T	5.53	6.00	7.02	N/A	ns
		XC6SLX45	5.76	6.18	7.22	8.77	ns
		XC6SLX45T	5.76	6.18	7.22	N/A	ns
		XC6SLX75	5.94	6.46	7.57	9.72	ns
		XC6SLX75T	5.94	6.46	7.57	N/A	ns
		XC6SLX100	6.09	6.53	7.60	9.66	ns
		XC6SLX100T	6.09	6.53	7.60	N/A	ns
		XC6SLX150	6.29	6.69	7.81	9.94	ns
		XC6SLX150T	6.29	6.69	7.81	N/A	ns
		XA6SLX4	5.83	N/A	6.95	N/A	ns
		XA6SLX9	5.83	N/A	6.95	N/A	ns
		XA6SLX16	5.65	N/A	6.68	N/A	ns
		XA6SLX25	5.85	N/A	7.03	N/A	ns
		XA6SLX25T	5.85	N/A	7.03	N/A	ns
		XA6SLX45	6.07	N/A	7.25	N/A	ns
		XA6SLX45T	6.07	N/A	7.25	N/A	ns
		XA6SLX75	6.26	N/A	7.57	N/A	ns
		XA6SLX75T	6.26	N/A	7.57	N/A	ns
		XA6SLX100	N/A	N/A	7.48	N/A	ns
		XQ6SLX75	N/A	N/A	7.57	9.72	ns
		XQ6SLX75T	6.26	N/A	7.57	N/A	ns
		XQ6SLX150	N/A	N/A	7.81	9.94	ns
		XQ6SLX150T	6.62	N/A	7.81	N/A	ns

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
08/26/09	1.1	Added V_{FS} to Table 1and Table 2. Added R_{FUSE} to Table 2. Added XC6SLX75 and XC6SLX75T to V_{BATT} and I_{BATT} in Table 1, Table 2, and Table 4. Corrected the quiescent supply current for the XC6SLX4 in Table 5. Updated Table 11. Removed DV_{PPIN} from Figure 2. Removed $F_{PCIECORE}$ from Table 24 and added values to $F_{PCIEUSER}$. Added more networking applications to Table 25. Updated values for $T_{SUSPENDLOW\_AWAKE}$, $T_{SUSPEND\_ENABLE}$, and T_{SCP_AWAKE} in Table 46. Numerous changes to Table 47, page 54 including the addition of new values to various specifications, revising the $T_{SMCKCSO}$ description, and changing the units of T_{POR}. Also, removed *Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK section* from Table 47 and updated all the notes. In Table 52, added to F_{INMAX}, revised F_{OUTMAX}, and removed PLL Maximum Output Frequency for BUFIO2. Revised values for DCM_DELAY_STEP in Table 54. Updated CLKIN_FREQ_FX values in Table 55.
01/04/10	1.2	Added -4 speed grade to entire document. Updated speed specification of -4, -3, -2 speed grades to version 1.03. Added -1L speed grade numbers per speed specification 1.00. Updated T_{SOL} in Table 1. Added -1L rows for LVCMOS12, LVCMOS15, and LVCMOS18 in Table 9. Revised much of the detail in GTP Transceiver Specifications in Table 12 through Table 23. Added -2 data to Table 25. Updated F_{MAX} in Table 44. Updated descriptions for $T_{DNACLKL}$ and $T_{DNACLKH}$ in Table 45 and revised values for all parameters. Removed $T_{INITADDR}$ from Table 47 and added new data. Updated values in Table 48 through Table 62. Added Table 51 (BUFPLL) and Table 57 (DCM_CLKGEN). Removed $T_{LOCKMAX}$ note from Table 52. Updated note 3 in Table 53. In Table 79: removed XC6SLX75CSG324 and XC6SLX75TCSG324; added XC6SLX75FG(G)484 and XC6SLX75FG(G)484.
02/22/10	1.3	Production release of XC6SLX16 -2 speed grade devices. The changes to Table 26 and Table 27 includes updating this data sheet to the data in ISE v11.5 software with speed specification v1.06. Updated maximum of V_{IN} and V_{TS} and note 2 in Table 1. In Table 2, changed V_{IN}, added I_{IN} and note 5, revised notes 1, 6, and 7, and added note 8 to R_{FUSE}. In Table 4, removed previous note 1 and added data to I_{RPU}, I_{RPD}, and I_{BATT}, changed C_{IN}, added R_{DT} and R_{IN_TERM}, and added note 2 and 3. Updated V_{CCO2} in Table 6. Added Table 7 and Table 8. Removed PCI66_3 from Table 9. Updated PCI33_3 and I2C in Table 9. Updated the description of Table 11. Completely updated Table 25. Updated Table 28 including adding values for PCI33_3. Updated V_{REF} value for HSTL_III_18 in Table 31. Updates missing V_{REF} values in Table 32. Added Simultaneously Switching Outputs, page 36. Removed T_{GSRQ} and T_{RPW} from Table 35 and Table 36. Also removed T_{DOQ} from Table 36. Removed T_{ISDO_DO} and note 1 from Table 37. Removed T_{OSCCK_S} and combinatorial section from Table 38. In Table 39, removed T_{IODDO_T} and added new tap parameters and note 2. In Table 40, Table 41, and Table 42, made typographical edits and removed notes. Removed clock CLK section in Table 41. Removed clock CLK section and T_{REG_MUX} and T_{REG_M31} in Table 42. Added block RAM F_{MAX} values to Table 43. Updated values and added note 2 to Table 45. Added values to Table 46 and removed note 1. Numerous changes to Table 47. Completely updated Table 57. Revised data in Table 62. Removed note 3 from Table 71. Added values to Table 79. Added data to Table 80 and Table 81.
03/10/10	1.4	Production release of XC6SLX45 -2 speed grade devices, which includes changes to Table 26 and Table 27 updating this data sheet to the data in ISE v11.5 software with speed specification v1.07. Fixed R_{IN_TERM} description in Table 4. Added PCI66_3 to Table 7 and replaced note 1. Corrected note 1 and the V, Max for TMDS_33 in Table 8. In Table 10, added note 1 to LVPECL_33 and TMDS_33. Also updated specifications for TMDS_33. Updated the GTP Transceiver Specifications section including adding values to Table 16, Table 17, and Table 20 through Table 23. Added PCI66_3 back into Table 9, Table 28, Table 31, Table 32, and Table 34. Updated note 3 on Table 32. In Table 34, corrected some typographical errors and fixed SSO limits for bank1/3 in FG(G)484 package. Corrected T_{OSCKC_OCE} in Table 38. In Table 57, updated CLKFX_FREEZE_VAR and CLKFX_FREEZE_TEMP_SLOPE and added typical values to $T_{CENTER\_LOW\_SPREAD}$ and $T_{CENTER\_HIGH\_SPREAD}$. Updated and added values to Table 63 through Table 78, and Table 81. In Table 79, revised the XC6SLX16-CSG324 and the XC6SLX45-CSG484 and FG(G)484 values.