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Details

Product Status	Active
Number of LABs/CLBs	300
Number of Logic Elements/Cells	3840
Total RAM Bits	221184
Number of I/O	102
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx4-l1tqg144c

Table 8: Recommended Operating Conditions for User I/Os Using Differential Signal Standards

I/O Standard	V _{CCO} for Drivers		
	V, Min	V, Nom	V, Max
LVDS_33	3.0	3.3	3.45
LVDS_25	2.25	2.5	2.75
BLVDS_25	2.25	2.5	2.75
MINI_LVDS_33	3.0	3.3	3.45
MINI_LVDS_25	2.25	2.5	2.75
LVPECL_33 ⁽¹⁾	N/A—Inputs Only		
LVPECL_25	N/A—Inputs Only		
RSDS_33	3.0	3.3	3.45
RSDS_25	2.25	2.5	2.75
TMDS_33 ⁽¹⁾	3.14	3.3	3.45
PPDS_33	3.0	3.3	3.45
PPDS_25	2.25	2.5	2.75
DISPLAY_PORT	2.3	2.5	2.7
DIFF_MOBILE_DDR	1.7	1.8	1.9
DIFF_HSTL_I	1.4	1.5	1.6
DIFF_HSTL_II	1.4	1.5	1.6
DIFF_HSTL_III	1.4	1.5	1.6
DIFF_HSTL_I_18	1.7	1.8	1.9
DIFF_HSTL_II_18	1.7	1.8	1.9
DIFF_HSTL_III_18	1.7	1.8	1.9
DIFF_SSTL3_I	3.0	3.3	3.45
DIFF_SSTL3_II	3.0	3.3	3.45
DIFF_SSTL2_I	2.3	2.5	2.7
DIFF_SSTL2_II	2.3	2.5	2.7
DIFF_SSTL18_I	1.7	1.8	1.9
DIFF_SSTL18_II	1.7	1.8	1.9
DIFF_SSTL15_II	1.425	1.5	1.575

Notes:

1. LVPECL_33 and TMDS_33 inputs require V_{CCAUX} = 3.3V nominal.

eFUSE Read Endurance

Table 11 lists the minimum guaranteed number of read cycle operations for Device DNA and for the AES eFUSE key. For more information, see [UG380: Spartan-6 FPGA Configuration User Guide](#).

Table 11: eFUSE Read Endurance

Symbol	Description	Speed Grade				Units (Min)
		-3	-3N	-2	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTP Transceiver Specifications

GTP transceivers are available in the Spartan-6 LXT devices. See [DS160: Spartan-6 Family Overview](#) for more information.

GTP Transceiver DC Characteristics

Table 12: Absolute Maximum Ratings for GTP Transceivers⁽¹⁾

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	-0.5	1.32	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	-0.5	1.32	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	-0.5	1.32	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	-0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	-0.5	1.32	V
V _{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	-0.5	1.32	V
V _{MGTREFCLK}	Reference clock absolute input voltage	-0.5	1.32	V

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 13: Recommended Operating Conditions for GTP Transceivers⁽¹⁾⁽²⁾⁽³⁾

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	1.14	1.20	1.26	V

Notes:

- Each voltage listed requires the filter circuit described in [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#).
- Voltages are specified for the temperature range of T_j = -40°C to +125°C.
- The voltage level of MGTAVCCPLL must not exceed the voltage level of MGTAVCC +10mV. The voltage level of MGTAVCC must not exceed the voltage level of MGTAVCCPLL.

Table 14: GTP Transceiver Current Supply (per Lane)

Symbol	Description	Typ ⁽¹⁾	Max	Units
I _{MGTAVCC}	GTP transceiver internal analog supply current	40.4	Note 2	mA
I _{MGTAVTTTX}	GTP transmitter termination supply current	27.4		mA
I _{MGTAVTTRX}	GTP receiver termination supply current	13.6		mA
I _{MGTAVCCPLL}	GTP transmitter and receiver PLL supply current	28.7		mA
R _{MGTRREF}	Precision reference resistor for internal calibration termination	50.0 ± 1% tolerance		Ω

Notes:

- Typical values are specified at nominal voltage, 25°C, with a 2.5 Gb/s line rate, with a shared PLL use mode.
- Values for currents of other transceiver configurations and conditions can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 15: GTP Transceiver Quiescent Supply Current (per Lane)⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

Symbol	Description	Typ ⁽⁵⁾	Max	Units
I _{MGTAVCCQ}	Quiescent MGTAVCC supply current	1.7	Note 2	mA
I _{MGTAVTTTXQ}	Quiescent MGTAVTTTX supply current	0.1		mA
I _{MGTAVTTRXQ}	Quiescent MGTAVTTRX supply current	1.2		mA
I _{MGTAVCCPLLQ}	Quiescent MGTAVCCPLL supply current	1.0		mA

Notes:

- Device powered and unconfigured.
- Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
- GTP transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTP transceivers.
- Does not include power-up MGTAVTTRCAL supply current during device configuration.
- Typical values are specified at nominal voltage, 25°C.

Table 21: GTP Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Conditions	Speed Grade				Units
			-3	-3N	-2	-1L	
F _{TXOUT}	TXOUTCLK maximum frequency		320	320	270	N/A	MHz
F _{RXREC}	RXRECCLK maximum frequency		320	320	270	N/A	MHz
T _{RX}	RXUSRCLK maximum frequency		320	320	270	N/A	MHz
T _{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz
T _{TX}	TXUSRCLK maximum frequency		320	320	270	N/A	MHz
T _{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz

Notes:

1. Clocking must be implemented as described in [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#).

Table 22: GTP Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
T _{RTX}	TX Rise time	20%–80%	–	140	–	ps
T _{FTX}	TX Fall time	80%–20%	–	120	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	400	ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–	20	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–	50	ns
T _{J3.125}	Total Jitter ⁽²⁾	3.125 Gb/s	–	–	0.35	UI
D _{J3.125}	Deterministic Jitter ⁽²⁾		–	–	0.15	UI
T _{J2.5}	Total Jitter ⁽²⁾	2.5 Gb/s	–	–	0.33	UI
D _{J2.5}	Deterministic Jitter ⁽²⁾		–	–	0.15	UI
T _{J1.62}	Total Jitter ⁽²⁾	1.62 Gb/s	–	–	0.20	UI
D _{J1.62}	Deterministic Jitter ⁽²⁾		–	–	0.10	UI
T _{J1.25}	Total Jitter ⁽²⁾	1.25 Gb/s	–	–	0.20	UI
D _{J1.25}	Deterministic Jitter ⁽²⁾		–	–	0.10	UI
T _{J614}	Total Jitter ⁽²⁾	614 Mb/s	–	–	0.10	UI
D _{J614}	Deterministic Jitter ⁽²⁾		–	–	0.05	UI

Notes:

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP transceiver sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVC MOS33, Fast, 8 mA	1.34	1.46	1.59	1.82	2.07	2.21	2.41	3.03	2.07	2.21	2.41	3.03	ns
LVC MOS33, Fast, 12 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns
LVC MOS33, Fast, 16 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns
LVC MOS33, Fast, 24 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns
LVC MOS25, QUIETIO, 2 mA	0.82	0.94	1.07	1.31	4.81	4.95	5.15	5.79	4.81	4.95	5.15	5.79	ns
LVC MOS25, QUIETIO, 4 mA	0.82	0.94	1.07	1.31	3.70	3.84	4.04	4.66	3.70	3.84	4.04	4.66	ns
LVC MOS25, QUIETIO, 6 mA	0.82	0.94	1.07	1.31	3.46	3.60	3.80	4.38	3.46	3.60	3.80	4.38	ns
LVC MOS25, QUIETIO, 8 mA	0.82	0.94	1.07	1.31	3.20	3.34	3.54	4.12	3.20	3.34	3.54	4.12	ns
LVC MOS25, QUIETIO, 12 mA	0.82	0.94	1.07	1.31	2.83	2.97	3.17	3.75	2.83	2.97	3.17	3.75	ns
LVC MOS25, QUIETIO, 16 mA	0.82	0.94	1.07	1.31	2.64	2.78	2.98	3.64	2.64	2.78	2.98	3.64	ns
LVC MOS25, QUIETIO, 24 mA	0.82	0.94	1.07	1.31	2.45	2.59	2.79	3.42	2.45	2.59	2.79	3.42	ns
LVC MOS25, Slow, 2 mA	0.82	0.94	1.07	1.31	3.78	3.92	4.12	4.76	3.78	3.92	4.12	4.76	ns
LVC MOS25, Slow, 4 mA	0.82	0.94	1.07	1.31	2.79	2.93	3.13	3.73	2.79	2.93	3.13	3.73	ns
LVC MOS25, Slow, 6 mA	0.82	0.94	1.07	1.31	2.73	2.87	3.07	3.66	2.73	2.87	3.07	3.66	ns
LVC MOS25, Slow, 8 mA	0.82	0.94	1.07	1.31	2.48	2.62	2.82	3.42	2.48	2.62	2.82	3.42	ns
LVC MOS25, Slow, 12 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.95	2.01	2.15	2.35	2.95	ns
LVC MOS25, Slow, 16 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.95	2.01	2.15	2.35	2.95	ns
LVC MOS25, Slow, 24 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.94	2.01	2.15	2.35	2.94	ns
LVC MOS25, Fast, 2 mA	0.82	0.94	1.07	1.31	3.35	3.49	3.69	4.31	3.35	3.49	3.69	4.31	ns
LVC MOS25, Fast, 4 mA	0.82	0.94	1.07	1.31	2.25	2.39	2.59	3.22	2.25	2.39	2.59	3.22	ns
LVC MOS25, Fast, 6 mA	0.82	0.94	1.07	1.31	2.09	2.23	2.43	3.05	2.09	2.23	2.43	3.05	ns
LVC MOS25, Fast, 8 mA	0.82	0.94	1.07	1.31	2.02	2.16	2.36	2.98	2.02	2.16	2.36	2.98	ns
LVC MOS25, Fast, 12 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns
LVC MOS25, Fast, 16 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns
LVC MOS25, Fast, 24 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns
LVC MOS18, QUIETIO, 2 mA	1.18	1.30	1.43	2.04	5.92	6.06	6.26	6.80	5.92	6.06	6.26	6.80	ns
LVC MOS18, QUIETIO, 4 mA	1.18	1.30	1.43	2.04	4.74	4.88	5.08	5.63	4.74	4.88	5.08	5.63	ns
LVC MOS18, QUIETIO, 6 mA	1.18	1.30	1.43	2.04	4.05	4.19	4.39	4.96	4.05	4.19	4.39	4.96	ns
LVC MOS18, QUIETIO, 8 mA	1.18	1.30	1.43	2.04	3.71	3.85	4.05	4.63	3.71	3.85	4.05	4.63	ns
LVC MOS18, QUIETIO, 12 mA	1.18	1.30	1.43	2.04	3.35	3.49	3.69	4.27	3.35	3.49	3.69	4.27	ns
LVC MOS18, QUIETIO, 16 mA	1.18	1.30	1.43	2.04	3.20	3.34	3.54	4.14	3.20	3.34	3.54	4.14	ns
LVC MOS18, QUIETIO, 24 mA	1.18	1.30	1.43	2.04	2.96	3.10	3.30	3.98	2.96	3.10	3.30	3.98	ns
LVC MOS18, Slow, 2 mA	1.18	1.30	1.43	2.04	4.62	4.76	4.96	5.54	4.62	4.76	4.96	5.54	ns
LVC MOS18, Slow, 4 mA	1.18	1.30	1.43	2.04	3.69	3.83	4.03	4.60	3.69	3.83	4.03	4.60	ns
LVC MOS18, Slow, 6 mA	1.18	1.30	1.43	2.04	3.00	3.14	3.34	3.94	3.00	3.14	3.34	3.94	ns
LVC MOS18, Slow, 8 mA	1.18	1.30	1.43	2.04	2.19	2.33	2.53	3.17	2.19	2.33	2.53	3.17	ns
LVC MOS18, Slow, 12 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVC MOS18, Slow, 16 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS12, QUIETIO, 6 mA	0.98	1.16	4.79	4.99	4.79	4.99	ns
LVC MOS12, QUIETIO, 8 mA	0.98	1.16	4.43	4.63	4.43	4.63	ns
LVC MOS12, QUIETIO, 12 mA	0.98	1.16	4.18	4.38	4.18	4.38	ns
LVC MOS12, Slow, 2 mA	0.98	1.16	5.12	5.32	5.12	5.32	ns
LVC MOS12, Slow, 4 mA	0.98	1.16	3.00	3.20	3.00	3.20	ns
LVC MOS12, Slow, 6 mA	0.98	1.16	2.91	3.11	2.91	3.11	ns
LVC MOS12, Slow, 8 mA	0.98	1.16	2.51	2.71	2.51	2.71	ns
LVC MOS12, Slow, 12 mA	0.98	1.16	2.25	2.45	2.25	2.45	ns
LVC MOS12, Fast, 2 mA	0.98	1.16	3.60	3.80	3.60	3.80	ns
LVC MOS12, Fast, 4 mA	0.98	1.16	2.49	2.69	2.49	2.69	ns
LVC MOS12, Fast, 6 mA	0.98	1.16	1.94	2.14	1.94	2.14	ns
LVC MOS12, Fast, 8 mA	0.98	1.16	1.82	2.02	1.82	2.02	ns
LVC MOS12, Fast, 12 mA	0.98	1.16	1.80	2.00	1.80	2.00	ns
LVC MOS12_JEDEC, QUIETIO, 2 mA	1.57	1.75	6.53	6.73	6.53	6.73	ns
LVC MOS12_JEDEC, QUIETIO, 4 mA	1.57	1.75	5.12	5.32	5.12	5.32	ns
LVC MOS12_JEDEC, QUIETIO, 6 mA	1.57	1.75	4.81	5.01	4.81	5.01	ns
LVC MOS12_JEDEC, QUIETIO, 8 mA	1.57	1.75	4.44	4.64	4.44	4.64	ns
LVC MOS12_JEDEC, QUIETIO, 12 mA	1.57	1.75	4.20	4.40	4.20	4.40	ns
LVC MOS12_JEDEC, Slow, 2 mA	1.57	1.75	5.14	5.34	5.14	5.34	ns
LVC MOS12_JEDEC, Slow, 4 mA	1.57	1.75	2.99	3.19	2.99	3.19	ns
LVC MOS12_JEDEC, Slow, 6 mA	1.57	1.75	2.90	3.10	2.90	3.10	ns
LVC MOS12_JEDEC, Slow, 8 mA	1.57	1.75	2.50	2.70	2.50	2.70	ns
LVC MOS12_JEDEC, Slow, 12 mA	1.57	1.75	2.26	2.46	2.26	2.46	ns
LVC MOS12_JEDEC, Fast, 2 mA	1.57	1.75	3.60	3.80	3.60	3.80	ns
LVC MOS12_JEDEC, Fast, 4 mA	1.57	1.75	2.49	2.69	2.49	2.69	ns
LVC MOS12_JEDEC, Fast, 6 mA	1.57	1.75	1.94	2.14	1.94	2.14	ns
LVC MOS12_JEDEC, Fast, 8 mA	1.57	1.75	1.83	2.03	1.83	2.03	ns
LVC MOS12_JEDEC, Fast, 12 mA	1.57	1.75	1.80	2.00	1.80	2.00	ns

Notes:

1. The Spartan-6Q FPGA -1L values are listed in Table 28.

Table 30 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). These delays are measured using LVC MOS25, Fast, 12 mA.

Table 30: IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T _{IOTPHZ}	T input to Pad high-impedance	1.39	1.59	1.59	1.91	ns

Table 34: SSO Limit per V_{CCO}/GND Pair

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
1.2V	LVCMOS12, LVCMOS12_JEDEC	2	Fast	30 ⁽¹⁾	35	30	35
			Slow	51	55	51	52
			QuietIO	71	58	71	70
		4	Fast	17	17	17	19
			Slow	23	25	23	22
			QuietIO	35	32	35	32
		6	Fast	13	15	13	14
			Slow	19	20	19	17
			QuietIO	26	24	26	24
		8	Fast	N/A	12	N/A	12
			Slow	N/A	15	N/A	13
			QuietIO	N/A	20	N/A	19
		12	Fast	N/A	5	N/A	4
			Slow	N/A	8	N/A	5
			QuietIO	N/A	11	N/A	10

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

V _{CCO}	I/O Standard	Drive	Slew	SSO Limit per V _{CCO} /GND Pair				
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324		
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5	
3.3V	LVTTTL	2	Fast	53	65	53	62	
			Slow	70	80	70	73	
			QuietIO	79	89	79	91	
		4	Fast	23	30	23	27	
			Slow	34	41	34	37	
			QuietIO	44	49	44	46	
		6	Fast	16	21	16	20	
			Slow	21	28	21	25	
			QuietIO	34	39	34	34	
		8	Fast	12	16	12	15	
			Slow	16	22	16	19	
			QuietIO	27	28	27	24	
		12	Fast	1	3	1	1	
			Slow	2	5	2	4	
			QuietIO	2	10	2	8	
		16	Fast	1	3	1	1	
			Slow	1	7	1	2	
			QuietIO	3	11	3	8	
		24	Fast	1	2	1	1	
			Slow	2	5	2	2	
			QuietIO	8	9	8	8	
	PCI33_3				18	19	18	19
	PCI66_3				18	19	18	19
	SSTL_3_I				5	8	5	8
	SSTL_3_II				3	5	3	3
	DIFF_SSTL_3_I				15	24	15	24
	DIFF_SSTL_3_II				9	15	9	9
	SDIO				17	18	17	15

CLB Switching Characteristics (SLICEM Only)

Table 40: CLB Switching Characteristics (SLICEM Only)

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT inputs to A to D outputs	0.21	0.26	0.26	0.46	ns, Max
	An – Dn LUT inputs through F7AMUX/F7BMUX to AMUX/CMUX output	0.37	0.43	0.43	0.77	ns, Max
T _{OPAB}	An – Dn LUT inputs through F7AMUX or F7BMUX and F8MUX to BMUX output	0.37	0.46	0.46	0.84	ns, Max
T _{ITO}	An – Dn LUT inputs through latch to AQ – DQ outputs	0.82	0.95	0.95	1.64	ns, Max
T _{TITO_LOGIC}	An – Dn LUT inputs to AQ – DQ outputs (latch as logic)	0.82	0.95	0.95	1.64	ns, Max
T _{OPCYA}	An LUT inputs to COUT output	0.38	0.48	0.48	0.69	ns, Max
T _{OPCYB}	Bn LUT inputs to COUT output	0.38	0.49	0.49	0.71	ns, Max
T _{OPCYC}	Cn LUT inputs to COUT output	0.28	0.33	0.33	0.55	ns, Max
T _{OPCYD}	Dn LUT inputs to COUT output	0.28	0.35	0.35	0.52	ns, Max
T _{AXCY}	AX input to COUT output	0.21	0.26	0.26	0.36	ns, Max
T _{BXCy}	BX input to COUT output	0.13	0.16	0.16	0.18	ns, Max
T _{CXCy}	CX input to COUT output	0.10	0.12	0.12	0.09	ns, Max
T _{DXCy}	DX input to COUT output	0.09	0.11	0.11	0.09	ns, Max
T _{BYP}	CIN input to COUT output	0.08	0.10	0.10	0.06	ns, Max
T _{CINA}	CIN input to AMUX output	0.21	0.22	0.22	0.47	ns, Max
T _{CINB}	CIN input to BMUX output	0.30	0.31	0.31	0.57	ns, Max
T _{CINC}	CIN input to CMUX output	0.29	0.31	0.31	0.58	ns, Max
T _{CIND}	CIN input to DMUX output	0.31	0.32	0.32	0.68	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.45	0.53	0.53	0.74	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{DICK} /T _{CKDI}	AX – DX input to CLK on A – D flip-flops	0.42/ 0.28	0.47/ 0.39	0.47/ 0.39	0.90/ 0.56	ns, Min
T _{CECK} /T _{CKCE}	CE input to CLK on A – D flip-flops	0.31/ –0.07	0.37/ –0.07	0.37/ –0.07	0.59/ –0.27	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D flip-flops for XC devices	0.41/ 0.02	0.42/ 0.02	0.42/ 0.02	0.68/ –0.29	ns, Min
	SR input to CLK on A – D flip-flops for XA and XQ devices	0.41/ 0.02	N/A	0.44/ 0.02	0.68/ –0.29	ns, Min
T _{CINCK} /T _{CKCIN}	CIN input to CLK on A – D flip-flops	0.31/ –0.17	0.31/ –0.13	0.31/ –0.13	0.81/ –0.42	ns, Min
Set/Reset						
T _{RPW}	SR input minimum pulse width	0.41	0.48	0.48	1.37	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.60	0.70	0.70	0.88	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.60	0.65	0.65	0.90	ns, Max
F _{TOG}	Toggle frequency (for export control)	862	806	667	500	MHz

DSP48A1 Switching Characteristics

Table 44: DSP48A1 Switching Characteristics

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-3	-3N	-2	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock									
T _{DSPDCK_A_A1REG} / T _{DSPCKD_A_A1REG}	A input to A1 register CLK	N/A	N/A	N/A	0.15/ 0.09	0.17/ 0.09	0.17/ 0.09	0.32/ 0.09	ns
T _{DSPDCK_D_B1REG} / T _{DSPCKD_D_B1REG}	D input to B1 register CLK	Yes	N/A	N/A	1.90/ −0.07	1.95/ −0.07	1.95/ −0.07	2.82/ −0.07	ns
T _{DSPDCK_C_CREG} / T _{DSPCKD_C_CREG}	C input to C register CLK for XC devices	N/A	N/A	N/A	0.11/ 0.15	0.13/ 0.15	0.13/ 0.15	0.24/ 0.09	ns
	C input to C register CLK for XA and XQ devices				0.11/ 0.19	N/A	0.13/ 0.23	0.24/ 0.09	
T _{DSPDCK_D_DREG} / T _{DSPCKD_D_DREG}	D input to D register CLK for XC devices	N/A	N/A	N/A	0.09/ 0.15	0.10/ 0.15	0.10/ 0.15	0.19/ 0.12	ns
	D input to D register CLK for XA and XQ devices				0.09/ 0.23	N/A	0.10/ 0.27	0.19/ 0.12	
T _{DSPDCK_OPMODE_B1REG} / T _{DSPCKD_OPMODE_B1REG}	OPMODE input to B1 register CLK	Yes	N/A	N/A	1.97/ 0.01	2.00/ 0.01	2.00/ 0.01	2.85/ 0.01	ns
T _{DSPDCK_OPMODE_OPMODEREG} / T _{DSPCKD_OPMODE_OPMODEREG}	OPMODE input to OPMODE register CLK for XC devices	N/A	N/A	N/A	0.18/ 0.12	0.21/ 0.12	0.21/ 0.12	0.40/ 0.12	ns
	OPMODE input to OPMODE register CLK for XA and XQ devices				0.18/ 0.16	N/A	0.21/ 0.22	0.40/ 0.12	
Setup and Hold Times of Data Pins to the Pipeline Register Clock									
T _{DSPDCK_A_MREG} / T _{DSPCKD_A_MREG}	A input to M register CLK	N/A	Yes	N/A	3.06/ −0.40	3.51/ −0.40	3.51/ −0.40	3.97/ −0.40	ns
T _{DSPDCK_B_MREG} / T _{DSPCKD_B_MREG}	B input to M register CLK	Yes	Yes	N/A	3.96/ −0.68	4.58/ −0.68	4.58/ −0.68	7.00/ −0.68	ns
T _{DSPDCK_D_MREG} / T _{DSPCKD_D_MREG}	D input to M register CLK	Yes	Yes	N/A	4.23/ −0.56	4.80/ −0.56	4.80/ −0.56	6.84/ −0.56	ns
T _{DSPDCK_OPMODE_MREG} / T _{DSPCKD_OPMODE_MREG}	OPMODE to M register CLK	Yes	Yes	N/A	4.18/ −0.48	4.80/ −0.48	4.80/ −0.48	6.88/ −0.48	ns
		No	Yes	N/A	2.37/ −0.48	2.70/ −0.48	2.70/ −0.48	4.28/ −0.48	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock									
T _{DSPDCK_A_PREG} / T _{DSPCKD_A_PREG}	A input to P register CLK	N/A	Yes	Yes	4.32/ −0.76	5.06/ −0.76	5.06/ −0.76	7.52/ −0.76	ns
T _{DSPDCK_B_PREG} / T _{DSPCKD_B_PREG}	B input to P register CLK	Yes	Yes	Yes	5.87/ −0.59	6.87/ −0.59	6.87/ −0.59	10.55/ −0.59	ns
		No	Yes	Yes	4.14/ −0.93	4.68/ −0.93	4.68/ −0.93	8.12/ −0.93	ns
T _{DSPDCK_C_PREG} / T _{DSPCKD_C_PREG}	C input to P register CLK	N/A	N/A	Yes	2.20/ −0.23	2.25/ −0.23	2.25/ −0.23	3.27/ −0.23	ns
T _{DSPDCK_D_PREG} / T _{DSPCKD_D_PREG}	D input to P register CLK	Yes	Yes	Yes	5.90/ −0.92	6.91/ −0.92	6.91/ −0.92	10.39/ −0.92	ns

Table 44: DSP48A1 Switching Characteristics (Cont'd)

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-3	-3N	-2	-1L	
T _{DSPDCK_OPMODE_PREG} / T _{DSPCKD_OPMODE_PREG}	OPMODE input to P register CLK	Yes	Yes	Yes	6.21/ −0.84	7.27/ −0.84	7.27/ −0.84	10.43/ −0.84	ns
		No	Yes	Yes	1.69/ −0.87	1.98/ −0.87	1.98/ −0.87	3.62/ −0.87	ns
		No	No	Yes	2.09/ −0.22	2.30/ −0.22	2.30/ −0.22	3.79/ −0.22	ns
Clock to Out from Output Register Clock to Output Pin									
T _{DSPCKO_P_PREG}	CLK (PREG) to P output	N/A	N/A	N/A	1.20	1.34	1.34	1.90	ns
Clock to Out from Pipeline Register Clock to Output Pins									
T _{DSPCKO_P_MREG}	CLK (MREG) to P output	N/A	N/A	Yes	3.38	3.95	3.95	5.83	ns
Clock to Out from Input Register Clock to Output Pins									
T _{DSPCKO_P_A1REG}	CLK (A1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.65	ns
T _{DSPCKO_P_B1REG}	CLK (B1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.63	ns
T _{DSPCKO_P_CREG}	CLK (CREG) to P output	N/A	N/A	Yes	3.12	3.64	3.64	5.24	ns
T _{DSPCKO_P_DREG}	CLK (DREG) to P output	Yes	Yes	Yes	6.77	7.92	7.92	12.53	ns
Combinatorial Delays from Input Pins to Output Pins									
T _{DSPDO_A_P}	A input to P output	N/A	No	Yes	2.85	3.33	3.33	4.73	ns
		N/A	Yes	No ⁽²⁾	3.35	3.93	3.93	6.74	ns
		N/A	Yes	Yes	4.56	5.22	5.22	8.94	ns
T _{DSPDO_B_P}	B input to P output	Yes	No	No ⁽²⁾	3.22	3.76	3.76	5.55	ns
		Yes	Yes	No ⁽²⁾	6.01	6.54	6.54	9.76	ns
		Yes	Yes	Yes	6.27	7.34	7.34	11.96	ns
T _{DSPDO_C_P}	C input to P output	N/A	N/A	Yes	2.69	3.15	3.15	4.68	ns
T _{DSPDO_D_P}	D input to P output	Yes	Yes	Yes	6.31	7.38	7.38	11.81	ns
T _{DSPDO_OPMODE_P}	OPMODE input to P output	Yes	Yes	Yes	6.43	7.52	7.52	11.84	ns
		No	Yes	Yes	4.84	5.66	5.66	9.25	ns
		No	No	Yes	3.11	3.49	3.49	5.03	ns
Maximum Frequency									
F _{MAX}	All registers used	Yes	Yes	Yes	390	333	333	213	MHz

Notes:

1. A Yes signifies that the component is in the path. A No signifies that the component is being bypassed. N/A signifies not applicable because no path exists.
2. Implemented in the post-adder by adding to zero.

Table 47: Configuration Switching Characteristics⁽¹⁾ (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
BPI Master Flash Mode Programming Switching ⁽⁴⁾						
T _{BPICCO} ⁽⁵⁾	A[25:0], FCS_B, FOE_B, FWE_B, LDC outputs valid after CCLK falling edge	15	15	15	20	ns, Max
T _{BPIICK}	Master BPI CCLK (output) delay	10/100	10/100	10/100	10/130	μs, Min/Max
T _{BPIDCC} /T _{BPICCD}	Setup/Hold on D[15:0] data input pins	5.0/1.0	5.0/1.0	5.0/1.0	6.0/2.0	ns, Min
SPI Master Flash Mode Programming Switching ⁽⁶⁾						
T _{SPIDCC} /T _{SPIDCCD}	DIN, MISO0, MISO1, MISO2, MISO3, Setup/Hold before/after the rising CCLK edge	5.0/1.0	5.0/1.0	5.0/1.0	7.0/1.0	ns, Min
T _{SPIICK}	Master SPI CCLK (output) delay	0.4/7.0	0.4/7.0	0.4/7.0	0.4/10.0	μs, Min/Max
T _{SPICCM}	MOSI clock to out	13	13	13	19	ns, Max
T _{SPICCF}	CSO_B clock to out	16	16	16	26	ns, Max
CCLK Output (Master Modes)						
T _{MCCKL}	Master CCLK clock duty cycle Low	40/60				%, Min/Max
T _{MCCKH}	Master CCLK clock duty cycle High	40/60				%, Min/Max
F _{MCCK}	Maximum frequency, serial mode (Master Serial/SPI) All devices	40	40	40	30	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T	40	40	40	25	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x8 mode, LX150, and LX150T	40	40	40	20	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x16 mode	35	35	35	20	MHz, Max
F _{MCCKTOL}	Frequency Tolerance, master mode	±50	±50	±50	±50	%
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time	5	5	5	8	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time	5	5	5	8	ns, Min
USERCCLK Input						
T _{USERCCKL}	USERCCLK clock minimum Low time	12	12	12	16	ns, Min
T _{USERCCKH}	USERCCLK clock minimum High time	12	12	12	16	ns, Min
F _{USERCCLK}	Maximum USERCCLK frequency	40	40	40	30	MHz, Max

Notes:

- Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
- To support longer delays in configuration, use the design solutions described in [UG380: Spartan-6 FPGA Configuration User Guide](#).
- [Table 6](#) specifies the power supply ramp time.
- BPI mode is not supported in:
 - LX4, LX25, or LX25T devices
 - LX9 devices in the TQG144 package
 - LX9 or LX16 devices in the CPG196 package.
- Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
- Defense-grade Spartan-6Q -2Q devices configure in single default SPI Master (x1) mode at $T_j = -55^{\circ}\text{C}$. During operation and when using all other configuration functions, the minimum operating temperature is -40°C .

DCM Switching Characteristics

Table 53: Operating Frequency Ranges and Conditions for the Delay-Locked Loop (DLL)⁽¹⁾

Symbol	Description	Speed Grade								Units	
		-3		-3N		-2		-1L			
		Min	Max	Min	Max	Min	Max	Min	Max		
Input Frequency Ranges											
CLKIN_FREQ_DLL	Frequency of the CLKIN clock input when the CLKDV output is not used.	5 ⁽²⁾	280 ⁽³⁾	5 ⁽²⁾	280 ⁽³⁾	5 ⁽²⁾	250 ⁽³⁾	5 ⁽²⁾	175 ⁽³⁾	MHz	
	Frequency of the CLKIN clock input when using the CLKDV output.	5 ⁽²⁾	280 ⁽³⁾	5 ⁽²⁾	280 ⁽³⁾	5 ⁽²⁾	250 ⁽³⁾	5 ⁽²⁾	133 ⁽³⁾	MHz	
Input Pulse Requirements											
CLKIN_PULSE	CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL < 150 MHz	40	60	40	60	40	60	40	60	%	
	CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL > 150 MHz	45	55	45	55	45	55	45	55	%	
Input Clock Jitter Tolerance and Delay Path Variation ⁽⁴⁾											
CLKIN_CYC_JITT_DLL_LF	Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL < 150 MHz	–	±300	–	±300	–	±300	–	±300	ps	
CLKIN_CYC_JITT_DLL_HF	Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL > 150 MHz.	–	±150	–	±150	–	±150	–	±150	ps	
CLKIN_PER_JITT_DLL	Period jitter at the CLKIN input.	–	±1	–	±1	–	±1	–	±1	ns	
CLKFB_DELAY_VAR_EXT	Allowable variation of the off-chip feedback delay from the DCM output to the CLKFB input.	–	±1	–	±1	–	±1	–	±1	ns	

Notes:

- DLL specifications apply when using any of the DLL outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV.
- When operating independently of the DLL, the DFS supports lower CLKIN_FREQ_DLL frequencies. See Table 55.
- The CLKIN_DIVIDE_BY_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the F_{MAX} (see Table 48 and Table 49 for BUFG and BUFGIO2 limits). When used with CLK_FEEDBACK=2X, the input clock frequency matches the frequency for CLK2X, and is limited to CLKOUT_FREQ_2X.
- CLKIN_FREQ_DLL input jitter beyond these limits can cause the DCM to lose LOCK, indicated by the LOCKED output deasserting. The user must then reset the DCM.
- When using both DCMs in a CMT, both DCMs must be LOCKED.

Table 54: Switching Characteristics for the Delay-Locked Loop (DLL)⁽¹⁾

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges										
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs.	5	280	5	280	5	250	5	175	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs.	5	200	5	200	5	200	5	175	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs.	10	375	10	375	10	334	10	250	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output.	0.3125	186	0.3125	186	0.3125	166	0.3125	88.6	MHz
Output Clock Jitter ⁽²⁾⁽³⁾⁽⁴⁾										
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output.	–	±100	–	±100	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs.	Maximum = ±[0.5% of CLKIN period + 100]								ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division.	Maximum = ±[0.5% of CLKIN period + 100]								ps
Duty Cycle ⁽⁴⁾										
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion.	Typical = ±[1% of CLKIN period + 350]								ps
Phase Alignment ⁽⁴⁾										
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 1X).	–	±150	–	±150	–	±150	–	±250	ps
	Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 2X). ⁽⁶⁾	–	±250	–	±250	–	±250	–	±350	
CLKOUT_PHASE_DLL	Phase offset between DLL outputs for CLK0 to CLK2X (not CLK2X180).	Maximum = ±[1% of CLKIN period + 100]								ps
	Phase offset between DLL outputs for all others.	Maximum = ±[1% of CLKIN period + 150]						Maximum = ±[1% of CLKIN period + 200]		ps

Table 57: Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)⁽¹⁾

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges (DCM_CLKGEN)										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz
CLKOUT_FREQ_FXDV	Frequency for the CLKFXDV output	0.15625	187.5	0.15625	187.5	0.15625	166.5	0.15625	100	MHz
Output Clock Jitter ⁽²⁾⁽³⁾										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKOUT_PER_JITT_FXDV	Period jitter at the CLKFXDV output.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKFX_FREEZE_VAR	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX > 50 MHz	Maximum = ±3% of CLKFX period								ps
	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX < 50 MHz	Maximum = ±5% of CLKFX period								ps
CLKFX_FREEZE_TEMP_SLOPE	CLKFX period will change in free_oscillator mode over temperature. Add to CLKFX_FREEZE_VAR to determine total CLKFX period change. Percentage change for CLKFX period over 1°C.	Maximum = 0.1								%/°C
Duty Cycle ⁽⁴⁾⁽⁵⁾										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
CLKOUT_DUTY_CYCLE_FXDV	Duty cycle precision for the CLKFXDV outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
Lock Time										
LOCK_FX ⁽²⁾	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX, CLKFX180, and CLKFXDV signals are valid. Lock time requires CLKFX_DIVIDE < F _{IN} /(0.50 MHz) when: F _{CLKIN} < 50 MHz	—	50	—	50	—	50	—	50	ms
	when: F _{CLKIN} > 50 MHz	—	5	—	5	—	5	—	5	ms

Table 67: Global Clock Input to Output Delay With PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> PLL in Source-Synchronous Mode.							
T _{ICKOFFLL_0}	Global Clock and OUTFF <i>with</i> PLL	XC6SLX4	5.49	N/A	7.44	8.55	ns
		XC6SLX9	5.49	6.29	7.44	8.55	ns
		XC6SLX16	5.23	5.77	6.79	8.21	ns
		XC6SLX25	5.00	5.35	6.10	8.54	ns
		XC6SLX25T	5.00	5.35	6.10	N/A	ns
		XC6SLX45	5.59	6.03	7.02	8.39	ns
		XC6SLX45T	5.59	6.03	7.02	N/A	ns
		XC6SLX75	4.96	5.41	6.22	8.32	ns
		XC6SLX75T	4.96	5.41	6.22	N/A	ns
		XC6SLX100	4.97	5.42	6.21	9.08	ns
		XC6SLX100T	5.01	5.42	6.21	N/A	ns
		XC6SLX150	4.59	5.06	5.86	8.13	ns
		XC6SLX150T	4.59	5.06	5.86	N/A	ns
		XA6SLX4	5.79	N/A	7.32	N/A	ns
		XA6SLX9	5.79	N/A	7.32	N/A	ns
		XA6SLX16	5.56	N/A	6.66	N/A	ns
		XA6SLX25	5.40	N/A	5.97	N/A	ns
		XA6SLX25T	5.40	N/A	6.07	N/A	ns
		XA6SLX45	5.89	N/A	6.90	N/A	ns
		XA6SLX45T	5.89	N/A	6.90	N/A	ns
		XA6SLX75	5.27	N/A	6.12	N/A	ns
		XA6SLX75T	5.27	N/A	6.12	N/A	ns
		XA6SLX100	N/A	N/A	6.80	N/A	ns
		XQ6SLX75	N/A	N/A	6.12	8.32	ns
		XQ6SLX75T	5.27	N/A	6.12	N/A	ns
		XQ6SLX150	N/A	N/A	5.88	8.13	ns
		XQ6SLX150T	5.21	N/A	5.88	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 72: Global Clock Setup and Hold With DCM in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard. ⁽¹⁾							
T _{PSDCM} / T _{PHDCM}	No Delay Global Clock and IFF ⁽²⁾ with DCM in System-Synchronous Mode	XC6SLX4	1.54/0.06	N/A	1.75/0.12	2.84/0.27	ns
		XC6SLX9	1.54/0.06	1.63/0.12	1.75/0.12	2.84/0.27	ns
		XC6SLX16	1.72/−0.18	1.87/−0.17	2.13/−0.17	2.31/0.26	ns
		XC6SLX25	1.70/−0.03	1.78/−0.02	2.00/−0.02	2.88/0.20	ns
		XC6SLX25T	1.70/0.07	1.78/0.08	2.00/0.08	N/A	ns
		XC6SLX45	1.74/−0.03	1.84/−0.02	2.02/−0.02	2.64/0.52	ns
		XC6SLX45T	1.74/−0.01	1.84/0.00	2.02/0.00	N/A	ns
		XC6SLX75	1.86/0.11	1.98/0.12	2.20/0.12	2.96/0.58	ns
		XC6SLX75T	1.86/0.11	1.98/0.12	2.20/0.12	N/A	ns
		XC6SLX100	1.64/0.07	1.72/0.08	1.97/0.08	2.70/0.99	ns
		XC6SLX100T	1.64/0.09	1.72/0.10	1.97/0.10	N/A	ns
		XC6SLX150	1.53/0.39	1.62/0.40	1.82/0.40	2.75/1.00	ns
		XC6SLX150T	1.53/0.39	1.62/0.40	1.82/0.40	N/A	ns
		XA6SLX4	1.65/0.16	N/A	1.75/0.26	N/A	ns
		XA6SLX9	1.65/0.16	N/A	1.75/0.26	N/A	ns
		XA6SLX16	1.88/0.02	N/A	2.13/0.03	N/A	ns
		XA6SLX25	1.80/0.16	N/A	2.05/0.17	N/A	ns
		XA6SLX25T	1.80/0.16	N/A	2.13/0.17	N/A	ns
		XA6SLX45	1.75/0.12	N/A	2.02/0.13	N/A	ns
		XA6SLX45T	1.75/0.12	N/A	2.02/0.13	N/A	ns
		XA6SLX75	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XA6SLX75T	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XA6SLX100	N/A	N/A	2.46/0.24	N/A	ns
		XQ6SLX75	N/A	N/A	2.20/0.12	2.96/0.58	ns
		XQ6SLX75T	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XQ6SLX150	N/A	N/A	1.82/0.56	2.75/1.00	ns
		XQ6SLX150T	1.65/0.55	N/A	1.82/0.56	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 77: Global Clock Setup and Hold With DCM and PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Example Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin, ⁽¹⁾ Using DCM, PLL, and Global Clock Buffer for the LVCMOS25 standard.							
T _{PSDCMPLL_0} / T _{PHDCMPLL_0}	No Delay Global Clock and IFF ⁽²⁾ with DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode.	XC6SLX4	0.43/1.07	N/A	0.43/1.43	1.10/1.67	ns
		XC6SLX9	0.43/1.03	0.45/1.14	0.45/1.43	1.10/1.67	ns
		XC6SLX16	0.74/0.93	0.74/1.12	0.74/1.21	0.77/1.35	ns
		XC6SLX25	0.67/1.02	0.76/1.11	0.84/1.18	1.23/1.46	ns
		XC6SLX25T	0.67/1.02	0.76/1.11	0.84/1.18	N/A	ns
		XC6SLX45	0.65/0.99	0.65/1.04	0.71/1.12	1.18/1.58	ns
		XC6SLX45T	0.65/1.00	0.65/1.04	0.71/1.12	N/A	ns
		XC6SLX75	0.86/1.01	0.88/1.06	0.94/1.14	1.29/1.67	ns
		XC6SLX75T	0.86/1.01	0.88/1.06	0.94/1.14	N/A	ns
		XC6SLX100	0.50/1.10	0.56/1.10	0.61/1.17	0.84/2.24	ns
		XC6SLX100T	0.50/1.10	0.56/1.10	0.61/1.17	N/A	ns
		XC6SLX150	0.45/1.28	0.47/1.28	0.52/1.28	1.27/1.56	ns
		XC6SLX150T	0.45/1.28	0.47/1.28	0.52/1.28	N/A	ns
		XA6SLX4	0.74/1.00	N/A	0.74/1.43	N/A	ns
		XA6SLX9	0.74/1.00	N/A	0.74/1.43	N/A	ns
		XA6SLX16	1.81/1.15	N/A	1.81/1.03	N/A	ns
		XA6SLX25	0.89/1.01	N/A	0.96/1.05	N/A	ns
		XA6SLX25T	0.89/1.01	N/A	1.04/1.15	N/A	ns
		XA6SLX45	0.69/0.95	N/A	0.83/0.96	N/A	ns
		XA6SLX45T	0.69/0.95	N/A	0.83/0.96	N/A	ns
		XA6SLX75	0.88/0.94	N/A	1.06/0.96	N/A	ns
		XA6SLX75T	0.88/0.94	N/A	1.06/0.96	N/A	ns
		XA6SLX100	N/A	N/A	1.55/1.33	N/A	ns
		XQ6SLX75	N/A	N/A	1.06/0.96	1.29/1.67	ns
		XQ6SLX75T	0.88/0.94	N/A	1.06/0.96	N/A	ns
		XQ6SLX150	N/A	N/A	0.64/1.30	1.27/1.56	ns
		XQ6SLX150T	0.58/1.30	N/A	0.64/1.30	N/A	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG. Package skew is not included in these measurements.
- IFF = Input Flip-Flop

Date	Version	Description of Revisions
06/14/10	1.5	In Table 2, added note 5 and added temperature range to V_{FS} and R_{FUSE}. Removed speed grade delineation, revised I_{RPD} description, and updated note 2 in Table 4. Added note 2 to Table 7. Added $DIFF_MOBILE_DDR$ to Table 8 and Table 10. Added note 4 to Table 15. Changed minimum DV_{PPIN} in Table 16. Updated $F_{GTPDRCLK}$ in Table 19. Increased maximum T_{LLSKEW} in Table 22. Updated descriptions and added data to Table 23. Removed note 1 and added new data to the Networking Applications section in Table 25. Updated Table 26 and Table 27 to the data in ISE v12.1 software with speed specification v1.08. In Table 28, added $DIFF_MOBILE_DDR$ and updated -4 speed grade data. Updated the maximum I/O pairs per bank in Table 33. Updated note 2 on Table 39. Revised the F_{MAX} in Table 44. In Table 47, updated description for $T_{SMCKCSO}$, revised values for T_{POR} and added Min value, added $T_{BPIICCK}$ and $T_{SPIICCK}$. Also in Table 47, added device dependencies to F_{SMCKCK} and F_{RBCKCK}. Updated and added data to Table 63 through Table 78, and Table 81. In Table 79, added data on the XC6SLX45-FG(G)676 and revised the XC6SLX45T and XC6SLX150T values. The following changes to this specification are addressed in the product change notice XC6SLX45-FG(G)676, <i>MCB Performance and JTAG Revision Code for Spartan-6 LX16 and LX45 FPGAs</i>. In Table 2, revised the V_{CCINT} to add the memory controller block extended performance specifications. In Table 25, changed the standard specifications and added extended performance specifications for the memory controller block and note 2. Added note 4 and updated values in Table 34.
06/24/10	1.6	Production release of XC6SLX45T (-2 and -3 speed grades), XC6SLX16 and XC6SLX45 (-3 speed grade) devices which includes changes to Table 26 and Table 27 (ISE v12.1 software with speed specification v1.08). Added the -3N speed grade, which designates Spartan-6 devices that do not support MCB functionality. This includes changes to Table 2 (note 2), Table 25 (note 4), and Switching Characteristics (Table 26). Updated Simultaneously Switching Outputs discussion. Added -3 speed grade values for T_{TAP} and F_{MINCAL} values in Table 39. In Table 40, updated T_{RPW} (-2 and -3 speed grade) values and F_{TOG} (-3 speed grade) values. In Table 48, updated T_{GIO} (-2 and -3 speed grade) values. Updated -3 values in spread spectrum section of Table 57.
07/16/10	1.7	Production release of specific devices listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 4 advising designers of the patch which contains v1.11. Also updated the -1L speed specification to v1.04. Updated numerous -4 and -1L values. Added -4 T_{TAP} values and F_{MINCAL} to Table 39. Revised T_{CINCK}/T_{CKCIN} in Table 40. In Table 41, revised T_{SHCKO}. In Table 42, revised T_{REQ}. Added new -1L values to Table 47. Added and updated values in Table 79.
07/26/10	1.8	Production release of XC6SLX25, XC6SLX25T, XC6SLX100 and XC6SLX100T in the specific speed grades listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 7 to Table 2 and moved V_{FS} and R_{FUSE} to a new Table 3. Added I_{HS} and note 4 to Table 4. Added note 1 to Table 28. Added and updated SSO limits per V_{CCO}/GND pairs in Table 34. Added note 3 to Table 47. In Table 54, removed -1L specifications for $CLKOUT_PER_JITT_DV1/2$ and revised $CLKIN_CLKFB_PHASE$ and $CLKOUT_PHASE_DLL$ values. Updated note 3 in both Table 56 and Table 57.
08/23/10	1.9	Updated values for $F_{GTPRANGE1}$, $F_{GTPRANGE2}$, and $F_{GPLLMIN}$ in Table 18. Revised -3 and -4 values in Table 21. Removed the -1L speed grade readback support restriction and note 3 in Table 47.
11/05/10	1.10	Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.3 software with speed specification v1.12 for the -2 speed grade available in the 12.3 <i>Speed Files Patch</i>. Added note 3 advising designers of the patch which contains v1.12. In Table 2, added note 4. In Table 4, added note 2. In Table 10, added notes 2 and 3. In Table 44, added note 2. In Table 47, updated symbol for $T_{SMWCKCK}/T_{SMCKCKW}$, changed -1L values for $T_{USERCCLKH}$ and $T_{USERCCLKL}$, and added and revised the modes for F_{MCKCK} and F_{SMCKCK}. In Table 53, redefined and expanded description for $CLKIN_FREQ_DLL$ and rewrote note 3. Updated title of Table 58. Also in Table 78, revised T_{DCD_CLK} for XC6SLX150 and XC6SLX150T. Changed description of T_{PSFD}/T_{PHFD} in Table 71. For the -1L speed grade, updated data sheet to ISE 12.3 software with speed specification v1.05 which revised the values in the following tables: Table 25, Table 28, Table 35, Table 36, Table 37, Table 40 through Table 43, Table 48 through Table 56, Table 62 through Table 78, Table 80, and Table 81. Updated Notice of Disclaimer.

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