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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	3411
Number of Logic Elements/Cells	43661
Total RAM Bits	2138112
Number of I/O	320
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA, CSPBGA
Supplier Device Package	484-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx45-2csg484c

Table 17: GTP Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	200	800	2000	mV
R_{IN}	Differential input resistance	80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult [UG386](#): *Spartan-6 FPGA GTP Transceivers User Guide* for further information.

Table 18: GTP Transceiver Performance

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
F_{GTPMAX}	Maximum GTP transceiver data rate	3.2	3.2	2.7	N/A	Gb/s
$F_{GTPRANGE1}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 1	1.88 to 3.2	1.88 to 3.2	1.88 to 2.7	N/A	Gb/s
$F_{GTPRANGE2}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 2	0.94 to 1.62	0.94 to 1.62	0.94 to 1.62	N/A	Gb/s
$F_{GTPRANGE3}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 4	0.6 to 0.81	0.6 to 0.81	0.6 to 0.81	N/A	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	1.62	1.62	1.62	N/A	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	0.94	0.94	0.94	N/A	GHz

Table 19: GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
$F_{GTPDRPCLK}$	GTP transceiver DCLK (DRP clock) maximum frequency	125	125	100	N/A	MHz

Table 20: GTP Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All LXT Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	160	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	μ s

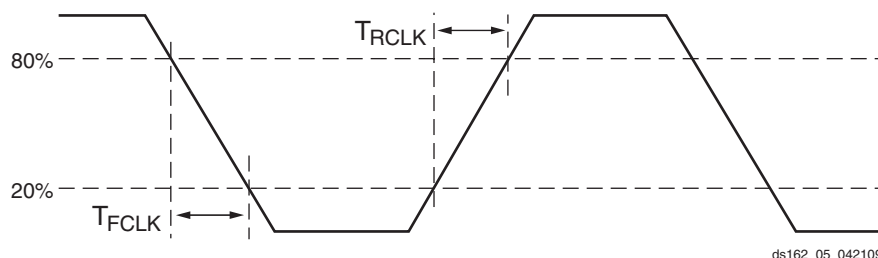


Figure 3: Reference Clock Timing Parameters

Table 23: GTP Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units	
T _{RXELECIDLE}	Time for RXELECIDLE to respond to loss or restoration of data		–	75	–	ns	
R _{XOOBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV	
R _{XSSST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	0	ppm	
R _{XRL}	Run length (CID)	Internal AC capacitor bypassed	–	–	150	UI	
R _{XPPMTOL}	Data/REFCLK PPM offset tolerance	CDR 2 nd -order loop disabled	–200	–	200	ppm	
		CDR 2 nd -order loop enabled	PLL_RXDIVSEL_OUT = 1	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 2	–2000	–	2000	ppm
		PLL_RXDIVSEL_OUT = 4	–1000	–	1000	ppm	
SJ Jitter Tolerance⁽²⁾							
JT_SJ _{3.125}	Sinusoidal Jitter ⁽³⁾	3.125 Gb/s	0.4	–	–	UI	
JT_SJ _{2.5}	Sinusoidal Jitter ⁽³⁾	2.5 Gb/s	0.4	–	–	UI	
JT_SJ _{1.62}	Sinusoidal Jitter ⁽³⁾	1.62 Gb/s	0.5	–	–	UI	
JT_SJ _{1.25}	Sinusoidal Jitter ⁽³⁾	1.25 Gb/s	0.5	–	–	UI	
JT_SJ ₆₁₄	Sinusoidal Jitter ⁽³⁾	614 Mb/s	0.5	–	–	UI	
SJ Jitter Tolerance with Stressed Eye⁽²⁾⁽⁵⁾							
JT_TJSE _{3.125}	Total Jitter with stressed eye ⁽⁴⁾	3.125 Gb/s	0.65	–	–	UI	
JT_SJSE _{3.125}	Sinusoidal Jitter with stressed eye	3.125 Gb/s	0.1	–	–	UI	
JT_TJSE _{2.7}	Total Jitter with stressed eye ⁽⁴⁾	2.7 Gb/s	0.65	–	–	UI	
JT_SJSE _{2.7}	Sinusoidal Jitter with stressed eye	2.7 Gb/s	0.1	–	–	UI	

Notes:

- Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
- All jitter values are based on a Bit Error Ratio of 1e⁻¹².
- Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
- Composed of 0.37 UI DJ in the form of ISI and 0.18 UI RJ.
- Measured using PRBS7 data pattern.

Endpoint Block for PCI Express Designs Switching Characteristics

The Endpoint block for PCI Express is available in the Spartan-6 LXT devices. Consult the [Spartan-6 FPGA Integrated Endpoint Block for PCI Express](#) for further information.

Table 24: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
F _{PCIEUSER}	User clock maximum frequency	62.5	62.5	62.5	N/A	MHz

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
PPDS_33	1.17	1.29	1.42	1.68	1.57	1.71	1.91	2.43	3000	3000	3000	3000	ns
PPDS_25	1.01	1.13	1.26	1.56	1.68	1.82	2.02	2.47	3000	3000	3000	3000	ns
PCI33_3	1.07	1.19	1.32	1.57 ⁽²⁾	3.51	3.65	3.85	4.38 ⁽²⁾	3.51	3.65	3.85	4.38 ⁽¹⁾	ns
PCI66_3	1.07	1.19	1.32	1.57 ⁽²⁾	3.53	3.67	3.87	4.39 ⁽²⁾	3.53	3.67	3.87	4.39 ⁽¹⁾	ns
DISPLAY_PORT	1.02	1.14	1.27	1.56	3.15	3.29	3.49	4.08	3.15	3.29	3.49	4.08	ns
I2C	1.33	1.45	1.58	1.82	11.56	11.70	11.90	12.52	11.56	11.70	11.90	12.52	ns
SMBUS	1.33	1.45	1.58	1.82	11.56	11.70	11.90	12.52	11.56	11.70	11.90	12.52	ns
SDIO	1.36	1.48	1.61	1.84	2.64	2.78	2.98	3.60	2.64	2.78	2.98	3.60	ns
MOBILE_DDR	0.94	1.06	1.19	1.43	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns
HSTL_I	0.90	1.02	1.15	1.39	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
HSTL_II	0.91	1.03	1.16	1.40	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
HSTL_III	0.95	1.07	1.20	1.44	1.67	1.81	2.01	2.61	1.67	1.81	2.01	2.61	ns
HSTL_I_18	0.94	1.06	1.19	1.43	1.77	1.91	2.11	2.73	1.77	1.91	2.11	2.73	ns
HSTL_II_18	0.94	1.06	1.19	1.43	1.85	1.99	2.19	2.81	1.85	1.99	2.19	2.81	ns
HSTL_III_18	0.99	1.11	1.24	1.47	1.79	1.93	2.13	2.72	1.79	1.93	2.13	2.72	ns
SSTL3_I	1.58	1.70	1.83	2.16	1.83	1.97	2.17	2.72	1.83	1.97	2.17	2.72	ns
SSTL3_II	1.58	1.70	1.83	2.16	2.01	2.15	2.35	2.94	2.01	2.15	2.35	2.94	ns
SSTL2_I	1.30	1.42	1.55	1.87	1.77	1.91	2.11	2.69	1.77	1.91	2.11	2.69	ns
SSTL2_II	1.30	1.42	1.55	1.88	1.86	2.00	2.20	2.82	1.86	2.00	2.20	2.82	ns
SSTL18_I	0.92	1.04	1.17	1.41	1.63	1.77	1.97	2.59	1.63	1.77	1.97	2.59	ns
SSTL18_II	0.92	1.04	1.17	1.41	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
SSTL15_II	0.92	1.04	1.17	1.41	1.67	1.81	2.01	2.63	1.67	1.81	2.01	2.63	ns
DIFF_HSTL_I	0.94	1.06	1.19	1.46	1.77	1.91	2.11	2.62	1.77	1.91	2.11	2.62	ns
DIFF_HSTL_II	0.93	1.05	1.18	1.45	1.72	1.86	2.06	2.54	1.72	1.86	2.06	2.54	ns
DIFF_HSTL_III	0.93	1.05	1.18	1.46	1.69	1.83	2.03	2.53	1.69	1.83	2.03	2.53	ns
DIFF_HSTL_I_18	0.97	1.09	1.22	1.50	1.79	1.93	2.13	2.63	1.79	1.93	2.13	2.63	ns
DIFF_HSTL_II_18	0.97	1.09	1.22	1.49	1.69	1.83	2.03	2.51	1.69	1.83	2.03	2.51	ns
DIFF_HSTL_III_18	0.97	1.09	1.22	1.50	1.69	1.83	2.03	2.53	1.69	1.83	2.03	2.53	ns
DIFF_SSTL3_I	1.18	1.30	1.43	1.68	1.81	1.95	2.15	2.64	1.81	1.95	2.15	2.64	ns
DIFF_SSTL3_II	1.19	1.31	1.44	1.68	1.80	1.94	2.14	2.63	1.80	1.94	2.14	2.63	ns
DIFF_SSTL2_I	1.02	1.14	1.27	1.57	1.80	1.94	2.14	2.62	1.80	1.94	2.14	2.62	ns
DIFF_SSTL2_II	1.02	1.14	1.27	1.57	1.76	1.90	2.10	2.57	1.76	1.90	2.10	2.57	ns
DIFF_SSTL18_I	0.97	1.09	1.22	1.51	1.72	1.86	2.06	2.56	1.72	1.86	2.06	2.56	ns
DIFF_SSTL18_II	0.98	1.10	1.23	1.50	1.68	1.82	2.02	2.52	1.68	1.82	2.02	2.52	ns
DIFF_SSTL15_II	0.94	1.06	1.19	1.46	1.67	1.81	2.01	2.50	1.67	1.81	2.01	2.50	ns
DIFF_MOBILE_DDR	0.97	1.09	1.22	1.51	1.75	1.89	2.09	2.57	1.75	1.89	2.09	2.57	ns

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVTTTL, QUIETIO, 2 mA	1.35	1.47	1.60	1.82	5.39	5.53	5.73	6.37	5.39	5.53	5.73	6.37	ns
LVTTTL, QUIETIO, 4 mA	1.35	1.47	1.60	1.82	4.29	4.43	4.63	5.22	4.29	4.43	4.63	5.22	ns
LVTTTL, QUIETIO, 6 mA	1.35	1.47	1.60	1.82	3.75	3.89	4.09	4.69	3.75	3.89	4.09	4.69	ns
LVTTTL, QUIETIO, 8 mA	1.35	1.47	1.60	1.82	3.23	3.37	3.57	4.20	3.23	3.37	3.57	4.20	ns
LVTTTL, QUIETIO, 12 mA	1.35	1.47	1.60	1.82	3.28	3.42	3.62	4.22	3.28	3.42	3.62	4.22	ns
LVTTTL, QUIETIO, 16 mA	1.35	1.47	1.60	1.82	2.94	3.08	3.28	3.92	2.94	3.08	3.28	3.92	ns
LVTTTL, QUIETIO, 24 mA	1.35	1.47	1.60	1.82	2.69	2.83	3.03	3.67	2.69	2.83	3.03	3.67	ns
LVTTTL, Slow, 2 mA	1.35	1.47	1.60	1.82	4.36	4.50	4.70	5.30	4.36	4.50	4.70	5.30	ns
LVTTTL, Slow, 4 mA	1.35	1.47	1.60	1.82	3.17	3.31	3.51	4.16	3.17	3.31	3.51	4.16	ns
LVTTTL, Slow, 6 mA	1.35	1.47	1.60	1.82	2.76	2.90	3.10	3.75	2.76	2.90	3.10	3.75	ns
LVTTTL, Slow, 8 mA	1.35	1.47	1.60	1.82	2.59	2.73	2.93	3.55	2.59	2.73	2.93	3.55	ns
LVTTTL, Slow, 12 mA	1.35	1.47	1.60	1.82	2.58	2.72	2.92	3.54	2.58	2.72	2.92	3.54	ns
LVTTTL, Slow, 16 mA	1.35	1.47	1.60	1.82	2.39	2.53	2.73	3.40	2.39	2.53	2.73	3.40	ns
LVTTTL, Slow, 24 mA	1.35	1.47	1.60	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVTTTL, Fast, 2 mA	1.35	1.47	1.60	1.82	3.78	3.92	4.12	4.74	3.78	3.92	4.12	4.74	ns
LVTTTL, Fast, 4 mA	1.35	1.47	1.60	1.82	2.49	2.63	2.83	3.45	2.49	2.63	2.83	3.45	ns
LVTTTL, Fast, 6 mA	1.35	1.47	1.60	1.82	2.44	2.58	2.78	3.40	2.44	2.58	2.78	3.40	ns
LVTTTL, Fast, 8 mA	1.35	1.47	1.60	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns
LVTTTL, Fast, 12 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTTL, Fast, 16 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTTL, Fast, 24 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVC MOS33, QUIETIO, 2 mA	1.34	1.46	1.59	1.82	5.40	5.54	5.74	6.37	5.40	5.54	5.74	6.37	ns
LVC MOS33, QUIETIO, 4 mA	1.34	1.46	1.59	1.82	4.03	4.17	4.37	5.01	4.03	4.17	4.37	5.01	ns
LVC MOS33, QUIETIO, 6 mA	1.34	1.46	1.59	1.82	3.51	3.65	3.85	4.47	3.51	3.65	3.85	4.47	ns
LVC MOS33, QUIETIO, 8 mA	1.34	1.46	1.59	1.82	3.37	3.51	3.71	4.33	3.37	3.51	3.71	4.33	ns
LVC MOS33, QUIETIO, 12 mA	1.34	1.46	1.59	1.82	2.94	3.08	3.28	3.93	2.94	3.08	3.28	3.93	ns
LVC MOS33, QUIETIO, 16 mA	1.34	1.46	1.59	1.82	2.77	2.91	3.11	3.78	2.77	2.91	3.11	3.78	ns
LVC MOS33, QUIETIO, 24 mA	1.34	1.46	1.59	1.82	2.59	2.73	2.93	3.58	2.59	2.73	2.93	3.58	ns
LVC MOS33, Slow, 2 mA	1.34	1.46	1.59	1.82	4.37	4.51	4.71	5.28	4.37	4.51	4.71	5.28	ns
LVC MOS33, Slow, 4 mA	1.34	1.46	1.59	1.82	2.98	3.12	3.32	3.94	2.98	3.12	3.32	3.94	ns
LVC MOS33, Slow, 6 mA	1.34	1.46	1.59	1.82	2.58	2.72	2.92	3.61	2.58	2.72	2.92	3.61	ns
LVC MOS33, Slow, 8 mA	1.34	1.46	1.59	1.82	2.65	2.79	2.99	3.61	2.65	2.79	2.99	3.61	ns
LVC MOS33, Slow, 12 mA	1.34	1.46	1.59	1.82	2.39	2.53	2.73	3.31	2.39	2.53	2.73	3.31	ns
LVC MOS33, Slow, 16 mA	1.34	1.46	1.59	1.82	2.31	2.45	2.65	3.27	2.31	2.45	2.65	3.27	ns
LVC MOS33, Slow, 24 mA	1.34	1.46	1.59	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVC MOS33, Fast, 2 mA	1.34	1.46	1.59	1.82	3.76	3.90	4.10	4.70	3.76	3.90	4.10	4.70	ns
LVC MOS33, Fast, 4 mA	1.34	1.46	1.59	1.82	2.48	2.62	2.82	3.44	2.48	2.62	2.82	3.44	ns
LVC MOS33, Fast, 6 mA	1.34	1.46	1.59	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVC MOS12, Fast, 2 mA	0.91	1.03	1.16	1.51	3.46	3.60	3.80	4.44	3.46	3.60	3.80	4.44	ns
LVC MOS12, Fast, 4 mA	0.91	1.03	1.16	1.51	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVC MOS12, Fast, 6 mA	0.91	1.03	1.16	1.51	1.79	1.93	2.13	2.75	1.79	1.93	2.13	2.75	ns
LVC MOS12, Fast, 8 mA	0.91	1.03	1.16	1.51	1.68	1.82	2.02	2.64	1.68	1.82	2.02	2.64	ns
LVC MOS12, Fast, 12 mA	0.91	1.03	1.16	1.51	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
LVC MOS12_JEDEC, QUIETIO, 2 mA	1.50	1.62	1.75	1.88	6.39	6.53	6.73	7.31	6.39	6.53	6.73	7.31	ns
LVC MOS12_JEDEC, QUIETIO, 4 mA	1.50	1.62	1.75	1.88	4.98	5.12	5.32	5.88	4.98	5.12	5.32	5.88	ns
LVC MOS12_JEDEC, QUIETIO, 6 mA	1.50	1.62	1.75	1.88	4.67	4.81	5.01	5.54	4.67	4.81	5.01	5.54	ns
LVC MOS12_JEDEC, QUIETIO, 8 mA	1.50	1.62	1.75	1.88	4.23	4.37	4.57	5.22	4.23	4.37	4.57	5.22	ns
LVC MOS12_JEDEC, QUIETIO, 12 mA	1.50	1.62	1.75	1.88	3.99	4.13	4.33	4.94	3.99	4.13	4.33	4.94	ns
LVC MOS12_JEDEC, Slow, 2 mA	1.50	1.62	1.75	1.88	5.00	5.14	5.34	5.90	5.00	5.14	5.34	5.90	ns
LVC MOS12_JEDEC, Slow, 4 mA	1.50	1.62	1.75	1.88	2.85	2.99	3.19	3.80	2.85	2.99	3.19	3.80	ns
LVC MOS12_JEDEC, Slow, 6 mA	1.50	1.62	1.75	1.88	2.76	2.90	3.10	3.72	2.76	2.90	3.10	3.72	ns
LVC MOS12_JEDEC, Slow, 8 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVC MOS12_JEDEC, Slow, 12 mA	1.50	1.62	1.75	1.88	2.09	2.23	2.43	3.05	2.09	2.23	2.43	3.05	ns
LVC MOS12_JEDEC, Fast, 2 mA	1.50	1.62	1.75	1.88	3.46	3.60	3.80	4.42	3.46	3.60	3.80	4.42	ns
LVC MOS12_JEDEC, Fast, 4 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns
LVC MOS12_JEDEC, Fast, 6 mA	1.50	1.62	1.75	1.88	1.79	1.93	2.13	2.76	1.79	1.93	2.13	2.76	ns
LVC MOS12_JEDEC, Fast, 8 mA	1.50	1.62	1.75	1.88	1.69	1.83	2.03	2.65	1.69	1.83	2.03	2.65	ns
LVC MOS12_JEDEC, Fast, 12 mA	1.50	1.62	1.75	1.88	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns

Notes:

1. The -1L values listed in this table are also applicable to the Spartan-6Q devices.
2. Devices with a -1L speed grade do not support Xilinx PCI IP.

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS15, QUIETIO, 2 mA	1.05	1.23	5.63	5.83	5.63	5.83	ns
LVC MOS15, QUIETIO, 4 mA	1.05	1.23	4.75	4.95	4.75	4.95	ns
LVC MOS15, QUIETIO, 6 mA	1.05	1.23	4.21	4.41	4.21	4.41	ns
LVC MOS15, QUIETIO, 8 mA	1.05	1.23	4.05	4.25	4.05	4.25	ns
LVC MOS15, QUIETIO, 12 mA	1.05	1.23	3.74	3.94	3.74	3.94	ns
LVC MOS15, QUIETIO, 16 mA	1.05	1.23	3.52	3.72	3.52	3.72	ns
LVC MOS15, Slow, 2 mA	1.05	1.23	4.32	4.52	4.32	4.52	ns
LVC MOS15, Slow, 4 mA	1.05	1.23	3.58	3.78	3.58	3.78	ns
LVC MOS15, Slow, 6 mA	1.05	1.23	2.45	2.65	2.45	2.65	ns
LVC MOS15, Slow, 8 mA	1.05	1.23	2.46	2.66	2.46	2.66	ns
LVC MOS15, Slow, 12 mA	1.05	1.23	2.17	2.37	2.17	2.37	ns
LVC MOS15, Slow, 16 mA	1.05	1.23	2.15	2.35	2.15	2.35	ns
LVC MOS15, Fast, 2 mA	1.05	1.23	3.43	3.63	3.43	3.63	ns
LVC MOS15, Fast, 4 mA	1.05	1.23	2.42	2.62	2.42	2.62	ns
LVC MOS15, Fast, 6 mA	1.05	1.23	1.92	2.12	1.92	2.12	ns
LVC MOS15, Fast, 8 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVC MOS15, Fast, 12 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVC MOS15, Fast, 16 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVC MOS15_JEDEC, QUIETIO, 2 mA	1.10	1.28	5.64	5.84	5.64	5.84	ns
LVC MOS15_JEDEC, QUIETIO, 4 mA	1.10	1.28	4.75	4.95	4.75	4.95	ns
LVC MOS15_JEDEC, QUIETIO, 6 mA	1.10	1.28	4.21	4.41	4.21	4.41	ns
LVC MOS15_JEDEC, QUIETIO, 8 mA	1.10	1.28	4.06	4.26	4.06	4.26	ns
LVC MOS15_JEDEC, QUIETIO, 12 mA	1.10	1.28	3.75	3.95	3.75	3.95	ns
LVC MOS15_JEDEC, QUIETIO, 16 mA	1.10	1.28	3.53	3.73	3.53	3.73	ns
LVC MOS15_JEDEC, Slow, 2 mA	1.10	1.28	4.32	4.52	4.32	4.52	ns
LVC MOS15_JEDEC, Slow, 4 mA	1.10	1.28	3.56	3.76	3.56	3.76	ns
LVC MOS15_JEDEC, Slow, 6 mA	1.10	1.28	2.44	2.64	2.44	2.64	ns
LVC MOS15_JEDEC, Slow, 8 mA	1.10	1.28	2.47	2.67	2.47	2.67	ns
LVC MOS15_JEDEC, Slow, 12 mA	1.10	1.28	2.15	2.35	2.15	2.35	ns
LVC MOS15_JEDEC, Slow, 16 mA	1.10	1.28	2.15	2.35	2.15	2.35	ns
LVC MOS15_JEDEC, Fast, 2 mA	1.10	1.28	3.43	3.63	3.43	3.63	ns
LVC MOS15_JEDEC, Fast, 4 mA	1.10	1.28	2.42	2.62	2.42	2.62	ns
LVC MOS15_JEDEC, Fast, 6 mA	1.10	1.28	1.92	2.12	1.92	2.12	ns
LVC MOS15_JEDEC, Fast, 8 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVC MOS15_JEDEC, Fast, 12 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVC MOS15_JEDEC, Fast, 16 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVC MOS12, QUIETIO, 2 mA	0.98	1.16	6.54	6.74	6.54	6.74	ns
LVC MOS12, QUIETIO, 4 mA	0.98	1.16	5.12	5.32	5.12	5.32	ns

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 4 and Figure 5.

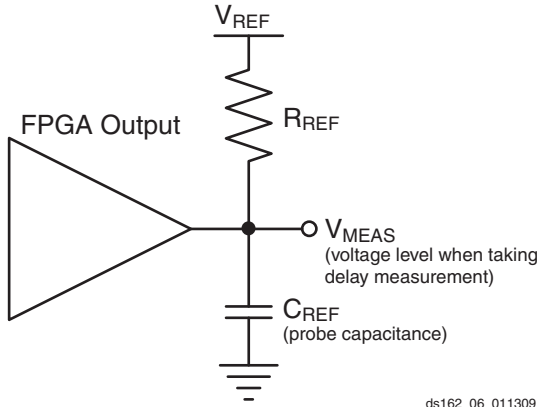
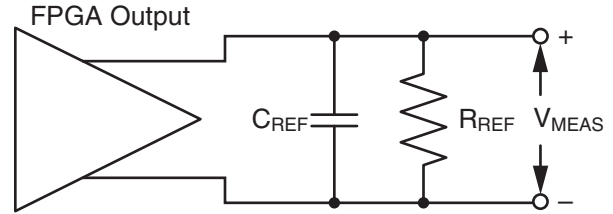


Figure 4: Single-Ended Test Setup



ds162_07_011309

Figure 5: Differential Test Setup

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 32.
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 32: Output Delay Measurement Methodology

Description	I/O Standard Attribute	R_{REF} (Ω)	$C_{REF}^{(1)}$ (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTTL (Low-Voltage Transistor-Transistor Logic)	LVTTTL (all)	1M	0	1.4	0
LVC MOS (Low-Voltage CMOS), 3.3V	LVC MOS33	1M	0	1.65	0
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS, 1.2V	LVC MOS12	1M	0	0.6	0
PCI (Peripheral Component Interface) 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3 (rising edge)	25	10 ⁽²⁾	0.94	0
	PCI33_3, PCI66_3 (falling edge)	25	10 ⁽²⁾	2.03	3.3
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25

Table 44: DSP48A1 Switching Characteristics (Cont'd)

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-3	-3N	-2	-1L	
T _{DSPDCK_OPMODE_PREG} / T _{DSPCKD_OPMODE_PREG}	OPMODE input to P register CLK	Yes	Yes	Yes	6.21/ -0.84	7.27/ -0.84	7.27/ -0.84	10.43/ -0.84	ns
		No	Yes	Yes	1.69/ -0.87	1.98/ -0.87	1.98/ -0.87	3.62/ -0.87	ns
		No	No	Yes	2.09/ -0.22	2.30/ -0.22	2.30/ -0.22	3.79/ -0.22	ns
Clock to Out from Output Register Clock to Output Pin									
T _{DSPCKO_P_PREG}	CLK (PREG) to P output	N/A	N/A	N/A	1.20	1.34	1.34	1.90	ns
Clock to Out from Pipeline Register Clock to Output Pins									
T _{DSPCKO_P_MREG}	CLK (MREG) to P output	N/A	N/A	Yes	3.38	3.95	3.95	5.83	ns
Clock to Out from Input Register Clock to Output Pins									
T _{DSPCKO_P_A1REG}	CLK (A1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.65	ns
T _{DSPCKO_P_B1REG}	CLK (B1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.63	ns
T _{DSPCKO_P_CREG}	CLK (CREG) to P output	N/A	N/A	Yes	3.12	3.64	3.64	5.24	ns
T _{DSPCKO_P_DREG}	CLK (DREG) to P output	Yes	Yes	Yes	6.77	7.92	7.92	12.53	ns
Combinatorial Delays from Input Pins to Output Pins									
T _{DSPDO_A_P}	A input to P output	N/A	No	Yes	2.85	3.33	3.33	4.73	ns
		N/A	Yes	No ⁽²⁾	3.35	3.93	3.93	6.74	ns
		N/A	Yes	Yes	4.56	5.22	5.22	8.94	ns
T _{DSPDO_B_P}	B input to P output	Yes	No	No ⁽²⁾	3.22	3.76	3.76	5.55	ns
		Yes	Yes	No ⁽²⁾	6.01	6.54	6.54	9.76	ns
		Yes	Yes	Yes	6.27	7.34	7.34	11.96	ns
T _{DSPDO_C_P}	C input to P output	N/A	N/A	Yes	2.69	3.15	3.15	4.68	ns
T _{DSPDO_D_P}	D input to P output	Yes	Yes	Yes	6.31	7.38	7.38	11.81	ns
T _{DSPDO_OPMODE_P}	OPMODE input to P output	Yes	Yes	Yes	6.43	7.52	7.52	11.84	ns
		No	Yes	Yes	4.84	5.66	5.66	9.25	ns
		No	No	Yes	3.11	3.49	3.49	5.03	ns
Maximum Frequency									
F _{MAX}	All registers used	Yes	Yes	Yes	390	333	333	213	MHz

Notes:

1. A Yes signifies that the component is in the path. A No signifies that the component is being bypassed. N/A signifies not applicable because no path exists.
2. Implemented in the post-adder by adding to zero.

Clock Buffers and Networks

Table 48: Global Clock Switching Characteristics (BUFGMUX)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{GSI}	S pin Setup to I0/I1 inputs	LX devices	0.25	0.31	0.48	0.48	ns
		LXT devices	0.25	0.31	0.48	N/A	ns
T _{GIO}	BUFGMUX delay from I0/I1 to O	LX devices	0.21	0.21	0.21	0.21	ns
		LXT devices	0.21	0.21	0.21	N/A	ns
Maximum Frequency							
F _{MAX}	Global clock tree (BUFGMUX)	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 49: Input/Output Clock Switching Characteristics (BUFIO2)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{BUFCO_O}	Clock to out delay from I to O	LX devices	0.67	0.82	1.09	1.50	ns
		LXT devices	0.67	0.82	1.09	N/A	ns
Maximum Frequency							
F _{MAX}	I/O clock tree (BUFIO2)	LX devices	540	525	500	300	MHz
		LXT devices	540	525	500	N/A	MHz

Table 50: Input/Output Clock Switching Characteristics (BUFIO2FB)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
Maximum Frequency							
F _{MAX}	I/O clock tree (BUFIO2FB)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

Table 51: Input/Output Clock Switching Characteristics (BUFPLL)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
Maximum Frequency							
F _{MAX}	BUFPLL clock tree (BUFPLL)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

PLL Switching Characteristics

Table 52: PLL Specification

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
F _{INMAX}	Maximum Input Clock Frequency from I/O Clock	LX devices	540	525	450	300	MHz
		LXT devices	540	525	450	N/A	MHz
	Maximum Input Clock Frequency from Global Clock	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 54: Switching Characteristics for the Delay-Locked Loop (DLL)⁽¹⁾

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges										
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs.	5	280	5	280	5	250	5	175	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs.	5	200	5	200	5	200	5	175	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs.	10	375	10	375	10	334	10	250	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output.	0.3125	186	0.3125	186	0.3125	166	0.3125	88.6	MHz
Output Clock Jitter⁽²⁾⁽³⁾⁽⁴⁾										
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output.	–	±100	–	±100	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs.	Maximum = ±[0.5% of CLKIN period + 100]								ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division.	Maximum = ±[0.5% of CLKIN period + 100]								ps
Duty Cycle⁽⁴⁾										
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion.	Typical = ±[1% of CLKIN period + 350]								ps
Phase Alignment⁽⁴⁾										
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 1X).	–	±150	–	±150	–	±150	–	±250	ps
	Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 2X). ⁽⁶⁾	–	±250	–	±250	–	±250	–	±350	
CLKOUT_PHASE_DLL	Phase offset between DLL outputs for CLK0 to CLK2X (not CLK2X180).	Maximum = ±[1% of CLKIN period + 100]								ps
	Phase offset between DLL outputs for all others.	Maximum = ±[1% of CLKIN period + 150]						Maximum = ±[1% of CLKIN period + 200]		ps

Table 54: Switching Characteristics for the Delay-Locked Loop (DLL)⁽¹⁾ (Cont'd)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
LOCK_DLL ⁽³⁾	When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. CLKIN_FREQ_DLL < 50 MHz.	-	5	-	5	-	5	-	5	ms
	When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. CLKIN_FREQ_DLL > 50 MHz.	-	0.60	-	0.60	-	0.60	-	0.60	ms
Delay Lines										
DCM_DELAY_STEP ⁽⁵⁾	Finest delay resolution, averaged over all steps.	10	40	10	40	10	40	10	40	ps

Notes:

1. The values in this table are based on the operating conditions described in Table 2 and Table 53.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster LOCK time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, this data sheet specifies a maximum jitter of ±(1% of CLKIN period + 150 ps). Assuming that the CLKIN frequency is 100 MHz, the equivalent CLKIN period is 10 ns. Since 1% of 10 ns is 0.1 ns or 100 ps, the maximum jitter is ±(100 ps + 150 ps) = ±250 ps.
5. A typical delay step size is 23 ps.
6. The timing analysis tools use the CLK_FEEDBACK = 1X condition for the CLKIN_CLKFB_PHASE value (reported as phase error). When using CLK_FEEDBACK = 2X, add 100 ps to the phase error for the CLKIN_CLKFB_PHASE value (as shown in this table).

Table 55: Recommended Operating Conditions for the Digital Frequency Synthesizer (DFS)⁽¹⁾

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Input Frequency Ranges⁽²⁾										
CLKIN_FREQ_FX	Frequency for the CLKIN input. Also described as F _{CLKIN} .	0.5	375 ⁽³⁾	0.5	375 ⁽³⁾	0.5	333 ⁽³⁾	0.5	200 ⁽³⁾	MHz
Input Clock Jitter Tolerance⁽⁴⁾										
CLKIN_CYC_JITT_FX_LF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: F _{CLKFX} < 150 MHz.	-	±300	-	±300	-	±300	-	±300	ps
CLKIN_CYC_JITT_FX_HF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: F _{CLKFX} > 150 MHz.	-	±150	-	±150	-	±150	-	±150	ps
CLKIN_PER_JITT_FX	Period jitter at the CLKIN input.	-	±1	-	±1	-	±1	-	±1	ns

Notes:

1. DFS specifications apply when using either of the DFS outputs (CLKFX or CLKFX180).
2. When using both DFS and DLL outputs on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 53.
3. The CLKIN_DIVIDE_BY_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the F_{MAX} (see Table 48 and Table 49 for BUFIO2 and BUFG2 limits).
4. CLKIN input jitter beyond these limits can cause the DCM to lose LOCK.

Table 59: Switching Characteristics for the Phase-Shift Clock in Variable Phase Mode⁽¹⁾

Symbol	Description	Amount of Phase Shift	Units
Phase Shifting Range			
MAX_STEPS ⁽²⁾	When CLKIN < 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period.	$\pm(\text{INTEGER}(10 \times (\text{TCLKIN} - 3 \text{ ns})))$	steps
	When CLKIN ≥ 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period.	$\pm(\text{INTEGER}(15 \times (\text{TCLKIN} - 3 \text{ ns})))$	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting.	$\pm(\text{MAX_STEPS} \times \text{DCM_DELAY_STEP_MIN})$	ps
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	$\pm(\text{MAX_STEPS} \times \text{DCM_DELAY_STEP_MAX})$	ps

Notes:

1. The values in this table are based on the operating conditions described in Table 53 and Table 58.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM has no initial fixed-phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the end of Table 54.

Table 60: Miscellaneous DCM Timing Parameters⁽¹⁾

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	3	–	CLKIN cycles

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFXDV, CLKFX180) are unaffected.

Table 61: Frequency Synthesis

Attribute	Min	Max
CLKFX_MULTIPLY (DCM_SP)	2	32
CLKFX_DIVIDE (DCM_SP)	1	32
CLKDV_DIVIDE (DCM_SP)	1.5	16
CLKFX_MULTIPLY (DCM_CLKGEN)	2	256
CLKFX_DIVIDE (DCM_CLKGEN)	1	256
CLKFXDV_DIVIDE (DCM_CLKGEN)	2	32

Table 62: DCM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T _{DMCK_PSEN} /T _{DMCKC_PSEN}	PSEN Setup/Hold	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	ns
T _{DMCK_PSINCDEC} /T _{DMCKC_PSINCDEC}	PSINCDEC Setup/Hold	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	ns
T _{DMCKO_PSDONE}	Clock to out of PSDONE	1.50	1.50	1.50	1.50	ns

Table 66: Global Clock Input to Output Delay With PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> PLL in System-Synchronous Mode.							
T _{ICKOFFPLL}	Global Clock and OUTFF <i>with</i> PLL	XC6SLX4	4.57	N/A	6.25	7.34	ns
		XC6SLX9	4.57	5.25	6.25	7.34	ns
		XC6SLX16	4.41	4.64	5.39	6.92	ns
		XC6SLX25	4.03	4.32	4.91	7.64	ns
		XC6SLX25T	4.03	4.32	4.91	N/A	ns
		XC6SLX45	4.63	4.96	5.75	7.36	ns
		XC6SLX45T	4.63	4.96	5.75	N/A	ns
		XC6SLX75	4.01	4.30	4.88	7.15	ns
		XC6SLX75T	4.01	4.30	4.88	N/A	ns
		XC6SLX100	4.02	4.33	4.90	7.37	ns
		XC6SLX100T	4.06	4.33	4.90	N/A	ns
		XC6SLX150	3.65	3.98	4.58	6.94	ns
		XC6SLX150T	3.65	3.98	4.58	N/A	ns
		XA6SLX4	4.88	N/A	6.13	N/A	ns
		XA6SLX9	4.88	N/A	6.13	N/A	ns
		XA6SLX16	4.74	N/A	5.27	N/A	ns
		XA6SLX25	4.43	N/A	4.78	N/A	ns
		XA6SLX25T	4.43	N/A	4.88	N/A	ns
		XA6SLX45	4.94	N/A	5.62	N/A	ns
		XA6SLX45T	4.94	N/A	5.62	N/A	ns
		XA6SLX75	4.32	N/A	4.77	N/A	ns
		XA6SLX75T	4.32	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.41	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	7.15	ns
XQ6SLX75T	4.32	N/A	4.77	N/A	ns		
XQ6SLX150	N/A	N/A	4.60	6.94	ns		
XQ6SLX150T	4.35	N/A	4.60	N/A	ns		

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 72: Global Clock Setup and Hold With DCM in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.⁽¹⁾							
T _{PSDCM} / T _{PHDCM}	No Delay Global Clock and IFF ⁽²⁾ with DCM in System-Synchronous Mode	XC6SLX4	1.54/0.06	N/A	1.75/0.12	2.84/0.27	ns
		XC6SLX9	1.54/0.06	1.63/0.12	1.75/0.12	2.84/0.27	ns
		XC6SLX16	1.72/-0.18	1.87/-0.17	2.13/-0.17	2.31/0.26	ns
		XC6SLX25	1.70/-0.03	1.78/-0.02	2.00/-0.02	2.88/0.20	ns
		XC6SLX25T	1.70/0.07	1.78/0.08	2.00/0.08	N/A	ns
		XC6SLX45	1.74/-0.03	1.84/-0.02	2.02/-0.02	2.64/0.52	ns
		XC6SLX45T	1.74/-0.01	1.84/0.00	2.02/0.00	N/A	ns
		XC6SLX75	1.86/0.11	1.98/0.12	2.20/0.12	2.96/0.58	ns
		XC6SLX75T	1.86/0.11	1.98/0.12	2.20/0.12	N/A	ns
		XC6SLX100	1.64/0.07	1.72/0.08	1.97/0.08	2.70/0.99	ns
		XC6SLX100T	1.64/0.09	1.72/0.10	1.97/0.10	N/A	ns
		XC6SLX150	1.53/0.39	1.62/0.40	1.82/0.40	2.75/1.00	ns
		XC6SLX150T	1.53/0.39	1.62/0.40	1.82/0.40	N/A	ns
		XA6SLX4	1.65/0.16	N/A	1.75/0.26	N/A	ns
		XA6SLX9	1.65/0.16	N/A	1.75/0.26	N/A	ns
		XA6SLX16	1.88/0.02	N/A	2.13/0.03	N/A	ns
		XA6SLX25	1.80/0.16	N/A	2.05/0.17	N/A	ns
		XA6SLX25T	1.80/0.16	N/A	2.13/0.17	N/A	ns
		XA6SLX45	1.75/0.12	N/A	2.02/0.13	N/A	ns
		XA6SLX45T	1.75/0.12	N/A	2.02/0.13	N/A	ns
		XA6SLX75	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XA6SLX75T	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XA6SLX100	N/A	N/A	2.46/0.24	N/A	ns
		XQ6SLX75	N/A	N/A	2.20/0.12	2.96/0.58	ns
		XQ6SLX75T	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XQ6SLX150	N/A	N/A	1.82/0.56	2.75/1.00	ns
		XQ6SLX150T	1.65/0.55	N/A	1.82/0.56	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 73: Global Clock Setup and Hold With DCM in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.⁽¹⁾							
T _{PSDCMO} / T _{PHDCMO}	No Delay Global Clock and IFF ⁽²⁾ with DCM in Source-Synchronous Mode	XC6SLX4	0.71/0.65	N/A	0.72/1.22	1.58/1.18	ns
		XC6SLX9	0.71/0.69	0.71/1.19	0.72/1.36	1.58/1.18	ns
		XC6SLX16	0.86/0.52	0.92/0.57	1.04/0.60	1.02/1.06	ns
		XC6SLX25	0.84/0.58	0.90/0.59	1.01/0.59	1.58/1.07	ns
		XC6SLX25T	0.84/0.58	0.90/0.59	1.01/0.59	N/A	ns
		XC6SLX45	0.85/0.70	0.90/0.76	0.98/0.79	1.34/1.34	ns
		XC6SLX45T	0.85/0.70	0.90/0.76	0.98/0.79	N/A	ns
		XC6SLX75	1.00/0.62	1.06/0.63	1.15/0.63	1.65/1.46	ns
		XC6SLX75T	1.00/0.71	1.06/0.72	1.15/0.72	N/A	ns
		XC6SLX100	0.81/0.68	0.81/0.69	0.94/0.69	1.42/2.07	ns
		XC6SLX100T	0.81/0.68	0.81/0.69	0.94/0.69	N/A	ns
		XC6SLX150	0.68/0.98	0.69/0.99	0.79/0.99	1.45/1.60	ns
		XC6SLX150T	0.68/0.98	0.69/0.99	0.79/0.99	N/A	ns
		XA6SLX4	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX9	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX16	1.01/0.56	N/A	1.04/0.60	N/A	ns
		XA6SLX25	0.94/0.76	N/A	1.06/0.77	N/A	ns
		XA6SLX25T	0.94/0.76	N/A	1.14/0.77	N/A	ns
		XA6SLX45	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX45T	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX75	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX100	N/A	N/A	1.37/0.75	N/A	ns
		XQ6SLX75	N/A	N/A	1.15/0.72	1.65/1.46	ns
		XQ6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XQ6SLX150	N/A	N/A	0.79/1.15	1.45/1.60	ns
XQ6SLX150T	0.73/1.15	N/A	0.79/1.15	N/A	ns		

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 75: Global Clock Setup and Hold With PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.⁽¹⁾							
T _{PSPLL0} / T _{PHPLL0}	No Delay Global Clock and IFF ⁽²⁾ with PLL in Source-Synchronous Mode	XC6SLX4	0.47/1.08	N/A	0.47/1.60	1.15/1.68	ns
		XC6SLX9	0.47/1.08	0.47/1.35	0.47/1.60	1.15/1.68	ns
		XC6SLX16	0.37/0.75	0.37/0.82	0.51/0.94	0.57/1.31	ns
		XC6SLX25	0.69/1.06	0.69/1.06	0.69/1.06	1.86/1.67	ns
		XC6SLX25T	0.69/1.06	0.69/1.06	0.69/1.06	N/A	ns
		XC6SLX45	0.57/1.05	0.65/1.10	0.65/1.18	1.02/1.65	ns
		XC6SLX45T	0.57/1.06	0.65/1.10	0.65/1.18	N/A	ns
		XC6SLX75	0.86/1.04	0.87/1.04	0.90/1.04	1.34/1.55	ns
		XC6SLX75T	0.86/1.04	0.87/1.04	0.90/1.04	N/A	ns
		XC6SLX100	0.53/1.13	0.54/1.13	0.55/1.13	0.89/2.39	ns
		XC6SLX100T	0.53/1.13	0.54/1.13	0.55/1.13	N/A	ns
		XC6SLX150	0.50/1.31	0.51/1.31	0.52/1.31	1.02/1.72	ns
		XC6SLX150T	0.50/1.31	0.51/1.31	0.52/1.31	N/A	ns
		XA6SLX4	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX9	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX16	0.92/0.69	N/A	0.63/0.82	N/A	ns
		XA6SLX25	0.99/0.94	N/A	0.96/0.94	N/A	ns
		XA6SLX25T	0.99/0.94	N/A	1.04/0.94	N/A	ns
		XA6SLX45	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX45T	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX75	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX100	N/A	N/A	1.25/0.96	N/A	ns
		XQ6SLX75	N/A	N/A	1.02/0.89	1.34/1.55	ns
XQ6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns		
XQ6SLX150	N/A	N/A	0.63/1.19	1.02/1.72	ns		
XQ6SLX150T	0.60/1.19	N/A	0.63/1.19	N/A	ns		

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Spartan-6 FPGA source-synchronous transmitter and receiver data-valid windows.

Table 78: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{DCD_CLK}	Global Clock Tree Duty Cycle Distortion ⁽²⁾	LX4	0.20	N/A	0.20	0.35	ns
		LX9	0.20	0.20	0.20	0.35	ns
		LX16	0.20	0.20	0.20	0.35	ns
		LX25	0.20	0.20	0.20	0.35	ns
		LX25T	0.20	0.20	0.20	N/A	ns
		LX45	0.20	0.20	0.20	0.35	ns
		LX45T	0.20	0.20	0.20	N/A	ns
		LX75	0.20	0.20	0.20	0.35	ns
		LX75T	0.20	0.20	0.20	N/A	ns
		LX100	0.20	0.20	0.20	0.35	ns
		LX100T	0.20	0.20	0.20	N/A	ns
		LX150	0.35	0.35	0.35	0.35	ns
		LX150T	0.35	0.35	0.35	N/A	ns
T _{CKSKEW}	Global Clock Tree Skew ⁽³⁾	LX4	0.25	N/A	0.25	0.29	ns
		LX9	0.25	0.25	0.25	0.29	ns
		LX16	0.15	0.15	0.15	0.22	ns
		LX25	0.26	0.26	0.26	0.41	ns
		LX25T	0.26	0.26	0.26	N/A	ns
		LX45	0.20	0.20	0.20	0.28	ns
		LX45T	0.20	0.20	0.20	N/A	ns
		LX75	0.56	0.56	0.56	0.50	ns
		LX75T	0.56	0.56	0.56	N/A	ns
		XC6SLX100 ⁽⁴⁾	0.22	0.22	0.22	0.21	ns
		XA6SLX100 ⁽⁴⁾	N/A	N/A	0.43	N/A	ns
		LX100T	0.22	0.22	0.22	N/A	ns
		LX150	0.48	0.48	0.48	0.35	ns
LX150T	0.48	0.48	0.48	N/A	ns		
T _{DCD_BUFIO2}	I/O clock tree duty cycle distortion	LX devices	0.25	0.25	0.25	0.50	ns
		LXT devices	0.25	0.25	0.25	N/A	ns

Table 78: Duty Cycle Distortion and Clock-Tree Skew (Cont'd)

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{BUFIOSKEW}	I/O clock tree skew across one clock region	LX4	0.06	N/A	0.06	0.07	ns
		LX9	0.06	0.06	0.06	0.07	ns
		LX16	0.06	0.06	0.06	0.07	ns
		LX25	0.06	0.06	0.06	0.07	ns
		LX25T	0.06	0.06	0.06	N/A	ns
		LX45	0.06	0.06	0.06	0.07	ns
		LX45T	0.06	0.06	0.06	N/A	ns
		LX75	0.06	0.06	0.06	0.07	ns
		LX75T	0.06	0.06	0.06	N/A	ns
		LX100	0.06	0.06	0.06	0.07	ns
		LX100T	0.06	0.06	0.06	N/A	ns
		LX150	0.06	0.06	0.06	0.07	ns
		LX150T	0.06	0.06	0.06	N/A	ns

Notes:

- LXT devices are not available with a -1L speed grade. The LX4 is not available in -3N speed grade.
- These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
- The T_{CKSKEW} is 0.43 ns for the XA6SLX100 device using a -2 speed grade and 0.22 ns for the XC6SLX100 devices using the -2 speed grade.

Table 79: Package Skew

Symbol	Description	Device	Package ⁽²⁾	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	LX4	TQG144	N/A	ps
			CPG196	23	ps
			CSG225	58	ps
		LX9	TQG144	N/A	ps
			CPG196	23	ps
			CSG225	58	ps
			FT(G)256	88	ps
			CSG324	64	ps
		LX16	CPG196	19	ps
			CSG225	70	ps
			FT(G)256	71	ps
			CSG324	54	ps
		LX25	FT(G)256	90	ps
			CSG324	61	ps
			FG(G)484	84	ps
LX25T	CSG324	48	ps		
	FG(G)484	112	ps		

Table 79: Package Skew (Cont'd)

Symbol	Description	Device	Package ⁽²⁾	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	LX45	CSG324	70	ps
			CS(G)484	99	ps
			FG(G)484	109	ps
			FG(G)676	138	ps
		LX45T	CSG324	75	ps
			CS(G)484	100	ps
			FG(G)484	95	ps
		LX75	CS(G)484	101	ps
			FG(G)484	107	ps
		LX75T	FG(G)676	161	ps
			CS(G)484	107	ps
			FG(G)484	110	ps
		LX100	FG(G)676	134	ps
			CS(G)484	95	ps
			FG(G)484	155	ps
		LX100T	FG(G)676	144	ps
			CS(G)484	88	ps
			FG(G)484	111	ps
			FG(G)676	147	ps
		LX150	FG(G)900	134	ps
			CS(G)484	84	ps
			FG(G)484	103	ps
			FG(G)676	115	ps
		LX150T	FG(G)900	121	ps
CS(G)484	83		ps		
FG(G)484	88		ps		
FG(G)676	141		ps		
			FG(G)900	120	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from Pad to Ball.
2. Some of the devices are available in both Pb and Pb-free (additional G) packages as standard ordering options. See [DS160: Spartan-6 Family Overview](#) for more information.

Table 80: Sample Window

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{SAMP}	Sampling Error at Receiver Pins ⁽²⁾	All	510	510	530	740	ps
T _{SAMP_BUFIO2}	Sampling Error at Receiver Pins using BUFIO2 ⁽³⁾	All	430	430	450	590	ps

Notes:

1. LXT devices are not available with a -1L speed grade.
2. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 DCM jitter
 - DCM accuracy (phase offset)
 - DCM phase shift resolution
 These measurements do not include package or clock tree skew.
3. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO2 clock network and IODELAY2 to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

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