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### Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### Details

Product Status	Active
Number of LABs/CLBs	3411
Number of Logic Elements/Cells	43661
Total RAM Bits	2138112
Number of I/O	320
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-FBGA, CSPBGA
Supplier Device Package	484-CSPBGA (19x19)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xc6slx45-2csg484i">https://www.e-xfl.com/product-detail/xilinx/xc6slx45-2csg484i</a>

Table 3: eFUSE Programming Conditions<sup>(1)</sup>

Symbol	Description	Min	Typ	Max	Units
$V_{FS}^{(2)}$	External voltage supply	3.2	3.3	3.4	V
$I_{FS}$	$V_{FS}$ supply current	–	–	40	mA
$V_{CCAUX}$	Auxiliary supply voltage relative to GND	3.2	3.3	3.45	V
$R_{FUSE}^{(3)}$	External resistor from $R_{FUSE}$ pin to GND	1129	1140	1151	$\Omega$
$V_{CCINT}$	Internal supply voltage relative to GND	1.14	1.2	1.26	V
$t_j$	Temperature range	15	–	85	$^{\circ}\text{C}$

**Notes:**

1. These specifications apply during programming of the eFUSE AES key. Programming is only supported through JTAG. The AES key is only supported in the following devices: LX75, LX75T, LX100, LX100T, LX150, and LX150T.
2. When programming eFUSE,  $V_{FS}$  must be less than or equal to  $V_{CCAUX}$ . When not programming or when eFUSE is not used, Xilinx recommends connecting  $V_{FS}$  to GND. However,  $V_{FS}$  can be between GND and 3.45 V.
3. An  $R_{FUSE}$  resistor is required when programming the eFUSE AES key. When not programming or when eFUSE is not used, Xilinx recommends connecting the  $R_{FUSE}$  pin to  $V_{CCAUX}$  or GND. However,  $R_{FUSE}$  can be unconnected.

In [Table 9](#) and [Table 10](#), values for  $V_{IL}$  and  $V_{IH}$  are recommended input voltages. Values for  $I_{OL}$  and  $I_{OH}$  are guaranteed over the recommended operating conditions at the  $V_{OL}$  and  $V_{OH}$  test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum  $V_{CCO}$  with the respective  $V_{OL}$  and  $V_{OH}$  voltage levels shown. Other standards are sample tested.

**Table 9: Single-Ended I/O Standard DC Input and Output Levels**

I/O Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTTL	-0.5	0.8	2.0	4.1	0.4	2.4	Note 2	Note 2
LVC MOS33	-0.5	0.8	2.0	4.1	0.4	$V_{CCO} - 0.4$	Note 2	Note 2
LVC MOS25	-0.5	0.7	1.7	4.1	0.4	$V_{CCO} - 0.4$	Note 2	Note 2
LVC MOS18	-0.5	0.38	0.8	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS18 (-1L)	-0.5	0.33	0.71	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS18 JEDEC	-0.5	35% $V_{CCO}$	65% $V_{CCO}$	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS15	-0.5	0.38	0.8	4.1	25% $V_{CCO}$	75% $V_{CCO}$	Note 3	Note 3
LVC MOS15 (-1L)	-0.5	0.33	0.71	4.1	25% $V_{CCO}$	75% $V_{CCO}$	Note 3	Note 3
LVC MOS15 JEDEC	-0.5	35% $V_{CCO}$	65% $V_{CCO}$	4.1	25% $V_{CCO}$	75% $V_{CCO}$	Note 3	Note 3
LVC MOS12	-0.5	0.38	0.8	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
LVC MOS12 (-1L)	-0.5	0.33	0.71	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
LVC MOS12 JEDEC	-0.5	35% $V_{CCO}$	65% $V_{CCO}$	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
PCI33_3	-0.5	30% $V_{CCO}$	50% $V_{CCO}$	$V_{CCO} + 0.5$	10% $V_{CCO}$	90% $V_{CCO}$	1.5	-0.5
PCI66_3	-0.5	30% $V_{CCO}$	50% $V_{CCO}$	$V_{CCO} + 0.5$	10% $V_{CCO}$	90% $V_{CCO}$	1.5	-0.5
I2C	-0.5	25% $V_{CCO}$	70% $V_{CCO}$	4.1	20% $V_{CCO}$	-	3	-
SMBUS	-0.5	0.8	2.1	4.1	0.4	-	4	-
SDIO	-0.5	12.5% $V_{CCO}$	75% $V_{CCO}$	4.1	12.5% $V_{CCO}$	75% $V_{CCO}$	0.1	-0.1
MOBILE_DDR	-0.5	20% $V_{CCO}$	80% $V_{CCO}$	4.1	10% $V_{CCO}$	90% $V_{CCO}$	0.1	-0.1
HSTL_I	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	8	-8
HSTL_II	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	16	-16
HSTL_III	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	24	-8
HSTL_I_18	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	11	-11
HSTL_II_18	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	22	-22
HSTL_III_18	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	30	-11
SSTL3_I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	4.1	$V_{TT} - 0.6$	$V_{TT} + 0.6$	8	-8
SSTL3_II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	4.1	$V_{TT} - 0.8$	$V_{TT} + 0.8$	16	-16
SSTL2_I	-0.5	$V_{REF} - 0.15$	$V_{REF} + 0.15$	4.1	$V_{TT} - 0.61$	$V_{TT} + 0.61$	8.1	-8.1
SSTL2_II	-0.5	$V_{REF} - 0.15$	$V_{REF} + 0.15$	4.1	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	-16.2
SSTL18_I	-0.5	$V_{REF} - 0.125$	$V_{REF} + 0.125$	4.1	$V_{TT} - 0.47$	$V_{TT} + 0.47$	6.7	-6.7
SSTL18_II	-0.5	$V_{REF} - 0.125$	$V_{REF} + 0.125$	4.1	$V_{TT} - 0.60$	$V_{TT} + 0.60$	13.4	-13.4
SSTL15_II	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	$V_{TT} - 0.4$	$V_{TT} + 0.4$	13.4	-13.4

**Notes:**

1. Tested according to relevant specifications.
2. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
3. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
4. Using drive strengths of 2, 4, 6, 8, or 12 mA.
5. For more information, refer to [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.

## eFUSE Read Endurance

Table 11 lists the minimum guaranteed number of read cycle operations for Device DNA and for the AES eFUSE key. For more information, see [UG380: Spartan-6 FPGA Configuration User Guide](#).

Table 11: eFUSE Read Endurance

Symbol	Description	Speed Grade				Units (Min)
		-3	-3N	-2	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

## GTP Transceiver Specifications

GTP transceivers are available in the Spartan-6 LXT devices. See [DS160: Spartan-6 Family Overview](#) for more information.

### GTP Transceiver DC Characteristics

Table 12: Absolute Maximum Ratings for GTP Transceivers<sup>(1)</sup>

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	-0.5	1.32	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	-0.5	1.32	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	-0.5	1.32	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	-0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	-0.5	1.32	V
V <sub>IN</sub>	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	-0.5	1.32	V
V <sub>MGTREFCLK</sub>	Reference clock absolute input voltage	-0.5	1.32	V

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 13: Recommended Operating Conditions for GTP Transceivers<sup>(1)(2)(3)</sup>

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	1.14	1.20	1.26	V

**Notes:**

- Each voltage listed requires the filter circuit described in [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#).
- Voltages are specified for the temperature range of T<sub>j</sub> = -40°C to +125°C.
- The voltage level of MGTAVCCPLL must not exceed the voltage level of MGTAVCC +10mV. The voltage level of MGTAVCC must not exceed the voltage level of MGTAVCCPLL.

Table 21: GTP Transceiver User Clock Switching Characteristics<sup>(1)</sup>

Symbol	Description	Conditions	Speed Grade				Units
			-3	-3N	-2	-1L	
F <sub>TXOUT</sub>	TXOUTCLK maximum frequency		320	320	270	N/A	MHz
F <sub>RXREC</sub>	RXRECCLK maximum frequency		320	320	270	N/A	MHz
T <sub>RX</sub>	RXUSRCLK maximum frequency		320	320	270	N/A	MHz
T <sub>RX2</sub>	RXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz
T <sub>TX</sub>	TXUSRCLK maximum frequency		320	320	270	N/A	MHz
T <sub>TX2</sub>	TXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz

Notes:

1. Clocking must be implemented as described in [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#).

Table 22: GTP Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
T <sub>RTX</sub>	TX Rise time	20%–80%	–	140	–	ps
T <sub>FTX</sub>	TX Fall time	80%–20%	–	120	–	ps
T <sub>LLSKEW</sub>	TX lane-to-lane skew <sup>(1)</sup>		–	–	400	ps
V <sub>TXOOBVDPP</sub>	Electrical idle amplitude		–	–	20	mV
T <sub>TXOOBTRANSITION</sub>	Electrical idle transition time		–	–	50	ns
T <sub>J3.125</sub>	Total Jitter <sup>(2)</sup>	3.125 Gb/s	–	–	0.35	UI
D <sub>J3.125</sub>	Deterministic Jitter <sup>(2)</sup>		–	–	0.15	UI
T <sub>J2.5</sub>	Total Jitter <sup>(2)</sup>	2.5 Gb/s	–	–	0.33	UI
D <sub>J2.5</sub>	Deterministic Jitter <sup>(2)</sup>		–	–	0.15	UI
T <sub>J1.62</sub>	Total Jitter <sup>(2)</sup>	1.62 Gb/s	–	–	0.20	UI
D <sub>J1.62</sub>	Deterministic Jitter <sup>(2)</sup>		–	–	0.10	UI
T <sub>J1.25</sub>	Total Jitter <sup>(2)</sup>	1.25 Gb/s	–	–	0.20	UI
D <sub>J1.25</sub>	Deterministic Jitter <sup>(2)</sup>		–	–	0.10	UI
T <sub>J614</sub>	Total Jitter <sup>(2)</sup>	614 Mb/s	–	–	0.10	UI
D <sub>J614</sub>	Deterministic Jitter <sup>(2)</sup>		–	–	0.05	UI

Notes:

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP transceiver sites.
2. Using PLL\_DIVSEL\_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.

## Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.20 for -3, -3N, and -2; and v1.08 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

### Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

The -1L speed grade refers to the lower-power Spartan-6 devices. The -3N speed grade refers to the Spartan-6 devices that do not support MCB functionality.

[Table 26](#) correlates the current status of each Spartan-6 device on a per speed grade basis.

## Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-6 devices.

Table 26: Spartan-6 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6SLX4 <sup>(1)</sup>			-3, -2, -1L
XC6SLX9			-3, -3N, -2, -1L
XC6SLX16			-3, -3N, -2, -1L
XC6SLX25			-3, -3N, -2, -1L
XC6SLX25T			-3, -3N, -2
XC6SLX45			-3, -3N, -2, -1L
XC6SLX45T			-3, -3N, -2
XC6SLX75			-3, -3N, -2, -1L
XC6SLX75T			-3, -3N, -2
XC6SLX100			-3, -3N, -2, -1L
XC6SLX100T			-3, -3N, -2
XC6SLX150			-3, -3N, -2, -1L
XC6SLX150T			-3, -3N, -2
XA6SLX4			-3, -2
XA6SLX9			-3, -2
XA6SLX16			-3, -2
XA6SLX25			-3, -2
XA6SLX25T			-3, -2
XA6SLX45			-3, -2
XA6SLX45T			-3, -2
XA6SLX75			-3, -2
XA6SLX75T			-3, -2
XA6SLX100			-2
XQ6SLX75			-2, -1L
XQ6SLX75T			-3, -2
XQ6SLX150			-2, -1L
XQ6SLX150T			-3, -2

### Notes:

1. The XC6SLX4 is not available in the -3N speed grade.

## Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. [Table 27](#) lists the production released Spartan-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE® software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

**Table 27: Spartan-6 Device Production Software and Speed Specification Release<sup>(1)</sup>**

Device	Speed Grade Designations <sup>(2)</sup>			
	-3 <sup>(3)</sup>	-3N	-2 <sup>(4)</sup>	-1L
XC6SLX4	ISE 12.4 v1.15	N/A	ISE 12.3 v1.12 <sup>(5)</sup>	ISE 13.2 v1.07
XC6SLX9	ISE 12.4 v1.15	ISE 13.1 Update v1.18 <sup>(7)</sup>	ISE 12.3 v1.12 <sup>(5)</sup>	ISE 13.2 v1.07
XC6SLX16	ISE 12.1 v1.08	ISE 13.1 Update v1.18 <sup>(7)</sup>	ISE 11.5 v1.06	ISE 13.2 v1.07
XC6SLX25	ISE 12.2 v1.11 <sup>(6)</sup>	ISE 13.1 Update v1.18 <sup>(7)</sup>	ISE 12.2 v1.11 <sup>(6)</sup>	ISE 13.2 v1.07
XC6SLX25T	ISE 12.2 v1.11 <sup>(6)</sup>	ISE 13.1 Update v1.18 <sup>(7)</sup>	ISE 12.2 v1.11 <sup>(6)</sup>	N/A
XC6SLX45	ISE 12.1 v1.08	ISE 13.1 Update v1.18 <sup>(7)</sup>	ISE 11.5 v1.07	ISE 13.1 v1.06
XC6SLX45T	ISE 12.1 v1.08	ISE 13.1 Update v1.18 <sup>(7)</sup>	ISE 12.1 v1.08	N/A
XC6SLX75	ISE 12.2 v1.11 <sup>(6)</sup>	ISE 13.1 Update v1.18 <sup>(7)</sup>	ISE 12.2 v1.11 <sup>(6)</sup>	ISE 13.2 v1.07
XC6SLX75T	ISE 12.2 v1.11 <sup>(6)</sup>	ISE 13.1 Update v1.18 <sup>(7)</sup>	ISE 12.2 v1.11 <sup>(6)</sup>	N/A
XC6SLX100	ISE 12.2 v1.11 <sup>(6)</sup>	ISE 13.1 Update v1.18 <sup>(7)</sup>	ISE 12.2 v1.11 <sup>(6)</sup>	ISE 13.1 v1.06
XC6SLX100T	ISE 12.2 v1.11 <sup>(6)</sup>	ISE 13.1 Update v1.18 <sup>(7)</sup>	ISE 12.2 v1.11 <sup>(6)</sup>	N/A
XC6SLX150	ISE 12.2 v1.11 <sup>(6)</sup>	ISE 13.1 Update v1.18 <sup>(7)</sup>	ISE 12.2 v1.11 <sup>(6)</sup>	ISE 13.1 v1.06
XC6SLX150T	ISE 12.2 v1.11 <sup>(6)</sup>	ISE 13.1 Update v1.18 <sup>(7)</sup>	ISE 12.2 v1.11 <sup>(6)</sup>	N/A
XA6SLX4	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX9	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX16	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX25	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX25T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX45	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX45T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX75	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX75T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX100	N/A	N/A	ISE 13.3 v1.20	N/A

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T <sub>IOPI</sub>				T <sub>IOOP</sub>				T <sub>IOTP</sub>				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	
LVTTTL, QUIETIO, 2 mA	1.35	1.47	1.60	1.82	5.39	5.53	5.73	6.37	5.39	5.53	5.73	6.37	ns
LVTTTL, QUIETIO, 4 mA	1.35	1.47	1.60	1.82	4.29	4.43	4.63	5.22	4.29	4.43	4.63	5.22	ns
LVTTTL, QUIETIO, 6 mA	1.35	1.47	1.60	1.82	3.75	3.89	4.09	4.69	3.75	3.89	4.09	4.69	ns
LVTTTL, QUIETIO, 8 mA	1.35	1.47	1.60	1.82	3.23	3.37	3.57	4.20	3.23	3.37	3.57	4.20	ns
LVTTTL, QUIETIO, 12 mA	1.35	1.47	1.60	1.82	3.28	3.42	3.62	4.22	3.28	3.42	3.62	4.22	ns
LVTTTL, QUIETIO, 16 mA	1.35	1.47	1.60	1.82	2.94	3.08	3.28	3.92	2.94	3.08	3.28	3.92	ns
LVTTTL, QUIETIO, 24 mA	1.35	1.47	1.60	1.82	2.69	2.83	3.03	3.67	2.69	2.83	3.03	3.67	ns
LVTTTL, Slow, 2 mA	1.35	1.47	1.60	1.82	4.36	4.50	4.70	5.30	4.36	4.50	4.70	5.30	ns
LVTTTL, Slow, 4 mA	1.35	1.47	1.60	1.82	3.17	3.31	3.51	4.16	3.17	3.31	3.51	4.16	ns
LVTTTL, Slow, 6 mA	1.35	1.47	1.60	1.82	2.76	2.90	3.10	3.75	2.76	2.90	3.10	3.75	ns
LVTTTL, Slow, 8 mA	1.35	1.47	1.60	1.82	2.59	2.73	2.93	3.55	2.59	2.73	2.93	3.55	ns
LVTTTL, Slow, 12 mA	1.35	1.47	1.60	1.82	2.58	2.72	2.92	3.54	2.58	2.72	2.92	3.54	ns
LVTTTL, Slow, 16 mA	1.35	1.47	1.60	1.82	2.39	2.53	2.73	3.40	2.39	2.53	2.73	3.40	ns
LVTTTL, Slow, 24 mA	1.35	1.47	1.60	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVTTTL, Fast, 2 mA	1.35	1.47	1.60	1.82	3.78	3.92	4.12	4.74	3.78	3.92	4.12	4.74	ns
LVTTTL, Fast, 4 mA	1.35	1.47	1.60	1.82	2.49	2.63	2.83	3.45	2.49	2.63	2.83	3.45	ns
LVTTTL, Fast, 6 mA	1.35	1.47	1.60	1.82	2.44	2.58	2.78	3.40	2.44	2.58	2.78	3.40	ns
LVTTTL, Fast, 8 mA	1.35	1.47	1.60	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns
LVTTTL, Fast, 12 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTTL, Fast, 16 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTTL, Fast, 24 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVC MOS33, QUIETIO, 2 mA	1.34	1.46	1.59	1.82	5.40	5.54	5.74	6.37	5.40	5.54	5.74	6.37	ns
LVC MOS33, QUIETIO, 4 mA	1.34	1.46	1.59	1.82	4.03	4.17	4.37	5.01	4.03	4.17	4.37	5.01	ns
LVC MOS33, QUIETIO, 6 mA	1.34	1.46	1.59	1.82	3.51	3.65	3.85	4.47	3.51	3.65	3.85	4.47	ns
LVC MOS33, QUIETIO, 8 mA	1.34	1.46	1.59	1.82	3.37	3.51	3.71	4.33	3.37	3.51	3.71	4.33	ns
LVC MOS33, QUIETIO, 12 mA	1.34	1.46	1.59	1.82	2.94	3.08	3.28	3.93	2.94	3.08	3.28	3.93	ns
LVC MOS33, QUIETIO, 16 mA	1.34	1.46	1.59	1.82	2.77	2.91	3.11	3.78	2.77	2.91	3.11	3.78	ns
LVC MOS33, QUIETIO, 24 mA	1.34	1.46	1.59	1.82	2.59	2.73	2.93	3.58	2.59	2.73	2.93	3.58	ns
LVC MOS33, Slow, 2 mA	1.34	1.46	1.59	1.82	4.37	4.51	4.71	5.28	4.37	4.51	4.71	5.28	ns
LVC MOS33, Slow, 4 mA	1.34	1.46	1.59	1.82	2.98	3.12	3.32	3.94	2.98	3.12	3.32	3.94	ns
LVC MOS33, Slow, 6 mA	1.34	1.46	1.59	1.82	2.58	2.72	2.92	3.61	2.58	2.72	2.92	3.61	ns
LVC MOS33, Slow, 8 mA	1.34	1.46	1.59	1.82	2.65	2.79	2.99	3.61	2.65	2.79	2.99	3.61	ns
LVC MOS33, Slow, 12 mA	1.34	1.46	1.59	1.82	2.39	2.53	2.73	3.31	2.39	2.53	2.73	3.31	ns
LVC MOS33, Slow, 16 mA	1.34	1.46	1.59	1.82	2.31	2.45	2.65	3.27	2.31	2.45	2.65	3.27	ns
LVC MOS33, Slow, 24 mA	1.34	1.46	1.59	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVC MOS33, Fast, 2 mA	1.34	1.46	1.59	1.82	3.76	3.90	4.10	4.70	3.76	3.90	4.10	4.70	ns
LVC MOS33, Fast, 4 mA	1.34	1.46	1.59	1.82	2.48	2.62	2.82	3.44	2.48	2.62	2.82	3.44	ns
LVC MOS33, Fast, 6 mA	1.34	1.46	1.59	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns



## CLB Switching Characteristics (SLICEM Only)

Table 40: CLB Switching Characteristics (SLICEM Only)

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
<b>Combinatorial Delays</b>						
T <sub>ILO</sub>	An – Dn LUT inputs to A to D outputs	0.21	0.26	0.26	0.46	ns, Max
	An – Dn LUT inputs through F7AMUX/F7BMUX to AMUX/CMUX output	0.37	0.43	0.43	0.77	ns, Max
T <sub>OPAB</sub>	An – Dn LUT inputs through F7AMUX or F7BMUX and F8MUX to BMUX output	0.37	0.46	0.46	0.84	ns, Max
T <sub>ITO</sub>	An – Dn LUT inputs through latch to AQ – DQ outputs	0.82	0.95	0.95	1.64	ns, Max
T <sub>TITO_LOGIC</sub>	An – Dn LUT inputs to AQ – DQ outputs (latch as logic)	0.82	0.95	0.95	1.64	ns, Max
T <sub>OPCYA</sub>	An LUT inputs to COUT output	0.38	0.48	0.48	0.69	ns, Max
T <sub>OPCYB</sub>	Bn LUT inputs to COUT output	0.38	0.49	0.49	0.71	ns, Max
T <sub>OPCYC</sub>	Cn LUT inputs to COUT output	0.28	0.33	0.33	0.55	ns, Max
T <sub>OPCYD</sub>	Dn LUT inputs to COUT output	0.28	0.35	0.35	0.52	ns, Max
T <sub>AXCY</sub>	AX input to COUT output	0.21	0.26	0.26	0.36	ns, Max
T <sub>BXCY</sub>	BX input to COUT output	0.13	0.16	0.16	0.18	ns, Max
T <sub>CXCY</sub>	CX input to COUT output	0.10	0.12	0.12	0.09	ns, Max
T <sub>DXCY</sub>	DX input to COUT output	0.09	0.11	0.11	0.09	ns, Max
T <sub>BYP</sub>	CIN input to COUT output	0.08	0.10	0.10	0.06	ns, Max
T <sub>CINA</sub>	CIN input to AMUX output	0.21	0.22	0.22	0.47	ns, Max
T <sub>CINB</sub>	CIN input to BMUX output	0.30	0.31	0.31	0.57	ns, Max
T <sub>CINC</sub>	CIN input to CMUX output	0.29	0.31	0.31	0.58	ns, Max
T <sub>CIND</sub>	CIN input to DMUX output	0.31	0.32	0.32	0.68	ns, Max
<b>Sequential Delays</b>						
T <sub>CKO</sub>	Clock to AQ – DQ outputs	0.45	0.53	0.53	0.74	ns, Max
<b>Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK</b>						
T <sub>DICK</sub> /T <sub>CKDI</sub>	AX – DX input to CLK on A – D flip-flops	0.42/ 0.28	0.47/ 0.39	0.47/ 0.39	0.90/ 0.56	ns, Min
T <sub>CECK</sub> /T <sub>CKCE</sub>	CE input to CLK on A – D flip-flops	0.31/ –0.07	0.37/ –0.07	0.37/ –0.07	0.59/ –0.27	ns, Min
T <sub>SRCK</sub> /T <sub>CKSR</sub>	SR input to CLK on A – D flip-flops for XC devices	0.41/ 0.02	0.42/ 0.02	0.42/ 0.02	0.68/ –0.29	ns, Min
	SR input to CLK on A – D flip-flops for XA and XQ devices	0.41/ 0.02	N/A	0.44/ 0.02	0.68/ –0.29	ns, Min
T <sub>CINCK</sub> /T <sub>CKCIN</sub>	CIN input to CLK on A – D flip-flops	0.31/ –0.17	0.31/ –0.13	0.31/ –0.13	0.81/ –0.42	ns, Min
<b>Set/Reset</b>						
T <sub>RPW</sub>	SR input minimum pulse width	0.41	0.48	0.48	1.37	ns, Min
T <sub>RQ</sub>	Delay from SR input to AQ – DQ flip-flops	0.60	0.70	0.70	0.88	ns, Max
T <sub>CEO</sub>	Delay from CE input to AQ – DQ flip-flops	0.60	0.65	0.65	0.90	ns, Max
F <sub>TOG</sub>	Toggle frequency (for export control)	862	806	667	500	MHz

## Configuration Switching Characteristics

Table 47: Configuration Switching Characteristics<sup>(1)</sup>

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
<b>Power-up Timing Characteristics</b>						
T <sub>PL</sub> <sup>(2)</sup>	PROGRAM_B Latency	4	4	4	5	ms, Max
T <sub>POR</sub> <sup>(2)</sup>	Power-on reset (50 ms ramp time) <sup>(3)</sup>	5/30	5/34	5/40	5/40	ms, Min/Max
	Power-on reset (10 ms ramp time)	5/25	5/29	5/35	5/40	ms, Min/Max
T <sub>PROGRAM</sub>	PROGRAM_B Pulse Width	500	500	500	500	ns, Min
<b>Slave Serial Mode Programming Switching</b>						
T <sub>DCCK</sub> /T <sub>CCKD</sub>	DIN Setup/Hold, slave mode	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T <sub>CCO</sub>	CCLK to DOUT	12	12	12	17	ns, Max
F <sub>SCCK</sub>	Slave mode external CCLK	80	80	80	50	MHz, Max
<b>Slave SelectMAP Mode Programming Switching</b>						
T <sub>SMDCCK</sub> /T <sub>SMCCKD</sub>	SelectMAP Data Setup/Hold	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T <sub>SMCSCCK</sub> /T <sub>SMCCKCS</sub>	CSI_B Setup/Hold	7.0/0.0	7.0/0.0	7.0/0.0	9.0/2.0	ns, Min
T <sub>SMWCCK</sub> /T <sub>SMCCKW</sub>	RDWR_B Setup/Hold	17.0/1.0	17.0/1.0	17.0/1.0	27.0/2.0	ns, Min
T <sub>SMCKCSO</sub>	CSO_B clock to out	16	16	16	26	ns, Max
T <sub>SMCO</sub>	CCLK to DATA out in readback	13	13	13	25	ns, Max
T <sub>SMCKBY</sub>	CCLK to BUSY out in readback	12	12	12	17	ns, Max
F <sub>SMCCK</sub>	Maximum CCLK frequency (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	25	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x8 mode, LX150, and LX150T only)	40	40	40	20	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x16 mode only)	35	35	35	20	MHz, Max
F <sub>RBCK</sub>	Maximum Readback CCLK frequency, including block RAM (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	20	20	20	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	30	MHz, Max
	Maximum Readback CCLK frequency, including block RAM (LX100, LX100T, LX150, and LX150T only)	12	12	12	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX100, LX100T, LX150, and LX150T only)	35	35	35	20	MHz, Max
<b>Boundary-Scan Port Timing Specifications</b>						
T <sub>TAPTCK</sub>	TMS and TDI Setup time before TCK	10	10	10	17	ns, Min
T <sub>TCKTAP</sub>	TMS and TDI Hold time after TCK	5.5	5.5	5.5	5.5	ns, Min
T <sub>TCKTDO</sub>	TCK falling edge to TDO output valid	6.5	6.5	6.5	8	ns, Max
T <sub>TCKH</sub>	TCK clock minimum High time	12	12	12	21	ns, Min
T <sub>TCKL</sub>	TCK clock minimum Low time	12	12	12	21	ns, Min
F <sub>TCK</sub>	Maximum configuration TCK clock frequency	33	33	33	18	MHz, Max
F <sub>TCKB</sub>	Maximum boundary-scan TCK clock frequency	33	33	33	18	MHz, Max
F <sub>TCKAES</sub>	Maximum AES key TCK clock frequency	2	2	2	2	MHz, Max

## Clock Buffers and Networks

Table 48: Global Clock Switching Characteristics (BUFGMUX)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T <sub>GSI</sub>	S pin Setup to I0/I1 inputs	LX devices	0.25	0.31	0.48	0.48	ns
		LXT devices	0.25	0.31	0.48	N/A	ns
T <sub>GIO</sub>	BUFGMUX delay from I0/I1 to O	LX devices	0.21	0.21	0.21	0.21	ns
		LXT devices	0.21	0.21	0.21	N/A	ns
<b>Maximum Frequency</b>							
F <sub>MAX</sub>	Global clock tree (BUFGMUX)	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 49: Input/Output Clock Switching Characteristics (BUFIO2)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T <sub>BUFCO_O</sub>	Clock to out delay from I to O	LX devices	0.67	0.82	1.09	1.50	ns
		LXT devices	0.67	0.82	1.09	N/A	ns
<b>Maximum Frequency</b>							
F <sub>MAX</sub>	I/O clock tree (BUFIO2)	LX devices	540	525	500	300	MHz
		LXT devices	540	525	500	N/A	MHz

Table 50: Input/Output Clock Switching Characteristics (BUFIO2FB)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
<b>Maximum Frequency</b>							
F <sub>MAX</sub>	I/O clock tree (BUFIO2FB)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

Table 51: Input/Output Clock Switching Characteristics (BUFPLL)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
<b>Maximum Frequency</b>							
F <sub>MAX</sub>	BUFPLL clock tree (BUFPLL)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

## PLL Switching Characteristics

Table 52: PLL Specification

Symbol	Description	Device <sup>(1)</sup>	Speed Grade				Units
			-3	-3N	-2	-1L	
F <sub>INMAX</sub>	Maximum Input Clock Frequency from I/O Clock	LX devices	540	525	450	300	MHz
		LXT devices	540	525	450	N/A	MHz
	Maximum Input Clock Frequency from Global Clock	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 54: Switching Characteristics for the Delay-Locked Loop (DLL)<sup>(1)</sup> (Cont'd)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
LOCK_DLL <sup>(3)</sup>	When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. CLKIN_FREQ_DLL < 50 MHz.	-	5	-	5	-	5	-	5	ms
	When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. CLKIN_FREQ_DLL > 50 MHz	-	0.60	-	0.60	-	0.60	-	0.60	ms
<b>Delay Lines</b>										
DCM_DELAY_STEP <sup>(5)</sup>	Finest delay resolution, averaged over all steps.	10	40	10	40	10	40	10	40	ps

**Notes:**

1. The values in this table are based on the operating conditions described in Table 2 and Table 53.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster LOCK time, use the CLKIN\_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, this data sheet specifies a maximum jitter of ±(1% of CLKIN period + 150 ps). Assuming that the CLKIN frequency is 100 MHz, the equivalent CLKIN period is 10 ns. Since 1% of 10 ns is 0.1 ns or 100 ps, the maximum jitter is ±(100 ps + 150 ps) = ±250 ps.
5. A typical delay step size is 23 ps.
6. The timing analysis tools use the CLK\_FEEDBACK = 1X condition for the CLKIN\_CLKFB\_PHASE value (reported as phase error). When using CLK\_FEEDBACK = 2X, add 100 ps to the phase error for the CLKIN\_CLKFB\_PHASE value (as shown in this table).

Table 55: Recommended Operating Conditions for the Digital Frequency Synthesizer (DFS)<sup>(1)</sup>

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
<b>Input Frequency Ranges<sup>(2)</sup></b>										
CLKIN_FREQ_FX	Frequency for the CLKIN input. Also described as F <sub>CLKIN</sub> .	0.5	375 <sup>(3)</sup>	0.5	375 <sup>(3)</sup>	0.5	333 <sup>(3)</sup>	0.5	200 <sup>(3)</sup>	MHz
<b>Input Clock Jitter Tolerance<sup>(4)</sup></b>										
CLKIN_CYC_JITT_FX_LF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: F <sub>CLKFX</sub> < 150 MHz.	-	±300	-	±300	-	±300	-	±300	ps
CLKIN_CYC_JITT_FX_HF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: F <sub>CLKFX</sub> > 150 MHz.	-	±150	-	±150	-	±150	-	±150	ps
CLKIN_PER_JITT_FX	Period jitter at the CLKIN input.	-	±1	-	±1	-	±1	-	±1	ns

**Notes:**

1. DFS specifications apply when using either of the DFS outputs (CLKFX or CLKFX180).
2. When using both DFS and DLL outputs on the same DCM, follow the more restrictive CLKIN\_FREQ\_DLL specifications in Table 53.
3. The CLKIN\_DIVIDE\_BY\_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the F<sub>MAX</sub> (see Table 48 and Table 49 for BUFG and BUFI02 limits).
4. CLKIN input jitter beyond these limits can cause the DCM to lose LOCK.

Table 56: Switching Characteristics for the Digital Frequency Synthesizer (DFS) for DCM\_SP<sup>(1)</sup>

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
<b>Output Frequency Ranges</b>										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz
<b>Output Clock Jitter<sup>(2)(3)</sup></b>										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN < 20 MHz	Use the Clocking Wizard								ps
	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN > 20 MHz	Typical = ±(1% of CLKFX period + 100)								ps
<b>Duty Cycle<sup>(4)(5)</sup></b>										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±(1% of CLKFX period + 350)								ps
<b>Phase Alignment<sup>(5)</sup></b>										
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used	-	±200	-	±200	-	±200	-	±250	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used	Maximum = ±(1% of CLKFX period + 200)								ps
<b>LOCKED Time</b>										
LOCK_FX <sup>(2)</sup>	When FCLKIN < 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	-	5	-	5	-	5	-	5	ms
	When FCLKIN > 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	-	0.45	-	0.45	-	0.45	-	0.60	ms

**Notes:**

1. The values in this table are based on the operating conditions described in Table 2 and Table 55.
2. For optimal jitter tolerance and a faster LOCK time, use the CLKIN\_PERIOD attribute.
3. Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
5. Some duty cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.

Table 64: Global Clock Input to Output Delay With DCM in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, with DCM in System-Synchronous Mode.							
T <sub>ICKOFDCM</sub>	Global Clock and OUTFF with DCM	XC6SLX4	4.23	N/A	6.11	6.60	ns
		XC6SLX9	4.23	5.17	6.11	6.60	ns
		XC6SLX16	4.28	4.57	5.34	6.36	ns
		XC6SLX25	3.95	4.18	4.59	6.91	ns
		XC6SLX25T	3.95	4.18	4.59	N/A	ns
		XC6SLX45	4.37	4.70	5.50	6.85	ns
		XC6SLX45T	4.37	4.70	5.50	N/A	ns
		XC6SLX75	3.90	4.23	4.77	6.31	ns
		XC6SLX75T	3.90	4.23	4.77	N/A	ns
		XC6SLX100	3.86	4.16	4.66	7.25	ns
		XC6SLX100T	3.90	4.16	4.66	N/A	ns
		XC6SLX150	4.03	4.33	4.83	6.63	ns
		XC6SLX150T	4.03	4.33	4.83	N/A	ns
		XA6SLX4	4.55	N/A	6.11	N/A	ns
		XA6SLX9	4.55	N/A	6.11	N/A	ns
		XA6SLX16	4.62	N/A	5.33	N/A	ns
		XA6SLX25	4.27	N/A	4.59	N/A	ns
		XA6SLX25T	4.27	N/A	4.69	N/A	ns
		XA6SLX45	4.69	N/A	5.50	N/A	ns
		XA6SLX45T	4.69	N/A	5.50	N/A	ns
		XA6SLX75	4.22	N/A	4.77	N/A	ns
		XA6SLX75T	4.22	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.34	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	6.31	ns
		XQ6SLX75T	4.22	N/A	4.77	N/A	ns
		XQ6SLX150	N/A	N/A	4.96	6.63	ns
		XQ6SLX150T	4.62	N/A	4.96	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

**Table 66: Global Clock Input to Output Delay With PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> PLL in System-Synchronous Mode.							
T <sub>ICKOFFPLL</sub>	Global Clock and OUTFF <i>with</i> PLL	XC6SLX4	4.57	N/A	6.25	7.34	ns
		XC6SLX9	4.57	5.25	6.25	7.34	ns
		XC6SLX16	4.41	4.64	5.39	6.92	ns
		XC6SLX25	4.03	4.32	4.91	7.64	ns
		XC6SLX25T	4.03	4.32	4.91	N/A	ns
		XC6SLX45	4.63	4.96	5.75	7.36	ns
		XC6SLX45T	4.63	4.96	5.75	N/A	ns
		XC6SLX75	4.01	4.30	4.88	7.15	ns
		XC6SLX75T	4.01	4.30	4.88	N/A	ns
		XC6SLX100	4.02	4.33	4.90	7.37	ns
		XC6SLX100T	4.06	4.33	4.90	N/A	ns
		XC6SLX150	3.65	3.98	4.58	6.94	ns
		XC6SLX150T	3.65	3.98	4.58	N/A	ns
		XA6SLX4	4.88	N/A	6.13	N/A	ns
		XA6SLX9	4.88	N/A	6.13	N/A	ns
		XA6SLX16	4.74	N/A	5.27	N/A	ns
		XA6SLX25	4.43	N/A	4.78	N/A	ns
		XA6SLX25T	4.43	N/A	4.88	N/A	ns
		XA6SLX45	4.94	N/A	5.62	N/A	ns
		XA6SLX45T	4.94	N/A	5.62	N/A	ns
		XA6SLX75	4.32	N/A	4.77	N/A	ns
		XA6SLX75T	4.32	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.41	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	7.15	ns
XQ6SLX75T	4.32	N/A	4.77	N/A	ns		
XQ6SLX150	N/A	N/A	4.60	6.94	ns		
XQ6SLX150T	4.35	N/A	4.60	N/A	ns		

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

**Table 67: Global Clock Input to Output Delay With PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> PLL in Source-Synchronous Mode.							
T <sub>ICKOFFLL_0</sub>	Global Clock and OUTFF <i>with</i> PLL	XC6SLX4	5.49	N/A	7.44	8.55	ns
		XC6SLX9	5.49	6.29	7.44	8.55	ns
		XC6SLX16	5.23	5.77	6.79	8.21	ns
		XC6SLX25	5.00	5.35	6.10	8.54	ns
		XC6SLX25T	5.00	5.35	6.10	N/A	ns
		XC6SLX45	5.59	6.03	7.02	8.39	ns
		XC6SLX45T	5.59	6.03	7.02	N/A	ns
		XC6SLX75	4.96	5.41	6.22	8.32	ns
		XC6SLX75T	4.96	5.41	6.22	N/A	ns
		XC6SLX100	4.97	5.42	6.21	9.08	ns
		XC6SLX100T	5.01	5.42	6.21	N/A	ns
		XC6SLX150	4.59	5.06	5.86	8.13	ns
		XC6SLX150T	4.59	5.06	5.86	N/A	ns
		XA6SLX4	5.79	N/A	7.32	N/A	ns
		XA6SLX9	5.79	N/A	7.32	N/A	ns
		XA6SLX16	5.56	N/A	6.66	N/A	ns
		XA6SLX25	5.40	N/A	5.97	N/A	ns
		XA6SLX25T	5.40	N/A	6.07	N/A	ns
		XA6SLX45	5.89	N/A	6.90	N/A	ns
		XA6SLX45T	5.89	N/A	6.90	N/A	ns
		XA6SLX75	5.27	N/A	6.12	N/A	ns
		XA6SLX75T	5.27	N/A	6.12	N/A	ns
		XA6SLX100	N/A	N/A	6.80	N/A	ns
		XQ6SLX75	N/A	N/A	6.12	8.32	ns
		XQ6SLX75T	5.27	N/A	6.12	N/A	ns
		XQ6SLX150	N/A	N/A	5.88	8.13	ns
XQ6SLX150T	5.21	N/A	5.88	N/A	ns		

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.



Table 68: Global Clock Input to Output Delay With DCM and PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, with DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.							
T <sub>ICKOFDCM_PLL</sub>	Global Clock and OUTFF with DCM and PLL	XC6SLX4	4.78	N/A	6.32	7.09	ns
		XC6SLX9	4.78	5.24	6.32	7.09	ns
		XC6SLX16	4.70	5.12	5.94	6.63	ns
		XC6SLX25	4.70	5.09	5.92	7.30	ns
		XC6SLX25T	4.70	5.09	5.92	N/A	ns
		XC6SLX45	4.63	4.98	5.83	7.26	ns
		XC6SLX45T	4.63	4.98	5.83	N/A	ns
		XC6SLX75	4.68	5.04	5.88	6.90	ns
		XC6SLX75T	4.68	5.04	5.88	N/A	ns
		XC6SLX100	4.72	5.07	5.92	7.77	ns
		XC6SLX100T	4.76	5.07	5.92	N/A	ns
		XC6SLX150	4.44	4.73	5.31	6.96	ns
		XC6SLX150T	4.44	4.73	5.31	N/A	ns
		XA6SLX4	5.07	N/A	6.18	N/A	ns
		XA6SLX9	5.07	N/A	6.18	N/A	ns
		XA6SLX16	5.22	N/A	5.77	N/A	ns
		XA6SLX25	5.01	N/A	5.80	N/A	ns
		XA6SLX25T	5.01	N/A	5.90	N/A	ns
		XA6SLX45	4.93	N/A	5.67	N/A	ns
		XA6SLX45T	4.93	N/A	5.67	N/A	ns
		XA6SLX75	4.94	N/A	5.70	N/A	ns
		XA6SLX75T	4.94	N/A	5.70	N/A	ns
		XA6SLX100	N/A	N/A	5.77	N/A	ns
		XQ6SLX75	N/A	N/A	5.70	6.90	ns
XQ6SLX75T	4.94	N/A	5.70	N/A	ns		
XQ6SLX150	N/A	N/A	5.31	6.96	ns		
XQ6SLX150T	5.02	N/A	5.31	N/A	ns		

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 69: Global Clock Input to Output Delay With DCM and PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, with DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode.							
T <sub>ICKOFDCM0_PLL</sub>	Global Clock and OUTFF with DCM and PLL	XC6SLX4	5.58	N/A	7.42	8.54	ns
		XC6SLX9	5.58	6.19	7.42	8.54	ns
		XC6SLX16	5.50	6.06	7.05	8.24	ns
		XC6SLX25	5.57	6.04	7.02	8.33	ns
		XC6SLX25T	5.57	6.04	7.02	N/A	ns
		XC6SLX45	5.53	5.97	6.96	8.32	ns
		XC6SLX45T	5.53	5.97	6.96	N/A	ns
		XC6SLX75	5.55	6.00	6.99	8.54	ns
		XC6SLX75T	5.55	6.00	6.99	N/A	ns
		XC6SLX100	5.58	6.03	7.02	9.11	ns
		XC6SLX100T	5.62	6.03	7.02	N/A	ns
		XC6SLX150	5.32	5.70	6.41	8.26	ns
		XC6SLX150T	5.32	5.70	6.41	N/A	ns
		XA6SLX4	5.87	N/A	7.28	N/A	ns
		XA6SLX9	5.87	N/A	7.28	N/A	ns
		XA6SLX16	6.02	N/A	6.87	N/A	ns
		XA6SLX25	5.88	N/A	6.90	N/A	ns
		XA6SLX25T	5.88	N/A	7.00	N/A	ns
		XA6SLX45	5.82	N/A	6.81	N/A	ns
		XA6SLX45T	5.82	N/A	6.81	N/A	ns
		XA6SLX75	5.81	N/A	6.80	N/A	ns
		XA6SLX75T	5.81	N/A	6.80	N/A	ns
		XA6SLX100	N/A	N/A	6.88	N/A	ns
		XQ6SLX75	N/A	N/A	6.80	8.54	ns
XQ6SLX75T	5.81	N/A	6.80	N/A	ns		
XQ6SLX150	N/A	N/A	6.41	8.26	ns		
XQ6SLX150T	5.90	N/A	6.41	N/A	ns		

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 72: Global Clock Setup and Hold With DCM in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
<b>Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.<sup>(1)</sup></b>							
T <sub>PSDCM</sub> / T <sub>PHDCM</sub>	No Delay Global Clock and IFF <sup>(2)</sup> with DCM in System-Synchronous Mode	XC6SLX4	1.54/0.06	N/A	1.75/0.12	2.84/0.27	ns
		XC6SLX9	1.54/0.06	1.63/0.12	1.75/0.12	2.84/0.27	ns
		XC6SLX16	1.72/-0.18	1.87/-0.17	2.13/-0.17	2.31/0.26	ns
		XC6SLX25	1.70/-0.03	1.78/-0.02	2.00/-0.02	2.88/0.20	ns
		XC6SLX25T	1.70/0.07	1.78/0.08	2.00/0.08	N/A	ns
		XC6SLX45	1.74/-0.03	1.84/-0.02	2.02/-0.02	2.64/0.52	ns
		XC6SLX45T	1.74/-0.01	1.84/0.00	2.02/0.00	N/A	ns
		XC6SLX75	1.86/0.11	1.98/0.12	2.20/0.12	2.96/0.58	ns
		XC6SLX75T	1.86/0.11	1.98/0.12	2.20/0.12	N/A	ns
		XC6SLX100	1.64/0.07	1.72/0.08	1.97/0.08	2.70/0.99	ns
		XC6SLX100T	1.64/0.09	1.72/0.10	1.97/0.10	N/A	ns
		XC6SLX150	1.53/0.39	1.62/0.40	1.82/0.40	2.75/1.00	ns
		XC6SLX150T	1.53/0.39	1.62/0.40	1.82/0.40	N/A	ns
		XA6SLX4	1.65/0.16	N/A	1.75/0.26	N/A	ns
		XA6SLX9	1.65/0.16	N/A	1.75/0.26	N/A	ns
		XA6SLX16	1.88/0.02	N/A	2.13/0.03	N/A	ns
		XA6SLX25	1.80/0.16	N/A	2.05/0.17	N/A	ns
		XA6SLX25T	1.80/0.16	N/A	2.13/0.17	N/A	ns
		XA6SLX45	1.75/0.12	N/A	2.02/0.13	N/A	ns
		XA6SLX45T	1.75/0.12	N/A	2.02/0.13	N/A	ns
		XA6SLX75	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XA6SLX75T	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XA6SLX100	N/A	N/A	2.46/0.24	N/A	ns
		XQ6SLX75	N/A	N/A	2.20/0.12	2.96/0.58	ns
		XQ6SLX75T	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XQ6SLX150	N/A	N/A	1.82/0.56	2.75/1.00	ns
		XQ6SLX150T	1.65/0.55	N/A	1.82/0.56	N/A	ns

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 79: Package Skew (Cont'd)

Symbol	Description	Device	Package <sup>(2)</sup>	Value	Units
T <sub>PKGSKEW</sub>	Package Skew <sup>(1)</sup>	LX45	CSG324	70	ps
			CS(G)484	99	ps
			FG(G)484	109	ps
			FG(G)676	138	ps
		LX45T	CSG324	75	ps
			CS(G)484	100	ps
			FG(G)484	95	ps
		LX75	CS(G)484	101	ps
			FG(G)484	107	ps
			FG(G)676	161	ps
			LX75T	CS(G)484	107
		FG(G)484		110	ps
		FG(G)676		134	ps
		LX100	CS(G)484	95	ps
			FG(G)484	155	ps
			FG(G)676	144	ps
		LX100T	CS(G)484	88	ps
			FG(G)484	111	ps
			FG(G)676	147	ps
			FG(G)900	134	ps
		LX150	CS(G)484	84	ps
			FG(G)484	103	ps
			FG(G)676	115	ps
			FG(G)900	121	ps
LX150T	CS(G)484	83	ps		
	FG(G)484	88	ps		
	FG(G)676	141	ps		
	FG(G)900	120	ps		

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from Pad to Ball.
2. Some of the devices are available in both Pb and Pb-free (additional G) packages as standard ordering options. See [DS160: Spartan-6 Family Overview](#) for more information.

Table 80: Sample Window

Symbol	Description	Device <sup>(1)</sup>	Speed Grade				Units
			-3	-3N	-2	-1L	
T <sub>SAMP</sub>	Sampling Error at Receiver Pins <sup>(2)</sup>	All	510	510	530	740	ps
T <sub>SAMP_BUFIO2</sub>	Sampling Error at Receiver Pins using BUFIO2 <sup>(3)</sup>	All	430	430	450	590	ps

Notes:

1. LXT devices are not available with a -1L speed grade.
2. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
  - CLK0 DCM jitter
  - DCM accuracy (phase offset)
  - DCM phase shift resolution
 These measurements do not include package or clock tree skew.
3. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO2 clock network and IODELAY2 to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

## Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
08/26/09	1.1	Added $V_{FS}$ to <a href="#">Table 1</a> and <a href="#">Table 2</a> . Added $R_{FUSE}$ to <a href="#">Table 2</a> . Added XC6SLX75 and XC6SLX75T to $V_{BATT}$ and $I_{BATT}$ in <a href="#">Table 1</a> , <a href="#">Table 2</a> , and <a href="#">Table 4</a> . Corrected the quiescent supply current for the XC6SLX4 in <a href="#">Table 5</a> . Updated <a href="#">Table 11</a> . Removed $DV_{PPIN}$ from <a href="#">Figure 2</a> . Removed $F_{PCIECORE}$ from <a href="#">Table 24</a> and added values to $F_{PCIEUSER}$ . Added more networking applications to <a href="#">Table 25</a> . Updated values for $T_{SUSPENDLOW\_AWAKE}$ , $T_{SUSPEND\_ENABLE}$ , and $T_{SCP\_AWAKE}$ in <a href="#">Table 46</a> . Numerous changes to <a href="#">Table 47</a> , <a href="#">page 54</a> including the addition of new values to various specifications, revising the $T_{SMCKCSO}$ description, and changing the units of $T_{POR}$ . Also, removed <i>Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK</i> section from <a href="#">Table 47</a> and updated all the notes. In <a href="#">Table 52</a> , added to $F_{INMAX}$ , revised $F_{OUTMAX}$ , and removed PLL Maximum Output Frequency for BUFIO2. Revised values for DCM_DELAY_STEP in <a href="#">Table 54</a> . Updated CLKIN_FREQ_FX values in <a href="#">Table 55</a> .
01/04/10	1.2	Added -4 speed grade to entire document. Updated speed specification of -4, -3, -2 speed grades to version 1.03. Added -1L speed grade numbers per speed specification 1.00. Updated $T_{SOL}$ in <a href="#">Table 1</a> . Added -1L rows for LVCMOS12, LVCMOS15, and LVCMOS18 in <a href="#">Table 9</a> . Revised much of the detail in <i>GTP Transceiver Specifications</i> in <a href="#">Table 12</a> through <a href="#">Table 23</a> . Added -2 data to <a href="#">Table 25</a> . Updated $F_{MAX}$ in <a href="#">Table 44</a> . Updated descriptions for $T_{DNACLKL}$ and $T_{DNACLKH}$ in <a href="#">Table 45</a> and revised values for all parameters. Removed $T_{INITADDR}$ from <a href="#">Table 47</a> and added new data. Updated values in <a href="#">Table 48</a> through <a href="#">Table 62</a> . Added <a href="#">Table 51</a> (BUFPLL) and <a href="#">Table 57</a> (DCM_CLKGEN). Removed $T_{LOCKMAX}$ note from <a href="#">Table 52</a> . Updated note 3 in <a href="#">Table 53</a> . In <a href="#">Table 79</a> : removed XC6SLX75CSG324 and XC6SLX75TCSG324; added XC6SLX75FG(G)484 and XC6SLX75FG(G)484.
02/22/10	1.3	Production release of XC6SLX16 -2 speed grade devices. The changes to <a href="#">Table 26</a> and <a href="#">Table 27</a> includes updating this data sheet to the data in ISE v11.5 software with speed specification v1.06. Updated maximum of $V_{IN}$ and $V_{TS}$ and note 2 in <a href="#">Table 1</a> . In <a href="#">Table 2</a> , changed $V_{IN}$ , added $I_{IN}$ and note 5, revised notes 1, 6, and 7, and added note 8 to $R_{FUSE}$ . In <a href="#">Table 4</a> , removed previous note 1 and added data to $I_{RPU}$ , $I_{RPD}$ , and $I_{BATT}$ , changed $C_{IN}$ , added $R_{DT}$ and $R_{IN\_TERM}$ , and added note 2 and 3. Updated $V_{CCO2}$ in <a href="#">Table 6</a> . Added <a href="#">Table 7</a> and <a href="#">Table 8</a> . Removed PCI66_3 from <a href="#">Table 9</a> . Updated PCI33_3 and I2C in <a href="#">Table 9</a> . Updated the description of <a href="#">Table 11</a> . Completely updated <a href="#">Table 25</a> . Updated <a href="#">Table 28</a> including adding values for PCI33_3. Updated $V_{REF}$ value for HSTL_III_18 in <a href="#">Table 31</a> . Updates missing $V_{REF}$ values in <a href="#">Table 32</a> . Added <i>Simultaneously Switching Outputs</i> , <a href="#">page 36</a> . Removed $T_{GSRQ}$ and $T_{RPW}$ from <a href="#">Table 35</a> and <a href="#">Table 36</a> . Also removed $T_{DOQ}$ from <a href="#">Table 36</a> . Removed $T_{ISDO\_DO}$ and note 1 from <a href="#">Table 37</a> . Removed $T_{OSCK\_S}$ and combinatorial section from <a href="#">Table 38</a> . In <a href="#">Table 39</a> , removed $T_{IODDO\_T}$ and added new tap parameters and note 2. In <a href="#">Table 40</a> , <a href="#">Table 41</a> , and <a href="#">Table 42</a> , made typographical edits and removed notes. Removed clock CLK section in <a href="#">Table 41</a> . Removed clock CLK section and $T_{REG\_MUX}$ and $T_{REG\_M31}$ in <a href="#">Table 42</a> . Added block RAM $F_{MAX}$ values to <a href="#">Table 43</a> . Updated values and added note 2 to <a href="#">Table 45</a> . Added values to <a href="#">Table 46</a> and removed note 1. Numerous changes to <a href="#">Table 47</a> . Completely updated <a href="#">Table 57</a> . Revised data in <a href="#">Table 62</a> . Removed note 3 from <a href="#">Table 71</a> . Added values to <a href="#">Table 79</a> . Added data to <a href="#">Table 80</a> and <a href="#">Table 81</a> .
03/10/10	1.4	Production release of XC6SLX45 -2 speed grade devices, which includes changes to <a href="#">Table 26</a> and <a href="#">Table 27</a> updating this data sheet to the data in ISE v11.5 software with speed specification v1.07. Fixed $R_{IN\_TERM}$ description in <a href="#">Table 4</a> . Added PCI66_3 to <a href="#">Table 7</a> and replaced note 1. Corrected note 1 and the V, Max for TMDS_33 in <a href="#">Table 8</a> . In <a href="#">Table 10</a> , added note 1 to LVPECL_33 and TMDS_33. Also updated specifications for TMDS_33. Updated the <i>GTP Transceiver Specifications</i> section including adding values to <a href="#">Table 16</a> , <a href="#">Table 17</a> , and <a href="#">Table 20</a> through <a href="#">Table 23</a> . Added PCI66_3 back into <a href="#">Table 9</a> , <a href="#">Table 28</a> , <a href="#">Table 31</a> , <a href="#">Table 32</a> , and <a href="#">Table 34</a> . Updated note 3 on <a href="#">Table 32</a> . In <a href="#">Table 34</a> , corrected some typographical errors and fixed SSO limits for bank1/3 in FG(G)484 package. Corrected $T_{OSCKC\_OCE}$ in <a href="#">Table 38</a> . In <a href="#">Table 57</a> , updated CLKFX_FREEZE_VAR and CLKFX_FREEZE_TEMP_SLOPE and added typical values to $T_{CENTER\_LOW\_SPREAD}$ and $T_{CENTER\_HIGH\_SPREAD}$ . Updated and added values to <a href="#">Table 63</a> through <a href="#">Table 78</a> , and <a href="#">Table 81</a> . In <a href="#">Table 79</a> , revised the XC6SLX16-CSG324 and the XC6SLX45-CSG484 and FG(G)484 values.