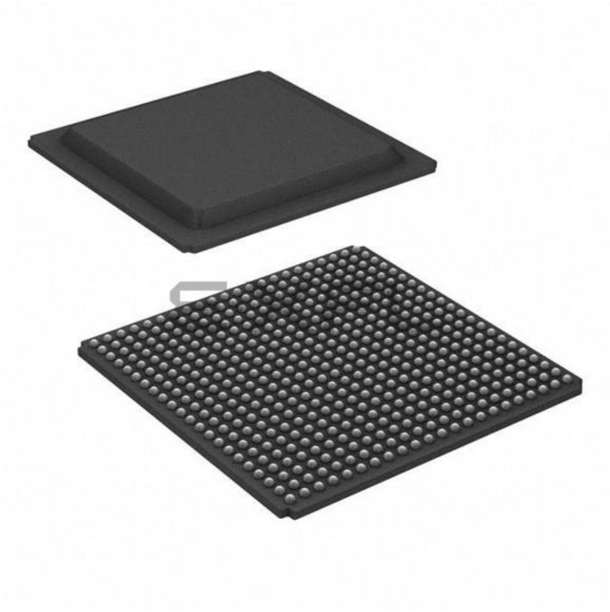
AMD Xilinx - XC6SLX45-2FGG484C Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	3411
Number of Logic Elements/Cells	43661
Total RAM Bits	2138112
Number of I/O	316
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx45-2fgg484c

Quiescent Current

Typical values for quiescent supply current are specified at nominal voltage, 25°C junction temperatures (T_j). Quiescent supply current is specified by speed grade for Spartan-6 devices. Xilinx recommends analyzing static power consumption using the XPOWER™ Estimator (XPE) tool (download at http://www.xilinx.com/power) for conditions other than those specified in Table 5.

Table 5: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	LX4	4.0	4.0	4.0	2.4	mA
		LX9	4.0	4.0	4.0	2.4	mA
		LX16	6.0	6.0	6.0	4.0	mA
		LX25	11.0	11.0	11.0	6.6	mA
		LX25T	11.0	11.0	11.0	N/A	mA
		LX45	15.0	15.0	15.0	9.0	mA
		LX45T	15.0	15.0	15.0	N/A	mA
		LX75	29.0	29.0	29.0	17.4	mA
		LX75T	29.0	29.0	29.0	N/A	mA
		LX100	36.0	36.0	36.0	21.6	mA
		LX100T	36.0	36.0	36.0	N/A	mA
		LX150	51.0	51.0	51.0	31.0	mA
		LX150T	51.0	51.0	51.0	N/A	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	LX4	1.0	1.0	1.0	1.0	mA
		LX9	1.0	1.0	1.0	1.0	mA
		LX16	2.0	2.0	2.0	2.0	mA
		LX25	2.0	2.0	2.0	2.0	mA
		LX25T	2.0	2.0	2.0	N/A	mA
		LX45	3.0	3.0	3.0	3.0	mA
		LX45T	3.0	3.0	3.0	N/A	mA
		LX75	4.0	4.0	4.0	4.0	mA
		LX75T	4.0	4.0	4.0	N/A	mA
		LX100	5.0	5.0	5.0	5.0	mA
		LX100T	5.0	5.0	5.0	N/A	mA
		LX150	7.0	7.0	7.0	7.0	mA
		LX150T	7.0	7.0	7.0	N/A	mA

SelectIO™ Interface DC Input and Output Levels

Table 7: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

I/O Standard	V_{CCO} for Drivers[1]			V_{REF} for Inputs		
	V, Min	V, Nom	V, Max	V, Min	V, Nom	V, Max
LVTTL	3.0	3.3	3.45	V_{REF} is not used for these I/O standards		
LVCMOS33	3.0	3.3	3.45			
LVCMOS25	2.3	2.5	2.7			
LVCMOS18	1.65	1.8	1.95			
LVCMOS18_JEDEC	1.65	1.8	1.95			
LVCMOS15	1.4	1.5	1.6			
LVCMOS15_JEDEC	1.4	1.5	1.6			
LVCMOS12	1.1	1.2	1.3			
LVCMOS12_JEDEC	1.1	1.2	1.3			
PCI33_3[2]	3.0	3.3	3.45			
PCI66_3[2]	3.0	3.3	3.45			
I2C	2.7	3.0	3.45			
SMBUS	2.7	3.0	3.45			
SDIO	3.0	3.3	3.45			
MOBILE_DDR	1.7	1.8	1.9			
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_II	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_III	1.4	1.5	1.6	–	0.9	–
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–
HSTL_III_18	1.7	1.8	1.9	–	1.1	–
SSTL3_I	3.0	3.3	3.45	1.3	1.5	1.7
SSTL3_II	3.0	3.3	3.45	1.3	1.5	1.7
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38
SSTL18_I	1.7	1.8	1.9	0.833	0.9	0.969
SSTL18_II	1.7	1.8	1.9	0.833	0.9	0.969
SSTL15_II	1.425	1.5	1.575	0.69	0.75	0.81

Notes:

1. V_{CCO} range required when using I/O standard for an output. Also required for MOBILE_DDR, PCI33_3, LVCMOS18_JEDEC, LVCMOS15_JEDEC, and LVCMOS12_JEDEC inputs, and for LVCMOS25 inputs when V_{CCAUX} = 3.3V.
2. For PCI systems, the transmitter and receiver should have common supplies for V_{CCO}.

In Table 9 and Table 10, values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: **Single-Ended I/O Standard DC Input and Output Levels**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL	–0.5	0.8	2.0	4.1	0.4	2.4	Note 2	Note 2
LVCMOS33	–0.5	0.8	2.0	4.1	0.4	V_{CCO} – 0.4	Note 2	Note 2
LVCMOS25	–0.5	0.7	1.7	4.1	0.4	V_{CCO} – 0.4	Note 2	Note 2
LVCMOS18	–0.5	0.38	0.8	4.1	0.45	V_{CCO} – 0.45	Note 2	Note 2
LVCMOS18 (-1L)	–0.5	0.33	0.71	4.1	0.45	V_{CCO} – 0.45	Note 2	Note 2
LVCMOS18_JEDEC	–0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.45	V_{CCO} – 0.45	Note 2	Note 2
LVCMOS15	–0.5	0.38	0.8	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVCMOS15 (-1L)	–0.5	0.33	0.71	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVCMOS15_JEDEC	–0.5	35% V_{CCO}	65% V_{CCO}	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVCMOS12	–0.5	0.38	0.8	4.1	0.4	V_{CCO} – 0.4	Note 4	Note 4
LVCMOS12 (-1L)	–0.5	0.33	0.71	4.1	0.4	V_{CCO} – 0.4	Note 4	Note 4
LVCMOS12_JEDEC	–0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.4	V_{CCO} – 0.4	Note 4	Note 4
PCI33_3	–0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
PCI66_3	–0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
I2C	–0.5	25% V_{CCO}	70% V_{CCO}	4.1	20% V_{CCO}	–	3	–
SMBUS	–0.5	0.8	2.1	4.1	0.4	–	4	–
SDIO	–0.5	12.5% V_{CCO}	75% V_{CCO}	4.1	12.5% V_{CCO}	75% V_{CCO}	0.1	–0.1
MOBILE_DDR	–0.5	20% V_{CCO}	80% V_{CCO}	4.1	10% V_{CCO}	90% V_{CCO}	0.1	–0.1
HSTL_I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	8	–8
HSTL_II	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	16	–16
HSTL_III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	24	–8
HSTL_I_18	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	11	–11
HSTL_II_18	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	22	–22
HSTL_III_18	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	0.4	V_{CCO} – 0.4	30	–11
SSTL3_I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	4.1	V_{TT} – 0.6	V_{TT} + 0.6	8	–8
SSTL3_II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	4.1	V_{TT} – 0.8	V_{TT} + 0.8	16	–16
SSTL2_I	–0.5	V_{REF} – 0.15	V_{REF} + 0.15	4.1	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2_II	–0.5	V_{REF} – 0.15	V_{REF} + 0.15	4.1	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL18_I	–0.5	V_{REF} – 0.125	V_{REF} + 0.125	4.1	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18_II	–0.5	V_{REF} – 0.125	V_{REF} + 0.125	4.1	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
SSTL15_II	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	4.1	V_{TT} – 0.4	V_{TT} + 0.4	13.4	–13.4

Notes:

1. Tested according to relevant specifications.
2. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
3. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
4. Using drive strengths of 2, 4, 6, 8, or 12 mA.
5. For more information, refer to UG381: *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 10: **Differential I/O Standard DC Input and Output Levels**

I/O Standard	V_{ID}		V_{ICM}		V_{OD}		V_{OCM}		V_{OH}	V_{OL}
	mV, Min	mV, Max	V, Min	V, Max	mV, Min	mV, Max	V, Min	V, Max	V, Min	V, Max
LVDS_33(2)(3)	100	600	0.3	2.35	247	454	1.125	1.375	–	–
LVDS_25(2)(3)	100	600	0.3	2.35	247	454	1.125	1.375	–	–
BLVDS_25(2)(3)	100	–	0.3	2.35	240	460	Typical 50% V_{CCO}		–	–
MINI_LVDS_33	200	600	0.3	1.95	300	600	1.0	1.4	–	–
MINI_LVDS_25	200	600	0.3	1.95	300	600	1.0	1.4	–	–
LVPECL_33(2)(3)	100	1000	0.3	2.8(1)	Inputs only					
LVPECL_25(2)(3)	100	1000	0.3	1.95	Inputs only					
RSDS_33(2)(3)	100	–	0.3	1.5	100	400	1.0	1.4	–	–
RSDS_25(2)(3)	100	–	0.3	1.5	100	400	1.0	1.4	–	–
TMDS_33	150	1200	2.7	3.23(1)	400	800	$V_{CCO} - 0.405$	$V_{CCO} - 0.190$	–	–
PPDS_33(2)(3)	100	400	0.2	2.3	100	400	0.5	1.4	–	–
PPDS_25(2)(3)	100	400	0.2	2.3	100	400	0.5	1.4	–	–
DISPLAY_PORT	190	1260	0.3	2.35	–	–	Typical 50% V_{CCO}		–	–
DIFF_MOBILE_DDR	100	–	0.78	1.02	–	–	–	–	90% V_{CCO}	10% V_{CCO}
DIFF_HSTL_I	100	–	0.68	0.9	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_II	100	–	0.68	0.9	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_III	100	–	0.68	0.9	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_I_18	100	–	0.8	1.1	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_II_18	100	–	0.8	1.1	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_III_18	100	–	0.8	1.1	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_SSTL3_I	100	–	1.0	1.9	–	–	–	–	$V_{TT} + 0.6$	$V_{TT} - 0.6$
DIFF_SSTL3_II	100	–	1.0	1.9	–	–	–	–	$V_{TT} + 0.8$	$V_{TT} - 0.8$
DIFF_SSTL2_I	100	–	1.0	1.5	–	–	–	–	$V_{TT} + 0.61$	$V_{TT} - 0.61$
DIFF_SSTL2_II	100	–	1.0	1.5	–	–	–	–	$V_{TT} + 0.81$	$V_{TT} - 0.81$
DIFF_SSTL18_I	100	–	0.7	1.1	–	–	–	–	$V_{TT} + 0.47$	$V_{TT} - 0.47$
DIFF_SSTL18_II	100	–	0.7	1.1	–	–	–	–	$V_{TT} + 0.6$	$V_{TT} - 0.6$
DIFF_SSTL15_II	100	–	0.55	0.95	–	–	–	–	$V_{TT} + 0.4$	$V_{TT} - 0.4$

Notes:

1. LVPECL_33 and TMDS_33 maximum V_{ICM} is the lower of V (maximum) or $V_{CCAUX} - (V_{ID}/2)$
2. When $V_{CCAUX} = 3.3V$, the DCD can be higher than 5% for $V_{ICM} < 0.7V$ when using these I/O standards: LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, LVPECL_33, RSDS_25, RSDS_33, PPDS_25, and PPDS_33.
3. The -1L devices require $V_{CCAUX} = 2.5V$ when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 27 lists the production released Spartan-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE® software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 27: **Spartan-6 Device Production Software and Speed Specification Release[1]**

Device	Speed Grade Designations[2]			
	-3[3]	-3N	-2[4]	-1L
XC6SLX4	ISE 12.4 v1.15	N/A	ISE 12.3 v1.12[5]	ISE 13.2 v1.07
XC6SLX9	ISE 12.4 v1.15	ISE 13.1 Update v1.18[7]	ISE 12.3 v1.12[5]	ISE 13.2 v1.07
XC6SLX16	ISE 12.1 v1.08	ISE 13.1 Update v1.18[7]	ISE 11.5 v1.06	ISE 13.2 v1.07
XC6SLX25	ISE 12.2 v1.11[6]	ISE 13.1 Update v1.18[7]	ISE 12.2 v1.11[6]	ISE 13.2 v1.07
XC6SLX25T	ISE 12.2 v1.11[6]	ISE 13.1 Update v1.18[7]	ISE 12.2 v1.11[6]	N/A
XC6SLX45	ISE 12.1 v1.08	ISE 13.1 Update v1.18[7]	ISE 11.5 v1.07	ISE 13.1 v1.06
XC6SLX45T	ISE 12.1 v1.08	ISE 13.1 Update v1.18[7]	ISE 12.1 v1.08	N/A
XC6SLX75	ISE 12.2 v1.11[6]	ISE 13.1 Update v1.18[7]	ISE 12.2 v1.11[6]	ISE 13.2 v1.07
XC6SLX75T	ISE 12.2 v1.11[6]	ISE 13.1 Update v1.18[7]	ISE 12.2 v1.11[6]	N/A
XC6SLX100	ISE 12.2 v1.11[6]	ISE 13.1 Update v1.18[7]	ISE 12.2 v1.11[6]	ISE 13.1 v1.06
XC6SLX100T	ISE 12.2 v1.11[6]	ISE 13.1 Update v1.18[7]	ISE 12.2 v1.11[6]	N/A
XC6SLX150	ISE 12.2 v1.11[6]	ISE 13.1 Update v1.18[7]	ISE 12.2 v1.11[6]	ISE 13.1 v1.06
XC6SLX150T	ISE 12.2 v1.11[6]	ISE 13.1 Update v1.18[7]	ISE 12.2 v1.11[6]	N/A
XA6SLX4	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX9	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX16	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX25	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX25T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX45	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX45T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX75	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX75T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX100	N/A	N/A	ISE 13.3 v1.20	N/A

Table 27: **Spartan-6 Device Production Software and Speed Specification Release[1] *(Cont'd)***

Device	Speed Grade Designations[2]			
	-3[3]	-3N	-2[4]	-1L
XQ6SLX75	N/A	N/A	ISE 13.2 v1.19	ISE 13.2 v1.07
XQ6SLX75T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XQ6SLX150	N/A	N/A	ISE 13.2 v1.19	ISE 13.2 v1.07
XQ6SLX150T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A

Notes:

1. ISE 13.3 software with v1.20 for -3, -3N, and -2; and v1.08 for -1L speed specification reflects the changes outlined in XCN11028: *Spartan-6 FPGA Speed File Changes*.
2. As marked with an N/A, LXT devices and all XA devices are not available with a -1L speed grade; LX4 devices and all XA and XQ devices are not available with a -3N speed grade.
3. Improved -3 specifications reflected in this data sheet require ISE 12.4 software with v1.15 speed specification.
4. Improved -2 specifications reflected in this data sheet require ISE 12.4 software and the *12.4 Speed Files Patch* which contains the v1.17 speed specification available on the Xilinx Download Center.
5. ISE 12.3 software with v1.12 speed specification is available using ISE 12.3 software and the *12.3 Speed Files Patch* available on the Xilinx Download Center.
6. ISE 12.2 software with v1.11 speed specification is available using ISE 12.2 software and the *12.2 Speed Files Patch* available on the Xilinx Download Center.
7. ISE 13.1 software with v1.18 speed specification is available using ISE 13.1 software and the *13.1 Update* available on the Xilinx Download Center. See XCN11012: *Speed File Change for -3N Devices*.

IOB Pad Input/Output/3-State Switching Characteristics

Table 28 (for commercial (XC) Spartan-6 devices) and Table 29 (for Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices) summarizes the values of standard-specific data input delays, output delays terminating at pads (based on standard), and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

See the TRACE report for further information on delays when using an I/O standard with UNTUNED termination on inputs or outputs.

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	
LVDS_33	1.17	1.29	1.42	1.68	1.55	1.69	1.89	2.42	3000	3000	3000	3000	ns
LVDS_25	1.01	1.13	1.26	1.57	1.65	1.79	1.99	2.47	3000	3000	3000	3000	ns
BLVDS_25	1.02	1.14	1.27	1.57	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
MINI_LVDS_33	1.17	1.29	1.42	1.68	1.57	1.71	1.91	2.41	3000	3000	3000	3000	ns
MINI_LVDS_25	1.01	1.13	1.26	1.57	1.65	1.79	1.99	2.47	3000	3000	3000	3000	ns
LVPECL_33	1.18	1.30	1.43	1.68	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL_25	1.02	1.14	1.27	1.57	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
RSDS_33 (point to point)	1.17	1.29	1.42	1.68	1.57	1.71	1.91	2.42	3000	3000	3000	3000	ns
RSDS_25 (point to point)	1.01	1.13	1.26	1.56	1.65	1.79	1.99	2.47	3000	3000	3000	3000	ns
TMDS_33	1.21	1.33	1.46	1.71	1.54	1.68	1.88	2.50	3000	3000	3000	3000	ns

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L(1)	-3	-3N	-2	-1L(1)	-3	-3N	-2	-1L(1)	
LVCMOS33, Fast, 8 mA	1.34	1.46	1.59	1.82	2.07	2.21	2.41	3.03	2.07	2.21	2.41	3.03	ns
LVCMOS33, Fast, 12 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns
LVCMOS33, Fast, 16 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns
LVCMOS33, Fast, 24 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns
LVCMOS25, QUIETIO, 2 mA	0.82	0.94	1.07	1.31	4.81	4.95	5.15	5.79	4.81	4.95	5.15	5.79	ns
LVCMOS25, QUIETIO, 4 mA	0.82	0.94	1.07	1.31	3.70	3.84	4.04	4.66	3.70	3.84	4.04	4.66	ns
LVCMOS25, QUIETIO, 6 mA	0.82	0.94	1.07	1.31	3.46	3.60	3.80	4.38	3.46	3.60	3.80	4.38	ns
LVCMOS25, QUIETIO, 8 mA	0.82	0.94	1.07	1.31	3.20	3.34	3.54	4.12	3.20	3.34	3.54	4.12	ns
LVCMOS25, QUIETIO, 12 mA	0.82	0.94	1.07	1.31	2.83	2.97	3.17	3.75	2.83	2.97	3.17	3.75	ns
LVCMOS25, QUIETIO, 16 mA	0.82	0.94	1.07	1.31	2.64	2.78	2.98	3.64	2.64	2.78	2.98	3.64	ns
LVCMOS25, QUIETIO, 24 mA	0.82	0.94	1.07	1.31	2.45	2.59	2.79	3.42	2.45	2.59	2.79	3.42	ns
LVCMOS25, Slow, 2 mA	0.82	0.94	1.07	1.31	3.78	3.92	4.12	4.76	3.78	3.92	4.12	4.76	ns
LVCMOS25, Slow, 4 mA	0.82	0.94	1.07	1.31	2.79	2.93	3.13	3.73	2.79	2.93	3.13	3.73	ns
LVCMOS25, Slow, 6 mA	0.82	0.94	1.07	1.31	2.73	2.87	3.07	3.66	2.73	2.87	3.07	3.66	ns
LVCMOS25, Slow, 8 mA	0.82	0.94	1.07	1.31	2.48	2.62	2.82	3.42	2.48	2.62	2.82	3.42	ns
LVCMOS25, Slow, 12 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.95	2.01	2.15	2.35	2.95	ns
LVCMOS25, Slow, 16 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.95	2.01	2.15	2.35	2.95	ns
LVCMOS25, Slow, 24 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.94	2.01	2.15	2.35	2.94	ns
LVCMOS25, Fast, 2 mA	0.82	0.94	1.07	1.31	3.35	3.49	3.69	4.31	3.35	3.49	3.69	4.31	ns
LVCMOS25, Fast, 4 mA	0.82	0.94	1.07	1.31	2.25	2.39	2.59	3.22	2.25	2.39	2.59	3.22	ns
LVCMOS25, Fast, 6 mA	0.82	0.94	1.07	1.31	2.09	2.23	2.43	3.05	2.09	2.23	2.43	3.05	ns
LVCMOS25, Fast, 8 mA	0.82	0.94	1.07	1.31	2.02	2.16	2.36	2.98	2.02	2.16	2.36	2.98	ns
LVCMOS25, Fast, 12 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns
LVCMOS25, Fast, 16 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns
LVCMOS25, Fast, 24 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns
LVCMOS18, QUIETIO, 2 mA	1.18	1.30	1.43	2.04	5.92	6.06	6.26	6.80	5.92	6.06	6.26	6.80	ns
LVCMOS18, QUIETIO, 4 mA	1.18	1.30	1.43	2.04	4.74	4.88	5.08	5.63	4.74	4.88	5.08	5.63	ns
LVCMOS18, QUIETIO, 6 mA	1.18	1.30	1.43	2.04	4.05	4.19	4.39	4.96	4.05	4.19	4.39	4.96	ns
LVCMOS18, QUIETIO, 8 mA	1.18	1.30	1.43	2.04	3.71	3.85	4.05	4.63	3.71	3.85	4.05	4.63	ns
LVCMOS18, QUIETIO, 12 mA	1.18	1.30	1.43	2.04	3.35	3.49	3.69	4.27	3.35	3.49	3.69	4.27	ns
LVCMOS18, QUIETIO, 16 mA	1.18	1.30	1.43	2.04	3.20	3.34	3.54	4.14	3.20	3.34	3.54	4.14	ns
LVCMOS18, QUIETIO, 24 mA	1.18	1.30	1.43	2.04	2.96	3.10	3.30	3.98	2.96	3.10	3.30	3.98	ns
LVCMOS18, Slow, 2 mA	1.18	1.30	1.43	2.04	4.62	4.76	4.96	5.54	4.62	4.76	4.96	5.54	ns
LVCMOS18, Slow, 4 mA	1.18	1.30	1.43	2.04	3.69	3.83	4.03	4.60	3.69	3.83	4.03	4.60	ns
LVCMOS18, Slow, 6 mA	1.18	1.30	1.43	2.04	3.00	3.14	3.34	3.94	3.00	3.14	3.34	3.94	ns
LVCMOS18, Slow, 8 mA	1.18	1.30	1.43	2.04	2.19	2.33	2.53	3.17	2.19	2.33	2.53	3.17	ns
LVCMOS18, Slow, 12 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18, Slow, 16 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns

Table 29: **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices**(1)

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVDS_33	1.24	1.42	1.69	1.89	3000	3000	ns
LVDS_25	1.08	1.26	1.79	1.99	3000	3000	ns
BLVDS_25	1.09	1.27	1.86	2.06	1.86	2.06	ns
MINI_LVDS_33	1.25	1.43	1.71	1.91	3000	3000	ns
MINI_LVDS_25	1.08	1.26	1.79	1.99	3000	3000	ns
LVPECL_33	1.25	1.43	N/A	N/A	N/A	N/A	ns
LVPECL_25	1.09	1.27	N/A	N/A	N/A	N/A	ns
RSDS_33 (point to point)	1.24	1.42	1.71	1.91	3000	3000	ns
RSDS_25 (point to point)	1.08	1.26	1.79	1.99	3000	3000	ns
TMDS_33	1.29	1.47	1.68	1.88	3000	3000	ns
PPDS_33	1.25	1.43	1.71	1.91	3000	3000	ns
PPDS_25	1.08	1.26	1.82	2.02	3000	3000	ns
PCI33_3	1.14	1.32	3.81	4.01	3.81	4.01	ns
PCI66_3	1.14	1.32	3.81	4.01	3.81	4.01	ns
DISPLAY_PORT	1.09	1.27	3.29	3.49	3.29	3.49	ns
I2C	1.40	1.58	11.70	11.90	11.70	11.90	ns
SMBUS	1.40	1.58	11.70	11.90	11.70	11.90	ns
SDIO	1.43	1.61	2.78	2.98	2.78	2.98	ns
MOBILE_DDR	1.01	1.19	2.50	2.70	2.50	2.70	ns
HSTL_I	1.01	1.19	1.80	2.00	1.80	2.00	ns
HSTL_II	1.01	1.19	1.86	2.06	1.86	2.06	ns
HSTL_III	1.07	1.25	1.81	2.01	1.81	2.01	ns
HSTL_I _18	1.05	1.23	1.91	2.11	1.91	2.11	ns
HSTL_II _18	1.05	1.23	1.99	2.19	1.99	2.19	ns
HSTL_III _18	1.13	1.31	1.93	2.13	1.93	2.13	ns
SSTL3_I	1.65	1.83	1.97	2.17	1.97	2.17	ns
SSTL3_II	1.65	1.83	2.15	2.35	2.15	2.35	ns
SSTL2_I	1.37	1.55	1.91	2.11	1.91	2.11	ns
SSTL2_II	1.37	1.55	2.00	2.20	2.00	2.20	ns
SSTL18_I	0.99	1.17	1.77	1.97	1.77	1.97	ns
SSTL18_II	1.00	1.18	1.80	2.00	1.80	2.00	ns
SSTL15_II	1.00	1.18	1.81	2.01	1.81	2.01	ns
DIFF_HSTL_I	1.01	1.19	1.91	2.11	1.91	2.11	ns
DIFF_HSTL_II	1.00	1.18	1.86	2.06	1.86	2.06	ns
DIFF_HSTL_III	1.00	1.18	1.83	2.03	1.83	2.03	ns
DIFF_HSTL_I_18	1.04	1.22	1.93	2.13	1.93	2.13	ns
DIFF_HSTL_II_18	1.04	1.22	1.83	2.03	1.83	2.03	ns
DIFF_HSTL_III_18	1.04	1.22	1.83	2.03	1.83	2.03	ns

Table 29: **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices[1]** ***(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVCMOS33, Slow, 6 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVCMOS33, Slow, 8 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVCMOS33, Slow, 12 mA	1.41	1.59	2.53	2.73	2.53	2.73	ns
LVCMOS33, Slow, 16 mA	1.41	1.59	2.45	2.65	2.45	2.65	ns
LVCMOS33, Slow, 24 mA	1.41	1.59	2.42	2.62	2.42	2.62	ns
LVCMOS33, Fast, 2 mA	1.41	1.59	4.05	4.25	4.05	4.25	ns
LVCMOS33, Fast, 4 mA	1.41	1.59	2.66	2.86	2.66	2.86	ns
LVCMOS33, Fast, 6 mA	1.41	1.59	2.46	2.66	2.46	2.66	ns
LVCMOS33, Fast, 8 mA	1.41	1.59	2.21	2.41	2.21	2.41	ns
LVCMOS33, Fast, 12 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVCMOS33, Fast, 16 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVCMOS33, Fast, 24 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVCMOS25, QUIETIO, 2 mA	0.89	1.07	5.00	5.20	5.00	5.20	ns
LVCMOS25, QUIETIO, 4 mA	0.89	1.07	3.85	4.05	3.85	4.05	ns
LVCMOS25, QUIETIO, 6 mA	0.89	1.07	3.60	3.80	3.60	3.80	ns
LVCMOS25, QUIETIO, 8 mA	0.89	1.07	3.34	3.54	3.34	3.54	ns
LVCMOS25, QUIETIO, 12 mA	0.89	1.07	2.98	3.18	2.98	3.18	ns
LVCMOS25, QUIETIO, 16 mA	0.89	1.07	2.79	2.99	2.79	2.99	ns
LVCMOS25, QUIETIO, 24 mA	0.89	1.07	2.64	2.84	2.64	2.84	ns
LVCMOS25, Slow, 2 mA	0.89	1.07	3.96	4.16	3.96	4.16	ns
LVCMOS25, Slow, 4 mA	0.89	1.07	2.96	3.16	2.96	3.16	ns
LVCMOS25, Slow, 6 mA	0.89	1.07	2.88	3.08	2.88	3.08	ns
LVCMOS25, Slow, 8 mA	0.89	1.07	2.63	2.83	2.63	2.83	ns
LVCMOS25, Slow, 12 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVCMOS25, Slow, 16 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVCMOS25, Slow, 24 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVCMOS25, Fast, 2 mA	0.89	1.07	3.52	3.72	3.52	3.72	ns
LVCMOS25, Fast, 4 mA	0.89	1.07	2.43	2.63	2.43	2.63	ns
LVCMOS25, Fast, 6 mA	0.89	1.07	2.23	2.43	2.23	2.43	ns
LVCMOS25, Fast, 8 mA	0.89	1.07	2.16	2.36	2.16	2.36	ns
LVCMOS25, Fast, 12 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVCMOS25, Fast, 16 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVCMOS25, Fast, 24 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVCMOS18, QUIETIO, 2 mA	1.25	1.43	6.11	6.31	6.11	6.31	ns
LVCMOS18, QUIETIO, 4 mA	1.25	1.43	4.88	5.08	4.88	5.08	ns
LVCMOS18, QUIETIO, 6 mA	1.25	1.43	4.20	4.40	4.20	4.40	ns
LVCMOS18, QUIETIO, 8 mA	1.25	1.43	3.86	4.06	3.86	4.06	ns
LVCMOS18, QUIETIO, 12 mA	1.25	1.43	3.49	3.69	3.49	3.69	ns

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 4 and Figure 5.

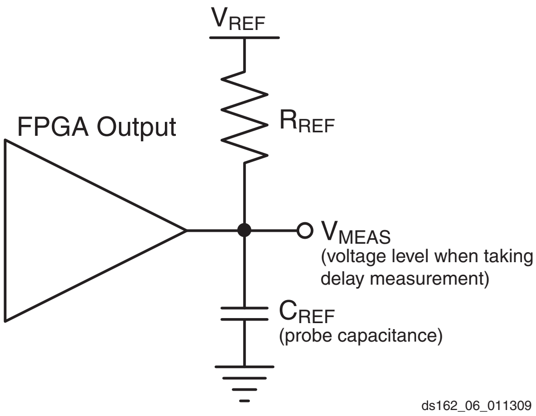


Figure 4: **Single-Ended Test Setup**

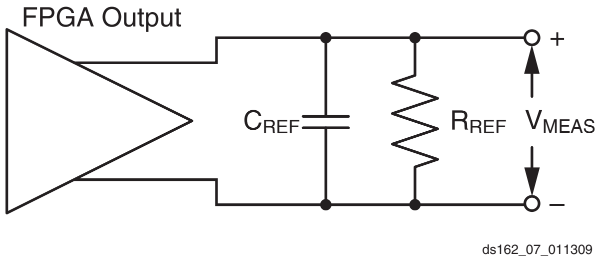


Figure 5: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 32.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 32: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}(1) (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.4	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
PCI (Peripheral Component Interface) 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3 (rising edge)	25	10(2)	0.94	0
	PCI33_3, PCI66_3 (falling edge)	25	10(2)	2.03	3.3
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25

Table 32: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[(1)] (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
SSTL, Class II, 1.5V	SSTL15_II	25	0	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	100	0	0(3)	–
BLVDS (Bus LVDS), 2.5V	BLVDS_25	Note 4	0	0(3)	–
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	100	0	0(3)	–
RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RSDS_25, RSDS_33	100	0	0(3)	–
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	Note 5	0	0(3)	–
PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V	PPDS_25, PPDS_33	100	0	0(3)	–

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. The value given is the differential output voltage.
4. See the *BLVDS Output Termination* section in UG381, *Spartan-6 FPGA SelectIO Resources User Guide*.
5. See the *TMDS_33 Termination* section in UG381, *Spartan-6 FPGA SelectIO Resources User Guide*.

Simultaneously Switching Outputs

Due to package electrical parasitics, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. Table 33 and Table 34 provide guidelines for the recommended maximum allowable number of SSOs. These guidelines describe the maximum number of user I/O pins of an output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise for that particular signal standard. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of GND and power bounce.

For each device/package combination, Table 33 provides the number of equivalent V_{CCO}/GND pairs per bank. For each output signal standard and drive strength, Table 34 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines are categorized by package style, slew rate, and output drive current. The number of SSOs are also specified by I/O bank. Multiply the appropriate numbers from each table to calculate the maximum number of SSOs allowed within an I/O bank. The guidelines assume that all pins within a bank use the same I/O standard. Exceeding these SSO guidelines can result in increased power or GND bounce, degraded signal integrity, or increased system jitter. For a given I/O standard, if the SSO limit per pair in Table 34 is greater than the maximum I/O per pair in Table 33, then there is no SSO limit for the exclusive use of that I/O standard.

The recommended maximum SSO values assume that the FPGA is soldered on a printed circuit board and that the board uses sound design practices. Due to the additional inductance introduced by the socket, the SSO values do not apply for FPGAs mounted in sockets. The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics. For more detail, see UG381: *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 34: **SSO Limit per V_{CCO}/GND Pair *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
Various	LVDS_33			16	N/A	16	N/A
	LVDS_25			20	N/A	20	N/A
	BLVDS_25			20	48	20	20
	MINI_LVDS_33			13	N/A	13	N/A
	MINI_LVDS_25			18	N/A	18	N/A
	RSDS_33			12	N/A	12	N/A
	RSDS_25			15	N/A	15	N/A
	TMDS_33			83	N/A	83	N/A
	PPDS_33			12	N/A	12	N/A
	PPDS_25			16	N/A	16	N/A
	DISPLAY_PORT			42	40	42	30
	I2C			47	55	47	42
	SMBUS			44	52	44	40

Notes:

1. SSO limits greater than the number of I/O per V_{CCO}/GND pair (Table 33) indicate No Limit for the given I/O standard. They are provided in this table to calculate limits when using multiple I/O standards in a bank.
2. Not available (N/A) indicates that the I/O standard is not available in the given bank.
3. When used with the MCB, these signals are exempt from SSO analysis due to the known activity of the MCB switching patterns. SSO performance is validated for all MCB instances. MCB outputs can, in some cases, exceed the SSO limits.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 41: **CLB Distributed RAM Switching Characteristics (SLICEM Only)**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Sequential Delays						
T_{SHCKO}	Clock to A – D outputs	1.26	1.55	1.55	2.35	ns, Max
	Clock to A – D outputs (direct output path)	0.96	1.20	1.20	1.87	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS}/T_{DH}	AX – DX or AI – DI inputs to CLK	0.59/ 0.17	0.73/ 0.22	0.73/ 0.22	1.17/ 0.33	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock for XC devices	0.28/ 0.35	0.32/ 0.42	0.32/ 0.42	0.26/ 0.71	ns, Min
	Address An inputs to clock for XA and XQ devices	0.28/ 0.51	N/A	0.32/ 0.51	0.26/ 0.71	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.31/ –0.08	0.37/ –0.08	0.37/ –0.08	0.59/ –0.27	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.31/ –0.08	0.37/ –0.08	0.37/ –0.08	0.59/ –0.27	ns, Min

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 42: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	1.35	1.78	1.78	2.74	ns, Max
	Clock to A – D outputs (direct output path)	1.24	1.65	1.65	2.48	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS}/T_{WH}	WE input to CLK	0.20/ –0.07	0.24/ –0.07	0.24/ –0.07	0.29/ –0.27	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK for XC devices	0.30/ 0.30	0.30/ 0.38	0.30/ 0.38	0.82/ –0.41	ns, Min
	CE input to CLK for XA and XQ devices	0.32/ 0.30	N/A	0.40/ 0.38	0.82/ –0.41	ns, Min
T_{DS}/T_{DH}	AX – DX or AI – DI inputs to CLK	0.07/ 0.11	0.09/ 0.14	0.09/ 0.14	0.11/ 0.23	ns, Min

Block RAM Switching Characteristics

Table 43: **Block RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Block RAM Clock to Out Delays						
T_{RCKO_DO}	Clock CLK to DOUT output (without output register)(1)	1.85	2.10	2.10	3.50	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register)(2)	1.60	1.75	1.75	2.30	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs for XC devices(3)	0.35/0.10	0.40/0.12	0.40/0.12	0.50/0.15	ns, Min
	ADDR inputs for XA and XQ devices(3)	0.35/0.17	N/A	0.40/0.17	0.50/0.15	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs(4)	0.30/0.10	0.30/0.10	0.30/0.10	0.40/0.15	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.22/0.05	0.25/0.06	0.25/0.06	0.44/0.10	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.20/0.10	0.20/0.10	0.20/0.10	0.28/0.15	ns, Min
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input	0.25/0.10	0.33/0.10	0.33/0.10	0.28/0.15	ns, Min
Maximum Frequency						
F_{MAX}	Block RAM in all modes	320	280	280	150	MHz

Notes:

1. T_{RCKO_DO} includes T_{RCKO_DOA} and T_{RCKO_DOPA} as well as the B port equivalent timing parameters.
2. $T_{RCKO\_DO\_REG}$ includes $T_{RCKO\_DOA\_REG}$ and $T_{RCKO\_DOPA\_REG}$ as well as the B port equivalent timing parameters.
3. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
4. T_{RDCK_DI} includes both A and B inputs as well as the parity inputs of A and B.

Clock Buffers and Networks

Table 48: **Global Clock Switching Characteristics (BUFGMUX)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T_{GSI}	S pin Setup to I0/I1 inputs	LX devices	0.25	0.31	0.48	0.48	ns
		LXT devices	0.25	0.31	0.48	N/A	ns
T_{GIO}	BUFGMUX delay from I0/I1 to O	LX devices	0.21	0.21	0.21	0.21	ns
		LXT devices	0.21	0.21	0.21	N/A	ns
Maximum Frequency							
F_{MAX}	Global clock tree (BUFGMUX)	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 49: **Input/Output Clock Switching Characteristics (BUFIO2)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T_{BUFCKO_O}	Clock to out delay from I to O	LX devices	0.67	0.82	1.09	1.50	ns
		LXT devices	0.67	0.82	1.09	N/A	ns
Maximum Frequency							
F_{MAX}	I/O clock tree (BUFIO2)	LX devices	540	525	500	300	MHz
		LXT devices	540	525	500	N/A	MHz

Table 50: **Input/Output Clock Switching Characteristics (BUFIO2FB)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
Maximum Frequency							
F_{MAX}	I/O clock tree (BUFIO2FB)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

Table 51: **Input/Output Clock Switching Characteristics (BUFPLL)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
Maximum Frequency							
F_{MAX}	BUFPLL clock tree (BUFPLL)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

PLL Switching Characteristics

Table 52: **PLL Specification**

Symbol	Description	Device(1)	Speed Grade				Units
			-3	-3N	-2	-1L	
F_{INMAX}	Maximum Input Clock Frequency from I/O Clock	LX devices	540	525	450	300	MHz
		LXT devices	540	525	450	N/A	MHz
	Maximum Input Clock Frequency from Global Clock	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 65: **Global Clock Input to Output Delay With DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in Source-Synchronous Mode.							
$T_{ICKOFDCM\_0}$	Global Clock and OUTFF *with* DCM	XC6SLX4	5.03	N/A	7.21	8.05	ns
		XC6SLX9	5.03	6.13	7.21	8.05	ns
		XC6SLX16	5.08	5.51	6.44	7.96	ns
		XC6SLX25	4.81	5.13	5.69	7.94	ns
		XC6SLX25T	4.81	5.13	5.69	N/A	ns
		XC6SLX45	5.26	5.69	6.63	7.92	ns
		XC6SLX45T	5.26	5.69	6.63	N/A	ns
		XC6SLX75	4.77	5.18	5.88	7.95	ns
		XC6SLX75T	4.77	5.18	5.88	N/A	ns
		XC6SLX100	4.72	5.11	5.76	8.59	ns
		XC6SLX100T	4.76	5.11	5.76	N/A	ns
		XC6SLX150	4.90	5.30	5.93	7.93	ns
		XC6SLX150T	4.90	5.30	5.93	N/A	ns
		XA6SLX4	5.35	N/A	7.21	N/A	ns
		XA6SLX9	5.35	N/A	7.21	N/A	ns
		XA6SLX16	5.42	N/A	6.44	N/A	ns
		XA6SLX25	5.13	N/A	5.69	N/A	ns
		XA6SLX25T	5.13	N/A	5.79	N/A	ns
		XA6SLX45	5.58	N/A	6.63	N/A	ns
		XA6SLX45T	5.58	N/A	6.63	N/A	ns
		XA6SLX75	5.09	N/A	5.87	N/A	ns
		XA6SLX75T	5.09	N/A	5.87	N/A	ns
		XA6SLX100	N/A	N/A	6.44	N/A	ns
		XQ6SLX75	N/A	N/A	5.87	7.95	ns
		XQ6SLX75T	5.09	N/A	5.87	N/A	ns
		XQ6SLX150	N/A	N/A	6.06	7.93	ns
		XQ6SLX150T	5.50	N/A	6.06	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 74: Global Clock Setup and Hold With PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.[1]							
T_{PSPLL}/ T_{PHPLL}	No Delay Global Clock and IFF[2] with PLL in System-Synchronous Mode	XC6SLX4	1.37/0.25	N/A	1.52/0.41	2.07/0.69	ns
		XC6SLX9	1.37/0.21	1.48/0.21	1.52/0.26	2.07/0.69	ns
		XC6SLX16	1.33/–0.03	1.53/–0.02	1.60/–0.02	1.57/0.48	ns
		XC6SLX25	1.65/0.28	1.71/0.28	1.91/0.28	2.44/0.76	ns
		XC6SLX25T	1.65/0.28	1.71/0.28	1.91/0.28	N/A	ns
		XC6SLX45	1.55/0.18	1.64/0.18	1.75/0.18	2.02/0.90	ns
		XC6SLX45T	1.55/0.18	1.64/0.18	1.75/0.18	N/A	ns
		XC6SLX75	1.77/0.21	1.89/0.21	2.13/0.21	2.46/0.53	ns
		XC6SLX75T	1.77/0.21	1.89/0.21	2.13/0.21	N/A	ns
		XC6SLX100	1.44/0.32	1.52/0.32	1.70/0.32	1.78/0.86	ns
		XC6SLX100T	1.44/0.32	1.52/0.32	1.70/0.32	N/A	ns
		XC6SLX150	1.39/0.49	1.48/0.49	1.67/0.49	1.94/0.94	ns
		XC6SLX150T	1.39/0.49	1.48/0.49	1.67/0.49	N/A	ns
		XA6SLX4	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX9	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX16	1.89/–0.08	N/A	1.72/–0.08	N/A	ns
		XA6SLX25	1.85/0.16	N/A	2.08/0.16	N/A	ns
		XA6SLX25T	1.85/0.16	N/A	2.17/0.16	N/A	ns
		XA6SLX45	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX45T	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX75	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX100	N/A	N/A	2.34/0.14	N/A	ns
		XQ6SLX75	N/A	N/A	2.25/0.06	2.46/0.53	ns
		XQ6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XQ6SLX150	N/A	N/A	1.79/0.37	1.94/0.94	ns
		XQ6SLX150T	1.43/0.37	N/A	1.79/0.37	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 81: **Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out Using BUFIO2**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO2							
T_{PSCS}/T_{PHCS}	IFF setup/hold using BUFIO2 clock	XC6SLX4	0.57/0.94	N/A	0.95/1.12	0.27/1.56	ns
		XC6SLX9	0.40/0.95	0.50/0.96	0.60/1.12	0.27/1.56	ns
		XC6SLX16	0.48/0.74	0.55/0.75	0.69/0.83	1.27/1.31	ns
		XC6SLX25	0.28/1.02	0.28/1.12	0.28/1.24	0.15/1.78	ns
		XC6SLX25T	0.28/1.02	0.28/1.12	0.28/1.24	N/A	ns
		XC6SLX45	0.42/1.19	0.44/1.29	0.50/1.40	0.12/1.83	ns
		XC6SLX45T	0.42/1.19	0.44/1.29	0.50/1.40	N/A	ns
		XC6SLX75	0.38/1.48	0.38/1.63	0.38/1.84	0.05/2.78	ns
		XC6SLX75T	0.38/1.48	0.38/1.63	0.38/1.84	N/A	ns
		XC6SLX100	0.06/1.48	0.06/1.63	0.06/1.87	–0.03/2.72	ns
		XC6SLX100T	0.06/1.48	0.06/1.63	0.06/1.87	N/A	ns
		XC6SLX150	0.04/1.73	0.04/1.75	0.04/1.98	–0.08/3.07	ns
		XC6SLX150T	0.04/1.73	0.04/1.75	0.04/1.98	N/A	ns
		XA6SLX4	0.64/0.96	N/A	0.97/1.12	N/A	ns
		XA6SLX9	0.44/0.99	N/A	0.62/1.16	N/A	ns
		XA6SLX16	0.50/0.78	N/A	0.69/0.83	N/A	ns
		XA6SLX25	0.28/1.04	N/A	0.28/1.25	N/A	ns
		XA6SLX25T	0.28/1.04	N/A	0.28/1.25	N/A	ns
		XA6SLX45	0.43/1.21	N/A	0.50/1.40	N/A	ns
		XA6SLX45T	0.43/1.21	N/A	0.50/1.40	N/A	ns
		XA6SLX75	0.38/1.49	N/A	0.38/1.84	N/A	ns
		XA6SLX75T	0.38/1.49	N/A	0.38/1.84	N/A	ns
		XA6SLX100	N/A	N/A	1.01/1.63	N/A	ns
		XQ6SLX75	N/A	N/A	0.38/1.84	0.05/2.78	ns
		XQ6SLX75T	0.38/1.49	N/A	0.38/1.84	N/A	ns
		XQ6SLX150	N/A	N/A	0.04/1.98	–0.08/3.07	ns
		XQ6SLX150T	0.04/1.75	N/A	0.04/1.98	N/A	ns

Table 81: **Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out Using BUFIO2** ***(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Pin-to-Pin Clock-to-Out Using BUFIO2							
$T_{ICKOFCS}$	OFF clock-to-out using BUFIO2 clock	XC6SLX4	5.51	N/A	6.95	8.45	ns
		XC6SLX9	5.51	5.89	6.95	8.45	ns
		XC6SLX16	5.31	5.70	6.67	8.21	ns
		XC6SLX25	5.53	6.00	7.02	8.72	ns
		XC6SLX25T	5.53	6.00	7.02	N/A	ns
		XC6SLX45	5.76	6.18	7.22	8.77	ns
		XC6SLX45T	5.76	6.18	7.22	N/A	ns
		XC6SLX75	5.94	6.46	7.57	9.72	ns
		XC6SLX75T	5.94	6.46	7.57	N/A	ns
		XC6SLX100	6.09	6.53	7.60	9.66	ns
		XC6SLX100T	6.09	6.53	7.60	N/A	ns
		XC6SLX150	6.29	6.69	7.81	9.94	ns
		XC6SLX150T	6.29	6.69	7.81	N/A	ns
		XA6SLX4	5.83	N/A	6.95	N/A	ns
		XA6SLX9	5.83	N/A	6.95	N/A	ns
		XA6SLX16	5.65	N/A	6.68	N/A	ns
		XA6SLX25	5.85	N/A	7.03	N/A	ns
		XA6SLX25T	5.85	N/A	7.03	N/A	ns
		XA6SLX45	6.07	N/A	7.25	N/A	ns
		XA6SLX45T	6.07	N/A	7.25	N/A	ns
		XA6SLX75	6.26	N/A	7.57	N/A	ns
		XA6SLX75T	6.26	N/A	7.57	N/A	ns
		XA6SLX100	N/A	N/A	7.48	N/A	ns
		XQ6SLX75	N/A	N/A	7.57	9.72	ns
		XQ6SLX75T	6.26	N/A	7.57	N/A	ns
		XQ6SLX150	N/A	N/A	7.81	9.94	ns
		XQ6SLX150T	6.62	N/A	7.81	N/A	ns

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
08/26/09	1.1	Added V_{FS} to Table 1and Table 2. Added R_{FUSE} to Table 2. Added XC6SLX75 and XC6SLX75T to V_{BATT} and I_{BATT} in Table 1, Table 2, and Table 4. Corrected the quiescent supply current for the XC6SLX4 in Table 5. Updated Table 11. Removed DV_{PPIN} from Figure 2. Removed $F_{PCIECORE}$ from Table 24 and added values to $F_{PCIEUSER}$. Added more networking applications to Table 25. Updated values for $T_{SUSPENDLOW\_AWAKE}$, $T_{SUSPEND\_ENABLE}$, and T_{SCP_AWAKE} in Table 46. Numerous changes to Table 47, page 54 including the addition of new values to various specifications, revising the $T_{SMCKCSO}$ description, and changing the units of T_{POR}. Also, removed *Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK section* from Table 47 and updated all the notes. In Table 52, added to F_{INMAX}, revised F_{OUTMAX}, and removed PLL Maximum Output Frequency for BUFIO2. Revised values for DCM_DELAY_STEP in Table 54. Updated CLKIN_FREQ_FX values in Table 55.
01/04/10	1.2	Added -4 speed grade to entire document. Updated speed specification of -4, -3, -2 speed grades to version 1.03. Added -1L speed grade numbers per speed specification 1.00. Updated T_{SOL} in Table 1. Added -1L rows for LVCMOS12, LVCMOS15, and LVCMOS18 in Table 9. Revised much of the detail in GTP Transceiver Specifications in Table 12 through Table 23. Added -2 data to Table 25. Updated F_{MAX} in Table 44. Updated descriptions for $T_{DNACLKL}$ and $T_{DNACLKH}$ in Table 45 and revised values for all parameters. Removed $T_{INITADDR}$ from Table 47 and added new data. Updated values in Table 48 through Table 62. Added Table 51 (BUFPLL) and Table 57 (DCM_CLKGEN). Removed $T_{LOCKMAX}$ note from Table 52. Updated note 3 in Table 53. In Table 79: removed XC6SLX75CSG324 and XC6SLX75TCSG324; added XC6SLX75FG(G)484 and XC6SLX75FG(G)484.
02/22/10	1.3	Production release of XC6SLX16 -2 speed grade devices. The changes to Table 26 and Table 27 includes updating this data sheet to the data in ISE v11.5 software with speed specification v1.06. Updated maximum of V_{IN} and V_{TS} and note 2 in Table 1. In Table 2, changed V_{IN}, added I_{IN} and note 5, revised notes 1, 6, and 7, and added note 8 to R_{FUSE}. In Table 4, removed previous note 1 and added data to I_{RPU}, I_{RPD}, and I_{BATT}, changed C_{IN}, added R_{DT} and R_{IN_TERM}, and added note 2 and 3. Updated V_{CCO2} in Table 6. Added Table 7 and Table 8. Removed PCI66_3 from Table 9. Updated PCI33_3 and I2C in Table 9. Updated the description of Table 11. Completely updated Table 25. Updated Table 28 including adding values for PCI33_3. Updated V_{REF} value for HSTL_III_18 in Table 31. Updates missing V_{REF} values in Table 32. Added Simultaneously Switching Outputs, page 36. Removed T_{GSRQ} and T_{RPW} from Table 35 and Table 36. Also removed T_{DOQ} from Table 36. Removed T_{ISDO_DO} and note 1 from Table 37. Removed T_{OSCCK_S} and combinatorial section from Table 38. In Table 39, removed T_{IODDO_T} and added new tap parameters and note 2. In Table 40, Table 41, and Table 42, made typographical edits and removed notes. Removed clock CLK section in Table 41. Removed clock CLK section and T_{REG_MUX} and T_{REG_M31} in Table 42. Added block RAM F_{MAX} values to Table 43. Updated values and added note 2 to Table 45. Added values to Table 46 and removed note 1. Numerous changes to Table 47. Completely updated Table 57. Revised data in Table 62. Removed note 3 from Table 71. Added values to Table 79. Added data to Table 80 and Table 81.
03/10/10	1.4	Production release of XC6SLX45 -2 speed grade devices, which includes changes to Table 26 and Table 27 updating this data sheet to the data in ISE v11.5 software with speed specification v1.07. Fixed R_{IN_TERM} description in Table 4. Added PCI66_3 to Table 7 and replaced note 1. Corrected note 1 and the V, Max for TMDS_33 in Table 8. In Table 10, added note 1 to LVPECL_33 and TMDS_33. Also updated specifications for TMDS_33. Updated the GTP Transceiver Specifications section including adding values to Table 16, Table 17, and Table 20 through Table 23. Added PCI66_3 back into Table 9, Table 28, Table 31, Table 32, and Table 34. Updated note 3 on Table 32. In Table 34, corrected some typographical errors and fixed SSO limits for bank1/3 in FG(G)484 package. Corrected T_{OSCKC_OCE} in Table 38. In Table 57, updated CLKFX_FREEZE_VAR and CLKFX_FREEZE_TEMP_SLOPE and added typical values to $T_{CENTER\_LOW\_SPREAD}$ and $T_{CENTER\_HIGH\_SPREAD}$. Updated and added values to Table 63 through Table 78, and Table 81. In Table 79, revised the XC6SLX16-CSG324 and the XC6SLX45-CSG484 and FG(G)484 values.