



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	3411
Number of Logic Elements/Cells	43661
Total RAM Bits	2138112
Number of I/O	358
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx45-3fg676i

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description					Units
V_{IN} and V_{TS} ⁽³⁾	I/O input voltage or voltage applied to 3-state output, relative to GND ⁽⁴⁾	All user and dedicated I/Os	Commercial	DC	–0.60 to 4.10	V
				20% overshoot duration	–0.75 to 4.25	V
				8% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
			Industrial	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
			Expanded (Q)	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
		Restricted to maximum of 100 user I/Os	Commercial	20% overshoot duration	–0.75 to 4.35	V
				15% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
				10% overshoot duration	–0.75 to 4.45	V
			Industrial	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
			Expanded (Q)	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
T_{STG}	Storage temperature (ambient)				–65 to 150	°C
T_{SOL}	Maximum soldering temperature ⁽⁶⁾ (TQG144, CPG196, CSG225, CSG324, CSG484, and FTG256)				+260	°C
	Maximum soldering temperature ⁽⁶⁾ (Pb-free packages: FGG484, FGG676, and FGG900)				+250	°C
	Maximum soldering temperature ⁽⁶⁾ (Pb packages: CS484, FT256, FG484, FG676, and FG900)				+220	°C
T_j	Maximum junction temperature ⁽⁶⁾				+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- When programming eFUSE, $V_{FS} \leq V_{CCAUX}$. Requires up to 40 mA current. For read mode, V_{FS} can be between GND and 3.45 V.
- I/O absolute maximum limit applied to DC and AC signals. Overshoot duration is the percentage of a data period that the I/O is stressed beyond 3.45V.
- For I/O operation, refer to [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.
- Maximum percent overshoot duration to meet 4.40V maximum.
- For soldering guidelines and thermal considerations, see [UG385](#): *Spartan-6 FPGA Packaging and Pinout Specification*.

Table 2: Recommended Operating Conditions⁽¹⁾

Symbol	Description			Min	Typ	Max	Units
V _{CCINT}	Internal supply voltage relative to GND	-3, -3N, -2	Standard performance ⁽²⁾	1.14	1.2	1.26	V
		-3, -2	Extended performance ⁽²⁾	1.2	1.23	1.26	V
		-1L	Standard performance ⁽²⁾	0.95	1.0	1.05	V
V _{CCAUX} ⁽³⁾⁽⁴⁾	Auxiliary supply voltage relative to GND	V _{CCAUX} = 2.5V ⁽⁵⁾		2.375	2.5	2.625	V
		V _{CCAUX} = 3.3V		3.15	3.3	3.45	V
V _{CCO} ⁽⁶⁾⁽⁷⁾⁽⁸⁾	Output supply voltage relative to GND			1.1	–	3.45	V
V _{IN}	Input voltage relative to GND	All I/O standards (except PCI)	Commercial temperature (C)	–0.5	–	4.0	V
			Industrial temperature (I)	–0.5	–	3.95	V
			Expanded (Q) temperature	–0.5	–	3.95	V
		PCI I/O standard ⁽⁹⁾		–0.5	–	V _{CCO} + 0.5	V
I _{IN} ⁽¹⁰⁾	Maximum current through pin using PCI I/O standard when forward biasing the clamp diode. ⁽⁹⁾	Commercial (C) and Industrial temperature (I)		–	–	10	mA
		Expanded (Q) temperature		–	–	7	mA
V _{BATT} ⁽¹¹⁾	Battery voltage relative to GND, T _j = 0°C to +85°C (LX75, LX75T, LX100, LX100T, LX150, and LX150T only)			1.0	–	3.6	V
T _j	Junction temperature operating range	Commercial (C) range		0	–	85	°C
		Industrial temperature (I) range		–40	–	100	°C
		Expanded (Q) temperature range		–40	–	125	°C

Notes:

- All voltages are relative to ground.
- See *Interface Performances for Memory Interfaces* in Table 25. The extended performance range is specified for designs not using the standard V_{CCINT} voltage range. The standard V_{CCINT} voltage range is used for:
 - Designs that do not use an MCB
 - LX4 devices
 - Devices in the TQG144 or CPG196 packages
 - Devices with the -3N speed grade
- Recommended maximum voltage droop for V_{CCAUX} is 10 mV/ms.
- During configuration, if V_{CCO_2} is 1.8V, then V_{CCAUX} must be 2.5V.
- The -1L devices require $V_{CCAUX} = 2.5V$ when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.
- Configuration data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
- For PCI systems, the transmitter and receiver should have common supplies for V_{CCO} .
- Devices with a -1L speed grade do not support Xilinx PCI IP.
- Do not exceed a total of 100 mA per bank.
- V_{BATT} is required to maintain the battery backed RAM (BBR) AES key when V_{CCAUX} is not applied. Once V_{CCAUX} is applied, V_{BATT} can be unconnected. When BBR is not used, Xilinx recommends connecting to V_{CCAUX} or GND. However, V_{BATT} can be unconnected.

Table 21: GTP Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Conditions	Speed Grade				Units
			-3	-3N	-2	-1L	
F _{TXOUT}	TXOUTCLK maximum frequency		320	320	270	N/A	MHz
F _{RXREC}	RXRECCLK maximum frequency		320	320	270	N/A	MHz
T _{RX}	RXUSRCLK maximum frequency		320	320	270	N/A	MHz
T _{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz
T _{TX}	TXUSRCLK maximum frequency		320	320	270	N/A	MHz
T _{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz

Notes:

1. Clocking must be implemented as described in [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#).

Table 22: GTP Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
T _{RTX}	TX Rise time	20%–80%	–	140	–	ps
T _{FTX}	TX Fall time	80%–20%	–	120	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	400	ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–	20	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–	50	ns
T _{J3.125}	Total Jitter ⁽²⁾	3.125 Gb/s	–	–	0.35	UI
D _{J3.125}	Deterministic Jitter ⁽²⁾		–	–	0.15	UI
T _{J2.5}	Total Jitter ⁽²⁾	2.5 Gb/s	–	–	0.33	UI
D _{J2.5}	Deterministic Jitter ⁽²⁾		–	–	0.15	UI
T _{J1.62}	Total Jitter ⁽²⁾	1.62 Gb/s	–	–	0.20	UI
D _{J1.62}	Deterministic Jitter ⁽²⁾		–	–	0.10	UI
T _{J1.25}	Total Jitter ⁽²⁾	1.25 Gb/s	–	–	0.20	UI
D _{J1.25}	Deterministic Jitter ⁽²⁾		–	–	0.10	UI
T _{J614}	Total Jitter ⁽²⁾	614 Mb/s	–	–	0.10	UI
D _{J614}	Deterministic Jitter ⁽²⁾		–	–	0.05	UI

Notes:

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP transceiver sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.

Table 23: GTP Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units	
T _{RXELECIDLE}	Time for RXELECIDLE to respond to loss or restoration of data		–	75	–	ns	
R _{XOVBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV	
R _{XSST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	0	ppm	
R _{XRL}	Run length (CID)	Internal AC capacitor bypassed	–	–	150	UI	
R _{XPMTOL}	Data/REFCLK PPM offset tolerance	CDR 2 nd -order loop disabled	–200	–	200	ppm	
		CDR 2 nd -order loop enabled	PLL_RXDIVSEL_OUT = 1	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 2	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 4	–1000	–	1000	ppm
SJ Jitter Tolerance ⁽²⁾							
JT_SJ _{3.125}	Sinusoidal Jitter ⁽³⁾	3.125 Gb/s	0.4	–	–	UI	
JT_SJ _{2.5}	Sinusoidal Jitter ⁽³⁾	2.5 Gb/s	0.4	–	–	UI	
JT_SJ _{1.62}	Sinusoidal Jitter ⁽³⁾	1.62 Gb/s	0.5	–	–	UI	
JT_SJ _{1.25}	Sinusoidal Jitter ⁽³⁾	1.25 Gb/s	0.5	–	–	UI	
JT_SJ ₆₁₄	Sinusoidal Jitter ⁽³⁾	614 Mb/s	0.5	–	–	UI	
SJ Jitter Tolerance with Stressed Eye ⁽²⁾⁽⁵⁾							
JT_TJSE _{3.125}	Total Jitter with stressed eye ⁽⁴⁾	3.125 Gb/s	0.65	–	–	UI	
JT_SJSE _{3.125}	Sinusoidal Jitter with stressed eye	3.125 Gb/s	0.1	–	–	UI	
JT_TJSE _{2.7}	Total Jitter with stressed eye ⁽⁴⁾	2.7 Gb/s	0.65	–	–	UI	
JT_SJSE _{2.7}	Sinusoidal Jitter with stressed eye	2.7 Gb/s	0.1	–	–	UI	

Notes:

- Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
- All jitter values are based on a Bit Error Ratio of 1e⁻¹².
- Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
- Composed of 0.37 UI DJ in the form of ISI and 0.18 UI RJ.
- Measured using PRBS7 data pattern.

Endpoint Block for PCI Express Designs Switching Characteristics

The Endpoint block for PCI Express is available in the Spartan-6 LXT devices. Consult the [Spartan-6 FPGA Integrated Endpoint Block for PCI Express](#) for further information.

Table 24: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
F _{PCIEUSER}	User clock maximum frequency	62.5	62.5	62.5	N/A	MHz

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVDS_33	1.24	1.42	1.69	1.89	3000	3000	ns
LVDS_25	1.08	1.26	1.79	1.99	3000	3000	ns
BLVDS_25	1.09	1.27	1.86	2.06	1.86	2.06	ns
MINI_LVDS_33	1.25	1.43	1.71	1.91	3000	3000	ns
MINI_LVDS_25	1.08	1.26	1.79	1.99	3000	3000	ns
LVPECL_33	1.25	1.43	N/A	N/A	N/A	N/A	ns
LVPECL_25	1.09	1.27	N/A	N/A	N/A	N/A	ns
RSDS_33 (point to point)	1.24	1.42	1.71	1.91	3000	3000	ns
RSDS_25 (point to point)	1.08	1.26	1.79	1.99	3000	3000	ns
TMDS_33	1.29	1.47	1.68	1.88	3000	3000	ns
PPDS_33	1.25	1.43	1.71	1.91	3000	3000	ns
PPDS_25	1.08	1.26	1.82	2.02	3000	3000	ns
PCI33_3	1.14	1.32	3.81	4.01	3.81	4.01	ns
PCI66_3	1.14	1.32	3.81	4.01	3.81	4.01	ns
DISPLAY_PORT	1.09	1.27	3.29	3.49	3.29	3.49	ns
I2C	1.40	1.58	11.70	11.90	11.70	11.90	ns
SMBUS	1.40	1.58	11.70	11.90	11.70	11.90	ns
SDIO	1.43	1.61	2.78	2.98	2.78	2.98	ns
MOBILE_DDR	1.01	1.19	2.50	2.70	2.50	2.70	ns
HSTL_I	1.01	1.19	1.80	2.00	1.80	2.00	ns
HSTL_II	1.01	1.19	1.86	2.06	1.86	2.06	ns
HSTL_III	1.07	1.25	1.81	2.01	1.81	2.01	ns
HSTL_I_18	1.05	1.23	1.91	2.11	1.91	2.11	ns
HSTL_II_18	1.05	1.23	1.99	2.19	1.99	2.19	ns
HSTL_III_18	1.13	1.31	1.93	2.13	1.93	2.13	ns
SSTL3_I	1.65	1.83	1.97	2.17	1.97	2.17	ns
SSTL3_II	1.65	1.83	2.15	2.35	2.15	2.35	ns
SSTL2_I	1.37	1.55	1.91	2.11	1.91	2.11	ns
SSTL2_II	1.37	1.55	2.00	2.20	2.00	2.20	ns
SSTL18_I	0.99	1.17	1.77	1.97	1.77	1.97	ns
SSTL18_II	1.00	1.18	1.80	2.00	1.80	2.00	ns
SSTL15_II	1.00	1.18	1.81	2.01	1.81	2.01	ns
DIFF_HSTL_I	1.01	1.19	1.91	2.11	1.91	2.11	ns
DIFF_HSTL_II	1.00	1.18	1.86	2.06	1.86	2.06	ns
DIFF_HSTL_III	1.00	1.18	1.83	2.03	1.83	2.03	ns
DIFF_HSTL_I_18	1.04	1.22	1.93	2.13	1.93	2.13	ns
DIFF_HSTL_II_18	1.04	1.22	1.83	2.03	1.83	2.03	ns
DIFF_HSTL_III_18	1.04	1.22	1.83	2.03	1.83	2.03	ns

I/O Standard Measurement Methodology

Input Delay Measurements

Table 31 shows the test setup parameters used for measuring input delay.

Table 31: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)}$	$V_H^{(1)}$	$V_{MEAS}^{(3)(4)}$	$V_{REF}^{(2)(4)}$
LVTTTL (Low-Voltage Transistor-Transistor Logic)	LVTTTL	0	3.0	1.4	—
LVC MOS (Low-Voltage CMOS), 3.3V	LVC MOS33	0	3.3	1.65	—
LVC MOS, 2.5V	LVC MOS25	0	2.5	1.25	—
LVC MOS, 1.8V	LVC MOS18	0	1.8	0.9	—
LVC MOS, 1.5V	LVC MOS15	0	1.5	0.75	—
LVC MOS, 1.2V	LVC MOS12	0	1.2	0.6	—
PCI (Peripheral Component Interface), 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3	Per PCI Specification			—
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III	HSTL_III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	1.1
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
SSTL, Class II, 1.5V	SSTL15_II	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	$1.25 - 0.125$	$1.25 + 0.125$	0 ⁽⁵⁾	—
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V & 3.3V	LVPECL_25, LVPECL_33	$1.2 - 0.3$	$1.2 + 0.3$	0 ⁽⁵⁾	—
BLVDS (Bus LVDS), 2.5V	BLVDS_25	$1.3 - 0.125$	$1.3 + 0.125$	0 ⁽⁵⁾	—
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	$1.2 - 0.125$	$1.2 + 0.125$	0 ⁽⁵⁾	—
RS DS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RS DS_25, RS DS_33	$1.2 - 0.1$	$1.2 + 0.1$	0 ⁽⁵⁾	—
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	$3.0 - 0.1$	$3.0 + 0.1$	0 ⁽⁵⁾	—
PPDS (Point-to-Point Differential Signaling), 2.5V & 3.3V	PPDS_25, PPDS_33	$1.25 - 0.1$	$1.25 + 0.1$	0 ⁽⁵⁾	—

Notes:

1. Input waveform switches between V_L and V_H .
2. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 4.
5. The value given is the differential input voltage.

Table 33: Spartan-6 FPGA V_{CCO}/GND Pairs per Bank

Package	Devices	Description	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5
TQG144	LX	V _{CCO} /GND Pairs	3	3	2	3	N/A	N/A
		Maximum I/O per Pair	8	8	13	8	N/A	N/A
CPG196	LX	V _{CCO} /GND Pairs	4	6	4	6	N/A	N/A
		Maximum I/O per Pair	6	4	7	4	N/A	N/A
CSG225	LX	V _{CCO} /GND Pairs	4	4	4	4	N/A	N/A
		Maximum I/O per Pair	10	10	9	10	N/A	N/A
FT(G)256	LX	V _{CCO} /GND Pairs	5	6	4	5	N/A	N/A
		Maximum I/O per Pair	8	9	9	10	N/A	N/A
CSG324	LX	V _{CCO} /GND Pairs	6	6	6	6	N/A	N/A
		Maximum I/O per Pair	10	9	10	9	N/A	N/A
	LXT	V _{CCO} /GND Pairs	4	6	6	6	N/A	N/A
		Maximum I/O per Pair	4	9	10	9	N/A	N/A
CS(G)484	LX	V _{CCO} /GND Pairs	8	13	8	13	N/A	N/A
		Maximum I/O per Pair	7	8	7	8	N/A	N/A
	LXT	V _{CCO} /GND Pairs	7	12	8	13	N/A	N/A
		Maximum I/O per Pair	5	8	6	8	N/A	N/A
FG(G)484	LX	V _{CCO} /GND Pairs	10	10	11	11	N/A	N/A
		Maximum I/O per Pair	6	8	9	8	N/A	N/A
	LXT	V _{CCO} /GND Pairs	6	10	11	10	N/A	N/A
		Maximum I/O per Pair	7	8	7	8	N/A	N/A
FG(G)676	LX45	V _{CCO} /GND Pairs	12	15	10	16	N/A	N/A
		Maximum I/O per Pair	3	7	8	7	N/A	N/A
	LX75, LX100, LX150	V _{CCO} /GND Pairs	12	9	10	10	6	6
		Maximum I/O per Pair	9	10	9	9	8	9
	LXT	V _{CCO} /GND Pairs	10	8	10	8	7	7
		Maximum I/O per Pair	8	7	8	8	7	7
FG(G)900	LX	V _{CCO} /GND Pairs	17	14	17	14	7	8
		Maximum I/O per Pair	7	6	7	8	7	6
	LXT	V _{CCO} /GND Pairs	15	14	13	14	7	8
		Maximum I/O per Pair	7	6	8	8	7	6

Input/Output Delay Switching Characteristics

Table 39: IODELAY2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L ⁽³⁾	
$T_{\text{IODCCK_CAL}} / T_{\text{IODCKC_CAL}}$	CAL pin Setup/Hold with respect to CK	0.28/ -0.13	0.33/ -0.13	0.48/ -0.13	N/A	ns
$T_{\text{IODCCK_CE}} / T_{\text{IODCKC_CE}}$	CE pin Setup/Hold with respect to CK	0.17/ -0.03	0.17/ -0.03	0.25/ -0.02	N/A	ns
$T_{\text{IODCCK_INC}} / T_{\text{IODCKC_INC}}$	INC pin Setup/Hold with respect to CK	0.10/ 0.02	0.12/ 0.03	0.18/ 0.06	N/A	ns
$T_{\text{IODCCK_RST}} / T_{\text{IODCKC_RST}}$	RST pin Setup/Hold with respect to CK	0.12/ -0.02	0.15/ -0.02	0.22/ -0.01	N/A	ns
T_{TAP1} ⁽²⁾	Maximum tap 1 delay	8	14	16	N/A	ps
T_{TAP2}	Maximum tap 2 delay	40	66	77	N/A	ps
T_{TAP3}	Maximum tap 3 delay	95	120	140	N/A	ps
T_{TAP4}	Maximum tap 4 delay	108	141	166	N/A	ps
T_{TAP5}	Maximum tap 5 delay	171	194	231	N/A	ps
T_{TAP6}	Maximum tap 6 delay	207	249	292	N/A	ps
T_{TAP7}	Maximum tap 7 delay	212	276	343	N/A	ps
T_{TAP8}	Maximum tap 8 delay	322	341	424	N/A	ps
F_{MINCAL}	Minimum allowed bit rate for calibration in variable mode: VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX, and DIFF_PHASE_DETECTOR.	188	188	188	N/A	Mb/s
$T_{\text{IODDO_IDATAIN}}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	—
$T_{\text{IODDO_ODATAIN}}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	—

Notes:

- Delay depends on IODELAY2 tap setting. See TRACE report for actual values.
- Maximum delay = integer (number of taps/8) $\times$ T_{TAP8} + T_{TAPn} (where n equals the remainder). For minimum delay consult the TRACE setup and hold report. Minimum delay is typically greater than 30% of the maximum delay. Tap delays can vary by device and overall conditions. See TRACE report for actual values.
- Spartan-6 -1L devices only support tap 0. See TRACE report for actual values.

CLB Switching Characteristics (SLICEM Only)

Table 40: CLB Switching Characteristics (SLICEM Only)

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT inputs to A to D outputs	0.21	0.26	0.26	0.46	ns, Max
	An – Dn LUT inputs through F7AMUX/F7BMUX to AMUX/CMUX output	0.37	0.43	0.43	0.77	ns, Max
T _{OPAB}	An – Dn LUT inputs through F7AMUX or F7BMUX and F8MUX to BMUX output	0.37	0.46	0.46	0.84	ns, Max
T _{ITO}	An – Dn LUT inputs through latch to AQ – DQ outputs	0.82	0.95	0.95	1.64	ns, Max
T _{TITO_LOGIC}	An – Dn LUT inputs to AQ – DQ outputs (latch as logic)	0.82	0.95	0.95	1.64	ns, Max
T _{OPCYA}	An LUT inputs to COUT output	0.38	0.48	0.48	0.69	ns, Max
T _{OPCYB}	Bn LUT inputs to COUT output	0.38	0.49	0.49	0.71	ns, Max
T _{OPCYC}	Cn LUT inputs to COUT output	0.28	0.33	0.33	0.55	ns, Max
T _{OPCYD}	Dn LUT inputs to COUT output	0.28	0.35	0.35	0.52	ns, Max
T _{AXCY}	AX input to COUT output	0.21	0.26	0.26	0.36	ns, Max
T _{BXCy}	BX input to COUT output	0.13	0.16	0.16	0.18	ns, Max
T _{CXCy}	CX input to COUT output	0.10	0.12	0.12	0.09	ns, Max
T _{DXCy}	DX input to COUT output	0.09	0.11	0.11	0.09	ns, Max
T _{BYP}	CIN input to COUT output	0.08	0.10	0.10	0.06	ns, Max
T _{CINA}	CIN input to AMUX output	0.21	0.22	0.22	0.47	ns, Max
T _{CINB}	CIN input to BMUX output	0.30	0.31	0.31	0.57	ns, Max
T _{CINC}	CIN input to CMUX output	0.29	0.31	0.31	0.58	ns, Max
T _{CIND}	CIN input to DMUX output	0.31	0.32	0.32	0.68	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.45	0.53	0.53	0.74	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{DICK} /T _{CKDI}	AX – DX input to CLK on A – D flip-flops	0.42/ 0.28	0.47/ 0.39	0.47/ 0.39	0.90/ 0.56	ns, Min
T _{CECK} /T _{CKCE}	CE input to CLK on A – D flip-flops	0.31/ –0.07	0.37/ –0.07	0.37/ –0.07	0.59/ –0.27	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D flip-flops for XC devices	0.41/ 0.02	0.42/ 0.02	0.42/ 0.02	0.68/ –0.29	ns, Min
	SR input to CLK on A – D flip-flops for XA and XQ devices	0.41/ 0.02	N/A	0.44/ 0.02	0.68/ –0.29	ns, Min
T _{CINCK} /T _{CKCIN}	CIN input to CLK on A – D flip-flops	0.31/ –0.17	0.31/ –0.13	0.31/ –0.13	0.81/ –0.42	ns, Min
Set/Reset						
T _{RPW}	SR input minimum pulse width	0.41	0.48	0.48	1.37	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.60	0.70	0.70	0.88	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.60	0.65	0.65	0.90	ns, Max
F _{TOG}	Toggle frequency (for export control)	862	806	667	500	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 41: CLB Distributed RAM Switching Characteristics (SLICEM Only)

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Sequential Delays						
T _{SHCKO}	Clock to A – D outputs	1.26	1.55	1.55	2.35	ns, Max
	Clock to A – D outputs (direct output path)	0.96	1.20	1.20	1.87	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{DS} /T _{DH}	AX – DX or AI – DI inputs to CLK	0.59/ 0.17	0.73/ 0.22	0.73/ 0.22	1.17/ 0.33	ns, Min
T _{AS} /T _{AH}	Address An inputs to clock for XC devices	0.28/ 0.35	0.32/ 0.42	0.32/ 0.42	0.26/ 0.71	ns, Min
	Address An inputs to clock for XA and XQ devices	0.28/ 0.51	N/A	0.32/ 0.51	0.26/ 0.71	ns, Min
T _{WS} /T _{WH}	WE input to clock	0.31/ –0.08	0.37/ –0.08	0.37/ –0.08	0.59/ –0.27	ns, Min
T _{CECK} /T _{CKCE}	CE input to CLK	0.31/ –0.08	0.37/ –0.08	0.37/ –0.08	0.59/ –0.27	ns, Min

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 42: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Sequential Delays						
T _{REG}	Clock to A – D outputs	1.35	1.78	1.78	2.74	ns, Max
	Clock to A – D outputs (direct output path)	1.24	1.65	1.65	2.48	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{WS} /T _{WH}	WE input to CLK	0.20/ –0.07	0.24/ –0.07	0.24/ –0.07	0.29/ –0.27	ns, Min
T _{CECK} /T _{CKCE}	CE input to CLK for XC devices	0.30/ 0.30	0.30/ 0.38	0.30/ 0.38	0.82/ –0.41	ns, Min
	CE input to CLK for XA and XQ devices	0.32/ 0.30	N/A	0.40/ 0.38	0.82/ –0.41	ns, Min
T _{DS} /T _{DH}	AX – DX or AI – DI inputs to CLK	0.07/ 0.11	0.09/ 0.14	0.09/ 0.14	0.11/ 0.23	ns, Min

Table 47: Configuration Switching Characteristics⁽¹⁾ (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
BPI Master Flash Mode Programming Switching ⁽⁴⁾						
T _{BPICCO} ⁽⁵⁾	A[25:0], FCS_B, FOE_B, FWE_B, LDC outputs valid after CCLK falling edge	15	15	15	20	ns, Max
T _{BPIICK}	Master BPI CCLK (output) delay	10/100	10/100	10/100	10/130	μs, Min/Max
T _{BPIDCC} /T _{BPICCD}	Setup/Hold on D[15:0] data input pins	5.0/1.0	5.0/1.0	5.0/1.0	6.0/2.0	ns, Min
SPI Master Flash Mode Programming Switching ⁽⁶⁾						
T _{SPIDCC} /T _{SPIDCCD}	DIN, MISO0, MISO1, MISO2, MISO3, Setup/Hold before/after the rising CCLK edge	5.0/1.0	5.0/1.0	5.0/1.0	7.0/1.0	ns, Min
T _{SPIICK}	Master SPI CCLK (output) delay	0.4/7.0	0.4/7.0	0.4/7.0	0.4/10.0	μs, Min/Max
T _{SPICCM}	MOSI clock to out	13	13	13	19	ns, Max
T _{SPICCF}	CSO_B clock to out	16	16	16	26	ns, Max
CCLK Output (Master Modes)						
T _{MCCKL}	Master CCLK clock duty cycle Low	40/60				%, Min/Max
T _{MCCKH}	Master CCLK clock duty cycle High	40/60				%, Min/Max
F _{MCCK}	Maximum frequency, serial mode (Master Serial/SPI) All devices	40	40	40	30	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T	40	40	40	25	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x8 mode, LX150, and LX150T	40	40	40	20	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x16 mode	35	35	35	20	MHz, Max
F _{MCCKTOL}	Frequency Tolerance, master mode	±50	±50	±50	±50	%
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time	5	5	5	8	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time	5	5	5	8	ns, Min
USERCCLK Input						
T _{USERCCKL}	USERCCLK clock minimum Low time	12	12	12	16	ns, Min
T _{USERCCKH}	USERCCLK clock minimum High time	12	12	12	16	ns, Min
F _{USERCCLK}	Maximum USERCCLK frequency	40	40	40	30	MHz, Max

Notes:

- Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
- To support longer delays in configuration, use the design solutions described in [UG380: Spartan-6 FPGA Configuration User Guide](#).
- [Table 6](#) specifies the power supply ramp time.
- BPI mode is not supported in:
 - LX4, LX25, or LX25T devices
 - LX9 devices in the TQG144 package
 - LX9 or LX16 devices in the CPG196 package.
- Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
- Defense-grade Spartan-6Q -2Q devices configure in single default SPI Master (x1) mode at $T_j = -55^{\circ}\text{C}$. During operation and when using all other configuration functions, the minimum operating temperature is -40°C .

Table 54: Switching Characteristics for the Delay-Locked Loop (DLL)⁽¹⁾

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges										
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs.	5	280	5	280	5	250	5	175	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs.	5	200	5	200	5	200	5	175	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs.	10	375	10	375	10	334	10	250	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output.	0.3125	186	0.3125	186	0.3125	166	0.3125	88.6	MHz
Output Clock Jitter ⁽²⁾⁽³⁾⁽⁴⁾										
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output.	–	±100	–	±100	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs.	Maximum = ±[0.5% of CLKIN period + 100]								ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division.	–	±150	–	±150	–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division.	Maximum = ±[0.5% of CLKIN period + 100]								ps
Duty Cycle ⁽⁴⁾										
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion.	Typical = ±[1% of CLKIN period + 350]								ps
Phase Alignment ⁽⁴⁾										
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 1X).	–	±150	–	±150	–	±150	–	±250	ps
	Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 2X). ⁽⁶⁾	–	±250	–	±250	–	±250	–	±350	
CLKOUT_PHASE_DLL	Phase offset between DLL outputs for CLK0 to CLK2X (not CLK2X180).	Maximum = ±[1% of CLKIN period + 100]								ps
	Phase offset between DLL outputs for all others.	Maximum = ±[1% of CLKIN period + 150]						Maximum = ±[1% of CLKIN period + 200]		ps

Table 54: Switching Characteristics for the Delay-Locked Loop (DLL)⁽¹⁾ (Cont'd)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
LOCK_DLL ⁽³⁾	When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. CLKIN_FREQ_DLL < 50 MHz.	–	5	–	5	–	5	–	5	ms
	When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. CLKIN_FREQ_DLL > 50 MHz	–	0.60	–	0.60	–	0.60	–	0.60	ms
Delay Lines										
DCM_DELAY_STEP ⁽⁵⁾	Finest delay resolution, averaged over all steps.	10	40	10	40	10	40	10	40	ps

Notes:

1. The values in this table are based on the operating conditions described in Table 2 and Table 53.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster LOCK time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, this data sheet specifies a maximum jitter of $\pm(1\% \text{ of CLKIN period} + 150 \text{ ps})$. Assuming that the CLKIN frequency is 100 MHz, the equivalent CLKIN period is 10 ns. Since 1% of 10 ns is 0.1 ns or 100 ps, the maximum jitter is $\pm(100 \text{ ps} + 150 \text{ ps}) = \pm250 \text{ ps}$.
5. A typical delay step size is 23 ps.
6. The timing analysis tools use the CLK_FEEDBACK = 1X condition for the CLKIN_CLKFB_PHASE value (reported as phase error). When using CLK_FEEDBACK = 2X, add 100 ps to the phase error for the CLKIN_CLKFB_PHASE value (as shown in this table).

Table 55: Recommended Operating Conditions for the Digital Frequency Synthesizer (DFS)⁽¹⁾

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Input Frequency Ranges ⁽²⁾										
CLKIN_FREQ_FX	Frequency for the CLKIN input. Also described as F _{CLKIN} .	0.5	375 ⁽³⁾	0.5	375 ⁽³⁾	0.5	333 ⁽³⁾	0.5	200 ⁽³⁾	MHz
Input Clock Jitter Tolerance ⁽⁴⁾										
CLKIN_CYC_JITT_FX_LF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: FCLKFX < 150 MHz.	–	±300	–	±300	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: FCLKFX > 150 MHz.	–	±150	–	±150	–	±150	–	±150	ps
CLKIN_PER_JITT_FX	Period jitter at the CLKIN input.	–	±1	–	±1	–	±1	–	±1	ns

Notes:

1. DFS specifications apply when using either of the DFS outputs (CLKFX or CLKFX180).
2. When using both DFS and DLL outputs on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 53.
3. The CLKIN_DIVIDE_BY_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the F_{MAX} (see Table 48 and Table 49 for BUFG and BUFGIO limits).
4. CLKIN input jitter beyond these limits can cause the DCM to lose LOCK.

Table 65: Global Clock Input to Output Delay With DCM in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in Source-Synchronous Mode.							
T _{ICKOFDCM_0}	Global Clock and OUTFF <i>with</i> DCM	XC6SLX4	5.03	N/A	7.21	8.05	ns
		XC6SLX9	5.03	6.13	7.21	8.05	ns
		XC6SLX16	5.08	5.51	6.44	7.96	ns
		XC6SLX25	4.81	5.13	5.69	7.94	ns
		XC6SLX25T	4.81	5.13	5.69	N/A	ns
		XC6SLX45	5.26	5.69	6.63	7.92	ns
		XC6SLX45T	5.26	5.69	6.63	N/A	ns
		XC6SLX75	4.77	5.18	5.88	7.95	ns
		XC6SLX75T	4.77	5.18	5.88	N/A	ns
		XC6SLX100	4.72	5.11	5.76	8.59	ns
		XC6SLX100T	4.76	5.11	5.76	N/A	ns
		XC6SLX150	4.90	5.30	5.93	7.93	ns
		XC6SLX150T	4.90	5.30	5.93	N/A	ns
		XA6SLX4	5.35	N/A	7.21	N/A	ns
		XA6SLX9	5.35	N/A	7.21	N/A	ns
		XA6SLX16	5.42	N/A	6.44	N/A	ns
		XA6SLX25	5.13	N/A	5.69	N/A	ns
		XA6SLX25T	5.13	N/A	5.79	N/A	ns
		XA6SLX45	5.58	N/A	6.63	N/A	ns
		XA6SLX45T	5.58	N/A	6.63	N/A	ns
		XA6SLX75	5.09	N/A	5.87	N/A	ns
		XA6SLX75T	5.09	N/A	5.87	N/A	ns
		XA6SLX100	N/A	N/A	6.44	N/A	ns
		XQ6SLX75	N/A	N/A	5.87	7.95	ns
		XQ6SLX75T	5.09	N/A	5.87	N/A	ns
		XQ6SLX150	N/A	N/A	6.06	7.93	ns
		XQ6SLX150T	5.50	N/A	6.06	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 72: Global Clock Setup and Hold With DCM in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard. ⁽¹⁾							
T _{PSDCM} / T _{PHDCM}	No Delay Global Clock and IFF ⁽²⁾ with DCM in System-Synchronous Mode	XC6SLX4	1.54/0.06	N/A	1.75/0.12	2.84/0.27	ns
		XC6SLX9	1.54/0.06	1.63/0.12	1.75/0.12	2.84/0.27	ns
		XC6SLX16	1.72/−0.18	1.87/−0.17	2.13/−0.17	2.31/0.26	ns
		XC6SLX25	1.70/−0.03	1.78/−0.02	2.00/−0.02	2.88/0.20	ns
		XC6SLX25T	1.70/0.07	1.78/0.08	2.00/0.08	N/A	ns
		XC6SLX45	1.74/−0.03	1.84/−0.02	2.02/−0.02	2.64/0.52	ns
		XC6SLX45T	1.74/−0.01	1.84/0.00	2.02/0.00	N/A	ns
		XC6SLX75	1.86/0.11	1.98/0.12	2.20/0.12	2.96/0.58	ns
		XC6SLX75T	1.86/0.11	1.98/0.12	2.20/0.12	N/A	ns
		XC6SLX100	1.64/0.07	1.72/0.08	1.97/0.08	2.70/0.99	ns
		XC6SLX100T	1.64/0.09	1.72/0.10	1.97/0.10	N/A	ns
		XC6SLX150	1.53/0.39	1.62/0.40	1.82/0.40	2.75/1.00	ns
		XC6SLX150T	1.53/0.39	1.62/0.40	1.82/0.40	N/A	ns
		XA6SLX4	1.65/0.16	N/A	1.75/0.26	N/A	ns
		XA6SLX9	1.65/0.16	N/A	1.75/0.26	N/A	ns
		XA6SLX16	1.88/0.02	N/A	2.13/0.03	N/A	ns
		XA6SLX25	1.80/0.16	N/A	2.05/0.17	N/A	ns
		XA6SLX25T	1.80/0.16	N/A	2.13/0.17	N/A	ns
		XA6SLX45	1.75/0.12	N/A	2.02/0.13	N/A	ns
		XA6SLX45T	1.75/0.12	N/A	2.02/0.13	N/A	ns
		XA6SLX75	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XA6SLX75T	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XA6SLX100	N/A	N/A	2.46/0.24	N/A	ns
		XQ6SLX75	N/A	N/A	2.20/0.12	2.96/0.58	ns
		XQ6SLX75T	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XQ6SLX150	N/A	N/A	1.82/0.56	2.75/1.00	ns
		XQ6SLX150T	1.65/0.55	N/A	1.82/0.56	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 73: Global Clock Setup and Hold With DCM in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.(1)							
T _{PSDCM0} / T _{PHDCM0}	No Delay Global Clock and IFF(2) with DCM in Source-Synchronous Mode	XC6SLX4	0.71/0.65	N/A	0.72/1.22	1.58/1.18	ns
		XC6SLX9	0.71/0.69	0.71/1.19	0.72/1.36	1.58/1.18	ns
		XC6SLX16	0.86/0.52	0.92/0.57	1.04/0.60	1.02/1.06	ns
		XC6SLX25	0.84/0.58	0.90/0.59	1.01/0.59	1.58/1.07	ns
		XC6SLX25T	0.84/0.58	0.90/0.59	1.01/0.59	N/A	ns
		XC6SLX45	0.85/0.70	0.90/0.76	0.98/0.79	1.34/1.34	ns
		XC6SLX45T	0.85/0.70	0.90/0.76	0.98/0.79	N/A	ns
		XC6SLX75	1.00/0.62	1.06/0.63	1.15/0.63	1.65/1.46	ns
		XC6SLX75T	1.00/0.71	1.06/0.72	1.15/0.72	N/A	ns
		XC6SLX100	0.81/0.68	0.81/0.69	0.94/0.69	1.42/2.07	ns
		XC6SLX100T	0.81/0.68	0.81/0.69	0.94/0.69	N/A	ns
		XC6SLX150	0.68/0.98	0.69/0.99	0.79/0.99	1.45/1.60	ns
		XC6SLX150T	0.68/0.98	0.69/0.99	0.79/0.99	N/A	ns
		XA6SLX4	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX9	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX16	1.01/0.56	N/A	1.04/0.60	N/A	ns
		XA6SLX25	0.94/0.76	N/A	1.06/0.77	N/A	ns
		XA6SLX25T	0.94/0.76	N/A	1.14/0.77	N/A	ns
		XA6SLX45	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX45T	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX75	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX100	N/A	N/A	1.37/0.75	N/A	ns
		XQ6SLX75	N/A	N/A	1.15/0.72	1.65/1.46	ns
		XQ6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XQ6SLX150	N/A	N/A	0.79/1.15	1.45/1.60	ns
		XQ6SLX150T	0.73/1.15	N/A	0.79/1.15	N/A	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 76: Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾							
T _{PSDCMPLL} / T _{PHDCMPLL}	No Delay Global Clock and IFF ⁽²⁾ with DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.	XC6SLX4	1.16/0.49	N/A	1.39/0.49	2.36/0.59	ns
		XC6SLX9	1.16/0.44	1.37/0.44	1.39/0.44	2.36/0.59	ns
		XC6SLX16	1.44/−0.08	1.49/−0.04	1.62/−0.04	2.06/0.55	ns
		XC6SLX25	1.52/0.42	1.65/0.42	1.83/0.42	2.52/0.43	ns
		XC6SLX25T	1.52/0.42	1.65/0.42	1.83/0.42	N/A	ns
		XC6SLX45	1.54/0.39	1.59/0.39	1.75/0.39	2.48/0.76	ns
		XC6SLX45T	1.54/0.39	1.59/0.39	1.75/0.39	N/A	ns
		XC6SLX75	1.72/0.41	1.80/0.41	1.99/0.41	2.60/0.75	ns
		XC6SLX75T	1.72/0.41	1.80/0.41	1.99/0.41	N/A	ns
		XC6SLX100	1.34/0.51	1.46/0.51	1.64/0.51	2.12/0.90	ns
		XC6SLX100T	1.34/0.51	1.46/0.51	1.64/0.51	N/A	ns
		XC6SLX150	1.30/0.60	1.40/0.60	1.55/0.60	2.57/0.97	ns
		XC6SLX150T	1.30/0.60	1.40/0.60	1.55/0.60	N/A	ns
		XA6SLX4	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX9	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX16	2.67/0.35	N/A	2.67/0.17	N/A	ns
		XA6SLX25	1.74/0.27	N/A	1.95/0.27	N/A	ns
		XA6SLX25T	1.74/0.27	N/A	2.03/0.27	N/A	ns
		XA6SLX45	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX45T	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX75	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX100	N/A	N/A	2.64/0.82	N/A	ns
		XQ6SLX75	N/A	N/A	2.11/0.24	2.60/0.75	ns
		XQ6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XQ6SLX150	N/A	N/A	1.67/0.70	2.57/0.97	ns
		XQ6SLX150T	1.50/0.70	N/A	1.67/0.70	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 77: Global Clock Setup and Hold With DCM and PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Example Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin, ⁽¹⁾ Using DCM, PLL, and Global Clock Buffer for the LVCMOS25 standard.							
T _{PSDCMPLL_0} / T _{PHDCMPLL_0}	No Delay Global Clock and IFF ⁽²⁾ with DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode.	XC6SLX4	0.43/1.07	N/A	0.43/1.43	1.10/1.67	ns
		XC6SLX9	0.43/1.03	0.45/1.14	0.45/1.43	1.10/1.67	ns
		XC6SLX16	0.74/0.93	0.74/1.12	0.74/1.21	0.77/1.35	ns
		XC6SLX25	0.67/1.02	0.76/1.11	0.84/1.18	1.23/1.46	ns
		XC6SLX25T	0.67/1.02	0.76/1.11	0.84/1.18	N/A	ns
		XC6SLX45	0.65/0.99	0.65/1.04	0.71/1.12	1.18/1.58	ns
		XC6SLX45T	0.65/1.00	0.65/1.04	0.71/1.12	N/A	ns
		XC6SLX75	0.86/1.01	0.88/1.06	0.94/1.14	1.29/1.67	ns
		XC6SLX75T	0.86/1.01	0.88/1.06	0.94/1.14	N/A	ns
		XC6SLX100	0.50/1.10	0.56/1.10	0.61/1.17	0.84/2.24	ns
		XC6SLX100T	0.50/1.10	0.56/1.10	0.61/1.17	N/A	ns
		XC6SLX150	0.45/1.28	0.47/1.28	0.52/1.28	1.27/1.56	ns
		XC6SLX150T	0.45/1.28	0.47/1.28	0.52/1.28	N/A	ns
		XA6SLX4	0.74/1.00	N/A	0.74/1.43	N/A	ns
		XA6SLX9	0.74/1.00	N/A	0.74/1.43	N/A	ns
		XA6SLX16	1.81/1.15	N/A	1.81/1.03	N/A	ns
		XA6SLX25	0.89/1.01	N/A	0.96/1.05	N/A	ns
		XA6SLX25T	0.89/1.01	N/A	1.04/1.15	N/A	ns
		XA6SLX45	0.69/0.95	N/A	0.83/0.96	N/A	ns
		XA6SLX45T	0.69/0.95	N/A	0.83/0.96	N/A	ns
		XA6SLX75	0.88/0.94	N/A	1.06/0.96	N/A	ns
		XA6SLX75T	0.88/0.94	N/A	1.06/0.96	N/A	ns
		XA6SLX100	N/A	N/A	1.55/1.33	N/A	ns
		XQ6SLX75	N/A	N/A	1.06/0.96	1.29/1.67	ns
		XQ6SLX75T	0.88/0.94	N/A	1.06/0.96	N/A	ns
		XQ6SLX150	N/A	N/A	0.64/1.30	1.27/1.56	ns
		XQ6SLX150T	0.58/1.30	N/A	0.64/1.30	N/A	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG. Package skew is not included in these measurements.
- IFF = Input Flip-Flop

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
08/26/09	1.1	Added V_{FS} to Table 1 and Table 2 . Added R_{FUSE} to Table 2 . Added XC6SLX75 and XC6SLX75T to V_{BATT} and I_{BATT} in Table 1 , Table 2 , and Table 4 . Corrected the quiescent supply current for the XC6SLX4 in Table 5 . Updated Table 11 . Removed DV_{PPIN} from Figure 2 . Removed $F_{PCIECORE}$ from Table 24 and added values to $F_{PCIEUSER}$. Added more networking applications to Table 25 . Updated values for $T_{SUSPENDLOW_AWAKE}$, $T_{SUSPEND_ENABLE}$, and T_{SCP_AWAKE} in Table 46 . Numerous changes to Table 47 , page 54 including the addition of new values to various specifications, revising the $T_{SMCKCSO}$ description, and changing the units of T_{POR} . Also, removed <i>Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK</i> section from Table 47 and updated all the notes. In Table 52 , added to F_{INMAX} , revised F_{OUTMAX} , and removed PLL Maximum Output Frequency for BUFIO2. Revised values for DCM_DELAY_STEP in Table 54 . Updated CLKIN_FREQ_FX values in Table 55 .
01/04/10	1.2	Added -4 speed grade to entire document. Updated speed specification of -4, -3, -2 speed grades to version 1.03. Added -1L speed grade numbers per speed specification 1.00. Updated T_{SOL} in Table 1 . Added -1L rows for LVCMOS12, LVCMOS15, and LVCMOS18 in Table 9 . Revised much of the detail in <i>GTP Transceiver Specifications</i> in Table 12 through Table 23 . Added -2 data to Table 25 . Updated F_{MAX} in Table 44 . Updated descriptions for T_{DNACKL} and T_{DNACKH} in Table 45 and revised values for all parameters. Removed $T_{INITADDR}$ from Table 47 and added new data. Updated values in Table 48 through Table 62 . Added Table 51 (BUFPLL) and Table 57 (DCM_CLKGEN). Removed $T_{LOCKMAX}$ note from Table 52 . Updated note 3 in Table 53 . In Table 79 : removed XC6SLX75CSG324 and XC6SLX75TCSG324; added XC6SLX75FG(G)484 and XC6SLX75FG(G)484.
02/22/10	1.3	Production release of XC6SLX16 -2 speed grade devices. The changes to Table 26 and Table 27 includes updating this data sheet to the data in ISE v11.5 software with speed specification v1.06. Updated maximum of V_{IN} and V_{TS} and note 2 in Table 1 . In Table 2 , changed V_{IN} , added I_{IN} and note 5, revised notes 1, 6, and 7, and added note 8 to R_{FUSE} . In Table 4 , removed previous note 1 and added data to I_{RPU} , I_{RPD} , and I_{BATT} , changed C_{IN} , added R_{DT} and R_{IN_TERM} , and added note 2 and 3. Updated V_{CCO2} in Table 6 . Added Table 7 and Table 8 . Removed PCI66_3 from Table 9 . Updated PCI33_3 and I2C in Table 9 . Updated the description of Table 11 . Completely updated Table 25 . Updated Table 28 including adding values for PCI33_3. Updated V_{REF} value for HSTL_III_18 in Table 31 . Updates missing V_{REF} values in Table 32 . Added <i>Simultaneously Switching Outputs</i> , page 36 . Removed T_{GSRQ} and T_{RPW} from Table 35 and Table 36 . Also removed T_{DOQ} from Table 36 . Removed T_{ISDO_DO} and note 1 from Table 37 . Removed T_{OSCK_S} and combinatorial section from Table 38 . In Table 39 , removed T_{IODDO_T} and added new tap parameters and note 2. In Table 40 , Table 41 , and Table 42 , made typographical edits and removed notes. Removed clock CLK section in Table 41 . Removed clock CLK section and T_{REG_MUX} and T_{REG_M31} in Table 42 . Added block RAM F_{MAX} values to Table 43 . Updated values and added note 2 to Table 45 . Added values to Table 46 and removed note 1. Numerous changes to Table 47 . Completely updated Table 57 . Revised data in Table 62 . Removed note 3 from Table 71 . Added values to Table 79 . Added data to Table 80 and Table 81 .
03/10/10	1.4	Production release of XC6SLX45 -2 speed grade devices, which includes changes to Table 26 and Table 27 updating this data sheet to the data in ISE v11.5 software with speed specification v1.07. Fixed R_{IN_TERM} description in Table 4 . Added PCI66_3 to Table 7 and replaced note 1. Corrected note 1 and the V, Max for TMDS_33 in Table 8 . In Table 10 , added note 1 to LVPECL_33 and TMDS_33. Also updated specifications for TMDS_33. Updated the <i>GTP Transceiver Specifications</i> section including adding values to Table 16 , Table 17 , and Table 20 through Table 23 . Added PCI66_3 back into Table 9 , Table 28 , Table 31 , Table 32 , and Table 34 . Updated note 3 on Table 32 . In Table 34 , corrected some typographical errors and fixed SSO limits for bank1/3 in FG(G)484 package. Corrected T_{OSCK_OCE} in Table 38 . In Table 57 , updated CLKFX_FREEZE_VAR and CLKFX_FREEZE_TEMP_SLOPE and added typical values to $T_{CENTER_LOW_SPREAD}$ and $T_{CENTER_HIGH_SPREAD}$. Updated and added values to Table 63 through Table 78 , and Table 81 . In Table 79 , revised the XC6SLX16-CSG324 and the XC6SLX45-CSG484 and FG(G)484 values.

Date	Version	Description of Revisions
01/10/11	1.11	Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.4 software with speed specification v1.15 for the -4, -3, -3N, and -2 speed grades. Added note 3 to Table 27. Also updated the -1L speed grade requirements to ISE v12.4 software with speed specification v1.06. Revised -3N definition throughout the document. Added note 4 to Table 2 and updated note 5. Added information on V_{CCINT} to note 1 in Table 5. Updated Networking Applications -3 values in Table 25 to match improvements made in ISE v12.4. In Table 28, added note 1 and revised the T_{IOTP} values for LVDS_33, LVDS_25, MINI_LVDS_33, MINI_LVDS_25, RSDS_33, RSDS_25, TMDS_33, PPDS_33, and PPDS_25. Added note 3 to Table 55.
02/11/11	1.12	As described in XCEN11008: Product Discontinuation Notice For Spartan-6 LXT -4 Devices, the -4 speed specifications have been discontinued. As outlined in page 2 of the XCN, designers currently using -4 speed specifications should rerun timing analysis using the new -3 speed specifications before moving to a replacement device. Updated the networking applications section of Table 25. Updated -2 speed specifications throughout document and added note 3 to Table 27 advising designers to use the -2 speed specification update (v1.17) with the ISE 12.4 software patch. Added F_{CLKDIV} to Table 37 and Table 38. Updated note 2 in Table 39. Updated units for $T_{SMCKCSO}$ and T_{BPICCO} in Table 47. Updated -1L in Table 71. Removed Note 2: <i>Package delay information is available for these device/package combinations. This information can be used to deskew the package</i> from Table 79.
03/31/11	2.0	Production release of XC6SLX45 in the -1L speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. In Table 39, removed values in the -1L column and added note 3 as IODELAY2 only supports Tap0 for lower-power devices. Updated copyright page 1 and Notice of Disclaimer.
05/20/11	2.1	Production release of XC6SLX100 and XC6SLX150 in the specific speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. Updated Table 27 and Note 7 with changes per XCEN11012: Speed File Change for -3N Devices. Revised Switching Characteristics section for speed specifications: v1.18 for -3, -3N, and -2; including improvements in Table 73 through Table 77 and Table 81. Removed <i>Memory Controller Block</i> from the performance heading in Table 2 and revised Note 2. In Table 4, added Note 1 to C_{IN} and updated the description of R_{IN_TERM}. Updated Note 1 in Table 5. Updated Note 1 of Table 7. In Table 25, added and removed -1L specifications, increased the standard performance DDR3 specifications, removed the extended performance DDR3 row and updated Note 3 and Note 4. Clarified the introductory information for Table 28 and Table 30. In Table 32: Revised V_{MEAS} value for LVCMOS12; revised V_{REF} for LVDS_25, LVDS_33, BLVDS_25, MINI_LVDS_25, MINI_LVDS_33, RSDS_25, and RSDS_33; revised R_{REF} for BLVDS_25 and TMDS_33; and added Note 4 and Note 5. Updated Note 2 and Note 3 in Table 39. In Table 47, revised the values and description of T_{POR} including adding Note 3. Also in Table 47, augmented the description and added specifications for F_{RBCK} and removed XC6SLX4 from F_{MCCK} (maximum frequency, parallel mode (Master SelectMAP/BPI)). Added BUFGMUX to Table 48 title. Added Table 50. In Table 52, revised specifications for $T_{EXTFVAR}$ and $F_{INJITTER}$. In Table 54 removed the 5 MHz < CLKIN_FREQ_DLL parameter in the LOCK_DLL description. In both Table 56 and Table 57, removed the 5 MHz < F_{CLKIN} parameter in the LOCK_FX description. In Table 58, updated description for PSCLK_FREQ and PSCLK_PULSE. Revised title and symbol of Table 70, added new speed specifications for -1L, and added Note 2. Added Table 71.
07/11/11	2.2	Added the Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices to all appropriate tables while sometimes removing the XC6S nomenclature. Added expanded temperature range (Q) to all appropriate tables. Updated T_{SOL} packages in Table 1. Added R_{OUT_TERM} to Table 4. Updated Note 2 on Table 13. Production release of the XC6SLX4, XC6SLX9, XC6SLX16, XC6SLX25, XC6SLX75, XQ6SLX75, and XQ6SLX150 in Table 26 and Table 27 using ISE v13.2 software with -1L speed specification v1.07. Production release of the XA6SLX16, XA6SLX25T, XA6SLX45, XA6SLX45T, XQ6SLX75, XQ6SLX75T, XQ6SLX150, and XQ6SLX150T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices(1). Updated CS(G)484 from CSG484 throughout data sheet. Clarified Note 3 in Table 39.
08/08/11	2.3	Production release of the XA6SLX25, XA6SLX75, and XA6SLX75T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19.