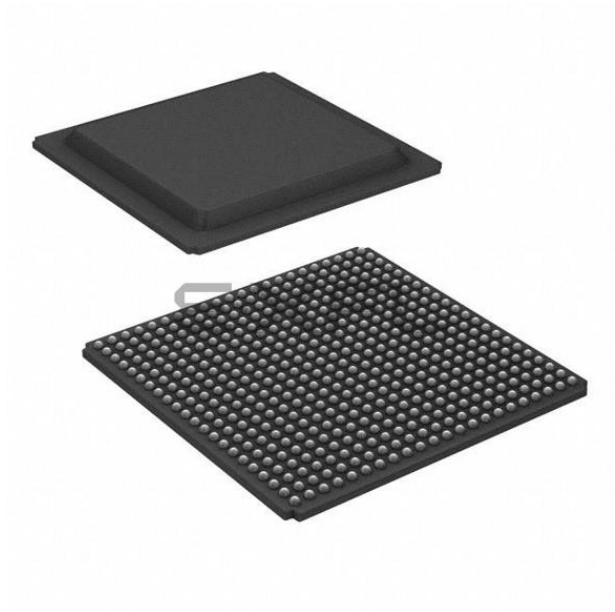
AMD Xilinx - XC6SLX45-3FGG484I Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3411
Number of Logic Elements/Cells	43661
Total RAM Bits	2138112
Number of I/O	316
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx45-3fgg484i

Quiescent Current

Typical values for quiescent supply current are specified at nominal voltage, 25°C junction temperatures (T_j). Quiescent supply current is specified by speed grade for Spartan-6 devices. Xilinx recommends analyzing static power consumption using the XPOWER™ Estimator (XPE) tool (download at http://www.xilinx.com/power) for conditions other than those specified in Table 5.

Table 5: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	LX4	4.0	4.0	4.0	2.4	mA
		LX9	4.0	4.0	4.0	2.4	mA
		LX16	6.0	6.0	6.0	4.0	mA
		LX25	11.0	11.0	11.0	6.6	mA
		LX25T	11.0	11.0	11.0	N/A	mA
		LX45	15.0	15.0	15.0	9.0	mA
		LX45T	15.0	15.0	15.0	N/A	mA
		LX75	29.0	29.0	29.0	17.4	mA
		LX75T	29.0	29.0	29.0	N/A	mA
		LX100	36.0	36.0	36.0	21.6	mA
		LX100T	36.0	36.0	36.0	N/A	mA
		LX150	51.0	51.0	51.0	31.0	mA
		LX150T	51.0	51.0	51.0	N/A	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	LX4	1.0	1.0	1.0	1.0	mA
		LX9	1.0	1.0	1.0	1.0	mA
		LX16	2.0	2.0	2.0	2.0	mA
		LX25	2.0	2.0	2.0	2.0	mA
		LX25T	2.0	2.0	2.0	N/A	mA
		LX45	3.0	3.0	3.0	3.0	mA
		LX45T	3.0	3.0	3.0	N/A	mA
		LX75	4.0	4.0	4.0	4.0	mA
		LX75T	4.0	4.0	4.0	N/A	mA
		LX100	5.0	5.0	5.0	5.0	mA
		LX100T	5.0	5.0	5.0	N/A	mA
		LX150	7.0	7.0	7.0	7.0	mA
		LX150T	7.0	7.0	7.0	N/A	mA

SelectIO™ Interface DC Input and Output Levels

Table 7: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

I/O Standard	V_{CCO} for Drivers[1]			V_{REF} for Inputs		
	V, Min	V, Nom	V, Max	V, Min	V, Nom	V, Max
LVTTL	3.0	3.3	3.45	V_{REF} is not used for these I/O standards		
LVCMOS33	3.0	3.3	3.45			
LVCMOS25	2.3	2.5	2.7			
LVCMOS18	1.65	1.8	1.95			
LVCMOS18_JEDEC	1.65	1.8	1.95			
LVCMOS15	1.4	1.5	1.6			
LVCMOS15_JEDEC	1.4	1.5	1.6			
LVCMOS12	1.1	1.2	1.3			
LVCMOS12_JEDEC	1.1	1.2	1.3			
PCI33_3[2]	3.0	3.3	3.45			
PCI66_3[2]	3.0	3.3	3.45			
I2C	2.7	3.0	3.45			
SMBUS	2.7	3.0	3.45			
SDIO	3.0	3.3	3.45			
MOBILE_DDR	1.7	1.8	1.9			
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_II	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_III	1.4	1.5	1.6	–	0.9	–
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–
HSTL_III_18	1.7	1.8	1.9	–	1.1	–
SSTL3_I	3.0	3.3	3.45	1.3	1.5	1.7
SSTL3_II	3.0	3.3	3.45	1.3	1.5	1.7
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38
SSTL18_I	1.7	1.8	1.9	0.833	0.9	0.969
SSTL18_II	1.7	1.8	1.9	0.833	0.9	0.969
SSTL15_II	1.425	1.5	1.575	0.69	0.75	0.81

Notes:

1. V_{CCO} range required when using I/O standard for an output. Also required for MOBILE_DDR, PCI33_3, LVCMOS18_JEDEC, LVCMOS15_JEDEC, and LVCMOS12_JEDEC inputs, and for LVCMOS25 inputs when V_{CCAUX} = 3.3V.
2. For PCI systems, the transmitter and receiver should have common supplies for V_{CCO}.

Table 10: **Differential I/O Standard DC Input and Output Levels**

I/O Standard	V_{ID}		V_{ICM}		V_{OD}		V_{OCM}		V_{OH}	V_{OL}
	mV, Min	mV, Max	V, Min	V, Max	mV, Min	mV, Max	V, Min	V, Max	V, Min	V, Max
LVDS_33[2][3]	100	600	0.3	2.35	247	454	1.125	1.375	–	–
LVDS_25[2][3]	100	600	0.3	2.35	247	454	1.125	1.375	–	–
BLVDS_25[2][3]	100	–	0.3	2.35	240	460	Typical 50% V_{CCO}		–	–
MINI_LVDS_33	200	600	0.3	1.95	300	600	1.0	1.4	–	–
MINI_LVDS_25	200	600	0.3	1.95	300	600	1.0	1.4	–	–
LVPECL_33[2][3]	100	1000	0.3	2.8[1]	Inputs only					
LVPECL_25[2][3]	100	1000	0.3	1.95	Inputs only					
RSDS_33[2][3]	100	–	0.3	1.5	100	400	1.0	1.4	–	–
RSDS_25[2][3]	100	–	0.3	1.5	100	400	1.0	1.4	–	–
TMDS_33	150	1200	2.7	3.23[1]	400	800	V_{CCO} – 0.405	V_{CCO} – 0.190	–	–
PPDS_33[2][3]	100	400	0.2	2.3	100	400	0.5	1.4	–	–
PPDS_25[2][3]	100	400	0.2	2.3	100	400	0.5	1.4	–	–
DISPLAY_PORT	190	1260	0.3	2.35	–	–	Typical 50% V_{CCO}		–	–
DIFF_MOBILE_DDR	100	–	0.78	1.02	–	–	–	–	90% V_{CCO}	10% V_{CCO}
DIFF_HSTL_I	100	–	0.68	0.9	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II	100	–	0.68	0.9	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III	100	–	0.68	0.9	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_I_18	100	–	0.8	1.1	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II_18	100	–	0.8	1.1	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	100	–	0.8	1.1	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL3_I	100	–	1.0	1.9	–	–	–	–	V_{TT} + 0.6	V_{TT} – 0.6
DIFF_SSTL3_II	100	–	1.0	1.9	–	–	–	–	V_{TT} + 0.8	V_{TT} – 0.8
DIFF_SSTL2_I	100	–	1.0	1.5	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61
DIFF_SSTL2_II	100	–	1.0	1.5	–	–	–	–	V_{TT} + 0.81	V_{TT} – 0.81
DIFF_SSTL18_I	100	–	0.7	1.1	–	–	–	–	V_{TT} + 0.47	V_{TT} – 0.47
DIFF_SSTL18_II	100	–	0.7	1.1	–	–	–	–	V_{TT} + 0.6	V_{TT} – 0.6
DIFF_SSTL15_II	100	–	0.55	0.95	–	–	–	–	V_{TT} + 0.4	V_{TT} – 0.4

Notes:

1. LVPECL_33 and TMDS_33 maximum V_{ICM} is the lower of V (maximum) or V_{CCAUX} – (V_{ID}/2)
2. When V_{CCAUX} = 3.3V, the DCD can be higher than 5% for V_{ICM} < 0.7V when using these I/O standards: LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, LVPECL_33, RSDS_25, RSDS_33, PPDS_25, and PPDS_33.
3. The -1L devices require V_{CCAUX} = 2.5V when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.

eFUSE Read Endurance

Table 11 lists the minimum guaranteed number of read cycle operations for Device DNA and for the AES eFUSE key. For more information, see UG380: *Spartan-6 FPGA Configuration User Guide*.

Table 11: **eFUSE Read Endurance**

Symbol	Description	Speed Grade				Units (Min)
		-3	-3N	-2	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTP Transceiver Specifications

GTP transceivers are available in the Spartan-6 LXT devices. See DS160: *Spartan-6 Family Overview* for more information.

GTP Transceiver DC Characteristics

Table 12: **Absolute Maximum Ratings for GTP Transceivers(1)**

Symbol	Description	Mln	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	–0.5	1.32	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	–0.5	1.32	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	–0.5	1.32	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 13: **Recommended Operating Conditions for GTP Transceivers(1)(2)(3)**

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	1.14	1.20	1.26	V

Notes:
1. Each voltage listed requires the filter circuit described in UG386: *Spartan-6 FPGA GTP Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +125°C.
3. The voltage level of MGTAVCCPLL must not exceed the voltage level of MGTAVCC +10mV. The voltage level of MGTAVCC must not exceed the voltage level of MGTAVCCPLL.

Table 21: **GTP Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade				Units
			-3	-3N	-2	-1L	
F_{TXOUT}	TXOUTCLK maximum frequency		320	320	270	N/A	MHz
F_{RXREC}	RXRECCLK maximum frequency		320	320	270	N/A	MHz
T_{RX}	RXUSRCLK maximum frequency		320	320	270	N/A	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz
T_{TX}	TXUSRCLK maximum frequency		320	320	270	N/A	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz

Notes:
1. Clocking must be implemented as described in UG386: *Spartan-6 FPGA GTP Transceivers User Guide*.

Table 22: **GTP Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
T_{RTX}	TX Rise time	20%–80%	–	140	–	ps
T_{FTX}	TX Fall time	80%–20%	–	120	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	400	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	20	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	50	ns
$T_{J3.125}$	Total Jitter(2)	3.125 Gb/s	–	–	0.35	UI
$D_{J3.125}$	Deterministic Jitter(2)		–	–	0.15	UI
$T_{J2.5}$	Total Jitter(2)	2.5 Gb/s	–	–	0.33	UI
$D_{J2.5}$	Deterministic Jitter(2)		–	–	0.15	UI
$T_{J1.62}$	Total Jitter(2)	1.62 Gb/s	–	–	0.20	UI
$D_{J1.62}$	Deterministic Jitter(2)		–	–	0.10	UI
$T_{J1.25}$	Total Jitter(2)	1.25 Gb/s	–	–	0.20	UI
$D_{J1.25}$	Deterministic Jitter(2)		–	–	0.10	UI
T_{J614}	Total Jitter(2)	614 Mb/s	–	–	0.10	UI
D_{J614}	Deterministic Jitter(2)		–	–	0.05	UI

Notes:
1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP transceiver sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.

Table 23: **GTP Transceiver Receiver Switching Characteristics**

Symbol	Description			Min	Typ	Max	Units
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data			–	75	–	ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak			60	–	150	mV
R_{XSST}	Receiver spread-spectrum tracking(1)		Modulated @ 33 KHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)	Internal AC capacitor bypassed		–	–	150	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	CDR 2nd-order loop disabled		–200	–	200	ppm
		CDR 2nd-order loop enabled	PLL_RXDIVSEL_OUT = 1	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 2	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 4	–1000	–	1000	ppm
SJ Jitter Tolerance(2)							
$JT\_SJ_{3.125}$	Sinusoidal Jitter(3)		3.125 Gb/s	0.4	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(3)		2.5 Gb/s	0.4	–	–	UI
$JT\_SJ_{1.62}$	Sinusoidal Jitter(3)		1.62 Gb/s	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(3)		1.25 Gb/s	0.5	–	–	UI
JT_SJ_{614}	Sinusoidal Jitter(3)		614 Mb/s	0.5	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)(5)							
$JT\_TJSE_{3.125}$	Total Jitter with stressed eye(4)		3.125 Gb/s	0.65	–	–	UI
$JT\_SJSE_{3.125}$	Sinusoidal Jitter with stressed eye		3.125 Gb/s	0.1	–	–	UI
$JT\_TJSE_{2.7}$	Total Jitter with stressed eye(4)		2.7 Gb/s	0.65	–	–	UI
$JT\_SJSE_{2.7}$	Sinusoidal Jitter with stressed eye		2.7 Gb/s	0.1	–	–	UI

Notes:
1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a Bit Error Ratio of $1e^{-12}$.
3. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
4. Composed of 0.37 UI DJ in the form of ISI and 0.18 UI RJ.
5. Measured using PRBS7 data pattern.

Endpoint Block for PCI Express Designs Switching Characteristics

The Endpoint block for PCI Express is available in the Spartan-6 LXT devices. Consult the Spartan-6 FPGA Integrated Endpoint Block for PCI Express for further information.

Table 24: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
$F_{PCIEUSER}$	User clock maximum frequency	62.5	62.5	62.5	N/A	MHz

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	
LVCMOS15, Slow, 8 mA	0.98	1.10	1.23	1.79	2.30	2.44	2.64	3.25	2.30	2.44	2.64	3.25	ns
LVCMOS15, Slow, 12 mA	0.98	1.10	1.23	1.79	2.03	2.17	2.37	2.99	2.03	2.17	2.37	2.99	ns
LVCMOS15, Slow, 16 mA	0.98	1.10	1.23	1.79	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVCMOS15, Fast, 2 mA	0.98	1.10	1.23	1.79	3.29	3.43	3.63	4.24	3.29	3.43	3.63	4.24	ns
LVCMOS15, Fast, 4 mA	0.98	1.10	1.23	1.79	2.27	2.41	2.61	3.22	2.27	2.41	2.61	3.22	ns
LVCMOS15, Fast, 6 mA	0.98	1.10	1.23	1.79	1.78	1.92	2.12	2.74	1.78	1.92	2.12	2.74	ns
LVCMOS15, Fast, 8 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.69	1.73	1.87	2.07	2.69	ns
LVCMOS15, Fast, 12 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.64	1.73	1.87	2.07	2.64	ns
LVCMOS15, Fast, 16 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.64	1.73	1.87	2.07	2.64	ns
LVCMOS15_JEDEC, QUIETIO, 2 mA	1.03	1.15	1.28	1.49	5.49	5.63	5.83	6.37	5.49	5.63	5.83	6.37	ns
LVCMOS15_JEDEC, QUIETIO, 4 mA	1.03	1.15	1.28	1.49	4.61	4.75	4.95	5.51	4.61	4.75	4.95	5.51	ns
LVCMOS15_JEDEC, QUIETIO, 6 mA	1.03	1.15	1.28	1.49	4.07	4.21	4.41	4.97	4.07	4.21	4.41	4.97	ns
LVCMOS15_JEDEC, QUIETIO, 8 mA	1.03	1.15	1.28	1.49	3.92	4.06	4.26	4.81	3.92	4.06	4.26	4.81	ns
LVCMOS15_JEDEC, QUIETIO, 12 mA	1.03	1.15	1.28	1.49	3.54	3.68	3.88	4.51	3.54	3.68	3.88	4.51	ns
LVCMOS15_JEDEC, QUIETIO, 16 mA	1.03	1.15	1.28	1.49	3.33	3.47	3.67	4.31	3.33	3.47	3.67	4.31	ns
LVCMOS15_JEDEC, Slow, 2 mA	1.03	1.15	1.28	1.49	4.18	4.32	4.52	5.13	4.18	4.32	4.52	5.13	ns
LVCMOS15_JEDEC, Slow, 4 mA	1.03	1.15	1.28	1.49	3.42	3.56	3.76	4.35	3.42	3.56	3.76	4.35	ns
LVCMOS15_JEDEC, Slow, 6 mA	1.03	1.15	1.28	1.49	2.29	2.43	2.63	3.25	2.29	2.43	2.63	3.25	ns
LVCMOS15_JEDEC, Slow, 8 mA	1.03	1.15	1.28	1.49	2.30	2.44	2.64	3.26	2.30	2.44	2.64	3.26	ns
LVCMOS15_JEDEC, Slow, 12 mA	1.03	1.15	1.28	1.49	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVCMOS15_JEDEC, Slow, 16 mA	1.03	1.15	1.28	1.49	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVCMOS15_JEDEC, Fast, 2 mA	1.03	1.15	1.28	1.49	3.28	3.42	3.62	4.22	3.28	3.42	3.62	4.22	ns
LVCMOS15_JEDEC, Fast, 4 mA	1.03	1.15	1.28	1.49	2.27	2.41	2.61	3.23	2.27	2.41	2.61	3.23	ns
LVCMOS15_JEDEC, Fast, 6 mA	1.03	1.15	1.28	1.49	1.78	1.92	2.12	2.74	1.78	1.92	2.12	2.74	ns
LVCMOS15_JEDEC, Fast, 8 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.69	1.73	1.87	2.07	2.69	ns
LVCMOS15_JEDEC, Fast, 12 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.63	1.73	1.87	2.07	2.63	ns
LVCMOS15_JEDEC, Fast, 16 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.63	1.73	1.87	2.07	2.63	ns
LVCMOS12, QUIETIO, 2 mA	0.91	1.03	1.16	1.51	6.40	6.54	6.74	7.30	6.40	6.54	6.74	7.30	ns
LVCMOS12, QUIETIO, 4 mA	0.91	1.03	1.16	1.51	4.98	5.12	5.32	5.90	4.98	5.12	5.32	5.90	ns
LVCMOS12, QUIETIO, 6 mA	0.91	1.03	1.16	1.51	4.65	4.79	4.99	5.55	4.65	4.79	4.99	5.55	ns
LVCMOS12, QUIETIO, 8 mA	0.91	1.03	1.16	1.51	4.23	4.37	4.57	5.21	4.23	4.37	4.57	5.21	ns
LVCMOS12, QUIETIO, 12 mA	0.91	1.03	1.16	1.51	3.98	4.12	4.32	4.94	3.98	4.12	4.32	4.94	ns
LVCMOS12, Slow, 2 mA	0.91	1.03	1.16	1.51	4.98	5.12	5.32	5.91	4.98	5.12	5.32	5.91	ns
LVCMOS12, Slow, 4 mA	0.91	1.03	1.16	1.51	2.84	2.98	3.18	3.81	2.84	2.98	3.18	3.81	ns
LVCMOS12, Slow, 6 mA	0.91	1.03	1.16	1.51	2.77	2.91	3.11	3.72	2.77	2.91	3.11	3.72	ns
LVCMOS12, Slow, 8 mA	0.91	1.03	1.16	1.51	2.34	2.48	2.68	3.31	2.34	2.48	2.68	3.31	ns
LVCMOS12, Slow, 12 mA	0.91	1.03	1.16	1.51	2.08	2.22	2.42	3.06	2.08	2.22	2.42	3.06	ns

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	
LVCMOS12, Fast, 2 mA	0.91	1.03	1.16	1.51	3.46	3.60	3.80	4.44	3.46	3.60	3.80	4.44	ns
LVCMOS12, Fast, 4 mA	0.91	1.03	1.16	1.51	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVCMOS12, Fast, 6 mA	0.91	1.03	1.16	1.51	1.79	1.93	2.13	2.75	1.79	1.93	2.13	2.75	ns
LVCMOS12, Fast, 8 mA	0.91	1.03	1.16	1.51	1.68	1.82	2.02	2.64	1.68	1.82	2.02	2.64	ns
LVCMOS12, Fast, 12 mA	0.91	1.03	1.16	1.51	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
LVCMOS12_JEDEC, QUIETIO, 2 mA	1.50	1.62	1.75	1.88	6.39	6.53	6.73	7.31	6.39	6.53	6.73	7.31	ns
LVCMOS12_JEDEC, QUIETIO, 4 mA	1.50	1.62	1.75	1.88	4.98	5.12	5.32	5.88	4.98	5.12	5.32	5.88	ns
LVCMOS12_JEDEC, QUIETIO, 6 mA	1.50	1.62	1.75	1.88	4.67	4.81	5.01	5.54	4.67	4.81	5.01	5.54	ns
LVCMOS12_JEDEC, QUIETIO, 8 mA	1.50	1.62	1.75	1.88	4.23	4.37	4.57	5.22	4.23	4.37	4.57	5.22	ns
LVCMOS12_JEDEC, QUIETIO, 12 mA	1.50	1.62	1.75	1.88	3.99	4.13	4.33	4.94	3.99	4.13	4.33	4.94	ns
LVCMOS12_JEDEC, Slow, 2 mA	1.50	1.62	1.75	1.88	5.00	5.14	5.34	5.90	5.00	5.14	5.34	5.90	ns
LVCMOS12_JEDEC, Slow, 4 mA	1.50	1.62	1.75	1.88	2.85	2.99	3.19	3.80	2.85	2.99	3.19	3.80	ns
LVCMOS12_JEDEC, Slow, 6 mA	1.50	1.62	1.75	1.88	2.76	2.90	3.10	3.72	2.76	2.90	3.10	3.72	ns
LVCMOS12_JEDEC, Slow, 8 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVCMOS12_JEDEC, Slow, 12 mA	1.50	1.62	1.75	1.88	2.09	2.23	2.43	3.05	2.09	2.23	2.43	3.05	ns
LVCMOS12_JEDEC, Fast, 2 mA	1.50	1.62	1.75	1.88	3.46	3.60	3.80	4.42	3.46	3.60	3.80	4.42	ns
LVCMOS12_JEDEC, Fast, 4 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns
LVCMOS12_JEDEC, Fast, 6 mA	1.50	1.62	1.75	1.88	1.79	1.93	2.13	2.76	1.79	1.93	2.13	2.76	ns
LVCMOS12_JEDEC, Fast, 8 mA	1.50	1.62	1.75	1.88	1.69	1.83	2.03	2.65	1.69	1.83	2.03	2.65	ns
LVCMOS12_JEDEC, Fast, 12 mA	1.50	1.62	1.75	1.88	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns

Notes:

1. The -1L values listed in this table are also applicable to the Spartan-6Q devices.
2. Devices with a -1L speed grade do not support Xilinx PCI IP.

Table 29: **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices[1] *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVCMOS15, QUIETIO, 2 mA	1.05	1.23	5.63	5.83	5.63	5.83	ns
LVCMOS15, QUIETIO, 4 mA	1.05	1.23	4.75	4.95	4.75	4.95	ns
LVCMOS15, QUIETIO, 6 mA	1.05	1.23	4.21	4.41	4.21	4.41	ns
LVCMOS15, QUIETIO, 8 mA	1.05	1.23	4.05	4.25	4.05	4.25	ns
LVCMOS15, QUIETIO, 12 mA	1.05	1.23	3.74	3.94	3.74	3.94	ns
LVCMOS15, QUIETIO, 16 mA	1.05	1.23	3.52	3.72	3.52	3.72	ns
LVCMOS15, Slow, 2 mA	1.05	1.23	4.32	4.52	4.32	4.52	ns
LVCMOS15, Slow, 4 mA	1.05	1.23	3.58	3.78	3.58	3.78	ns
LVCMOS15, Slow, 6 mA	1.05	1.23	2.45	2.65	2.45	2.65	ns
LVCMOS15, Slow, 8 mA	1.05	1.23	2.46	2.66	2.46	2.66	ns
LVCMOS15, Slow, 12 mA	1.05	1.23	2.17	2.37	2.17	2.37	ns
LVCMOS15, Slow, 16 mA	1.05	1.23	2.15	2.35	2.15	2.35	ns
LVCMOS15, Fast, 2 mA	1.05	1.23	3.43	3.63	3.43	3.63	ns
LVCMOS15, Fast, 4 mA	1.05	1.23	2.42	2.62	2.42	2.62	ns
LVCMOS15, Fast, 6 mA	1.05	1.23	1.92	2.12	1.92	2.12	ns
LVCMOS15, Fast, 8 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVCMOS15, Fast, 12 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVCMOS15, Fast, 16 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVCMOS15_JEDEC, QUIETIO, 2 mA	1.10	1.28	5.64	5.84	5.64	5.84	ns
LVCMOS15_JEDEC, QUIETIO, 4 mA	1.10	1.28	4.75	4.95	4.75	4.95	ns
LVCMOS15_JEDEC, QUIETIO, 6 mA	1.10	1.28	4.21	4.41	4.21	4.41	ns
LVCMOS15_JEDEC, QUIETIO, 8 mA	1.10	1.28	4.06	4.26	4.06	4.26	ns
LVCMOS15_JEDEC, QUIETIO, 12 mA	1.10	1.28	3.75	3.95	3.75	3.95	ns
LVCMOS15_JEDEC, QUIETIO, 16 mA	1.10	1.28	3.53	3.73	3.53	3.73	ns
LVCMOS15_JEDEC, Slow, 2 mA	1.10	1.28	4.32	4.52	4.32	4.52	ns
LVCMOS15_JEDEC, Slow, 4 mA	1.10	1.28	3.56	3.76	3.56	3.76	ns
LVCMOS15_JEDEC, Slow, 6 mA	1.10	1.28	2.44	2.64	2.44	2.64	ns
LVCMOS15_JEDEC, Slow, 8 mA	1.10	1.28	2.47	2.67	2.47	2.67	ns
LVCMOS15_JEDEC, Slow, 12 mA	1.10	1.28	2.15	2.35	2.15	2.35	ns
LVCMOS15_JEDEC, Slow, 16 mA	1.10	1.28	2.15	2.35	2.15	2.35	ns
LVCMOS15_JEDEC, Fast, 2 mA	1.10	1.28	3.43	3.63	3.43	3.63	ns
LVCMOS15_JEDEC, Fast, 4 mA	1.10	1.28	2.42	2.62	2.42	2.62	ns
LVCMOS15_JEDEC, Fast, 6 mA	1.10	1.28	1.92	2.12	1.92	2.12	ns
LVCMOS15_JEDEC, Fast, 8 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVCMOS15_JEDEC, Fast, 12 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVCMOS15_JEDEC, Fast, 16 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVCMOS12, QUIETIO, 2 mA	0.98	1.16	6.54	6.74	6.54	6.74	ns
LVCMOS12, QUIETIO, 4 mA	0.98	1.16	5.12	5.32	5.12	5.32	ns

Table 34: **SSO Limit per V_{CCO}/GND Pair *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
3.3V	LVTTL	2	Fast	53	65	53	62
			Slow	70	80	70	73
			QuietIO	79	89	79	91
		4	Fast	23	30	23	27
			Slow	34	41	34	37
			QuietIO	44	49	44	46
		6	Fast	16	21	16	20
			Slow	21	28	21	25
			QuietIO	34	39	34	34
		8	Fast	12	16	12	15
			Slow	16	22	16	19
			QuietIO	27	28	27	24
		12	Fast	1	3	1	1
			Slow	2	5	2	4
			QuietIO	2	10	2	8
		16	Fast	1	3	1	1
			Slow	1	7	1	2
			QuietIO	3	11	3	8
		24	Fast	1	2	1	1
			Slow	2	5	2	2
			QuietIO	8	9	8	8
	PCI33_3			18	19	18	19
	PCI66_3			18	19	18	19
	SSTL_3_I			5	8	5	8
	SSTL_3_II			3	5	3	3
	DIFF_SSTL_3_I			15	24	15	24
	DIFF_SSTL_3_II			9	15	9	9
	SDIO			17	18	17	15

Input/Output Delay Switching Characteristics

Table 39: **IODELAY2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L[3]	
T_{IODCCK_CAL} / T_{IODCKC_CAL}	CAL pin Setup/Hold with respect to CK	0.28/ –0.13	0.33/ –0.13	0.48/ –0.13	N/A	ns
T_{IODCCK_CE} / T_{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.17/ –0.03	0.17/ –0.03	0.25/ –0.02	N/A	ns
T_{IODCCK_INC}/ T_{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.10/ 0.02	0.12/ 0.03	0.18/ 0.06	N/A	ns
T_{IODCCK_RST}/ T_{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.12/ –0.02	0.15/ –0.02	0.22/ –0.01	N/A	ns
T_{TAP1}[2]	Maximum tap 1 delay	8	14	16	N/A	ps
T_{TAP2}	Maximum tap 2 delay	40	66	77	N/A	ps
T_{TAP3}	Maximum tap 3 delay	95	120	140	N/A	ps
T_{TAP4}	Maximum tap 4 delay	108	141	166	N/A	ps
T_{TAP5}	Maximum tap 5 delay	171	194	231	N/A	ps
T_{TAP6}	Maximum tap 6 delay	207	249	292	N/A	ps
T_{TAP7}	Maximum tap 7 delay	212	276	343	N/A	ps
T_{TAP8}	Maximum tap 8 delay	322	341	424	N/A	ps
F_{MINCAL}	Minimum allowed bit rate for calibration in variable mode: VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX, and DIFF_PHASE_DETECTOR.	188	188	188	N/A	Mb/s
$T_{IODDO\_IDATAIN}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	–
$T_{IODDO\_ODATAIN}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	–

Notes:

1. Delay depends on IODELAY2 tap setting. See TRACE report for actual values.
2. Maximum delay = integer (number of taps/8) × T_{TAP8} + T_{TAPn} (where n equals the remainder). For minimum delay consult the TRACE setup and hold report. Minimum delay is typically greater than 30% of the maximum delay. Tap delays can vary by device and overall conditions. See TRACE report for actual values.
3. Spartan-6 -1L devices only support tap 0. See TRACE report for actual values.

Table 45: **Device DNA Interface Port Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T_{DNASSU}	Setup time on SHIFT before the rising edge of CLK	7				ns, Min
T_{DNASH}	Hold time on SHIFT after the rising edge of CLK	1				ns, Min
T_{DNADSU}	Setup time on DIN before the rising edge of CLK	7				ns, Min
T_{DNADH}	Hold time on DIN after the rising edge of CLK	1				ns, Min
T_{DNARSU}	Setup time on READ before the rising edge of CLK	7				ns, Min
		1,000				ns, Max
T_{DNARH}	Hold time on READ after the rising edge of CLK	1				ns, Min
$T_{DNADCKO}$	Clock-to-output delay on DOUT after rising edge of CLK	0.5				ns, Min
		6				ns, Max
$T_{DNACLKF}$[(2)]	CLK frequency	2				MHz, Max
$T_{DNACLKL}$	CLK Low time	50				ns, Min
$T_{DNACLKH}$	CLK High time	50				ns, Min

Notes:
1. The minimum READ pulse width is 8 ns, the maximum READ pulse width is 1 µs.
2. Also applies to TCK when reading DNA through the boundary-scan port.

Table 46: **Suspend Mode Switching Characteristics**

Symbol	Description	Min	Max	Units
Entering Suspend Mode				
$T_{SUSPENDHIGH\_AWAKE}$	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter	2.5	14	ns
$T_{SUSPENDFILTER}$	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled	31	430	ns
$T_{SUSPEND\_GWE}$	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior (without glitch filter)	–	15	ns
$T_{SUSPEND\_GTS}$	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements (without glitch filter)	–	15	ns
$T_{SUSPEND\_DISABLE}$	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled (without glitch filter)	–	1500	ns
Exiting Suspend Mode				
$T_{SUSPENDLOW\_AWAKE}$	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM or PLL lock time.	7	75	µs
$T_{SUSPEND\_ENABLE}$	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	7	41	µs
T_{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using **sw_clk:InternalClock** and **sw_gwe_cycle:1**.	–	80	ns
T_{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using **sw_clk:InternalClock** and **sw_gwe_cycle:512**.	–	20.5	µs
T_{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using **sw_clk:InternalClock** and **sw_gts_cycle:1**.	–	80	ns
T_{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using **sw_clk:InternalClock** and **sw_gts_cycle:512**.	–	20.5	µs
T_{SCP_AWAKE}	Rising edge of SCP pins to rising edge of AWAKE pin	7	75	µs

Table 47: **Configuration Switching Characteristics[1] *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
BPI Master Flash Mode Programming Switching[4]						
T_{BPICCO}[5]	A[25:0], FCS_B, FOE_B, FWE_B, LDC outputs valid after CCLK falling edge	15	15	15	20	ns, Max
$T_{BPIICCK}$	Master BPI CCLK (output) delay	10/100	10/100	10/100	10/130	µs, Min/Max
T_{BPIDCC}/T_{BPICCD}	Setup/Hold on D[15:0] data input pins	5.0/1.0	5.0/1.0	5.0/1.0	6.0/2.0	ns, Min
SPI Master Flash Mode Programming Switching[6]						
$T_{SPIDCC}/T_{SPIDCCD}$	DIN, MISO0, MISO1, MISO2, MISO3, Setup/Hold before/after the rising CCLK edge	5.0/1.0	5.0/1.0	5.0/1.0	7.0/1.0	ns, Min
$T_{SPIICCK}$	Master SPI CCLK (output) delay	0.4/7.0	0.4/7.0	0.4/7.0	0.4/10.0	µs, Min/Max
T_{SPICCM}	MOSI clock to out	13	13	13	19	ns, Max
$T_{SPICCFC}$	CSO_B clock to out	16	16	16	26	ns, Max
CCLK Output (Master Modes)						
T_{MCCKL}	Master CCLK clock duty cycle Low	40/60				%, Min/Max
T_{MCCKH}	Master CCLK clock duty cycle High	40/60				%, Min/Max
F_{MCCK}	Maximum frequency, serial mode (Master Serial/SPI) All devices	40	40	40	30	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T	40	40	40	25	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x8 mode, LX150, and LX150T	40	40	40	20	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x16 mode	35	35	35	20	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode	±50	±50	±50	±50	%
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time	5	5	5	8	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	5	5	5	8	ns, Min
USERCCLK Input						
$T_{USERCCLKL}$	USERCCLK clock minimum Low time	12	12	12	16	ns, Min
$T_{USERCCLKH}$	USERCCLK clock minimum High time	12	12	12	16	ns, Min
$F_{USERCCLK}$	Maximum USERCCLK frequency	40	40	40	30	MHz, Max

Notes:

1. Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
2. To support longer delays in configuration, use the design solutions described in UG380: *Spartan-6 FPGA Configuration User Guide*.
3. Table 6 specifies the power supply ramp time.
4. BPI mode is not supported in:
   - LX4, LX25, or LX25T devices
   - LX9 devices in the TQG144 package
   - LX9 or LX16 devices in the CPG196 package.
5. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
6. Defense-grade Spartan-6Q -2Q devices configure in single default SPI Master (x1) mode at T_j = –55°C. During operation and when using all other configuration functions, the minimum operating temperature is –40°C.

Table 57: **Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)[1]**

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges (DCM_CLKGEN)										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz
CLKOUT_FREQ_FXDV	Frequency for the CLKFXDV output	0.15625	187.5	0.15625	187.5	0.15625	166.5	0.15625	100	MHz
Output Clock Jitter[2][3]										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKOUT_PER_JITT_FXDV	Period jitter at the CLKFXDV output.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKFX_FREEZE_VAR	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX > 50 MHz	Maximum = ±3% of CLKFX period								ps
	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX < 50 MHz	Maximum = ±5% of CLKFX period								ps
CLKFX_FREEZE_TEMP_SLOPE	CLKFX period will change in free_oscillator mode over temperature. Add to CLKFX_FREEZE_VAR to determine total CLKFX period change. Percentage change for CLKFX period over 1°C.	Maximum = 0.1								%/°C
Duty Cycle[4][5]										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
CLKOUT_DUTY_CYCLE_FXDV	Duty cycle precision for the CLKFXDV outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
Lock Time										
LOCK_FX[2]	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX, CLKFX180, and CLKFXDV signals are valid. Lock time requires CLKFX_DIVIDE < F_{IN}/(0.50 MHz) when: F_{CLKIN} < 50 MHz	–	50	–	50	–	50	–	50	ms
	when: F_{CLKIN} > 50 MHz	–	5	–	5	–	5	–	5	ms

Table 64: **Global Clock Input to Output Delay With DCM in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in System-Synchronous Mode.							
$T_{ICKOFDCM}$	Global Clock and OUTFF *with* DCM	XC6SLX4	4.23	N/A	6.11	6.60	ns
		XC6SLX9	4.23	5.17	6.11	6.60	ns
		XC6SLX16	4.28	4.57	5.34	6.36	ns
		XC6SLX25	3.95	4.18	4.59	6.91	ns
		XC6SLX25T	3.95	4.18	4.59	N/A	ns
		XC6SLX45	4.37	4.70	5.50	6.85	ns
		XC6SLX45T	4.37	4.70	5.50	N/A	ns
		XC6SLX75	3.90	4.23	4.77	6.31	ns
		XC6SLX75T	3.90	4.23	4.77	N/A	ns
		XC6SLX100	3.86	4.16	4.66	7.25	ns
		XC6SLX100T	3.90	4.16	4.66	N/A	ns
		XC6SLX150	4.03	4.33	4.83	6.63	ns
		XC6SLX150T	4.03	4.33	4.83	N/A	ns
		XA6SLX4	4.55	N/A	6.11	N/A	ns
		XA6SLX9	4.55	N/A	6.11	N/A	ns
		XA6SLX16	4.62	N/A	5.33	N/A	ns
		XA6SLX25	4.27	N/A	4.59	N/A	ns
		XA6SLX25T	4.27	N/A	4.69	N/A	ns
		XA6SLX45	4.69	N/A	5.50	N/A	ns
		XA6SLX45T	4.69	N/A	5.50	N/A	ns
		XA6SLX75	4.22	N/A	4.77	N/A	ns
		XA6SLX75T	4.22	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.34	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	6.31	ns
		XQ6SLX75T	4.22	N/A	4.77	N/A	ns
		XQ6SLX150	N/A	N/A	4.96	6.63	ns
		XQ6SLX150T	4.62	N/A	4.96	N/A	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 67: **Global Clock Input to Output Delay With PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* PLL in Source-Synchronous Mode.							
$T_{ICKOFPLL\_0}$	Global Clock and OUTFF *with* PLL	XC6SLX4	5.49	N/A	7.44	8.55	ns
		XC6SLX9	5.49	6.29	7.44	8.55	ns
		XC6SLX16	5.23	5.77	6.79	8.21	ns
		XC6SLX25	5.00	5.35	6.10	8.54	ns
		XC6SLX25T	5.00	5.35	6.10	N/A	ns
		XC6SLX45	5.59	6.03	7.02	8.39	ns
		XC6SLX45T	5.59	6.03	7.02	N/A	ns
		XC6SLX75	4.96	5.41	6.22	8.32	ns
		XC6SLX75T	4.96	5.41	6.22	N/A	ns
		XC6SLX100	4.97	5.42	6.21	9.08	ns
		XC6SLX100T	5.01	5.42	6.21	N/A	ns
		XC6SLX150	4.59	5.06	5.86	8.13	ns
		XC6SLX150T	4.59	5.06	5.86	N/A	ns
		XA6SLX4	5.79	N/A	7.32	N/A	ns
		XA6SLX9	5.79	N/A	7.32	N/A	ns
		XA6SLX16	5.56	N/A	6.66	N/A	ns
		XA6SLX25	5.40	N/A	5.97	N/A	ns
		XA6SLX25T	5.40	N/A	6.07	N/A	ns
		XA6SLX45	5.89	N/A	6.90	N/A	ns
		XA6SLX45T	5.89	N/A	6.90	N/A	ns
		XA6SLX75	5.27	N/A	6.12	N/A	ns
		XA6SLX75T	5.27	N/A	6.12	N/A	ns
		XA6SLX100	N/A	N/A	6.80	N/A	ns
		XQ6SLX75	N/A	N/A	6.12	8.32	ns
		XQ6SLX75T	5.27	N/A	6.12	N/A	ns
		XQ6SLX150	N/A	N/A	5.88	8.13	ns
		XQ6SLX150T	5.21	N/A	5.88	N/A	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 69: **Global Clock Input to Output Delay With DCM and PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode.							
$T_{ICKOFDCM0\_PLL}$	Global Clock and OUTFF with DCM and PLL	XC6SLX4	5.58	N/A	7.42	8.54	ns
		XC6SLX9	5.58	6.19	7.42	8.54	ns
		XC6SLX16	5.50	6.06	7.05	8.24	ns
		XC6SLX25	5.57	6.04	7.02	8.33	ns
		XC6SLX25T	5.57	6.04	7.02	N/A	ns
		XC6SLX45	5.53	5.97	6.96	8.32	ns
		XC6SLX45T	5.53	5.97	6.96	N/A	ns
		XC6SLX75	5.55	6.00	6.99	8.54	ns
		XC6SLX75T	5.55	6.00	6.99	N/A	ns
		XC6SLX100	5.58	6.03	7.02	9.11	ns
		XC6SLX100T	5.62	6.03	7.02	N/A	ns
		XC6SLX150	5.32	5.70	6.41	8.26	ns
		XC6SLX150T	5.32	5.70	6.41	N/A	ns
		XA6SLX4	5.87	N/A	7.28	N/A	ns
		XA6SLX9	5.87	N/A	7.28	N/A	ns
		XA6SLX16	6.02	N/A	6.87	N/A	ns
		XA6SLX25	5.88	N/A	6.90	N/A	ns
		XA6SLX25T	5.88	N/A	7.00	N/A	ns
		XA6SLX45	5.82	N/A	6.81	N/A	ns
		XA6SLX45T	5.82	N/A	6.81	N/A	ns
		XA6SLX75	5.81	N/A	6.80	N/A	ns
		XA6SLX75T	5.81	N/A	6.80	N/A	ns
		XA6SLX100	N/A	N/A	6.88	N/A	ns
		XQ6SLX75	N/A	N/A	6.80	8.54	ns
		XQ6SLX75T	5.81	N/A	6.80	N/A	ns
		XQ6SLX150	N/A	N/A	6.41	8.26	ns
		XQ6SLX150T	5.90	N/A	6.41	N/A	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 72: **Global Clock Setup and Hold With DCM in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSDCM}/ T_{PHDCM}	No Delay Global Clock and IFF(2) with DCM in System-Synchronous Mode	XC6SLX4	1.54/0.06	N/A	1.75/0.12	2.84/0.27	ns
		XC6SLX9	1.54/0.06	1.63/0.12	1.75/0.12	2.84/0.27	ns
		XC6SLX16	1.72/–0.18	1.87/–0.17	2.13/–0.17	2.31/0.26	ns
		XC6SLX25	1.70/–0.03	1.78/–0.02	2.00/–0.02	2.88/0.20	ns
		XC6SLX25T	1.70/0.07	1.78/0.08	2.00/0.08	N/A	ns
		XC6SLX45	1.74/–0.03	1.84/–0.02	2.02/–0.02	2.64/0.52	ns
		XC6SLX45T	1.74/–0.01	1.84/0.00	2.02/0.00	N/A	ns
		XC6SLX75	1.86/0.11	1.98/0.12	2.20/0.12	2.96/0.58	ns
		XC6SLX75T	1.86/0.11	1.98/0.12	2.20/0.12	N/A	ns
		XC6SLX100	1.64/0.07	1.72/0.08	1.97/0.08	2.70/0.99	ns
		XC6SLX100T	1.64/0.09	1.72/0.10	1.97/0.10	N/A	ns
		XC6SLX150	1.53/0.39	1.62/0.40	1.82/0.40	2.75/1.00	ns
		XC6SLX150T	1.53/0.39	1.62/0.40	1.82/0.40	N/A	ns
		XA6SLX4	1.65/0.16	N/A	1.75/0.26	N/A	ns
		XA6SLX9	1.65/0.16	N/A	1.75/0.26	N/A	ns
		XA6SLX16	1.88/0.02	N/A	2.13/0.03	N/A	ns
		XA6SLX25	1.80/0.16	N/A	2.05/0.17	N/A	ns
		XA6SLX25T	1.80/0.16	N/A	2.13/0.17	N/A	ns
		XA6SLX45	1.75/0.12	N/A	2.02/0.13	N/A	ns
		XA6SLX45T	1.75/0.12	N/A	2.02/0.13	N/A	ns
		XA6SLX75	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XA6SLX75T	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XA6SLX100	N/A	N/A	2.46/0.24	N/A	ns
		XQ6SLX75	N/A	N/A	2.20/0.12	2.96/0.58	ns
		XQ6SLX75T	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XQ6SLX150	N/A	N/A	1.82/0.56	2.75/1.00	ns
		XQ6SLX150T	1.65/0.55	N/A	1.82/0.56	N/A	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Date	Version	Description of Revisions
06/14/10	1.5	In Table 2, added note 5 and added temperature range to V_{FS} and R_{FUSE}. Removed speed grade delineation, revised I_{RPD} description, and updated note 2 in Table 4. Added note 2 to Table 7. Added DIFF_MOBILE_DDR to Table 8 and Table 10. Added note 4 to Table 15. Changed minimum DV_{PPIN} in Table 16. Updated $F_{GTPDRPCLK}$ in Table 19. Increased maximum T_{LLSKEW} in Table 22. Updated descriptions and added data to Table 23. Removed note 1 and added new data to the Networking Applications section in Table 25. Updated Table 26 and Table 27 to the data in ISE v12.1 software with speed specification v1.08. In Table 28, added DIFF_MOBILE_DDR and updated -4 speed grade data. Updated the maximum I/O pairs per bank in Table 33. Updated note 2 on Table 39. Revised the F_{MAX} in Table 44. In Table 47, updated description for $T_{SMCKCSO}$, revised values for T_{POR} and added Min value, added $T_{BPIICCK}$ and $T_{SPIICCK}$. Also in Table 47, added device dependencies to F_{SMCCK} and F_{RBCCK}. Updated and added data to Table 63 through Table 78, and Table 81. In Table 79, added data on the XC6SLX45-FG(G)676 and revised the XC6SLX45T and XC6SLX150T values. The following changes to this specification are addressed in the product change notice XCN10024, *MCB Performance and JTAG Revision Code for Spartan-6 LX16 and LX45 FPGAs*. In Table 2, revised the V_{CCINT} to add the memory controller block extended performance specifications. In Table 25, changed the standard specifications and added extended performance specifications for the memory controller block and note 2. Added note 4 and updated values in Table 34.
06/24/10	1.6	Production release of XC6SLX45T (-2 and -3 speed grades), XC6SLX16 and XC6SLX45 (-3 speed grade) devices which includes changes to Table 26 and Table 27 (ISE v12.1 software with speed specification v1.08). Added the -3N speed grade, which designates Spartan-6 devices that do not support MCB functionality. This includes changes to Table 2 (note 2), Table 25 (note 4), and Switching Characteristics (Table 26). Updated Simultaneously Switching Outputs discussion. Added -3 speed grade values for T_{TAP} and F_{MINCAL} values in Table 39. In Table 40, updated T_{RPW} (-2 and -3 speed grade) values and F_{TOG} (-3 speed grade) values. In Table 48, updated T_{GIO} (-2 and -3 speed grade) values. Updated -3 values in spread spectrum section of Table 57.
07/16/10	1.7	Production release of specific devices listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 4 advising designers of the patch which contains v1.11. Also updated the -1L speed specification to v1.04. Updated numerous -4 and -1L values. Added -4 T_{TAP} values and F_{MINCAL} to Table 39. Revised T_{CINCK}/T_{CKCIN} in Table 40. In Table 41, revised T_{SHCKO}. In Table 42, revised T_{REG}. Added new -1L values to Table 47. Added and updated values in Table 79.
07/26/10	1.8	Production release of XC6SLX25, XC6SLX25T, XC6SLX100 and XC6SLX100T in the specific speed grades listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 7 to Table 2 and moved V_{FS} and R_{FUSE} to a new Table 3. Added I_{HS} and note 4 to Table 4. Added note 1 to Table 28. Added and updated SSO limits per V_{CCO}/GND pairs in Table 34. Added note 3 to Table 47. In Table 54, removed -1L specifications for CLKOUT_PER_JITT_DV1/2 and revised CLKIN_CLKFB_PHASE and CLKOUT_PHASE_DLL values. Updated note 3 in both Table 56 and Table 57.
08/23/10	1.9	Updated values for $F_{GTPRANGE1}$, $F_{GTPRANGE2}$, and $F_{GPLLMIN}$ in Table 18. Revised -3 and -4 values in Table 21. Removed the -1L speed grade readback support restriction and note 3 in Table 47.
11/05/10	1.10	Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.3 software with speed specification v1.12 for the -2 speed grade available in the 12.3 *Speed Files Patch*. Added note 3 advising designers of the patch which contains v1.12. In Table 2, added note 4. In Table 4, added note 2. In Table 10, added notes 2 and 3. In Table 44, added note 2. In Table 47, updated symbol for T_{SMWCCK}/T_{SMCCKW}, changed -1L values for $T_{USERCCLKH}$ and $T_{USERCCLKL}$, and added and revised the modes for F_{MCCK} and F_{SMCCK}. In Table 53, redefined and expanded description for CLKIN_FREQ_DLL and rewrote note 3. Updated title of Table 58. Also in Table 78, revised T_{DCD_CLK} for XC6SLX150 and XC6SLX150T. Changed description of T_{PSFD}/ T_{PHFD} in Table 71. For the -1L speed grade, updated data sheet to ISE 12.3 software with speed specification v1.05 which revised the values in the following tables: Table 25, Table 28, Table 35, Table 36, Table 37, Table 40 through Table 43, Table 48 through Table 56, Table 62 through Table 78, Table 80, and Table 81. Updated Notice of Disclaimer.

Date	Version	Description of Revisions
01/10/11	1.11	Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.4 software with speed specification v1.15 for the -4, -3, -3N, and -2 speed grades. Added note 3 to Table 27. Also updated the -1L speed grade requirements to ISE v12.4 software with speed specification v1.06. Revised -3N definition throughout the document. Added note 4 to Table 2 and updated note 5. Added information on V_{CCINT} to note 1 in Table 5. Updated Networking Applications -3 values in Table 25 to match improvements made in ISE v12.4. In Table 28, added note 1 and revised the T_{IOTP} values for LVDS_33, LVDS_25, MINI_LVDS_33, MINI_LVDS_25, RSDS_33, RSDS_25, TMDS_33. PPDS_33, and PPDS_25. Added note 3 to Table 55.
02/11/11	1.12	As described in XCN11008: *Product Discontinuation Notice For Spartan-6 LXT -4 Devices*, the -4 speed specifications have been discontinued. As outlined in page 2 of the XCN, designers currently using -4 speed specifications should rerun timing analysis using the new -3 speed specifications before moving to a replacement device. Updated the networking applications section of Table 25. Updated -2 speed specifications throughout document and added note 3 to Table 27 advising designers to use the -2 speed specification update (v1.17) with the ISE 12.4 software patch. Added F_{CLKDIV} to Table 37 and Table 38. Updated note 2 in Table 39. Updated units for $T_{SMCKCSO}$ and T_{BPICCO} in Table 47. Updated -1L in Table 71. Removed Note 2: *Package delay information is available for these device/package combinations. This information can be used to deskew the package* from Table 79.
03/31/11	2.0	Production release of XC6SLX45 in the -1L speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. In Table 39, removed values in the -1L column and added note 3 as IODELAY2 only supports Tap0 for lower-power devices. Updated copyright page 1 and Notice of Disclaimer.
05/20/11	2.1	Production release of XC6SLX100 and XC6SLX150 in the specific speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. Updated Table 27 and Note 7 with changes per XCN11012: *Speed File Change for -3N Devices*. Revised Switching Characteristics section for speed specifications: v1.18 for -3, -3N, and -2; including improvements in Table 73 through Table 77 and Table 81. Removed *Memory Controller Block* from the performance heading in Table 2 and revised Note 2. In Table 4, added Note 1 to C_{IN} and updated the description of R_{IN_TERM}. Updated Note 1 in Table 5. Updated Note 1 of Table 7. In Table 25, added and removed -1L specifications, increased the standard performance DDR3 specifications, removed the extended performance DDR3 row and updated Note 3 and Note 4. Clarified the introductory information for Table 28 and Table 30. In Table 32: Revised V_{MEAS} value for LVCMOS12; revised V_{REF} for LVDS_25, LVDS_33, BLVDS_25,MINI_LVDS_25, MINI_LVDS_33, RSDS_25, and RSDS_33; revised R_{REF} for BLVDS_25 and TMDS_33; and added Note 4 and Note 5. Updated Note 2 and Note 3 in Table 39. In Table 47, revised the values and description of T_{POR} including adding Note 3. Also in Table 47, augmented the description and added specifications for F_{RBCCK} and removed XC6SLX4 from F_{MCCK} (maximum frequency, parallel mode (Master SelectMAP/BPI). Added BUFGMUX to Table 48 title. Added Table 50. In Table 52, revised specifications for $T_{EXTFDVAR}$ and $F_{INJITTER}$. In Table 54 removed the 5 MHz < CLKIN_FREQ_DLL parameter in the LOCK_DLL description. In both Table 56 and Table 57, removed the 5 MHz < F_{CLKIN} parameter in the LOCK_FX description. In Table 58, updated description for PSCLK_FREQ and PSCLK_PULSE. Revised title and symbol of Table 70, added new speed specifications for -1L, and added Note 2. Added Table 71.
07/11/11	2.2	Added the Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices to all appropriate tables while sometimes removing the XC6S nomenclature. Added expanded temperature range (Q) to all appropriate tables. Updated T_{SOL} packages in Table 1. Added R_{OUT_TERM} to Table 4. Updated Note 2 on Table 13. Production release of the XC6SLX4, XC6SLX9, XC6SLX16, XC6SLX25, XC6SLX75, XQ6SLX75, and XQ6SLX150 in Table 26 and Table 27 using ISE v13.2 software with -1L speed specification v1.07. Production release of the XA6SLX16, XA6SLX25T, XA6SLX45, XA6SLX45T, XQ6SLX75, XQ6SLX75T, XQ6SLX150, and XQ6SLX150T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices(1). Updated CS(G)484 from CSG484 throughout data sheet. Clarified Note 3 in Table 39.
08/08/11	2.3	Production release of the XA6SLX25, XA6SLX75, and XA6SLX75T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19.