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Details

Product Status	Active
Number of LABs/CLBs	3411
Number of Logic Elements/Cells	43661
Total RAM Bits	2138112
Number of I/O	296
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA, CSPBGA
Supplier Device Package	484-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx45t-2csg484c

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description					Units
V_{IN} and V_{TS} ⁽³⁾	I/O input voltage or voltage applied to 3-state output, relative to GND ⁽⁴⁾	All user and dedicated I/Os	Commercial	DC	–0.60 to 4.10	V
				20% overshoot duration	–0.75 to 4.25	V
				8% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
			Industrial	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
			Expanded (Q)	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
		Restricted to maximum of 100 user I/Os	Commercial	20% overshoot duration	–0.75 to 4.35	V
				15% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
				10% overshoot duration	–0.75 to 4.45	V
			Industrial	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
			Expanded (Q)	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
T_{STG}	Storage temperature (ambient)				–65 to 150	°C
T_{SOL}	Maximum soldering temperature ⁽⁶⁾ (TQG144, CPG196, CSG225, CSG324, CSG484, and FTG256)				+260	°C
	Maximum soldering temperature ⁽⁶⁾ (Pb-free packages: FGG484, FGG676, and FGG900)				+250	°C
	Maximum soldering temperature ⁽⁶⁾ (Pb packages: CS484, FT256, FG484, FG676, and FG900)				+220	°C
T_j	Maximum junction temperature ⁽⁶⁾				+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- When programming eFUSE, $V_{FS} \leq V_{CCAUX}$. Requires up to 40 mA current. For read mode, V_{FS} can be between GND and 3.45 V.
- I/O absolute maximum limit applied to DC and AC signals. Overshoot duration is the percentage of a data period that the I/O is stressed beyond 3.45V.
- For I/O operation, refer to [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.
- Maximum percent overshoot duration to meet 4.40V maximum.
- For soldering guidelines and thermal considerations, see [UG385](#): *Spartan-6 FPGA Packaging and Pinout Specification*.

Quiescent Current

Typical values for quiescent supply current are specified at nominal voltage, 25°C junction temperatures (T_j). Quiescent supply current is specified by speed grade for Spartan-6 devices. Xilinx recommends analyzing static power consumption using the XPOWER™ Estimator (XPE) tool (download at <http://www.xilinx.com/power>) for conditions other than those specified in Table 5.

Table 5: Typical Quiescent Supply Current

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	LX4	4.0	4.0	4.0	2.4	mA
		LX9	4.0	4.0	4.0	2.4	mA
		LX16	6.0	6.0	6.0	4.0	mA
		LX25	11.0	11.0	11.0	6.6	mA
		LX25T	11.0	11.0	11.0	N/A	mA
		LX45	15.0	15.0	15.0	9.0	mA
		LX45T	15.0	15.0	15.0	N/A	mA
		LX75	29.0	29.0	29.0	17.4	mA
		LX75T	29.0	29.0	29.0	N/A	mA
		LX100	36.0	36.0	36.0	21.6	mA
		LX100T	36.0	36.0	36.0	N/A	mA
		LX150	51.0	51.0	51.0	31.0	mA
		LX150T	51.0	51.0	51.0	N/A	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	LX4	1.0	1.0	1.0	1.0	mA
		LX9	1.0	1.0	1.0	1.0	mA
		LX16	2.0	2.0	2.0	2.0	mA
		LX25	2.0	2.0	2.0	2.0	mA
		LX25T	2.0	2.0	2.0	N/A	mA
		LX45	3.0	3.0	3.0	3.0	mA
		LX45T	3.0	3.0	3.0	N/A	mA
		LX75	4.0	4.0	4.0	4.0	mA
		LX75T	4.0	4.0	4.0	N/A	mA
		LX100	5.0	5.0	5.0	5.0	mA
		LX100T	5.0	5.0	5.0	N/A	mA
		LX150	7.0	7.0	7.0	7.0	mA
		LX150T	7.0	7.0	7.0	N/A	mA

Table 21: GTP Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Conditions	Speed Grade				Units
			-3	-3N	-2	-1L	
F _{TXOUT}	TXOUTCLK maximum frequency		320	320	270	N/A	MHz
F _{RXREC}	RXRECCLK maximum frequency		320	320	270	N/A	MHz
T _{RX}	RXUSRCLK maximum frequency		320	320	270	N/A	MHz
T _{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz
T _{TX}	TXUSRCLK maximum frequency		320	320	270	N/A	MHz
T _{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz

Notes:

1. Clocking must be implemented as described in [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#).

Table 22: GTP Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
T _{RTX}	TX Rise time	20%–80%	–	140	–	ps
T _{FTX}	TX Fall time	80%–20%	–	120	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	400	ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–	20	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–	50	ns
T _{J3.125}	Total Jitter ⁽²⁾	3.125 Gb/s	–	–	0.35	UI
D _{J3.125}	Deterministic Jitter ⁽²⁾		–	–	0.15	UI
T _{J2.5}	Total Jitter ⁽²⁾	2.5 Gb/s	–	–	0.33	UI
D _{J2.5}	Deterministic Jitter ⁽²⁾		–	–	0.15	UI
T _{J1.62}	Total Jitter ⁽²⁾	1.62 Gb/s	–	–	0.20	UI
D _{J1.62}	Deterministic Jitter ⁽²⁾		–	–	0.10	UI
T _{J1.25}	Total Jitter ⁽²⁾	1.25 Gb/s	–	–	0.20	UI
D _{J1.25}	Deterministic Jitter ⁽²⁾		–	–	0.10	UI
T _{J614}	Total Jitter ⁽²⁾	614 Mb/s	–	–	0.10	UI
D _{J614}	Deterministic Jitter ⁽²⁾		–	–	0.05	UI

Notes:

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP transceiver sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS33, Slow, 6 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVC MOS33, Slow, 8 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVC MOS33, Slow, 12 mA	1.41	1.59	2.53	2.73	2.53	2.73	ns
LVC MOS33, Slow, 16 mA	1.41	1.59	2.45	2.65	2.45	2.65	ns
LVC MOS33, Slow, 24 mA	1.41	1.59	2.42	2.62	2.42	2.62	ns
LVC MOS33, Fast, 2 mA	1.41	1.59	4.05	4.25	4.05	4.25	ns
LVC MOS33, Fast, 4 mA	1.41	1.59	2.66	2.86	2.66	2.86	ns
LVC MOS33, Fast, 6 mA	1.41	1.59	2.46	2.66	2.46	2.66	ns
LVC MOS33, Fast, 8 mA	1.41	1.59	2.21	2.41	2.21	2.41	ns
LVC MOS33, Fast, 12 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVC MOS33, Fast, 16 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVC MOS33, Fast, 24 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVC MOS25, QUIETIO, 2 mA	0.89	1.07	5.00	5.20	5.00	5.20	ns
LVC MOS25, QUIETIO, 4 mA	0.89	1.07	3.85	4.05	3.85	4.05	ns
LVC MOS25, QUIETIO, 6 mA	0.89	1.07	3.60	3.80	3.60	3.80	ns
LVC MOS25, QUIETIO, 8 mA	0.89	1.07	3.34	3.54	3.34	3.54	ns
LVC MOS25, QUIETIO, 12 mA	0.89	1.07	2.98	3.18	2.98	3.18	ns
LVC MOS25, QUIETIO, 16 mA	0.89	1.07	2.79	2.99	2.79	2.99	ns
LVC MOS25, QUIETIO, 24 mA	0.89	1.07	2.64	2.84	2.64	2.84	ns
LVC MOS25, Slow, 2 mA	0.89	1.07	3.96	4.16	3.96	4.16	ns
LVC MOS25, Slow, 4 mA	0.89	1.07	2.96	3.16	2.96	3.16	ns
LVC MOS25, Slow, 6 mA	0.89	1.07	2.88	3.08	2.88	3.08	ns
LVC MOS25, Slow, 8 mA	0.89	1.07	2.63	2.83	2.63	2.83	ns
LVC MOS25, Slow, 12 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVC MOS25, Slow, 16 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVC MOS25, Slow, 24 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVC MOS25, Fast, 2 mA	0.89	1.07	3.52	3.72	3.52	3.72	ns
LVC MOS25, Fast, 4 mA	0.89	1.07	2.43	2.63	2.43	2.63	ns
LVC MOS25, Fast, 6 mA	0.89	1.07	2.23	2.43	2.23	2.43	ns
LVC MOS25, Fast, 8 mA	0.89	1.07	2.16	2.36	2.16	2.36	ns
LVC MOS25, Fast, 12 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVC MOS25, Fast, 16 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVC MOS25, Fast, 24 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVC MOS18, QUIETIO, 2 mA	1.25	1.43	6.11	6.31	6.11	6.31	ns
LVC MOS18, QUIETIO, 4 mA	1.25	1.43	4.88	5.08	4.88	5.08	ns
LVC MOS18, QUIETIO, 6 mA	1.25	1.43	4.20	4.40	4.20	4.40	ns
LVC MOS18, QUIETIO, 8 mA	1.25	1.43	3.86	4.06	3.86	4.06	ns
LVC MOS18, QUIETIO, 12 mA	1.25	1.43	3.49	3.69	3.49	3.69	ns

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS18, QUIETIO, 16 mA	1.25	1.43	3.34	3.54	3.34	3.54	ns
LVC MOS18, QUIETIO, 24 mA	1.25	1.43	3.18	3.38	3.18	3.38	ns
LVC MOS18, Slow, 2 mA	1.25	1.43	4.79	4.99	4.79	4.99	ns
LVC MOS18, Slow, 4 mA	1.25	1.43	3.84	4.04	3.84	4.04	ns
LVC MOS18, Slow, 6 mA	1.25	1.43	3.17	3.37	3.17	3.37	ns
LVC MOS18, Slow, 8 mA	1.25	1.43	2.37	2.57	2.37	2.57	ns
LVC MOS18, Slow, 12 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns
LVC MOS18, Slow, 16 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns
LVC MOS18, Slow, 24 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns
LVC MOS18, Fast, 2 mA	1.25	1.43	3.78	3.98	3.78	3.98	ns
LVC MOS18, Fast, 4 mA	1.25	1.43	2.54	2.74	2.54	2.74	ns
LVC MOS18, Fast, 6 mA	1.25	1.43	2.02	2.22	2.02	2.22	ns
LVC MOS18, Fast, 8 mA	1.25	1.43	1.95	2.15	1.95	2.15	ns
LVC MOS18, Fast, 12 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns
LVC MOS18, Fast, 16 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns
LVC MOS18, Fast, 24 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns
LVC MOS18_JEDEC, QUIETIO, 2 mA	1.01	1.19	6.09	6.29	6.09	6.29	ns
LVC MOS18_JEDEC, QUIETIO, 4 mA	1.01	1.19	4.89	5.09	4.89	5.09	ns
LVC MOS18_JEDEC, QUIETIO, 6 mA	1.01	1.19	4.20	4.40	4.20	4.40	ns
LVC MOS18_JEDEC, QUIETIO, 8 mA	1.01	1.19	3.87	4.07	3.87	4.07	ns
LVC MOS18_JEDEC, QUIETIO, 12 mA	1.01	1.19	3.49	3.69	3.49	3.69	ns
LVC MOS18_JEDEC, QUIETIO, 16 mA	1.01	1.19	3.34	3.54	3.34	3.54	ns
LVC MOS18_JEDEC, QUIETIO, 24 mA	1.01	1.19	3.17	3.37	3.17	3.37	ns
LVC MOS18_JEDEC, Slow, 2 mA	1.01	1.19	4.79	4.99	4.79	4.99	ns
LVC MOS18_JEDEC, Slow, 4 mA	1.01	1.19	3.84	4.04	3.84	4.04	ns
LVC MOS18_JEDEC, Slow, 6 mA	1.01	1.19	3.18	3.38	3.18	3.38	ns
LVC MOS18_JEDEC, Slow, 8 mA	1.01	1.19	2.37	2.57	2.37	2.57	ns
LVC MOS18_JEDEC, Slow, 12 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns
LVC MOS18_JEDEC, Slow, 16 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns
LVC MOS18_JEDEC, Slow, 24 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns
LVC MOS18_JEDEC, Fast, 2 mA	1.01	1.19	3.75	3.95	3.75	3.95	ns
LVC MOS18_JEDEC, Fast, 4 mA	1.01	1.19	2.54	2.74	2.54	2.74	ns
LVC MOS18_JEDEC, Fast, 6 mA	1.01	1.19	2.02	2.22	2.02	2.22	ns
LVC MOS18_JEDEC, Fast, 8 mA	1.01	1.19	1.94	2.14	1.94	2.14	ns
LVC MOS18_JEDEC, Fast, 12 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns
LVC MOS18_JEDEC, Fast, 16 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns
LVC MOS18_JEDEC, Fast, 24 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns

I/O Standard Measurement Methodology

Input Delay Measurements

Table 31 shows the test setup parameters used for measuring input delay.

Table 31: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)}$	$V_H^{(1)}$	$V_{MEAS}^{(3)(4)}$	$V_{REF}^{(2)(4)}$
LVTTTL (Low-Voltage Transistor-Transistor Logic)	LVTTTL	0	3.0	1.4	—
LVC MOS (Low-Voltage CMOS), 3.3V	LVC MOS33	0	3.3	1.65	—
LVC MOS, 2.5V	LVC MOS25	0	2.5	1.25	—
LVC MOS, 1.8V	LVC MOS18	0	1.8	0.9	—
LVC MOS, 1.5V	LVC MOS15	0	1.5	0.75	—
LVC MOS, 1.2V	LVC MOS12	0	1.2	0.6	—
PCI (Peripheral Component Interface), 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3	Per PCI Specification			—
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III	HSTL_III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	1.1
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
SSTL, Class II, 1.5V	SSTL15_II	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	$1.25 - 0.125$	$1.25 + 0.125$	0 ⁽⁵⁾	—
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V & 3.3V	LVPECL_25, LVPECL_33	$1.2 - 0.3$	$1.2 + 0.3$	0 ⁽⁵⁾	—
BLVDS (Bus LVDS), 2.5V	BLVDS_25	$1.3 - 0.125$	$1.3 + 0.125$	0 ⁽⁵⁾	—
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	$1.2 - 0.125$	$1.2 + 0.125$	0 ⁽⁵⁾	—
RS DS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RS DS_25, RS DS_33	$1.2 - 0.1$	$1.2 + 0.1$	0 ⁽⁵⁾	—
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	$3.0 - 0.1$	$3.0 + 0.1$	0 ⁽⁵⁾	—
PPDS (Point-to-Point Differential Signaling), 2.5V & 3.3V	PPDS_25, PPDS_33	$1.25 - 0.1$	$1.25 + 0.1$	0 ⁽⁵⁾	—

Notes:

1. Input waveform switches between V_L and V_H .
2. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 4.
5. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 4 and Figure 5.

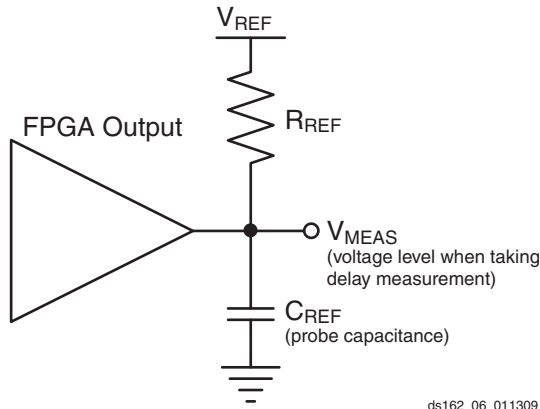
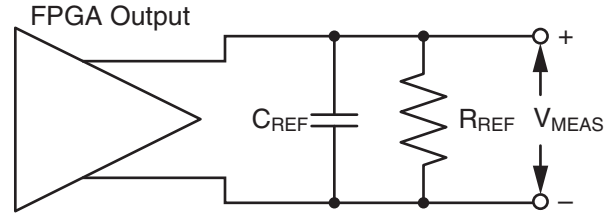


Figure 4: Single-Ended Test Setup



ds162_07_011309

Figure 5: Differential Test Setup

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 32.
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 32: Output Delay Measurement Methodology

Description	I/O Standard Attribute	R_{REF} (Ω)	$C_{REF}^{(1)}$ (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTTL (Low-Voltage Transistor-Transistor Logic)	LVTTTL (all)	1M	0	1.4	0
LVC MOS (Low-Voltage CMOS), 3.3V	LVC MOS33	1M	0	1.65	0
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS, 1.2V	LVC MOS12	1M	0	0.6	0
PCI (Peripheral Component Interface) 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3 (rising edge)	25	10 ⁽²⁾	0.94	0
	PCI33_3, PCI66_3 (falling edge)	25	10 ⁽²⁾	2.03	3.3
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25

Input/Output Logic Switching Characteristics

Table 35: ILOGIC2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T _{ICE0CK} /T _{ICKCE0}	CE0 pin Setup/Hold with respect to CLK	0.56/ −0.30	0.56/ −0.25	0.79/ −0.22	1.21/ −0.52	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.74/ −0.23	0.74/ −0.22	0.98/ −0.20	1.31/ −0.45	ns
T _{IDOCK} /T _{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	1.19/ −0.83	1.36/ −0.83	1.73/ −0.83	2.18/ −1.77	ns
T _{IDOCKD} /T _{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	0.31/ 0.00	0.47/ 0.00	0.54/ 0.00	0.63/ −0.39	ns
Combinatorial						
T _{IDI}	D pin to O pin propagation delay, no Delay	0.95	1.28	1.53	2.25	ns
T _{IDID}	DDLY pin to O pin propagation delay (using IODELAY2)	0.23	0.39	0.44	0.74	ns
Sequential Delays						
T _{IDLO}	D pin to Q pin using flip-flop as a latch without Delay	1.56	1.86	2.39	3.49	ns
T _{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY2)	0.68	0.97	1.20	1.94	ns
T _{ICKQ}	CLK to Q outputs for XC devices	1.03	1.24	1.43	2.11	ns
	CLK to Q outputs for XA and XQ devices	1.38	N/A	1.78	2.11	ns
T _{RQ_ILOGIC2}	SR pin to Q outputs	1.81	1.81	2.50	3.05	ns

Table 36: OLOGIC2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T _{ODCK} /T _{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.81/ −0.05	0.86/ −0.05	1.18/ 0.00	1.73/ −0.27	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.75/ −0.10	0.75/ −0.10	1.01/ −0.05	1.66/ −0.23	ns
T _{OSRCK} /T _{OCKSR}	SR pin Setup/Hold with respect to CLK	0.70/ −0.28	0.79/ −0.28	1.03/ −0.23	1.39/ −0.47	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.24/ −0.08	0.56/ −0.06	0.83/ −0.01	0.99/ −0.19	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.58/ −0.06	0.72/ −0.06	1.18/ −0.01	1.51/ −0.13	ns
Sequential Delays						
T _{OCKQ}	CLK to OQ/TQ out for XC devices	0.48	0.51	0.74	0.74	ns
	CLK to OQ/TQ out for XA and XQ devices	0.85	N/A	1.16	0.74	ns
T _{RQ_OLOGIC2}	SR pin to OQ/TQ out	1.81	1.81	2.50	3.05	ns

Input/Output Delay Switching Characteristics

Table 39: IODELAY2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L ⁽³⁾	
$T_{\text{IODCCK_CAL}} / T_{\text{IODCKC_CAL}}$	CAL pin Setup/Hold with respect to CK	0.28/ -0.13	0.33/ -0.13	0.48/ -0.13	N/A	ns
$T_{\text{IODCCK_CE}} / T_{\text{IODCKC_CE}}$	CE pin Setup/Hold with respect to CK	0.17/ -0.03	0.17/ -0.03	0.25/ -0.02	N/A	ns
$T_{\text{IODCCK_INC}} / T_{\text{IODCKC_INC}}$	INC pin Setup/Hold with respect to CK	0.10/ 0.02	0.12/ 0.03	0.18/ 0.06	N/A	ns
$T_{\text{IODCCK_RST}} / T_{\text{IODCKC_RST}}$	RST pin Setup/Hold with respect to CK	0.12/ -0.02	0.15/ -0.02	0.22/ -0.01	N/A	ns
$T_{\text{TAP1}}^{(2)}$	Maximum tap 1 delay	8	14	16	N/A	ps
T_{TAP2}	Maximum tap 2 delay	40	66	77	N/A	ps
T_{TAP3}	Maximum tap 3 delay	95	120	140	N/A	ps
T_{TAP4}	Maximum tap 4 delay	108	141	166	N/A	ps
T_{TAP5}	Maximum tap 5 delay	171	194	231	N/A	ps
T_{TAP6}	Maximum tap 6 delay	207	249	292	N/A	ps
T_{TAP7}	Maximum tap 7 delay	212	276	343	N/A	ps
T_{TAP8}	Maximum tap 8 delay	322	341	424	N/A	ps
F_{MINCAL}	Minimum allowed bit rate for calibration in variable mode: VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX, and DIFF_PHASE_DETECTOR.	188	188	188	N/A	Mb/s
$T_{\text{IODDO_IDATAIN}}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	—
$T_{\text{IODDO_ODATAIN}}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	—

Notes:

- Delay depends on IODELAY2 tap setting. See TRACE report for actual values.
- Maximum delay = integer (number of taps/8) $\times$ T_{TAP8} + T_{TAPn} (where n equals the remainder). For minimum delay consult the TRACE setup and hold report. Minimum delay is typically greater than 30% of the maximum delay. Tap delays can vary by device and overall conditions. See TRACE report for actual values.
- Spartan-6 -1L devices only support tap 0. See TRACE report for actual values.

DSP48A1 Switching Characteristics

Table 44: DSP48A1 Switching Characteristics

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-3	-3N	-2	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock									
$T_{\text{DSPDCK_A_A1REG}}/$ $T_{\text{DSPCKD_A_A1REG}}$	A input to A1 register CLK	N/A	N/A	N/A	0.15/ 0.09	0.17/ 0.09	0.17/ 0.09	0.32/ 0.09	ns
$T_{\text{DSPDCK_D_B1REG}}/$ $T_{\text{DSPCKD_D_B1REG}}$	D input to B1 register CLK	Yes	N/A	N/A	1.90/ −0.07	1.95/ −0.07	1.95/ −0.07	2.82/ −0.07	ns
$T_{\text{DSPDCK_C_CREG}}/$ $T_{\text{DSPCKD_C_CREG}}$	C input to C register CLK for XC devices	N/A	N/A	N/A	0.11/ 0.15	0.13/ 0.15	0.13/ 0.15	0.24/ 0.09	ns
	C input to C register CLK for XA and XQ devices				0.11/ 0.19	N/A	0.13/ 0.23	0.24/ 0.09	
$T_{\text{DSPDCK_D_DREG}}/$ $T_{\text{DSPCKD_D_DREG}}$	D input to D register CLK for XC devices	N/A	N/A	N/A	0.09/ 0.15	0.10/ 0.15	0.10/ 0.15	0.19/ 0.12	ns
	D input to D register CLK for XA and XQ devices				0.09/ 0.23	N/A	0.10/ 0.27	0.19/ 0.12	
$T_{\text{DSPDCK_OPMODE_B1REG}}/$ $T_{\text{DSPCKD_OPMODE_B1REG}}$	OPMODE input to B1 register CLK	Yes	N/A	N/A	1.97/ 0.01	2.00/ 0.01	2.00/ 0.01	2.85/ 0.01	ns
$T_{\text{DSPDCK_OPMODE_OPMODEREG}}/$ $T_{\text{DSPCKD_OPMODE_OPMODEREG}}$	OPMODE input to OPMODE register CLK for XC devices	N/A	N/A	N/A	0.18/ 0.12	0.21/ 0.12	0.21/ 0.12	0.40/ 0.12	ns
	OPMODE input to OPMODE register CLK for XA and XQ devices				0.18/ 0.16	N/A	0.21/ 0.22	0.40/ 0.12	
Setup and Hold Times of Data Pins to the Pipeline Register Clock									
$T_{\text{DSPDCK_A_MREG}}/$ $T_{\text{DSPCKD_A_MREG}}$	A input to M register CLK	N/A	Yes	N/A	3.06/ −0.40	3.51/ −0.40	3.51/ −0.40	3.97/ −0.40	ns
$T_{\text{DSPDCK_B_MREG}}/$ $T_{\text{DSPCKD_B_MREG}}$	B input to M register CLK	Yes	Yes	N/A	3.96/ −0.68	4.58/ −0.68	4.58/ −0.68	7.00/ −0.68	ns
$T_{\text{DSPDCK_D_MREG}}/$ $T_{\text{DSPCKD_D_MREG}}$	D input to M register CLK	Yes	Yes	N/A	4.23/ −0.56	4.80/ −0.56	4.80/ −0.56	6.84/ −0.56	ns
$T_{\text{DSPDCK_OPMODE_MREG}}/$ $T_{\text{DSPCKD_OPMODE_MREG}}$	OPMODE to M register CLK	Yes	Yes	N/A	4.18/ −0.48	4.80/ −0.48	4.80/ −0.48	6.88/ −0.48	ns
		No	Yes	N/A	2.37/ −0.48	2.70/ −0.48	2.70/ −0.48	4.28/ −0.48	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock									
$T_{\text{DSPDCK_A_PREG}}/$ $T_{\text{DSPCKD_A_PREG}}$	A input to P register CLK	N/A	Yes	Yes	4.32/ −0.76	5.06/ −0.76	5.06/ −0.76	7.52/ −0.76	ns
$T_{\text{DSPDCK_B_PREG}}/$ $T_{\text{DSPCKD_B_PREG}}$	B input to P register CLK	Yes	Yes	Yes	5.87/ −0.59	6.87/ −0.59	6.87/ −0.59	10.55/ −0.59	ns
		No	Yes	Yes	4.14/ −0.93	4.68/ −0.93	4.68/ −0.93	8.12/ −0.93	ns
$T_{\text{DSPDCK_C_PREG}}/$ $T_{\text{DSPCKD_C_PREG}}$	C input to P register CLK	N/A	N/A	Yes	2.20/ −0.23	2.25/ −0.23	2.25/ −0.23	3.27/ −0.23	ns
$T_{\text{DSPDCK_D_PREG}}/$ $T_{\text{DSPCKD_D_PREG}}$	D input to P register CLK	Yes	Yes	Yes	5.90/ −0.92	6.91/ −0.92	6.91/ −0.92	10.39/ −0.92	ns

Table 44: DSP48A1 Switching Characteristics (Cont'd)

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-3	-3N	-2	-1L	
T _{DSPDCK_OPMODE_PREG} / T _{DSPCKD_OPMODE_PREG}	OPMODE input to P register CLK	Yes	Yes	Yes	6.21/ −0.84	7.27/ −0.84	7.27/ −0.84	10.43/ −0.84	ns
		No	Yes	Yes	1.69/ −0.87	1.98/ −0.87	1.98/ −0.87	3.62/ −0.87	ns
		No	No	Yes	2.09/ −0.22	2.30/ −0.22	2.30/ −0.22	3.79/ −0.22	ns
Clock to Out from Output Register Clock to Output Pin									
T _{DSPCKO_P_PREG}	CLK (PREG) to P output	N/A	N/A	N/A	1.20	1.34	1.34	1.90	ns
Clock to Out from Pipeline Register Clock to Output Pins									
T _{DSPCKO_P_MREG}	CLK (MREG) to P output	N/A	N/A	Yes	3.38	3.95	3.95	5.83	ns
Clock to Out from Input Register Clock to Output Pins									
T _{DSPCKO_P_A1REG}	CLK (A1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.65	ns
T _{DSPCKO_P_B1REG}	CLK (B1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.63	ns
T _{DSPCKO_P_CREG}	CLK (CREG) to P output	N/A	N/A	Yes	3.12	3.64	3.64	5.24	ns
T _{DSPCKO_P_DREG}	CLK (DREG) to P output	Yes	Yes	Yes	6.77	7.92	7.92	12.53	ns
Combinatorial Delays from Input Pins to Output Pins									
T _{DSPDO_A_P}	A input to P output	N/A	No	Yes	2.85	3.33	3.33	4.73	ns
		N/A	Yes	No ⁽²⁾	3.35	3.93	3.93	6.74	ns
		N/A	Yes	Yes	4.56	5.22	5.22	8.94	ns
T _{DSPDO_B_P}	B input to P output	Yes	No	No ⁽²⁾	3.22	3.76	3.76	5.55	ns
		Yes	Yes	No ⁽²⁾	6.01	6.54	6.54	9.76	ns
		Yes	Yes	Yes	6.27	7.34	7.34	11.96	ns
T _{DSPDO_C_P}	C input to P output	N/A	N/A	Yes	2.69	3.15	3.15	4.68	ns
T _{DSPDO_D_P}	D input to P output	Yes	Yes	Yes	6.31	7.38	7.38	11.81	ns
T _{DSPDO_OPMODE_P}	OPMODE input to P output	Yes	Yes	Yes	6.43	7.52	7.52	11.84	ns
		No	Yes	Yes	4.84	5.66	5.66	9.25	ns
		No	No	Yes	3.11	3.49	3.49	5.03	ns
Maximum Frequency									
F _{MAX}	All registers used	Yes	Yes	Yes	390	333	333	213	MHz

Notes:

1. A Yes signifies that the component is in the path. A No signifies that the component is being bypassed. N/A signifies not applicable because no path exists.
2. Implemented in the post-adder by adding to zero.

Table 57: Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)⁽¹⁾ (Cont'd)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Spread Spectrum										
F _{CLKIN_FIXED_SPREAD_SPECTRUM}	Frequency of the CLKIN input for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD/ CENTER_HIGH_SPREAD)	30	200	30	200	30	200	30	200	MHz
T _{CENTER_LOW_SPREAD} ⁽⁶⁾	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD)	Typical = $\frac{100}{\text{CLKFX_DIVIDE}}$ Maximum = 250								ps
T _{CENTER_HIGH_SPREAD} ⁽⁶⁾	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM= CENTER_HIGH_SPREAD)	Typical = $\frac{240}{\text{CLKFX_DIVIDE}}$ Maximum = 400								ps
F _{MOD_FIXED_SPREAD_SPECTRUM} ⁽⁶⁾	Average modulation frequency when using fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD / CENTER_HIGH_SPREAD)	Typical = F _{IN} /1024								MHz

Notes:

- The values in this table are based on the operating conditions described in Table 2 and Table 55.
- For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
- Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
- The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
- Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of $\pm(1\% \text{ of CLKFX period} + 200 \text{ ps})$. Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is $\pm(100 \text{ ps} + 200 \text{ ps}) = \pm 300 \text{ ps}$.
- When using CENTER_LOW_SPREAD, CENTER_HIGH_SPREAD, the valid values for CLKFX_MULTIPLY are limited to 2 through 32, and the valid values for CLKFX_DIVIDE are limited to 1 through 4.

Table 58: Recommended Operating Conditions for the Phase-Shift Clock in Variable Phase Mode (DCM_SP) or Dynamic Frequency Synthesis (DCM_CLKGEN)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Operating Frequency Ranges										
PSCLK_FREQ	Frequency for the PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) input.	1	167	1	167	1	167	1	100	MHz
Input Pulse Requirements										
PSCLK_PULSE	PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) pulse width as a percentage of the clock period.	40	60	40	60	40	60	40	60	%

Table 59: Switching Characteristics for the Phase-Shift Clock in Variable Phase Mode⁽¹⁾

Symbol	Description	Amount of Phase Shift	Units
Phase Shifting Range			
MAX_STEPS ⁽²⁾	When CLKIN < 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period.	$\pm(\text{INTEGER}(10 \times (\text{TCLKIN} - 3 \text{ ns})))$	steps
	When CLKIN ≥ 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period.	$\pm(\text{INTEGER}(15 \times (\text{TCLKIN} - 3 \text{ ns})))$	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting.	$\pm(\text{MAX_STEPS} \times \text{DCM_DELAY_STEP_MIN})$	ps
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	$\pm(\text{MAX_STEPS} \times \text{DCM_DELAY_STEP_MAX})$	ps

Notes:

1. The values in this table are based on the operating conditions described in Table 53 and Table 58.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM has no initial fixed-phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the end of Table 54.

Table 60: Miscellaneous DCM Timing Parameters⁽¹⁾

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	3	–	CLKIN cycles

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFXDV, CLKFX180) are unaffected.

Table 61: Frequency Synthesis

Attribute	Min	Max
CLKFX_MULTIPLY (DCM_SP)	2	32
CLKFX_DIVIDE (DCM_SP)	1	32
CLKDV_DIVIDE (DCM_SP)	1.5	16
CLKFX_MULTIPLY (DCM_CLKGEN)	2	256
CLKFX_DIVIDE (DCM_CLKGEN)	1	256
CLKFXDV_DIVIDE (DCM_CLKGEN)	2	32

Table 62: DCM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T _{DMCK_PSEN} /T _{DMCKC_PSEN}	PSEN Setup/Hold	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	ns
T _{DMCK_PSINCDEC} /T _{DMCKC_PSINCDEC}	PSINCDEC Setup/Hold	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	ns
T _{DMCKO_PSDONE}	Clock to out of PSDONE	1.50	1.50	1.50	1.50	ns

Spartan-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 63 through Table 69. Values are expressed in nanoseconds unless otherwise noted.

Table 63: Global Clock Input to Output Delay Without DCM or PLL

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>without</i> DCM or PLL							
T _{ICKOF}	Global Clock and OUTFF <i>without</i> DCM or PLL	XC6SLX4	6.12	N/A	7.68	9.41	ns
		XC6SLX9	6.12	6.51	7.68	9.41	ns
		XC6SLX16	5.98	6.42	7.48	9.10	ns
		XC6SLX25	6.20	6.69	7.84	9.44	ns
		XC6SLX25T	6.20	6.69	7.84	N/A	ns
		XC6SLX45	6.37	6.88	8.10	9.61	ns
		XC6SLX45T	6.37	6.88	8.10	N/A	ns
		XC6SLX75	6.39	6.99	8.16	10.18	ns
		XC6SLX75T	6.39	6.99	8.16	N/A	ns
		XC6SLX100	6.59	7.18	8.41	10.31	ns
		XC6SLX100T	6.59	7.18	8.41	N/A	ns
		XC6SLX150	6.98	7.68	8.80	10.62	ns
		XC6SLX150T	6.98	7.68	8.80	N/A	ns
		XA6SLX4	6.44	N/A	7.68	N/A	ns
		XA6SLX9	6.44	N/A	7.68	N/A	ns
		XA6SLX16	6.30	N/A	7.48	N/A	ns
		XA6SLX25	6.52	N/A	7.84	N/A	ns
		XA6SLX25T	6.52	N/A	7.84	N/A	ns
		XA6SLX45	6.69	N/A	8.12	N/A	ns
		XA6SLX45T	6.69	N/A	8.12	N/A	ns
		XA6SLX75	6.89	N/A	8.16	N/A	ns
		XA6SLX75T	6.89	N/A	8.16	N/A	ns
		XA6SLX100	N/A	N/A	8.36	N/A	ns
		XQ6SLX75	N/A	N/A	8.16	10.18	ns
		XQ6SLX75T	6.89	N/A	8.16	N/A	ns
		XQ6SLX150	N/A	N/A	8.80	10.62	ns
		XQ6SLX150T	7.61	N/A	8.80	N/A	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 64: Global Clock Input to Output Delay With DCM in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in System-Synchronous Mode.							
T _{ICKOFDCM}	Global Clock and OUTFF <i>with</i> DCM	XC6SLX4	4.23	N/A	6.11	6.60	ns
		XC6SLX9	4.23	5.17	6.11	6.60	ns
		XC6SLX16	4.28	4.57	5.34	6.36	ns
		XC6SLX25	3.95	4.18	4.59	6.91	ns
		XC6SLX25T	3.95	4.18	4.59	N/A	ns
		XC6SLX45	4.37	4.70	5.50	6.85	ns
		XC6SLX45T	4.37	4.70	5.50	N/A	ns
		XC6SLX75	3.90	4.23	4.77	6.31	ns
		XC6SLX75T	3.90	4.23	4.77	N/A	ns
		XC6SLX100	3.86	4.16	4.66	7.25	ns
		XC6SLX100T	3.90	4.16	4.66	N/A	ns
		XC6SLX150	4.03	4.33	4.83	6.63	ns
		XC6SLX150T	4.03	4.33	4.83	N/A	ns
		XA6SLX4	4.55	N/A	6.11	N/A	ns
		XA6SLX9	4.55	N/A	6.11	N/A	ns
		XA6SLX16	4.62	N/A	5.33	N/A	ns
		XA6SLX25	4.27	N/A	4.59	N/A	ns
		XA6SLX25T	4.27	N/A	4.69	N/A	ns
		XA6SLX45	4.69	N/A	5.50	N/A	ns
		XA6SLX45T	4.69	N/A	5.50	N/A	ns
		XA6SLX75	4.22	N/A	4.77	N/A	ns
		XA6SLX75T	4.22	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.34	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	6.31	ns
		XQ6SLX75T	4.22	N/A	4.77	N/A	ns
		XQ6SLX150	N/A	N/A	4.96	6.63	ns
		XQ6SLX150T	4.62	N/A	4.96	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Spartan-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 70 through Table 77. Values are expressed in nanoseconds unless otherwise noted.

Table 70: Global Clock Setup and Hold Without DCM or PLL (No Delay)

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.(1)							
T _{PSND} / T _{PHND}	No Delay Global Clock and IFF(3) without DCM or PLL	XC6SLX4	0.10/1.56	N/A	0.10/1.83	0.07/2.54	ns
		XC6SLX9	0.10/1.56	0.10/1.57	0.10/1.84	0.07/2.54	ns
		XC6SLX16	0.12/1.42	0.12/1.48	0.12/1.64	0.13/2.19	ns
		XC6SLX25	0.18/1.64	0.18/1.75	0.18/1.99	0.11/2.57	ns
		XC6SLX25T	0.18/1.64	0.18/1.75	0.18/1.99	N/A	ns
		XC6SLX45	−0.08/1.80	−0.08/1.95	−0.08/2.27	−0.17/2.74	ns
		XC6SLX45T	−0.08/1.80	−0.08/1.95	−0.08/2.27	N/A	ns
		XC6SLX75	0.13/1.81	0.13/2.06	0.13/2.27	−0.12/3.30	ns
		XC6SLX75T	0.13/1.81	0.13/2.06	0.13/2.27	N/A	ns
		XC6SLX100	−0.14/2.03	−0.14/2.24	−0.14/2.56	−0.17/3.44	ns
		XC6SLX100T	−0.14/2.03	−0.14/2.24	−0.14/2.56	N/A	ns
		XC6SLX150	−0.24/2.42	−0.24/2.74	−0.24/2.95	−0.60/3.75	ns
		XC6SLX150T	−0.24/2.42	−0.24/2.74	−0.24/2.95	N/A	ns
		XA6SLX4	0.10/1.57	N/A	0.10/1.84	N/A	ns
		XA6SLX9	0.10/1.57	N/A	0.10/1.84	N/A	ns
		XA6SLX16	0.12/1.43	N/A	0.12/1.64	N/A	ns
		XA6SLX25	0.18/1.65	N/A	0.18/1.99	N/A	ns
		XA6SLX25T	0.18/1.65	N/A	0.18/1.99	N/A	ns
		XA6SLX45	−0.08/1.82	N/A	−0.08/2.27	N/A	ns
		XA6SLX45T	−0.08/1.82	N/A	−0.08/2.27	N/A	ns
		XA6SLX75	0.13/2.02	N/A	0.13/2.32	N/A	ns
		XA6SLX75T	0.13/2.02	N/A	0.13/2.32	N/A	ns
		XA6SLX100	N/A	N/A	0.10/2.51	N/A	ns
		XQ6SLX75	N/A	N/A	0.13/2.32	−0.12/3.30	ns
		XQ6SLX75T	0.13/2.02	N/A	0.13/2.32	N/A	ns
		XQ6SLX150	N/A	N/A	−0.24/2.95	−0.60/3.75	ns
		XQ6SLX150T	−0.24/2.74	N/A	−0.24/2.95	N/A	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch.

Table 76: Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾							
T _{PSDCMPLL} / T _{PHDCMPLL}	No Delay Global Clock and IFF ⁽²⁾ with DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.	XC6SLX4	1.16/0.49	N/A	1.39/0.49	2.36/0.59	ns
		XC6SLX9	1.16/0.44	1.37/0.44	1.39/0.44	2.36/0.59	ns
		XC6SLX16	1.44/−0.08	1.49/−0.04	1.62/−0.04	2.06/0.55	ns
		XC6SLX25	1.52/0.42	1.65/0.42	1.83/0.42	2.52/0.43	ns
		XC6SLX25T	1.52/0.42	1.65/0.42	1.83/0.42	N/A	ns
		XC6SLX45	1.54/0.39	1.59/0.39	1.75/0.39	2.48/0.76	ns
		XC6SLX45T	1.54/0.39	1.59/0.39	1.75/0.39	N/A	ns
		XC6SLX75	1.72/0.41	1.80/0.41	1.99/0.41	2.60/0.75	ns
		XC6SLX75T	1.72/0.41	1.80/0.41	1.99/0.41	N/A	ns
		XC6SLX100	1.34/0.51	1.46/0.51	1.64/0.51	2.12/0.90	ns
		XC6SLX100T	1.34/0.51	1.46/0.51	1.64/0.51	N/A	ns
		XC6SLX150	1.30/0.60	1.40/0.60	1.55/0.60	2.57/0.97	ns
		XC6SLX150T	1.30/0.60	1.40/0.60	1.55/0.60	N/A	ns
		XA6SLX4	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX9	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX16	2.67/0.35	N/A	2.67/0.17	N/A	ns
		XA6SLX25	1.74/0.27	N/A	1.95/0.27	N/A	ns
		XA6SLX25T	1.74/0.27	N/A	2.03/0.27	N/A	ns
		XA6SLX45	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX45T	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX75	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX100	N/A	N/A	2.64/0.82	N/A	ns
		XQ6SLX75	N/A	N/A	2.11/0.24	2.60/0.75	ns
		XQ6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XQ6SLX150	N/A	N/A	1.67/0.70	2.57/0.97	ns
		XQ6SLX150T	1.50/0.70	N/A	1.67/0.70	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Spartan-6 FPGA source-synchronous transmitter and receiver data-valid windows.

Table 78: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{DCD_CLK}	Global Clock Tree Duty Cycle Distortion ⁽²⁾	LX4	0.20	N/A	0.20	0.35	ns
		LX9	0.20	0.20	0.20	0.35	ns
		LX16	0.20	0.20	0.20	0.35	ns
		LX25	0.20	0.20	0.20	0.35	ns
		LX25T	0.20	0.20	0.20	N/A	ns
		LX45	0.20	0.20	0.20	0.35	ns
		LX45T	0.20	0.20	0.20	N/A	ns
		LX75	0.20	0.20	0.20	0.35	ns
		LX75T	0.20	0.20	0.20	N/A	ns
		LX100	0.20	0.20	0.20	0.35	ns
		LX100T	0.20	0.20	0.20	N/A	ns
		LX150	0.35	0.35	0.35	0.35	ns
		LX150T	0.35	0.35	0.35	N/A	ns
T _{CKSKEW}	Global Clock Tree Skew ⁽³⁾	LX4	0.25	N/A	0.25	0.29	ns
		LX9	0.25	0.25	0.25	0.29	ns
		LX16	0.15	0.15	0.15	0.22	ns
		LX25	0.26	0.26	0.26	0.41	ns
		LX25T	0.26	0.26	0.26	N/A	ns
		LX45	0.20	0.20	0.20	0.28	ns
		LX45T	0.20	0.20	0.20	N/A	ns
		LX75	0.56	0.56	0.56	0.50	ns
		LX75T	0.56	0.56	0.56	N/A	ns
		XC6SLX100 ⁽⁴⁾	0.22	0.22	0.22	0.21	ns
		XA6SLX100 ⁽⁴⁾	N/A	N/A	0.43	N/A	ns
		LX100T	0.22	0.22	0.22	N/A	ns
		LX150	0.48	0.48	0.48	0.35	ns
		LX150T	0.48	0.48	0.48	N/A	ns
T _{DCD_BUFIO2}	I/O clock tree duty cycle distortion	LX devices	0.25	0.25	0.25	0.50	ns
		LXT devices	0.25	0.25	0.25	N/A	ns

Date	Version	Description of Revisions
09/14/11	2.4	Production release of the XA6SLX4 and XA6SLX9 devices in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added production released version of the XA6SLX100 to Table 26 and Table 27 using ISE v13.3 software with -2 speed specification v1.20. Updated R_{OUT_TERM} description in Table 4. Fixed the LVPECL V_H error in Table 31. Updated introduction in Simultaneously Switching Outputs. Added the XA6SLX100 to Table 63 through Table 78, and Table 81. Added Note 4 to Table 78 because the T_{CKSKEW} for the XC6SLX100 is not the same as the T_{CKSKEW} for the XA6SLX100. Revised the revision history for version 1.6 dated 06/24/10. Removed the parenthetical statement about the -3N speed grade: (specifications are identical to the -3 speed grade).
10/17/11	3.0	Changed the data sheet from Preliminary Product Specification to Product Specification. Updated the Switching Characteristics, page 19 speed specification version ISE v13.3 software to -2 and -3 speed specification v1.20 and -1L speed specification of v1.08. Also updated Note 1 in Table 27. In Table 43, <i>Block RAM Switching Characteristics</i>, the F_{MAX} value for the -2 speed grade has been changed from 260 MHz to 280 MHz. In Table 54, <i>Switching Characteristics for the DLL</i>, a Note 6 was added and linked to CLKIN_CLKFB_PHASE.

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