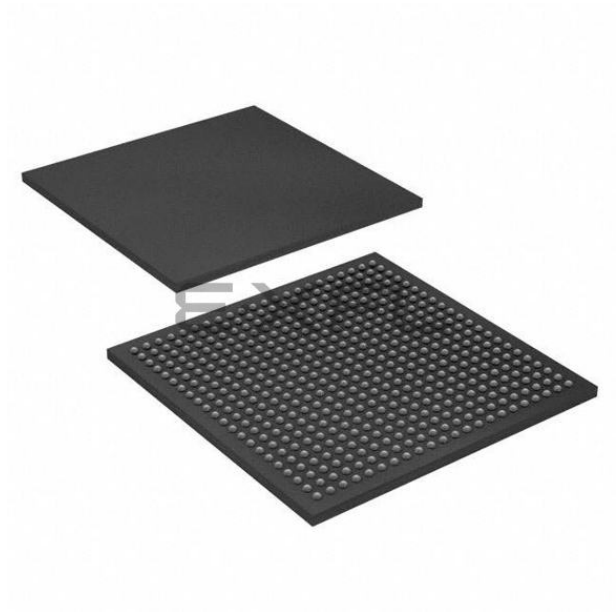
AMD Xilinx - XC6SLX45T-3CSG484C Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3411
Number of Logic Elements/Cells	43661
Total RAM Bits	2138112
Number of I/O	296
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA, CSPBGA
Supplier Device Package	484-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx45t-3csg484c

Table 5: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	LX4	2.5	2.5	2.5	2.5	mA
		LX9	2.5	2.5	2.5	2.5	mA
		LX16	3.0	3.0	3.0	3.0	mA
		LX25	4.0	4.0	4.0	4.0	mA
		LX25T	4.0	4.0	4.0	N/A	mA
		LX45	5.0	5.0	5.0	5.0	mA
		LX45T	5.0	5.0	5.0	N/A	mA
		LX75	7.0	7.0	7.0	7.0	mA
		LX75T	7.0	7.0	7.0	N/A	mA
		LX100	9.0	9.0	9.0	9.0	mA
		LX100T	9.0	9.0	9.0	N/A	mA
		LX150	12.0	12.0	12.0	12.0	mA
		LX150T	12.0	12.0	12.0	N/A	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C junction temperatures (Tj). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 25°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. Nominal V_{CCINT} is 1.20V; use the XPE tool to calculate 1.23V values for the nominal V_{CCINT} of the extended performance range.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 6: **Power Supply Ramp Time**

Symbol	Description	Speed Grade	Ramp Time	Units
V_{CCINTR}	Internal supply voltage ramp time	-3, -3N, -2	0.20 to 50.0	ms
		-1L	0.20 to 40.0	ms
V_{CCO2}(1)	Output drivers bank 2 supply voltage ramp time	All	0.20 to 50.0	ms
V_{CCAUXR}	Auxiliary supply voltage ramp time	All	0.20 to 50.0	ms

Notes:

1. The minimum V_{CCO2} for power-on reset and configuration is 1.65V.
2. Spartan-6 FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply. Use the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools to estimate current drain on these supplies. Spartan-6 devices do not have a required power-on sequence.

GTP Transceiver DC Input and Output Levels

Table 16 summarizes the DC output specifications of the GTP transceivers in Spartan-6 FPGAs. Figure 1 shows the single-ended output voltage swing. Figure 2 shows the peak-to-peak differential output voltage.

Consult UG386: *Spartan-6 FPGA GTP Transceivers User Guide* for further details.

Table 16: **GTP Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled	140	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTTRX = 1.2V	–400	–	MGTAVTTRX	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTTRX = 1.2V	–	3/4 MGTAVTTRX	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	–	–	1000	mV
V_{SEOUT}	Single-ended output voltage swing(1)		–	–	500	mV
$V_{CMOUTDC}$	Common mode output voltage	Equation based	MGTAVTTTX – V_{SEOUT}/2			mV
R_{IN}	Differential input resistance		80	100	130	Ω
R_{OUT}	Differential output resistance		80	100	130	Ω
T_{OSKEW}	Transmitter output skew		–	–	15	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		75	100	200	nF

Notes:
1. The output swing and preemphasis levels are programmable using the attributes discussed in UG386: *Spartan-6 FPGA GTP Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

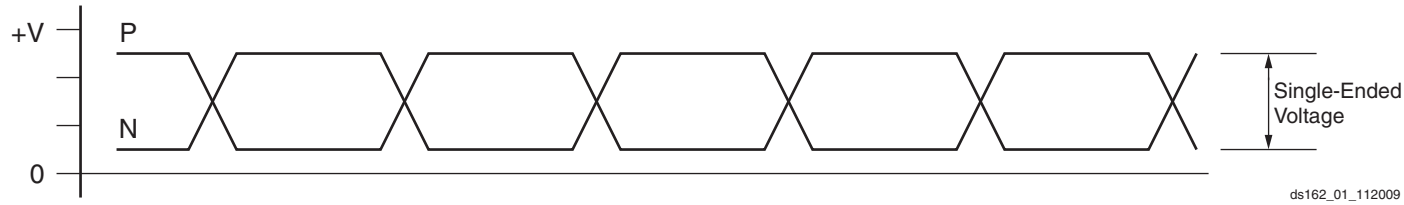

Figure 1: **Single-Ended Peak-to-Peak Voltage**

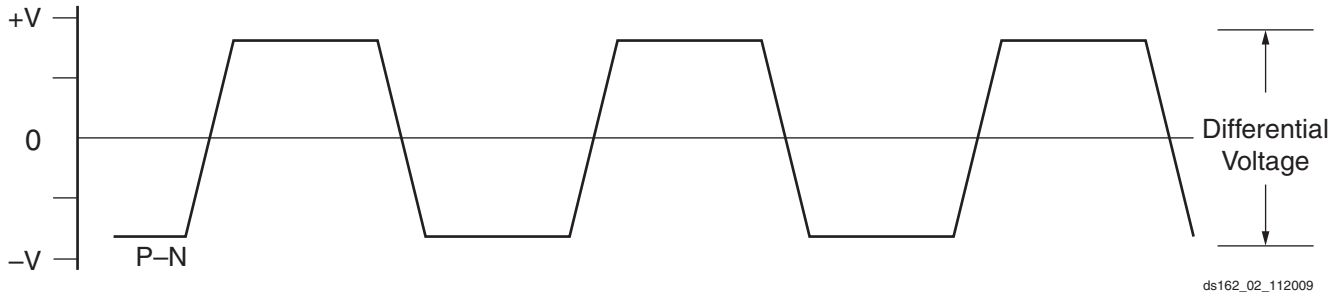

Figure 2: **Differential Peak-to-Peak Voltage**

Table 17 summarizes the DC specifications of the clock input of the GTP transceiver. Consult UG386: *Spartan-6 FPGA GTP Transceivers User Guide* for further details.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 27 lists the production released Spartan-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE® software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 27: **Spartan-6 Device Production Software and Speed Specification Release(1)**

Device	Speed Grade Designations(2)			
	-3(3)	-3N	-2(4)	-1L
XC6SLX4	ISE 12.4 v1.15	N/A	ISE 12.3 v1.12(5)	ISE 13.2 v1.07
XC6SLX9	ISE 12.4 v1.15	ISE 13.1 Update v1.18(7)	ISE 12.3 v1.12(5)	ISE 13.2 v1.07
XC6SLX16	ISE 12.1 v1.08	ISE 13.1 Update v1.18(7)	ISE 11.5 v1.06	ISE 13.2 v1.07
XC6SLX25	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	ISE 13.2 v1.07
XC6SLX25T	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	N/A
XC6SLX45	ISE 12.1 v1.08	ISE 13.1 Update v1.18(7)	ISE 11.5 v1.07	ISE 13.1 v1.06
XC6SLX45T	ISE 12.1 v1.08	ISE 13.1 Update v1.18(7)	ISE 12.1 v1.08	N/A
XC6SLX75	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	ISE 13.2 v1.07
XC6SLX75T	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	N/A
XC6SLX100	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	ISE 13.1 v1.06
XC6SLX100T	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	N/A
XC6SLX150	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	ISE 13.1 v1.06
XC6SLX150T	ISE 12.2 v1.11(6)	ISE 13.1 Update v1.18(7)	ISE 12.2 v1.11(6)	N/A
XA6SLX4	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX9	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX16	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX25	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX25T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX45	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX45T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX75	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX75T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XA6SLX100	N/A	N/A	ISE 13.3 v1.20	N/A

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	
LVCMOS18, Slow, 24 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18, Fast, 2 mA	1.18	1.30	1.43	2.04	3.59	3.73	3.93	4.53	3.59	3.73	3.93	4.53	ns
LVCMOS18, Fast, 4 mA	1.18	1.30	1.43	2.04	2.39	2.53	2.73	3.35	2.39	2.53	2.73	3.35	ns
LVCMOS18, Fast, 6 mA	1.18	1.30	1.43	2.04	1.88	2.02	2.22	2.84	1.88	2.02	2.22	2.84	ns
LVCMOS18, Fast, 8 mA	1.18	1.30	1.43	2.04	1.81	1.95	2.15	2.77	1.81	1.95	2.15	2.77	ns
LVCMOS18, Fast, 12 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVCMOS18, Fast, 16 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVCMOS18, Fast, 24 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVCMOS18_JEDEC, QUIETIO, 2 mA	0.94	1.06	1.19	1.41	5.91	6.05	6.25	6.79	5.91	6.05	6.25	6.79	ns
LVCMOS18_JEDEC, QUIETIO, 4 mA	0.94	1.06	1.19	1.41	4.75	4.89	5.09	5.64	4.75	4.89	5.09	5.64	ns
LVCMOS18_JEDEC, QUIETIO, 6 mA	0.94	1.06	1.19	1.41	4.04	4.18	4.38	4.96	4.04	4.18	4.38	4.96	ns
LVCMOS18_JEDEC, QUIETIO, 8 mA	0.94	1.06	1.19	1.41	3.71	3.85	4.05	4.62	3.71	3.85	4.05	4.62	ns
LVCMOS18_JEDEC, QUIETIO, 12 mA	0.94	1.06	1.19	1.41	3.35	3.49	3.69	4.28	3.35	3.49	3.69	4.28	ns
LVCMOS18_JEDEC, QUIETIO, 16 mA	0.94	1.06	1.19	1.41	3.20	3.34	3.54	4.13	3.20	3.34	3.54	4.13	ns
LVCMOS18_JEDEC, QUIETIO, 24 mA	0.94	1.06	1.19	1.41	2.96	3.10	3.30	3.98	2.96	3.10	3.30	3.98	ns
LVCMOS18_JEDEC, Slow, 2 mA	0.94	1.06	1.19	1.41	4.59	4.73	4.93	5.54	4.59	4.73	4.93	5.54	ns
LVCMOS18_JEDEC, Slow, 4 mA	0.94	1.06	1.19	1.41	3.69	3.83	4.03	4.60	3.69	3.83	4.03	4.60	ns
LVCMOS18_JEDEC, Slow, 6 mA	0.94	1.06	1.19	1.41	3.00	3.14	3.34	3.94	3.00	3.14	3.34	3.94	ns
LVCMOS18_JEDEC, Slow, 8 mA	0.94	1.06	1.19	1.41	2.19	2.33	2.53	3.18	2.19	2.33	2.53	3.18	ns
LVCMOS18_JEDEC, Slow, 12 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18_JEDEC, Slow, 16 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18_JEDEC, Slow, 24 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18_JEDEC, Fast, 2 mA	0.94	1.06	1.19	1.41	3.57	3.71	3.91	4.52	3.57	3.71	3.91	4.52	ns
LVCMOS18_JEDEC, Fast, 4 mA	0.94	1.06	1.19	1.41	2.39	2.53	2.73	3.35	2.39	2.53	2.73	3.35	ns
LVCMOS18_JEDEC, Fast, 6 mA	0.94	1.06	1.19	1.41	1.88	2.02	2.22	2.84	1.88	2.02	2.22	2.84	ns
LVCMOS18_JEDEC, Fast, 8 mA	0.94	1.06	1.19	1.41	1.80	1.94	2.14	2.76	1.80	1.94	2.14	2.76	ns
LVCMOS18_JEDEC, Fast, 12 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVCMOS18_JEDEC, Fast, 16 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVCMOS18_JEDEC, Fast, 24 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVCMOS15, QUIETIO, 2 mA	0.98	1.10	1.23	1.79	5.47	5.61	5.81	6.38	5.47	5.61	5.81	6.38	ns
LVCMOS15, QUIETIO, 4 mA	0.98	1.10	1.23	1.79	4.61	4.75	4.95	5.51	4.61	4.75	4.95	5.51	ns
LVCMOS15, QUIETIO, 6 mA	0.98	1.10	1.23	1.79	4.07	4.21	4.41	4.97	4.07	4.21	4.41	4.97	ns
LVCMOS15, QUIETIO, 8 mA	0.98	1.10	1.23	1.79	3.91	4.05	4.25	4.81	3.91	4.05	4.25	4.81	ns
LVCMOS15, QUIETIO, 12 mA	0.98	1.10	1.23	1.79	3.53	3.67	3.87	4.51	3.53	3.67	3.87	4.51	ns
LVCMOS15, QUIETIO, 16 mA	0.98	1.10	1.23	1.79	3.32	3.46	3.66	4.31	3.32	3.46	3.66	4.31	ns
LVCMOS15, Slow, 2 mA	0.98	1.10	1.23	1.79	4.18	4.32	4.52	5.11	4.18	4.32	4.52	5.11	ns
LVCMOS15, Slow, 4 mA	0.98	1.10	1.23	1.79	3.42	3.56	3.76	4.34	3.42	3.56	3.76	4.34	ns
LVCMOS15, Slow, 6 mA	0.98	1.10	1.23	1.79	2.29	2.43	2.63	3.24	2.29	2.43	2.63	3.24	ns

Table 29: **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices[1] *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVCMOS18, QUIETIO, 16 mA	1.25	1.43	3.34	3.54	3.34	3.54	ns
LVCMOS18, QUIETIO, 24 mA	1.25	1.43	3.18	3.38	3.18	3.38	ns
LVCMOS18, Slow, 2 mA	1.25	1.43	4.79	4.99	4.79	4.99	ns
LVCMOS18, Slow, 4 mA	1.25	1.43	3.84	4.04	3.84	4.04	ns
LVCMOS18, Slow, 6 mA	1.25	1.43	3.17	3.37	3.17	3.37	ns
LVCMOS18, Slow, 8 mA	1.25	1.43	2.37	2.57	2.37	2.57	ns
LVCMOS18, Slow, 12 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns
LVCMOS18, Slow, 16 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns
LVCMOS18, Slow, 24 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns
LVCMOS18, Fast, 2 mA	1.25	1.43	3.78	3.98	3.78	3.98	ns
LVCMOS18, Fast, 4 mA	1.25	1.43	2.54	2.74	2.54	2.74	ns
LVCMOS18, Fast, 6 mA	1.25	1.43	2.02	2.22	2.02	2.22	ns
LVCMOS18, Fast, 8 mA	1.25	1.43	1.95	2.15	1.95	2.15	ns
LVCMOS18, Fast, 12 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns
LVCMOS18, Fast, 16 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns
LVCMOS18, Fast, 24 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns
LVCMOS18_JEDEC, QUIETIO, 2 mA	1.01	1.19	6.09	6.29	6.09	6.29	ns
LVCMOS18_JEDEC, QUIETIO, 4 mA	1.01	1.19	4.89	5.09	4.89	5.09	ns
LVCMOS18_JEDEC, QUIETIO, 6 mA	1.01	1.19	4.20	4.40	4.20	4.40	ns
LVCMOS18_JEDEC, QUIETIO, 8 mA	1.01	1.19	3.87	4.07	3.87	4.07	ns
LVCMOS18_JEDEC, QUIETIO, 12 mA	1.01	1.19	3.49	3.69	3.49	3.69	ns
LVCMOS18_JEDEC, QUIETIO, 16 mA	1.01	1.19	3.34	3.54	3.34	3.54	ns
LVCMOS18_JEDEC, QUIETIO, 24 mA	1.01	1.19	3.17	3.37	3.17	3.37	ns
LVCMOS18_JEDEC, Slow, 2 mA	1.01	1.19	4.79	4.99	4.79	4.99	ns
LVCMOS18_JEDEC, Slow, 4 mA	1.01	1.19	3.84	4.04	3.84	4.04	ns
LVCMOS18_JEDEC, Slow, 6 mA	1.01	1.19	3.18	3.38	3.18	3.38	ns
LVCMOS18_JEDEC, Slow, 8 mA	1.01	1.19	2.37	2.57	2.37	2.57	ns
LVCMOS18_JEDEC, Slow, 12 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns
LVCMOS18_JEDEC, Slow, 16 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns
LVCMOS18_JEDEC, Slow, 24 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns
LVCMOS18_JEDEC, Fast, 2 mA	1.01	1.19	3.75	3.95	3.75	3.95	ns
LVCMOS18_JEDEC, Fast, 4 mA	1.01	1.19	2.54	2.74	2.54	2.74	ns
LVCMOS18_JEDEC, Fast, 6 mA	1.01	1.19	2.02	2.22	2.02	2.22	ns
LVCMOS18_JEDEC, Fast, 8 mA	1.01	1.19	1.94	2.14	1.94	2.14	ns
LVCMOS18_JEDEC, Fast, 12 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns
LVCMOS18_JEDEC, Fast, 16 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns
LVCMOS18_JEDEC, Fast, 24 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns

I/O Standard Measurement Methodology

Input Delay Measurements

Table 31 shows the test setup parameters used for measuring input delay.

Table 31: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L[1]	V_H[1]	V_{MEAS}[3][4]	V_{REF}[2][4]
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	0	3.0	1.4	–
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	0	3.3	1.65	–
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
LVCMOS, 1.2V	LVCMOS12	0	1.2	0.6	–
PCI (Peripheral Component Interface), 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3	Per PCI Specification			–
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III	HSTL_III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.1
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
SSTL, Class II, 1.5V	SSTL15_II	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	1.25 – 0.125	1.25 + 0.125	0[5]	–
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V & 3.3V	LVPECL_25, LVPECL_33	1.2 – 0.3	1.2 + 0.3	0[5]	–
BLVDS (Bus LVDS), 2.5V	BLVDS_25	1.3 – 0.125	1.3 + 0.125	0[5]	–
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	1.2 – 0.125	1.2 + 0.125	0[5]	–
RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RSDS_25, RSDS_33	1.2 – 0.1	1.2 + 0.1	0[5]	–
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	3.0 – 0.1	3.0 + 0.1	0[5]	–
PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V	PPDS_25, PPDS_33	1.25 – 0.1	1.25 + 0.1	0[5]	–

Notes:
1. Input waveform switches between V_L and V_H.
2. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 4.
5. The value given is the differential input voltage.

Table 32: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
SSTL, Class II, 1.5V	SSTL15_II	25	0	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	100	0	0[3]	–
BLVDS (Bus LVDS), 2.5V	BLVDS_25	Note 4	0	0[3]	–
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	100	0	0[3]	–
RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RSDS_25, RSDS_33	100	0	0[3]	–
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	Note 5	0	0[3]	–
PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V	PPDS_25, PPDS_33	100	0	0[3]	–

Notes:
1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. The value given is the differential output voltage.
4. See the *BLVDS Output Termination* section in UG381, *Spartan-6 FPGA SelectIO Resources User Guide*.
5. See the *TMDS_33 Termination* section in UG381, *Spartan-6 FPGA SelectIO Resources User Guide*.

Simultaneously Switching Outputs

Due to package electrical parasitics, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. Table 33 and Table 34 provide guidelines for the recommended maximum allowable number of SSOs. These guidelines describe the maximum number of user I/O pins of an output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise for that particular signal standard. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of GND and power bounce.

For each device/package combination, Table 33 provides the number of equivalent V_{CCO}/GND pairs per bank. For each output signal standard and drive strength, Table 34 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines are categorized by package style, slew rate, and output drive current. The number of SSOs are also specified by I/O bank. Multiply the appropriate numbers from each table to calculate the maximum number of SSOs allowed within an I/O bank. The guidelines assume that all pins within a bank use the same I/O standard. Exceeding these SSO guidelines can result in increased power or GND bounce, degraded signal integrity, or increased system jitter. For a given I/O standard, if the SSO limit per pair in Table 34 is greater than the maximum I/O per pair in Table 33, then there is no SSO limit for the exclusive use of that I/O standard.

The recommended maximum SSO values assume that the FPGA is soldered on a printed circuit board and that the board uses sound design practices. Due to the additional inductance introduced by the socket, the SSO values do not apply for FPGAs mounted in sockets. The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics. For more detail, see UG381: *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 34: **SSO Limit per V_{CCO}/GND Pair *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
2.5V	LVCMOS25	2	Fast	38	43	38	43
			Slow	46	52	46	48
			QuietIO	57	64	57	59
		4	Fast	21	24	21	23
			Slow	26	31	26	27
			QuietIO	33	32	33	30
		6	Fast	15	17	15	16
			Slow	19	22	19	19
			QuietIO	25	23	25	19
		8	Fast	12	15	12	14
			Slow	15	18	15	16
			QuietIO	21	19	21	16
		12	Fast	1	3	1	1
			Slow	2	7	2	4
			QuietIO	3	8	3	8
		16	Fast	1	3	1	1
			Slow	3	7	3	3
			QuietIO	4	9	4	8
		24	Fast	N/A	3	N/A	1
			Slow	N/A	5	N/A	2
			QuietIO	N/A	8	N/A	6
	SSTL_2_I (3)			10	11	10	11
	SSTL_2_II (3)			N/A	7	N/A	7
	DIFF_SSTL_2_I (3)			30	33	30	33
	DIFF_SSTL_2_II (3)			N/A	21	N/A	24

Table 34: **SSO Limit per V_{CCO}/GND Pair *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
3.3V	LVCMOS33	2	Fast	42	46	42	44
			Slow	50	55	50	49
			QuietIO	60	68	60	60
		4	Fast	21	27	21	25
			Slow	32	37	32	32
			QuietIO	39	42	39	37
		6	Fast	14	19	14	17
			Slow	19	25	19	22
			QuietIO	29	30	29	25
		8	Fast	11	15	11	14
			Slow	15	20	15	18
			QuietIO	25	24	25	20
		12	Fast	1	3	1	1
			Slow	2	5	2	2
			QuietIO	4	9	4	7
		16	Fast	1	2	1	1
			Slow	1	5	1	1
			QuietIO	3	10	3	8
		24	Fast	1	2	1	1
			Slow	2	5	2	1
			QuietIO	7	9	7	7

Input/Output Logic Switching Characteristics

Table 35: **ILOGIC2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T_{ICE0CK}/T_{ICKCE0}	CE0 pin Setup/Hold with respect to CLK	0.56/ –0.30	0.56/ –0.25	0.79/ –0.22	1.21/ –0.52	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.74/ –0.23	0.74/ –0.22	0.98/ –0.20	1.31/ –0.45	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	1.19/ –0.83	1.36/ –0.83	1.73/ –0.83	2.18/ –1.77	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	0.31/ 0.00	0.47/ 0.00	0.54/ 0.00	0.63/ –0.39	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.95	1.28	1.53	2.25	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY2)	0.23	0.39	0.44	0.74	ns
Sequential Delays						
T_{IDLO}	D pin to Q pin using flip-flop as a latch without Delay	1.56	1.86	2.39	3.49	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY2)	0.68	0.97	1.20	1.94	ns
T_{ICKQ}	CLK to Q outputs for XC devices	1.03	1.24	1.43	2.11	ns
	CLK to Q outputs for XA and XQ devices	1.38	N/A	1.78	2.11	ns
$T_{RQ\_ILOGIC2}$	SR pin to Q outputs	1.81	1.81	2.50	3.05	ns

Table 36: **OLOGIC2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.81/ –0.05	0.86/ –0.05	1.18/ 0.00	1.73/ –0.27	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.75/ –0.10	0.75/ –0.10	1.01/ –0.05	1.66/ –0.23	ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.70/ –0.28	0.79/ –0.28	1.03/ –0.23	1.39/ –0.47	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.24/ –0.08	0.56/ –0.06	0.83/ –0.01	0.99/ –0.19	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.58/ –0.06	0.72/ –0.06	1.18/ –0.01	1.51/ –0.13	ns
Sequential Delays						
T_{OCKQ}	CLK to OQ/TQ out for XC devices	0.48	0.51	0.74	0.74	ns
	CLK to OQ/TQ out for XA and XQ devices	0.85	N/A	1.16	0.74	ns
$T_{RQ\_OLOGIC2}$	SR pin to OQ/TQ out	1.81	1.81	2.50	3.05	ns

Input Serializer/Deserializer Switching Characteristics

Table 37: **ISERDES2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold for Control Lines						
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.16/ –0.09	0.20/ –0.09	0.31/ –0.09	0.34/ –0.14	ns
T_{ISCCK_CE} / T_{ISCKC_CE}	CE pin Setup/Hold with respect to CLK	0.71/ –0.47	0.71/ –0.42	0.97/ –0.42	1.39/ –0.71	ns
Setup/Hold for Data Lines						
T_{ISDCK_D} /T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.24/ –0.15	0.25/ –0.05	0.29/ –0.05	0.09/ –0.05	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	–0.25/ 0.30	–0.25/ 0.42	–0.25/ 0.56	–0.54/ 0.67	ns
$T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	–0.03/ 0.04	–0.03/ 0.16	–0.03/ 0.18	–0.05/ 0.12	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY2)	–0.40/ 0.48	–0.40/ 0.53	–0.40/ 0.71	–0.71/ 0.86	ns
Sequential Delays						
T_{ISCKO_Q}	CLKDIV to out at Q pin	1.30	1.44	2.02	2.22	ns
F_{CLKDIV}	CLKDIV maximum frequency	270	262.5	250	125	MHz

Output Serializer/Deserializer Switching Characteristics

Table 38: **OSERDES2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	–0.03/ 1.02	–0.03/ 1.17	–0.03/ 1.27	–0.02/ 0.23	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	–0.05/ 1.03	–0.05/ 1.13	–0.05/ 1.23	–0.05/ 0.24	ns
T_{OSCCK_OCE}/T_{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.12/ –0.03	0.15/ –0.03	0.24/ –0.03	0.28/ –0.17	ns
T_{OSCCK_TCE}/T_{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.14/ –0.08	0.17/ –0.08	0.27/ –0.08	0.31/ –0.16	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.94	1.11	1.51	1.89	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.94	1.11	1.51	1.91	ns
F_{CLKDIV}	CLKDIV maximum frequency	270	262.5	250	125	MHz

Notes:
1. T_{OSDCK_T2}/T_{OSCKD_T2} (T input setup/hold with respect to CLKDIV) are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 41: **CLB Distributed RAM Switching Characteristics (SLICEM Only)**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Sequential Delays						
T_{SHCKO}	Clock to A – D outputs	1.26	1.55	1.55	2.35	ns, Max
	Clock to A – D outputs (direct output path)	0.96	1.20	1.20	1.87	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS}/T_{DH}	AX – DX or AI – DI inputs to CLK	0.59/ 0.17	0.73/ 0.22	0.73/ 0.22	1.17/ 0.33	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock for XC devices	0.28/ 0.35	0.32/ 0.42	0.32/ 0.42	0.26/ 0.71	ns, Min
	Address An inputs to clock for XA and XQ devices	0.28/ 0.51	N/A	0.32/ 0.51	0.26/ 0.71	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.31/ –0.08	0.37/ –0.08	0.37/ –0.08	0.59/ –0.27	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.31/ –0.08	0.37/ –0.08	0.37/ –0.08	0.59/ –0.27	ns, Min

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 42: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	1.35	1.78	1.78	2.74	ns, Max
	Clock to A – D outputs (direct output path)	1.24	1.65	1.65	2.48	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS}/T_{WH}	WE input to CLK	0.20/ –0.07	0.24/ –0.07	0.24/ –0.07	0.29/ –0.27	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK for XC devices	0.30/ 0.30	0.30/ 0.38	0.30/ 0.38	0.82/ –0.41	ns, Min
	CE input to CLK for XA and XQ devices	0.32/ 0.30	N/A	0.40/ 0.38	0.82/ –0.41	ns, Min
T_{DS}/T_{DH}	AX – DX or AI – DI inputs to CLK	0.07/ 0.11	0.09/ 0.14	0.09/ 0.14	0.11/ 0.23	ns, Min

Block RAM Switching Characteristics

Table 43: **Block RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Block RAM Clock to Out Delays						
T_{RCKO_DO}	Clock CLK to DOUT output (without output register)(1)	1.85	2.10	2.10	3.50	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register)(2)	1.60	1.75	1.75	2.30	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs for XC devices(3)	0.35/ 0.10	0.40/ 0.12	0.40/ 0.12	0.50/ 0.15	ns, Min
	ADDR inputs for XA and XQ devices(3)	0.35/ 0.17	N/A	0.40/ 0.17	0.50/ 0.15	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs(4)	0.30/ 0.10	0.30/ 0.10	0.30/ 0.10	0.40/ 0.15	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.22/ 0.05	0.25/ 0.06	0.25/ 0.06	0.44/ 0.10	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.20/ 0.10	0.20/ 0.10	0.20/ 0.10	0.28/ 0.15	ns, Min
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input	0.25/ 0.10	0.33/ 0.10	0.33/ 0.10	0.28/ 0.15	ns, Min
Maximum Frequency						
F_{MAX}	Block RAM in all modes	320	280	280	150	MHz

Notes:
1. T_{RCKO_DO} includes T_{RCKO_DOA} and T_{RCKO_DOPA} as well as the B port equivalent timing parameters.
2. $T_{RCKO\_DO\_REG}$ includes $T_{RCKO\_DOA\_REG}$ and $T_{RCKO\_DOPA\_REG}$ as well as the B port equivalent timing parameters.
3. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
4. T_{RDCK_DI} includes both A and B inputs as well as the parity inputs of A and B.

Configuration Switching Characteristics

Table 47: **Configuration Switching Characteristics(1)**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Power-up Timing Characteristics						
T_{PL}(2)	PROGRAM_B Latency	4	4	4	5	ms, Max
T_{POR}(2)	Power-on reset (50 ms ramp time)(3)	5/30	5/34	5/40	5/40	ms, Min/Max
	Power-on reset (10 ms ramp time)	5/25	5/29	5/35	5/40	ms, Min/Max
$T_{PROGRAM}$	PROGRAM_B Pulse Width	500	500	500	500	ns, Min
Slave Serial Mode Programming Switching						
T_{DCCK}/T_{CCKD}	DIN Setup/Hold, slave mode	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T_{CCO}	CCLK to DOUT	12	12	12	17	ns, Max
F_{SCCK}	Slave mode external CCLK	80	80	80	50	MHz, Max
Slave SelectMAP Mode Programming Switching						
T_{SMDCCK}/T_{SMCCKD}	SelectMAP Data Setup/Hold	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold	7.0/0.0	7.0/0.0	7.0/0.0	9.0/2.0	ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B Setup/Hold	17.0/1.0	17.0/1.0	17.0/1.0	27.0/2.0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out	16	16	16	26	ns, Max
T_{SMCO}	CCLK to DATA out in readback	13	13	13	25	ns, Max
T_{SMCKBY}	CCLK to BUSY out in readback	12	12	12	17	ns, Max
F_{SMCCK}	Maximum CCLK frequency (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	25	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x8 mode, LX150, and LX150T only)	40	40	40	20	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x16 mode only)	35	35	35	20	MHz, Max
F_{RBCCK}	Maximum Readback CCLK frequency, including block RAM (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	20	20	20	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	30	MHz, Max
	Maximum Readback CCLK frequency, including block RAM (LX100, LX100T, LX150, and LX150T only)	12	12	12	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX100, LX100T, LX150, and LX150T only)	35	35	35	20	MHz, Max
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}	TMS and TDI Setup time before TCK	10	10	10	17	ns, Min
T_{TCKTAP}	TMS and TDI Hold time after TCK	5.5	5.5	5.5	5.5	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid	6.5	6.5	6.5	8	ns, Max
T_{TCKH}	TCK clock minimum High time	12	12	12	21	ns, Min
T_{TCKL}	TCK clock minimum Low time	12	12	12	21	ns, Min
F_{TCK}	Maximum configuration TCK clock frequency	33	33	33	18	MHz, Max
F_{TCKB}	Maximum boundary-scan TCK clock frequency	33	33	33	18	MHz, Max
F_{TCKAES}	Maximum AES key TCK clock frequency	2	2	2	2	MHz, Max

Table 57: **Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)[1] *(Cont'd)***

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Spread Spectrum										
$F_{CLKIN\_FIXED\_SPREAD\_SPECTRUM}$	Frequency of the CLKIN input for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD/ CENTER_HIGH_SPREAD)	30	200	30	200	30	200	30	200	MHz
$T_{CENTER\_LOW\_SPREAD}$[6]	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD)	Typical = $\frac{100}{CLKFX\_DIVIDE}$ Maximum = 250								ps
$T_{CENTER\_HIGH\_SPREAD}$[6]	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM= CENTER_HIGH_SPREAD)	Typical = $\frac{240}{CLKFX\_DIVIDE}$ Maximum = 400								ps
$F_{MOD\_FIXED\_SPREAD\_SPECTRUM}$[6]	Average modulation frequency when using fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD / CENTER_HIGH_SPREAD)	Typical = $F_{IN}/1024$								MHz

Notes:
1. The values in this table are based on the operating conditions described in Table 2 and Table 55.
2. For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
3. Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
5. Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.
6. When using CENTER_LOW_SPREAD, CENTER_HIGH_SPREAD, the valid values for CLKFX_MULTIPLY are limited to 2 through 32, and the valid values for CLKFX_DIVIDE are limited to 1 through 4.

Table 58: **Recommended Operating Conditions for the Phase-Shift Clock in Variable Phase Mode (DCM_SP) or Dynamic Frequency Synthesis (DCM_CLKGEN)**

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Operating Frequency Ranges										
PSCLK_FREQ	Frequency for the PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) input.	1	167	1	167	1	167	1	100	MHz
Input Pulse Requirements										
PSCLK_PULSE	PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) pulse width as a percentage of the clock period.	40	60	40	60	40	60	40	60	%

Table 59: **Switching Characteristics for the Phase-Shift Clock in Variable Phase Mode(1)**

Symbol	Description	Amount of Phase Shift	Units
Phase Shifting Range			
MAX_STEPS(2)	When CLKIN < 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period.	±(INTEGER(10 x (TCLKIN – 3 ns)))	steps
	When CLKIN ≥ 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period.	±(INTEGER(15 x (TCLKIN – 3 ns)))	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting.	±(MAX_STEPS x DCM_DELAY_STEP_MIN)	ps
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	±(MAX_STEPS x DCM_DELAY_STEP_MAX)	ps

Notes:
1. The values in this table are based on the operating conditions described in Table 53 and Table 58.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM has no initial fixed-phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the end of Table 54.

Table 60: **Miscellaneous DCM Timing Parameters(1)**

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	3	–	CLKIN cycles

Notes:
1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFXDV, CLKFX180) are unaffected.

Table 61: **Frequency Synthesis**

Attribute	Min	Max
CLKFX_MULTIPLY (DCM_SP)	2	32
CLKFX_DIVIDE (DCM_SP)	1	32
CLKDV_DIVIDE (DCM_SP)	1.5	16
CLKFX_MULTIPLY (DCM_CLKGEN)	2	256
CLKFX_DIVIDE (DCM_CLKGEN)	1	256
CLKFXDV_DIVIDE (DCM_CLKGEN)	2	32

Table 62: **DCM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T_{DMCCK_PSEN}/ T_{DMCKC_PSEN}	PSEN Setup/Hold	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	ns
$T_{DMCCK\_PSINCDEC}$/ $T_{DMCKC\_PSINCDEC}$	PSINCDEC Setup/Hold	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	ns
T_{DMCKO_PSDONE}	Clock to out of PSDONE	1.50	1.50	1.50	1.50	ns

Table 73: **Global Clock Setup and Hold With DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSDCM0}/ T_{PHDCM0}	No Delay Global Clock and IFF(2) with DCM in Source-Synchronous Mode	XC6SLX4	0.71/0.65	N/A	0.72/1.22	1.58/1.18	ns
		XC6SLX9	0.71/0.69	0.71/1.19	0.72/1.36	1.58/1.18	ns
		XC6SLX16	0.86/0.52	0.92/0.57	1.04/0.60	1.02/1.06	ns
		XC6SLX25	0.84/0.58	0.90/0.59	1.01/0.59	1.58/1.07	ns
		XC6SLX25T	0.84/0.58	0.90/0.59	1.01/0.59	N/A	ns
		XC6SLX45	0.85/0.70	0.90/0.76	0.98/0.79	1.34/1.34	ns
		XC6SLX45T	0.85/0.70	0.90/0.76	0.98/0.79	N/A	ns
		XC6SLX75	1.00/0.62	1.06/0.63	1.15/0.63	1.65/1.46	ns
		XC6SLX75T	1.00/0.71	1.06/0.72	1.15/0.72	N/A	ns
		XC6SLX100	0.81/0.68	0.81/0.69	0.94/0.69	1.42/2.07	ns
		XC6SLX100T	0.81/0.68	0.81/0.69	0.94/0.69	N/A	ns
		XC6SLX150	0.68/0.98	0.69/0.99	0.79/0.99	1.45/1.60	ns
		XC6SLX150T	0.68/0.98	0.69/0.99	0.79/0.99	N/A	ns
		XA6SLX4	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX9	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX16	1.01/0.56	N/A	1.04/0.60	N/A	ns
		XA6SLX25	0.94/0.76	N/A	1.06/0.77	N/A	ns
		XA6SLX25T	0.94/0.76	N/A	1.14/0.77	N/A	ns
		XA6SLX45	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX45T	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX75	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX100	N/A	N/A	1.37/0.75	N/A	ns
		XQ6SLX75	N/A	N/A	1.15/0.72	1.65/1.46	ns
		XQ6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XQ6SLX150	N/A	N/A	0.79/1.15	1.45/1.60	ns
		XQ6SLX150T	0.73/1.15	N/A	0.79/1.15	N/A	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Spartan-6 FPGA source-synchronous transmitter and receiver data-valid windows.

Table 78: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device[1]	Speed Grade				Units
			-3	-3N	-2	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion[2]	LX4	0.20	N/A	0.20	0.35	ns
		LX9	0.20	0.20	0.20	0.35	ns
		LX16	0.20	0.20	0.20	0.35	ns
		LX25	0.20	0.20	0.20	0.35	ns
		LX25T	0.20	0.20	0.20	N/A	ns
		LX45	0.20	0.20	0.20	0.35	ns
		LX45T	0.20	0.20	0.20	N/A	ns
		LX75	0.20	0.20	0.20	0.35	ns
		LX75T	0.20	0.20	0.20	N/A	ns
		LX100	0.20	0.20	0.20	0.35	ns
		LX100T	0.20	0.20	0.20	N/A	ns
		LX150	0.35	0.35	0.35	0.35	ns
		LX150T	0.35	0.35	0.35	N/A	ns
T_{CKSKEW}	Global Clock Tree Skew[3]	LX4	0.25	N/A	0.25	0.29	ns
		LX9	0.25	0.25	0.25	0.29	ns
		LX16	0.15	0.15	0.15	0.22	ns
		LX25	0.26	0.26	0.26	0.41	ns
		LX25T	0.26	0.26	0.26	N/A	ns
		LX45	0.20	0.20	0.20	0.28	ns
		LX45T	0.20	0.20	0.20	N/A	ns
		LX75	0.56	0.56	0.56	0.50	ns
		LX75T	0.56	0.56	0.56	N/A	ns
		XC6SLX100[4]	0.22	0.22	0.22	0.21	ns
		XA6SLX100[4]	N/A	N/A	0.43	N/A	ns
		LX100T	0.22	0.22	0.22	N/A	ns
		LX150	0.48	0.48	0.48	0.35	ns
		LX150T	0.48	0.48	0.48	N/A	ns
T_{DCD_BUFIO2}	I/O clock tree duty cycle distortion	LX devices	0.25	0.25	0.25	0.50	ns
		LXT devices	0.25	0.25	0.25	N/A	ns

Date	Version	Description of Revisions
09/14/11	2.4	Production release of the XA6SLX4 and XA6SLX9 devices in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added production released version of the XA6SLX100 to Table 26 and Table 27 using ISE v13.3 software with -2 speed specification v1.20. Updated R_{OUT_TERM} description in Table 4. Fixed the LVPECL V_H error in Table 31. Updated introduction in Simultaneously Switching Outputs. Added the XA6SLX100 to Table 63 through Table 78, and Table 81. Added Note 4 to Table 78 because the T_{CKSKEW} for the XC6SLX100 is not the same as the T_{CKSKEW} for the XA6SLX100. Revised the revision history for version 1.6 dated 06/24/10. Removed the parenthetical statement about the -3N speed grade: (specifications are identical to the -3 speed grade).
10/17/11	3.0	Changed the data sheet from Preliminary Product Specification to Product Specification. Updated the Switching Characteristics, page 19 speed specification version ISE v13.3 software to -2 and -3 speed specification v1.20 and -1L speed specification of v1.08. Also updated Note 1 in Table 27. In Table 43, *Block RAM Switching Characteristics*, the F_{MAX} value for the -2 speed grade has been changed from 260 MHz to 280 MHz. In Table 54, *Switching Characteristics for the DLL*, a Note 6 was added and linked to CLKIN_CLKFB_PHASE.

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