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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	3411
Number of Logic Elements/Cells	43661
Total RAM Bits	2138112
Number of I/O	296
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx45t-3fgg484c

Table 3: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
V_{FS} ⁽²⁾	External voltage supply	3.2	3.3	3.4	V
I_{FS}	V_{FS} supply current	–	–	40	mA
V_{CCAUX}	Auxiliary supply voltage relative to GND	3.2	3.3	3.45	V
R_{FUSE} ⁽³⁾	External resistor from R_{FUSE} pin to GND	1129	1140	1151	Ω
V_{CCINT}	Internal supply voltage relative to GND	1.14	1.2	1.26	V
t_j	Temperature range	15	–	85	°C

Notes:

1. These specifications apply during programming of the eFUSE AES key. Programming is only supported through JTAG. The AES key is only supported in the following devices: LX75, LX75T, LX100, LX100T, LX150, and LX150T.
2. When programming eFUSE, V_{FS} must be less than or equal to V_{CCAUX} . When not programming or when eFUSE is not used, Xilinx recommends connecting V_{FS} to GND. However, V_{FS} can be between GND and 3.45 V.
3. An R_{FUSE} resistor is required when programming the eFUSE AES key. When not programming or when eFUSE is not used, Xilinx recommends connecting the R_{FUSE} pin to V_{CCAUX} or GND. However, R_{FUSE} can be unconnected.

SelectIO™ Interface DC Input and Output Levels

Table 7: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

I/O Standard	V _{CCO} for Drivers ⁽¹⁾			V _{REF} for Inputs		
	V, Min	V, Nom	V, Max	V, Min	V, Nom	V, Max
LVTTTL	3.0	3.3	3.45	V _{REF} is not used for these I/O standards		
LVC MOS33	3.0	3.3	3.45			
LVC MOS25	2.3	2.5	2.7			
LVC MOS18	1.65	1.8	1.95			
LVC MOS18_JEDEC	1.65	1.8	1.95			
LVC MOS15	1.4	1.5	1.6			
LVC MOS15_JEDEC	1.4	1.5	1.6			
LVC MOS12	1.1	1.2	1.3			
LVC MOS12_JEDEC	1.1	1.2	1.3			
PCI33_3 ⁽²⁾	3.0	3.3	3.45			
PCI66_3 ⁽²⁾	3.0	3.3	3.45			
I2C	2.7	3.0	3.45			
SMBUS	2.7	3.0	3.45			
SDIO	3.0	3.3	3.45			
MOBILE_DDR	1.7	1.8	1.9			
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_II	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_III	1.4	1.5	1.6	–	0.9	–
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–
HSTL_III_18	1.7	1.8	1.9	–	1.1	–
SSTL3_I	3.0	3.3	3.45	1.3	1.5	1.7
SSTL3_II	3.0	3.3	3.45	1.3	1.5	1.7
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38
SSTL18_I	1.7	1.8	1.9	0.833	0.9	0.969
SSTL18_II	1.7	1.8	1.9	0.833	0.9	0.969
SSTL15_II	1.425	1.5	1.575	0.69	0.75	0.81

Notes:

1. V_{CCO} range required when using I/O standard for an output. Also required for MOBILE_DDR, PCI33_3, LVC MOS18_JEDEC, LVC MOS15_JEDEC, and LVC MOS12_JEDEC inputs, and for LVC MOS25 inputs when V_{CCAUX} = 3.3V.
2. For PCI systems, the transmitter and receiver should have common supplies for V_{CCO}.

eFUSE Read Endurance

Table 11 lists the minimum guaranteed number of read cycle operations for Device DNA and for the AES eFUSE key. For more information, see [UG380: Spartan-6 FPGA Configuration User Guide](#).

Table 11: eFUSE Read Endurance

Symbol	Description	Speed Grade				Units (Min)
		-3	-3N	-2	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTP Transceiver Specifications

GTP transceivers are available in the Spartan-6 LXT devices. See [DS160: Spartan-6 Family Overview](#) for more information.

GTP Transceiver DC Characteristics

Table 12: Absolute Maximum Ratings for GTP Transceivers⁽¹⁾

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	-0.5	1.32	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	-0.5	1.32	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	-0.5	1.32	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	-0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	-0.5	1.32	V
V _{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	-0.5	1.32	V
V _{MGTREFCLK}	Reference clock absolute input voltage	-0.5	1.32	V

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 13: Recommended Operating Conditions for GTP Transceivers⁽¹⁾⁽²⁾⁽³⁾

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	1.14	1.20	1.26	V

Notes:

- Each voltage listed requires the filter circuit described in [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#).
- Voltages are specified for the temperature range of T_j = -40°C to +125°C.
- The voltage level of MGTAVCCPLL must not exceed the voltage level of MGTAVCC +10mV. The voltage level of MGTAVCC must not exceed the voltage level of MGTAVCCPLL.

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVTTL, QUIETIO, 2 mA	1.35	1.47	1.60	1.82	5.39	5.53	5.73	6.37	5.39	5.53	5.73	6.37	ns
LVTTL, QUIETIO, 4 mA	1.35	1.47	1.60	1.82	4.29	4.43	4.63	5.22	4.29	4.43	4.63	5.22	ns
LVTTL, QUIETIO, 6 mA	1.35	1.47	1.60	1.82	3.75	3.89	4.09	4.69	3.75	3.89	4.09	4.69	ns
LVTTL, QUIETIO, 8 mA	1.35	1.47	1.60	1.82	3.23	3.37	3.57	4.20	3.23	3.37	3.57	4.20	ns
LVTTL, QUIETIO, 12 mA	1.35	1.47	1.60	1.82	3.28	3.42	3.62	4.22	3.28	3.42	3.62	4.22	ns
LVTTL, QUIETIO, 16 mA	1.35	1.47	1.60	1.82	2.94	3.08	3.28	3.92	2.94	3.08	3.28	3.92	ns
LVTTL, QUIETIO, 24 mA	1.35	1.47	1.60	1.82	2.69	2.83	3.03	3.67	2.69	2.83	3.03	3.67	ns
LVTTL, Slow, 2 mA	1.35	1.47	1.60	1.82	4.36	4.50	4.70	5.30	4.36	4.50	4.70	5.30	ns
LVTTL, Slow, 4 mA	1.35	1.47	1.60	1.82	3.17	3.31	3.51	4.16	3.17	3.31	3.51	4.16	ns
LVTTL, Slow, 6 mA	1.35	1.47	1.60	1.82	2.76	2.90	3.10	3.75	2.76	2.90	3.10	3.75	ns
LVTTL, Slow, 8 mA	1.35	1.47	1.60	1.82	2.59	2.73	2.93	3.55	2.59	2.73	2.93	3.55	ns
LVTTL, Slow, 12 mA	1.35	1.47	1.60	1.82	2.58	2.72	2.92	3.54	2.58	2.72	2.92	3.54	ns
LVTTL, Slow, 16 mA	1.35	1.47	1.60	1.82	2.39	2.53	2.73	3.40	2.39	2.53	2.73	3.40	ns
LVTTL, Slow, 24 mA	1.35	1.47	1.60	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVTTL, Fast, 2 mA	1.35	1.47	1.60	1.82	3.78	3.92	4.12	4.74	3.78	3.92	4.12	4.74	ns
LVTTL, Fast, 4 mA	1.35	1.47	1.60	1.82	2.49	2.63	2.83	3.45	2.49	2.63	2.83	3.45	ns
LVTTL, Fast, 6 mA	1.35	1.47	1.60	1.82	2.44	2.58	2.78	3.40	2.44	2.58	2.78	3.40	ns
LVTTL, Fast, 8 mA	1.35	1.47	1.60	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns
LVTTL, Fast, 12 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTL, Fast, 16 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVTTL, Fast, 24 mA	1.35	1.47	1.60	1.82	1.83	1.97	2.17	2.79	1.83	1.97	2.17	2.79	ns
LVC MOS33, QUIETIO, 2 mA	1.34	1.46	1.59	1.82	5.40	5.54	5.74	6.37	5.40	5.54	5.74	6.37	ns
LVC MOS33, QUIETIO, 4 mA	1.34	1.46	1.59	1.82	4.03	4.17	4.37	5.01	4.03	4.17	4.37	5.01	ns
LVC MOS33, QUIETIO, 6 mA	1.34	1.46	1.59	1.82	3.51	3.65	3.85	4.47	3.51	3.65	3.85	4.47	ns
LVC MOS33, QUIETIO, 8 mA	1.34	1.46	1.59	1.82	3.37	3.51	3.71	4.33	3.37	3.51	3.71	4.33	ns
LVC MOS33, QUIETIO, 12 mA	1.34	1.46	1.59	1.82	2.94	3.08	3.28	3.93	2.94	3.08	3.28	3.93	ns
LVC MOS33, QUIETIO, 16 mA	1.34	1.46	1.59	1.82	2.77	2.91	3.11	3.78	2.77	2.91	3.11	3.78	ns
LVC MOS33, QUIETIO, 24 mA	1.34	1.46	1.59	1.82	2.59	2.73	2.93	3.58	2.59	2.73	2.93	3.58	ns
LVC MOS33, Slow, 2 mA	1.34	1.46	1.59	1.82	4.37	4.51	4.71	5.28	4.37	4.51	4.71	5.28	ns
LVC MOS33, Slow, 4 mA	1.34	1.46	1.59	1.82	2.98	3.12	3.32	3.94	2.98	3.12	3.32	3.94	ns
LVC MOS33, Slow, 6 mA	1.34	1.46	1.59	1.82	2.58	2.72	2.92	3.61	2.58	2.72	2.92	3.61	ns
LVC MOS33, Slow, 8 mA	1.34	1.46	1.59	1.82	2.65	2.79	2.99	3.61	2.65	2.79	2.99	3.61	ns
LVC MOS33, Slow, 12 mA	1.34	1.46	1.59	1.82	2.39	2.53	2.73	3.31	2.39	2.53	2.73	3.31	ns
LVC MOS33, Slow, 16 mA	1.34	1.46	1.59	1.82	2.31	2.45	2.65	3.27	2.31	2.45	2.65	3.27	ns
LVC MOS33, Slow, 24 mA	1.34	1.46	1.59	1.82	2.28	2.42	2.62	3.24	2.28	2.42	2.62	3.24	ns
LVC MOS33, Fast, 2 mA	1.34	1.46	1.59	1.82	3.76	3.90	4.10	4.70	3.76	3.90	4.10	4.70	ns
LVC MOS33, Fast, 4 mA	1.34	1.46	1.59	1.82	2.48	2.62	2.82	3.44	2.48	2.62	2.82	3.44	ns
LVC MOS33, Fast, 6 mA	1.34	1.46	1.59	1.82	2.32	2.46	2.66	3.28	2.32	2.46	2.66	3.28	ns

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
DIFF_SSTL3_I	1.26	1.44	1.95	2.15	1.95	2.15	ns
DIFF_SSTL3_II	1.26	1.44	1.94	2.14	1.94	2.14	ns
DIFF_SSTL2_I	1.09	1.27	1.94	2.14	1.94	2.14	ns
DIFF_SSTL2_II	1.09	1.27	1.90	2.10	1.90	2.10	ns
DIFF_SSTL18_I	1.04	1.22	1.86	2.06	1.86	2.06	ns
DIFF_SSTL18_II	1.05	1.23	1.82	2.02	1.82	2.02	ns
DIFF_SSTL15_II	1.01	1.19	1.81	2.01	1.81	2.01	ns
DIFF_MOBILE_DDR	1.04	1.22	1.89	2.09	1.89	2.09	ns
LVTTL, QUIETIO, 2 mA	1.42	1.60	5.64	5.84	5.64	5.84	ns
LVTTL, QUIETIO, 4 mA	1.42	1.60	4.46	4.66	4.46	4.66	ns
LVTTL, QUIETIO, 6 mA	1.42	1.60	3.92	4.12	3.92	4.12	ns
LVTTL, QUIETIO, 8 mA	1.42	1.60	3.37	3.57	3.37	3.57	ns
LVTTL, QUIETIO, 12 mA	1.42	1.60	3.42	3.62	3.42	3.62	ns
LVTTL, QUIETIO, 16 mA	1.42	1.60	3.09	3.29	3.09	3.29	ns
LVTTL, QUIETIO, 24 mA	1.42	1.60	2.83	3.03	2.83	3.03	ns
LVTTL, Slow, 2 mA	1.42	1.60	4.58	4.78	4.58	4.78	ns
LVTTL, Slow, 4 mA	1.42	1.60	3.38	3.58	3.38	3.58	ns
LVTTL, Slow, 6 mA	1.42	1.60	2.95	3.15	2.95	3.15	ns
LVTTL, Slow, 8 mA	1.42	1.60	2.73	2.93	2.73	2.93	ns
LVTTL, Slow, 12 mA	1.42	1.60	2.72	2.92	2.72	2.92	ns
LVTTL, Slow, 16 mA	1.42	1.60	2.53	2.73	2.53	2.73	ns
LVTTL, Slow, 24 mA	1.42	1.60	2.42	2.62	2.42	2.62	ns
LVTTL, Fast, 2 mA	1.42	1.60	4.04	4.24	4.04	4.24	ns
LVTTL, Fast, 4 mA	1.42	1.60	2.66	2.86	2.66	2.86	ns
LVTTL, Fast, 6 mA	1.42	1.60	2.58	2.78	2.58	2.78	ns
LVTTL, Fast, 8 mA	1.42	1.60	2.46	2.66	2.46	2.66	ns
LVTTL, Fast, 12 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns
LVTTL, Fast, 16 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns
LVTTL, Fast, 24 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns
LVC MOS33, QUIETIO, 2 mA	1.41	1.59	5.65	5.85	5.65	5.85	ns
LVC MOS33, QUIETIO, 4 mA	1.41	1.59	4.20	4.40	4.20	4.40	ns
LVC MOS33, QUIETIO, 6 mA	1.41	1.59	3.65	3.85	3.65	3.85	ns
LVC MOS33, QUIETIO, 8 mA	1.41	1.59	3.51	3.71	3.51	3.71	ns
LVC MOS33, QUIETIO, 12 mA	1.41	1.59	3.09	3.29	3.09	3.29	ns
LVC MOS33, QUIETIO, 16 mA	1.41	1.59	2.91	3.11	2.91	3.11	ns
LVC MOS33, QUIETIO, 24 mA	1.41	1.59	2.73	2.93	2.73	2.93	ns
LVC MOS33, Slow, 2 mA	1.41	1.59	4.59	4.79	4.59	4.79	ns
LVC MOS33, Slow, 4 mA	1.41	1.59	3.14	3.34	3.14	3.34	ns

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS33, Slow, 6 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVC MOS33, Slow, 8 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVC MOS33, Slow, 12 mA	1.41	1.59	2.53	2.73	2.53	2.73	ns
LVC MOS33, Slow, 16 mA	1.41	1.59	2.45	2.65	2.45	2.65	ns
LVC MOS33, Slow, 24 mA	1.41	1.59	2.42	2.62	2.42	2.62	ns
LVC MOS33, Fast, 2 mA	1.41	1.59	4.05	4.25	4.05	4.25	ns
LVC MOS33, Fast, 4 mA	1.41	1.59	2.66	2.86	2.66	2.86	ns
LVC MOS33, Fast, 6 mA	1.41	1.59	2.46	2.66	2.46	2.66	ns
LVC MOS33, Fast, 8 mA	1.41	1.59	2.21	2.41	2.21	2.41	ns
LVC MOS33, Fast, 12 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVC MOS33, Fast, 16 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVC MOS33, Fast, 24 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVC MOS25, QUIETIO, 2 mA	0.89	1.07	5.00	5.20	5.00	5.20	ns
LVC MOS25, QUIETIO, 4 mA	0.89	1.07	3.85	4.05	3.85	4.05	ns
LVC MOS25, QUIETIO, 6 mA	0.89	1.07	3.60	3.80	3.60	3.80	ns
LVC MOS25, QUIETIO, 8 mA	0.89	1.07	3.34	3.54	3.34	3.54	ns
LVC MOS25, QUIETIO, 12 mA	0.89	1.07	2.98	3.18	2.98	3.18	ns
LVC MOS25, QUIETIO, 16 mA	0.89	1.07	2.79	2.99	2.79	2.99	ns
LVC MOS25, QUIETIO, 24 mA	0.89	1.07	2.64	2.84	2.64	2.84	ns
LVC MOS25, Slow, 2 mA	0.89	1.07	3.96	4.16	3.96	4.16	ns
LVC MOS25, Slow, 4 mA	0.89	1.07	2.96	3.16	2.96	3.16	ns
LVC MOS25, Slow, 6 mA	0.89	1.07	2.88	3.08	2.88	3.08	ns
LVC MOS25, Slow, 8 mA	0.89	1.07	2.63	2.83	2.63	2.83	ns
LVC MOS25, Slow, 12 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVC MOS25, Slow, 16 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVC MOS25, Slow, 24 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVC MOS25, Fast, 2 mA	0.89	1.07	3.52	3.72	3.52	3.72	ns
LVC MOS25, Fast, 4 mA	0.89	1.07	2.43	2.63	2.43	2.63	ns
LVC MOS25, Fast, 6 mA	0.89	1.07	2.23	2.43	2.23	2.43	ns
LVC MOS25, Fast, 8 mA	0.89	1.07	2.16	2.36	2.16	2.36	ns
LVC MOS25, Fast, 12 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVC MOS25, Fast, 16 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVC MOS25, Fast, 24 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVC MOS18, QUIETIO, 2 mA	1.25	1.43	6.11	6.31	6.11	6.31	ns
LVC MOS18, QUIETIO, 4 mA	1.25	1.43	4.88	5.08	4.88	5.08	ns
LVC MOS18, QUIETIO, 6 mA	1.25	1.43	4.20	4.40	4.20	4.40	ns
LVC MOS18, QUIETIO, 8 mA	1.25	1.43	3.86	4.06	3.86	4.06	ns
LVC MOS18, QUIETIO, 12 mA	1.25	1.43	3.49	3.69	3.49	3.69	ns

Table 32: Output Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	R_{REF} (Ω)	$C_{REF}^{(1)}$ (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
SSTL, Class II, 1.5V	SSTL15_II	25	0	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	100	0	0 ⁽³⁾	—
BLVDS (Bus LVDS), 2.5V	BLVDS_25	Note 4	0	0 ⁽³⁾	—
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	100	0	0 ⁽³⁾	—
RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RSDS_25, RSDS_33	100	0	0 ⁽³⁾	—
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	Note 5	0	0 ⁽³⁾	—
PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V	PPDS_25, PPDS_33	100	0	0 ⁽³⁾	—

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. The value given is the differential output voltage.
4. See the *BLVDS Output Termination* section in [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.
5. See the *TMDS_33 Termination* section in [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.

Simultaneously Switching Outputs

Due to package electrical parasitics, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. [Table 33](#) and [Table 34](#) provide guidelines for the recommended maximum allowable number of SSOs. These guidelines describe the maximum number of user I/O pins of an output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise for that particular signal standard. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of GND and power bounce.

For each device/package combination, [Table 33](#) provides the number of equivalent V_{CCO} /GND pairs per bank. For each output signal standard and drive strength, [Table 34](#) recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO} /GND pair within an I/O bank. The guidelines are categorized by package style, slew rate, and output drive current. The number of SSOs are also specified by I/O bank. Multiply the appropriate numbers from each table to calculate the maximum number of SSOs allowed within an I/O bank. The guidelines assume that all pins within a bank use the same I/O standard. Exceeding these SSO guidelines can result in increased power or GND bounce, degraded signal integrity, or increased system jitter. For a given I/O standard, if the SSO limit per pair in [Table 34](#) is greater than the maximum I/O per pair in [Table 33](#), then there is no SSO limit for the exclusive use of that I/O standard.

The recommended maximum SSO values assume that the FPGA is soldered on a printed circuit board and that the board uses sound design practices. Due to the additional inductance introduced by the socket, the SSO values do not apply for FPGAs mounted in sockets. The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics. For more detail, see [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 33: Spartan-6 FPGA V_{CCO}/GND Pairs per Bank

Package	Devices	Description	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5
TQG144	LX	V _{CCO} /GND Pairs	3	3	2	3	N/A	N/A
		Maximum I/O per Pair	8	8	13	8	N/A	N/A
CPG196	LX	V _{CCO} /GND Pairs	4	6	4	6	N/A	N/A
		Maximum I/O per Pair	6	4	7	4	N/A	N/A
CSG225	LX	V _{CCO} /GND Pairs	4	4	4	4	N/A	N/A
		Maximum I/O per Pair	10	10	9	10	N/A	N/A
FT(G)256	LX	V _{CCO} /GND Pairs	5	6	4	5	N/A	N/A
		Maximum I/O per Pair	8	9	9	10	N/A	N/A
CSG324	LX	V _{CCO} /GND Pairs	6	6	6	6	N/A	N/A
		Maximum I/O per Pair	10	9	10	9	N/A	N/A
	LXT	V _{CCO} /GND Pairs	4	6	6	6	N/A	N/A
		Maximum I/O per Pair	4	9	10	9	N/A	N/A
CS(G)484	LX	V _{CCO} /GND Pairs	8	13	8	13	N/A	N/A
		Maximum I/O per Pair	7	8	7	8	N/A	N/A
	LXT	V _{CCO} /GND Pairs	7	12	8	13	N/A	N/A
		Maximum I/O per Pair	5	8	6	8	N/A	N/A
FG(G)484	LX	V _{CCO} /GND Pairs	10	10	11	11	N/A	N/A
		Maximum I/O per Pair	6	8	9	8	N/A	N/A
	LXT	V _{CCO} /GND Pairs	6	10	11	10	N/A	N/A
		Maximum I/O per Pair	7	8	7	8	N/A	N/A
FG(G)676	LX45	V _{CCO} /GND Pairs	12	15	10	16	N/A	N/A
		Maximum I/O per Pair	3	7	8	7	N/A	N/A
	LX75, LX100, LX150	V _{CCO} /GND Pairs	12	9	10	10	6	6
		Maximum I/O per Pair	9	10	9	9	8	9
	LXT	V _{CCO} /GND Pairs	10	8	10	8	7	7
		Maximum I/O per Pair	8	7	8	8	7	7
FG(G)900	LX	V _{CCO} /GND Pairs	17	14	17	14	7	8
		Maximum I/O per Pair	7	6	7	8	7	6
	LXT	V _{CCO} /GND Pairs	15	14	13	14	7	8
		Maximum I/O per Pair	7	6	8	8	7	6

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

V _{CCO}	I/O Standard	Drive	Slew	SSO Limit per V _{CCO} /GND Pair				
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324		
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5	
1.8V	LVCMOS18, LVCMOS18_JEDEC	2	Fast	39	46	39	47	
			Slow	65	75	65	74	
			QuietIO	80	80	80	85	
		4	Fast	22	25	22	25	
			Slow	38	36	38	29	
			QuietIO	45	40	45	35	
		6	Fast	16	18	16	17	
			Slow	27	25	27	19	
			QuietIO	30	28	30	23	
		8	Fast	13	15	13	14	
			Slow	16	18	16	16	
			QuietIO	25	22	25	18	
		12	Fast	5	7	5	5	
			Slow	7	8	7	6	
			QuietIO	11	10	11	8	
		16	Fast	4	5	4	4	
			Slow	7	8	7	5	
			QuietIO	11	10	11	8	
		24	Fast	N/A	5	N/A	3	
			Slow	N/A	8	N/A	8	
			QuietIO	N/A	10	N/A	8	
	HSTL_I_18				9	10	9	9
	HSTL_II_18				N/A	5	N/A	6
	HSTL_III_18				9	10	9	11
	DIFF_HSTL_I_18				27	30	27	27
	DIFF_HSTL_II_18				N/A	15	N/A	18
	DIFF_HSTL_III_18				27	30	27	33
MOBILE_DDR ⁽³⁾				12	14	12	14	
DIFF_MOBILE_DDR ⁽³⁾				36	42	36	42	
SSTL_18_I ⁽³⁾				9	10	9	10	
SSTL_18_II ⁽³⁾				N/A	5	N/A	4	
DIFF_SSTL_18_I ⁽³⁾				27	30	27	30	
DIFF_SSTL_18_II ⁽³⁾				N/A	15	N/A	12	

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

V _{CCO}	I/O Standard	Drive	Slew	SSO Limit per V _{CCO} /GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
3.3V	LVCMOS33	2	Fast	42	46	42	44
			Slow	50	55	50	49
			QuietIO	60	68	60	60
		4	Fast	21	27	21	25
			Slow	32	37	32	32
			QuietIO	39	42	39	37
		6	Fast	14	19	14	17
			Slow	19	25	19	22
			QuietIO	29	30	29	25
		8	Fast	11	15	11	14
			Slow	15	20	15	18
			QuietIO	25	24	25	20
		12	Fast	1	3	1	1
			Slow	2	5	2	2
			QuietIO	4	9	4	7
		16	Fast	1	2	1	1
			Slow	1	5	1	1
			QuietIO	3	10	3	8
		24	Fast	1	2	1	1
			Slow	2	5	2	1
			QuietIO	7	9	7	7

Table 44: DSP48A1 Switching Characteristics (Cont'd)

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-3	-3N	-2	-1L	
T _{DSPDCK_OPMODE_PREG} / T _{DSPCKD_OPMODE_PREG}	OPMODE input to P register CLK	Yes	Yes	Yes	6.21/ −0.84	7.27/ −0.84	7.27/ −0.84	10.43/ −0.84	ns
		No	Yes	Yes	1.69/ −0.87	1.98/ −0.87	1.98/ −0.87	3.62/ −0.87	ns
		No	No	Yes	2.09/ −0.22	2.30/ −0.22	2.30/ −0.22	3.79/ −0.22	ns
Clock to Out from Output Register Clock to Output Pin									
T _{DSPCKO_P_PREG}	CLK (PREG) to P output	N/A	N/A	N/A	1.20	1.34	1.34	1.90	ns
Clock to Out from Pipeline Register Clock to Output Pins									
T _{DSPCKO_P_MREG}	CLK (MREG) to P output	N/A	N/A	Yes	3.38	3.95	3.95	5.83	ns
Clock to Out from Input Register Clock to Output Pins									
T _{DSPCKO_P_A1REG}	CLK (A1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.65	ns
T _{DSPCKO_P_B1REG}	CLK (B1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.63	ns
T _{DSPCKO_P_CREG}	CLK (CREG) to P output	N/A	N/A	Yes	3.12	3.64	3.64	5.24	ns
T _{DSPCKO_P_DREG}	CLK (DREG) to P output	Yes	Yes	Yes	6.77	7.92	7.92	12.53	ns
Combinatorial Delays from Input Pins to Output Pins									
T _{DSPDO_A_P}	A input to P output	N/A	No	Yes	2.85	3.33	3.33	4.73	ns
		N/A	Yes	No ⁽²⁾	3.35	3.93	3.93	6.74	ns
		N/A	Yes	Yes	4.56	5.22	5.22	8.94	ns
T _{DSPDO_B_P}	B input to P output	Yes	No	No ⁽²⁾	3.22	3.76	3.76	5.55	ns
		Yes	Yes	No ⁽²⁾	6.01	6.54	6.54	9.76	ns
		Yes	Yes	Yes	6.27	7.34	7.34	11.96	ns
T _{DSPDO_C_P}	C input to P output	N/A	N/A	Yes	2.69	3.15	3.15	4.68	ns
T _{DSPDO_D_P}	D input to P output	Yes	Yes	Yes	6.31	7.38	7.38	11.81	ns
T _{DSPDO_OPMODE_P}	OPMODE input to P output	Yes	Yes	Yes	6.43	7.52	7.52	11.84	ns
		No	Yes	Yes	4.84	5.66	5.66	9.25	ns
		No	No	Yes	3.11	3.49	3.49	5.03	ns
Maximum Frequency									
F _{MAX}	All registers used	Yes	Yes	Yes	390	333	333	213	MHz

Notes:

1. A Yes signifies that the component is in the path. A No signifies that the component is being bypassed. N/A signifies not applicable because no path exists.
2. Implemented in the post-adder by adding to zero.

Table 45: Device DNA Interface Port Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T _{DNASSU}	Setup time on SHIFT before the rising edge of CLK	7				ns, Min
T _{DNASH}	Hold time on SHIFT after the rising edge of CLK	1				ns, Min
T _{DNADSU}	Setup time on DIN before the rising edge of CLK	7				ns, Min
T _{DNADH}	Hold time on DIN after the rising edge of CLK	1				ns, Min
T _{DNARSU}	Setup time on READ before the rising edge of CLK	7				ns, Min
		1,000				ns, Max
T _{DNARH}	Hold time on READ after the rising edge of CLK	1				ns, Min
T _{DNADCKO}	Clock-to-output delay on DOUT after rising edge of CLK	0.5				ns, Min
		6				ns, Max
T _{DNACKF} ⁽²⁾	CLK frequency	2				MHz, Max
T _{DNACKL}	CLK Low time	50				ns, Min
T _{DNACKH}	CLK High time	50				ns, Min

Notes:

1. The minimum READ pulse width is 8 ns, the maximum READ pulse width is 1 μ s.
2. Also applies to TCK when reading DNA through the boundary-scan port.

Table 46: Suspend Mode Switching Characteristics

Symbol	Description	Min	Max	Units
Entering Suspend Mode				
T _{SUSPENDHIGH_AWAKE}	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter	2.5	14	ns
T _{SUSPENDFILTER}	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled	31	430	ns
T _{SUSPEND_GWE}	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior (without glitch filter)	–	15	ns
T _{SUSPEND_GTS}	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements (without glitch filter)	–	15	ns
T _{SUSPEND_DISABLE}	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled (without glitch filter)	–	1500	ns
Exiting Suspend Mode				
T _{SUSPENDLOW_AWAKE}	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM or PLL lock time.	7	75	μ s
T _{SUSPEND_ENABLE}	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	7	41	μ s
T _{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using sw_clk:InternalClock and sw_gwe_cycle:1 .	–	80	ns
T _{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using sw_clk:InternalClock and sw_gwe_cycle:512 .	–	20.5	μ s
T _{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using sw_clk:InternalClock and sw_gts_cycle:1 .	–	80	ns
T _{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using sw_clk:InternalClock and sw_gts_cycle:512 .	–	20.5	μ s
T _{SCP_AWAKE}	Rising edge of SCP pins to rising edge of AWAKE pin	7	75	μ s

Configuration Switching Characteristics

Table 47: Configuration Switching Characteristics⁽¹⁾

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Power-up Timing Characteristics						
T _{PL} ⁽²⁾	PROGRAM_B Latency	4	4	4	5	ms, Max
T _{POR} ⁽²⁾	Power-on reset (50 ms ramp time) ⁽³⁾	5/30	5/34	5/40	5/40	ms, Min/Max
	Power-on reset (10 ms ramp time)	5/25	5/29	5/35	5/40	ms, Min/Max
T _{PROGRAM}	PROGRAM_B Pulse Width	500	500	500	500	ns, Min
Slave Serial Mode Programming Switching						
T _{DCCK} /T _{CCKD}	DIN Setup/Hold, slave mode	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T _{CCO}	CCLK to DOUT	12	12	12	17	ns, Max
F _{SCCK}	Slave mode external CCLK	80	80	80	50	MHz, Max
Slave SelectMAP Mode Programming Switching						
T _{SMDCK} /T _{SMCCKD}	SelectMAP Data Setup/Hold	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T _{SMCSCCK} /T _{SMCCKCS}	CSI_B Setup/Hold	7.0/0.0	7.0/0.0	7.0/0.0	9.0/2.0	ns, Min
T _{SMWCK} /T _{SMCCKW}	RDWR_B Setup/Hold	17.0/1.0	17.0/1.0	17.0/1.0	27.0/2.0	ns, Min
T _{SMCKCSO}	CSO_B clock to out	16	16	16	26	ns, Max
T _{SMCO}	CCLK to DATA out in readback	13	13	13	25	ns, Max
T _{SMCKBY}	CCLK to BUSY out in readback	12	12	12	17	ns, Max
F _{SMCK}	Maximum CCLK frequency (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	25	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x8 mode, LX150, and LX150T only)	40	40	40	20	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x16 mode only)	35	35	35	20	MHz, Max
F _{RBCK}	Maximum Readback CCLK frequency, including block RAM (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	20	20	20	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	30	MHz, Max
	Maximum Readback CCLK frequency, including block RAM (LX100, LX100T, LX150, and LX150T only)	12	12	12	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX100, LX100T, LX150, and LX150T only)	35	35	35	20	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK}	TMS and TDI Setup time before TCK	10	10	10	17	ns, Min
T _{TCKTAP}	TMS and TDI Hold time after TCK	5.5	5.5	5.5	5.5	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output valid	6.5	6.5	6.5	8	ns, Max
T _{TCKH}	TCK clock minimum High time	12	12	12	21	ns, Min
T _{TCKL}	TCK clock minimum Low time	12	12	12	21	ns, Min
F _{TCK}	Maximum configuration TCK clock frequency	33	33	33	18	MHz, Max
F _{TCKB}	Maximum boundary-scan TCK clock frequency	33	33	33	18	MHz, Max
F _{TCKAES}	Maximum AES key TCK clock frequency	2	2	2	2	MHz, Max

Table 52: PLL Specification (Cont'd)

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
F _{INMIN}	Minimum Input Clock Frequency	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
F _{INJITTER}	Maximum Input Clock Period Jitter: 19–200 MHz	All	1 ns Maximum				
	Maximum Input Clock Period Jitter: > 200 MHz	All	<20% of clock input period Maximum				
F _{INDUTY}	Allowable Input Duty Cycle: 19—199 MHz	All	25/75				%
	Allowable Input Duty Cycle: 200—299 MHz	All	35/65				%
	Allowable Input Duty Cycle: > 300 MHz	All	45/55				%
F _{VCOMIN}	Minimum PLL VCO Frequency	LX devices	400	400	400	400	MHz
		LXT devices	400	400	400	N/A	MHz
F _{VCOMAX}	Maximum PLL VCO Frequency	LX devices	1080	1050	1000	1000	MHz
		LXT devices	1080	1050	1000	N/A	MHz
F _{BANDWIDTH}	Low PLL Bandwidth at Typical ⁽³⁾	All	1	1	1	1	MHz
	High PLL Bandwidth at Typical ⁽³⁾	All	4	4	4	4	MHz
T _{STAPHAOFFSET}	Static Phase Offset of the PLL Outputs	All	0.12	0.12	0.12	0.15	ns
T _{OUTJITTER}	PLL Output Jitter ⁽³⁾	All	Note 2				
T _{OUTDUTY}	PLL Output Clock Duty Cycle Precision ⁽⁴⁾	All	0.15	0.15	0.20	0.25	ns
T _{LOCKMAX}	PLL Maximum Lock Time	All	100	100	100	100	µs
F _{OUTMAX}	PLL Maximum Output Frequency for BUFGMUX	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz
	PLL Maximum Output Frequency for BUFPLL	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz
F _{OUTMIN}	PLL Minimum Output Frequency ⁽⁵⁾	All	3.125	3.125	3.125	3.125	MHz
T _{EXTFDVAR}	External Clock Feedback Variation: 19–200 MHz	All	1 ns Maximum				
	External Clock Feedback Variation: > 200 MHz	All	< 20% of clock input period Maximum				
RST _{MINPULSE}	Minimum Reset Pulse Width	All	5	5	5	5	ns
F _{PFDMAX} ⁽⁵⁾	Maximum Frequency at the Phase Frequency Detector	LX devices	500	500	400	300	MHz
		LXT devices	500	500	400	N/A	MHz
F _{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
T _{FBDELAY}	Maximum Delay in the Feedback Path	All	3 ns Max or one CLKIN cycle				

Notes:

1. LXT devices are not available with a -1L speed grade.
2. Values for this parameter are available in the Clocking Wizard.
3. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When using CLK_FEEDBACK = CLKOUT0 with BUFIO2 feedback, the feedback frequency will be higher than the phase frequency detector frequency. $F_{PFDMAX} = F_{CLKFB} / CLKFBOUT_MULT$

Table 68: Global Clock Input to Output Delay With DCM and PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.							
T _{ICKOFDCM_PLL}	Global Clock and OUTFF with DCM and PLL	XC6SLX4	4.78	N/A	6.32	7.09	ns
		XC6SLX9	4.78	5.24	6.32	7.09	ns
		XC6SLX16	4.70	5.12	5.94	6.63	ns
		XC6SLX25	4.70	5.09	5.92	7.30	ns
		XC6SLX25T	4.70	5.09	5.92	N/A	ns
		XC6SLX45	4.63	4.98	5.83	7.26	ns
		XC6SLX45T	4.63	4.98	5.83	N/A	ns
		XC6SLX75	4.68	5.04	5.88	6.90	ns
		XC6SLX75T	4.68	5.04	5.88	N/A	ns
		XC6SLX100	4.72	5.07	5.92	7.77	ns
		XC6SLX100T	4.76	5.07	5.92	N/A	ns
		XC6SLX150	4.44	4.73	5.31	6.96	ns
		XC6SLX150T	4.44	4.73	5.31	N/A	ns
		XA6SLX4	5.07	N/A	6.18	N/A	ns
		XA6SLX9	5.07	N/A	6.18	N/A	ns
		XA6SLX16	5.22	N/A	5.77	N/A	ns
		XA6SLX25	5.01	N/A	5.80	N/A	ns
		XA6SLX25T	5.01	N/A	5.90	N/A	ns
		XA6SLX45	4.93	N/A	5.67	N/A	ns
		XA6SLX45T	4.93	N/A	5.67	N/A	ns
		XA6SLX75	4.94	N/A	5.70	N/A	ns
		XA6SLX75T	4.94	N/A	5.70	N/A	ns
		XA6SLX100	N/A	N/A	5.77	N/A	ns
		XQ6SLX75	N/A	N/A	5.70	6.90	ns
		XQ6SLX75T	4.94	N/A	5.70	N/A	ns
		XQ6SLX150	N/A	N/A	5.31	6.96	ns
		XQ6SLX150T	5.02	N/A	5.31	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 69: Global Clock Input to Output Delay With DCM and PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode.							
T _{ICKOFDCM0_PLL}	Global Clock and OUTFF with DCM and PLL	XC6SLX4	5.58	N/A	7.42	8.54	ns
		XC6SLX9	5.58	6.19	7.42	8.54	ns
		XC6SLX16	5.50	6.06	7.05	8.24	ns
		XC6SLX25	5.57	6.04	7.02	8.33	ns
		XC6SLX25T	5.57	6.04	7.02	N/A	ns
		XC6SLX45	5.53	5.97	6.96	8.32	ns
		XC6SLX45T	5.53	5.97	6.96	N/A	ns
		XC6SLX75	5.55	6.00	6.99	8.54	ns
		XC6SLX75T	5.55	6.00	6.99	N/A	ns
		XC6SLX100	5.58	6.03	7.02	9.11	ns
		XC6SLX100T	5.62	6.03	7.02	N/A	ns
		XC6SLX150	5.32	5.70	6.41	8.26	ns
		XC6SLX150T	5.32	5.70	6.41	N/A	ns
		XA6SLX4	5.87	N/A	7.28	N/A	ns
		XA6SLX9	5.87	N/A	7.28	N/A	ns
		XA6SLX16	6.02	N/A	6.87	N/A	ns
		XA6SLX25	5.88	N/A	6.90	N/A	ns
		XA6SLX25T	5.88	N/A	7.00	N/A	ns
		XA6SLX45	5.82	N/A	6.81	N/A	ns
		XA6SLX45T	5.82	N/A	6.81	N/A	ns
		XA6SLX75	5.81	N/A	6.80	N/A	ns
		XA6SLX75T	5.81	N/A	6.80	N/A	ns
		XA6SLX100	N/A	N/A	6.88	N/A	ns
		XQ6SLX75	N/A	N/A	6.80	8.54	ns
		XQ6SLX75T	5.81	N/A	6.80	N/A	ns
		XQ6SLX150	N/A	N/A	6.41	8.26	ns
		XQ6SLX150T	5.90	N/A	6.41	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 73: Global Clock Setup and Hold With DCM in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.(1)							
T _{PSDCM0} / T _{PHDCM0}	No Delay Global Clock and IFF(2) with DCM in Source-Synchronous Mode	XC6SLX4	0.71/0.65	N/A	0.72/1.22	1.58/1.18	ns
		XC6SLX9	0.71/0.69	0.71/1.19	0.72/1.36	1.58/1.18	ns
		XC6SLX16	0.86/0.52	0.92/0.57	1.04/0.60	1.02/1.06	ns
		XC6SLX25	0.84/0.58	0.90/0.59	1.01/0.59	1.58/1.07	ns
		XC6SLX25T	0.84/0.58	0.90/0.59	1.01/0.59	N/A	ns
		XC6SLX45	0.85/0.70	0.90/0.76	0.98/0.79	1.34/1.34	ns
		XC6SLX45T	0.85/0.70	0.90/0.76	0.98/0.79	N/A	ns
		XC6SLX75	1.00/0.62	1.06/0.63	1.15/0.63	1.65/1.46	ns
		XC6SLX75T	1.00/0.71	1.06/0.72	1.15/0.72	N/A	ns
		XC6SLX100	0.81/0.68	0.81/0.69	0.94/0.69	1.42/2.07	ns
		XC6SLX100T	0.81/0.68	0.81/0.69	0.94/0.69	N/A	ns
		XC6SLX150	0.68/0.98	0.69/0.99	0.79/0.99	1.45/1.60	ns
		XC6SLX150T	0.68/0.98	0.69/0.99	0.79/0.99	N/A	ns
		XA6SLX4	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX9	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX16	1.01/0.56	N/A	1.04/0.60	N/A	ns
		XA6SLX25	0.94/0.76	N/A	1.06/0.77	N/A	ns
		XA6SLX25T	0.94/0.76	N/A	1.14/0.77	N/A	ns
		XA6SLX45	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX45T	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX75	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX100	N/A	N/A	1.37/0.75	N/A	ns
		XQ6SLX75	N/A	N/A	1.15/0.72	1.65/1.46	ns
		XQ6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XQ6SLX150	N/A	N/A	0.79/1.15	1.45/1.60	ns
		XQ6SLX150T	0.73/1.15	N/A	0.79/1.15	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 81: Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out Using BUFIO2

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO2							
T _{PSCS} /T _{PHCS}	IFF setup/hold using BUFIO2 clock	XC6SLX4	0.57/0.94	N/A	0.95/1.12	0.27/1.56	ns
		XC6SLX9	0.40/0.95	0.50/0.96	0.60/1.12	0.27/1.56	ns
		XC6SLX16	0.48/0.74	0.55/0.75	0.69/0.83	1.27/1.31	ns
		XC6SLX25	0.28/1.02	0.28/1.12	0.28/1.24	0.15/1.78	ns
		XC6SLX25T	0.28/1.02	0.28/1.12	0.28/1.24	N/A	ns
		XC6SLX45	0.42/1.19	0.44/1.29	0.50/1.40	0.12/1.83	ns
		XC6SLX45T	0.42/1.19	0.44/1.29	0.50/1.40	N/A	ns
		XC6SLX75	0.38/1.48	0.38/1.63	0.38/1.84	0.05/2.78	ns
		XC6SLX75T	0.38/1.48	0.38/1.63	0.38/1.84	N/A	ns
		XC6SLX100	0.06/1.48	0.06/1.63	0.06/1.87	−0.03/2.72	ns
		XC6SLX100T	0.06/1.48	0.06/1.63	0.06/1.87	N/A	ns
		XC6SLX150	0.04/1.73	0.04/1.75	0.04/1.98	−0.08/3.07	ns
		XC6SLX150T	0.04/1.73	0.04/1.75	0.04/1.98	N/A	ns
		XA6SLX4	0.64/0.96	N/A	0.97/1.12	N/A	ns
		XA6SLX9	0.44/0.99	N/A	0.62/1.16	N/A	ns
		XA6SLX16	0.50/0.78	N/A	0.69/0.83	N/A	ns
		XA6SLX25	0.28/1.04	N/A	0.28/1.25	N/A	ns
		XA6SLX25T	0.28/1.04	N/A	0.28/1.25	N/A	ns
		XA6SLX45	0.43/1.21	N/A	0.50/1.40	N/A	ns
		XA6SLX45T	0.43/1.21	N/A	0.50/1.40	N/A	ns
		XA6SLX75	0.38/1.49	N/A	0.38/1.84	N/A	ns
		XA6SLX75T	0.38/1.49	N/A	0.38/1.84	N/A	ns
		XA6SLX100	N/A	N/A	1.01/1.63	N/A	ns
		XQ6SLX75	N/A	N/A	0.38/1.84	0.05/2.78	ns
		XQ6SLX75T	0.38/1.49	N/A	0.38/1.84	N/A	ns
		XQ6SLX150	N/A	N/A	0.04/1.98	−0.08/3.07	ns
		XQ6SLX150T	0.04/1.75	N/A	0.04/1.98	N/A	ns

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
08/26/09	1.1	Added V_{FS} to Table 1 and Table 2 . Added R_{FUSE} to Table 2 . Added XC6SLX75 and XC6SLX75T to V_{BATT} and I_{BATT} in Table 1 , Table 2 , and Table 4 . Corrected the quiescent supply current for the XC6SLX4 in Table 5 . Updated Table 11 . Removed DV_{PPIN} from Figure 2 . Removed $F_{PCIECORE}$ from Table 24 and added values to $F_{PCIEUSER}$. Added more networking applications to Table 25 . Updated values for $T_{SUSPENDLOW_AWAKE}$, $T_{SUSPEND_ENABLE}$, and T_{SCP_AWAKE} in Table 46 . Numerous changes to Table 47 , page 54 including the addition of new values to various specifications, revising the $T_{SMCKCSO}$ description, and changing the units of T_{POR} . Also, removed <i>Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK</i> section from Table 47 and updated all the notes. In Table 52 , added to F_{INMAX} , revised F_{OUTMAX} , and removed PLL Maximum Output Frequency for BUFIO2. Revised values for DCM_DELAY_STEP in Table 54 . Updated CLKIN_FREQ_FX values in Table 55 .
01/04/10	1.2	Added -4 speed grade to entire document. Updated speed specification of -4, -3, -2 speed grades to version 1.03. Added -1L speed grade numbers per speed specification 1.00. Updated T_{SOL} in Table 1 . Added -1L rows for LVCMOS12, LVCMOS15, and LVCMOS18 in Table 9 . Revised much of the detail in GTP Transceiver Specifications in Table 12 through Table 23 . Added -2 data to Table 25 . Updated F_{MAX} in Table 44 . Updated descriptions for T_{DNACKL} and T_{DNACKH} in Table 45 and revised values for all parameters. Removed $T_{INITADDR}$ from Table 47 and added new data. Updated values in Table 48 through Table 62 . Added Table 51 (BUFPLL) and Table 57 (DCM_CLKGEN). Removed $T_{LOCKMAX}$ note from Table 52 . Updated note 3 in Table 53 . In Table 79 : removed XC6SLX75CSG324 and XC6SLX75TCSG324; added XC6SLX75FG(G)484 and XC6SLX75FG(G)484.
02/22/10	1.3	Production release of XC6SLX16 -2 speed grade devices. The changes to Table 26 and Table 27 includes updating this data sheet to the data in ISE v11.5 software with speed specification v1.06. Updated maximum of V_{IN} and V_{TS} and note 2 in Table 1 . In Table 2 , changed V_{IN} , added I_{IN} and note 5, revised notes 1, 6, and 7, and added note 8 to R_{FUSE} . In Table 4 , removed previous note 1 and added data to I_{RPU} , I_{RPD} , and I_{BATT} , changed C_{IN} , added R_{DT} and R_{IN_TERM} , and added note 2 and 3. Updated V_{CCO2} in Table 6 . Added Table 7 and Table 8 . Removed PCI66_3 from Table 9 . Updated PCI33_3 and I2C in Table 9 . Updated the description of Table 11 . Completely updated Table 25 . Updated Table 28 including adding values for PCI33_3. Updated V_{REF} value for HSTL_III_18 in Table 31 . Updates missing V_{REF} values in Table 32 . Added Simultaneously Switching Outputs , page 36 . Removed T_{GSRQ} and T_{RPW} from Table 35 and Table 36 . Also removed T_{DOQ} from Table 36 . Removed T_{ISDO_DO} and note 1 from Table 37 . Removed T_{OSCK_S} and combinatorial section from Table 38 . In Table 39 , removed T_{IODDO_T} and added new tap parameters and note 2. In Table 40 , Table 41 , and Table 42 , made typographical edits and removed notes. Removed clock CLK section in Table 41 . Removed clock CLK section and T_{REG_MUX} and T_{REG_M31} in Table 42 . Added block RAM F_{MAX} values to Table 43 . Updated values and added note 2 to Table 45 . Added values to Table 46 and removed note 1. Numerous changes to Table 47 . Completely updated Table 57 . Revised data in Table 62 . Removed note 3 from Table 71 . Added values to Table 79 . Added data to Table 80 and Table 81 .
03/10/10	1.4	Production release of XC6SLX45 -2 speed grade devices, which includes changes to Table 26 and Table 27 updating this data sheet to the data in ISE v11.5 software with speed specification v1.07. Fixed R_{IN_TERM} description in Table 4 . Added PCI66_3 to Table 7 and replaced note 1. Corrected note 1 and the V, Max for TMDS_33 in Table 8 . In Table 10 , added note 1 to LVPECL_33 and TMDS_33. Also updated specifications for TMDS_33. Updated the GTP Transceiver Specifications section including adding values to Table 16 , Table 17 , and Table 20 through Table 23 . Added PCI66_3 back into Table 9 , Table 28 , Table 31 , Table 32 , and Table 34 . Updated note 3 on Table 32 . In Table 34 , corrected some typographical errors and fixed SSO limits for bank1/3 in FG(G)484 package. Corrected T_{OSCK_OCE} in Table 38 . In Table 57 , updated CLKFX_FREEZE_VAR and CLKFX_FREEZE_TEMP_SLOPE and added typical values to $T_{CENTER_LOW_SPREAD}$ and $T_{CENTER_HIGH_SPREAD}$. Updated and added values to Table 63 through Table 78 , and Table 81 . In Table 79 , revised the XC6SLX16-CSG324 and the XC6SLX45-CSG484 and FG(G)484 values.

Date	Version	Description of Revisions
01/10/11	1.11	Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.4 software with speed specification v1.15 for the -4, -3, -3N, and -2 speed grades. Added note 3 to Table 27. Also updated the -1L speed grade requirements to ISE v12.4 software with speed specification v1.06. Revised -3N definition throughout the document. Added note 4 to Table 2 and updated note 5. Added information on V_{CCINT} to note 1 in Table 5. Updated Networking Applications -3 values in Table 25 to match improvements made in ISE v12.4. In Table 28, added note 1 and revised the T_{IOTP} values for LVDS_33, LVDS_25, MINI_LVDS_33, MINI_LVDS_25, RSDS_33, RSDS_25, TMDS_33, PPDS_33, and PPDS_25. Added note 3 to Table 55.
02/11/11	1.12	As described in XCEN11008: Product Discontinuation Notice For Spartan-6 LXT -4 Devices, the -4 speed specifications have been discontinued. As outlined in page 2 of the XCN, designers currently using -4 speed specifications should rerun timing analysis using the new -3 speed specifications before moving to a replacement device. Updated the networking applications section of Table 25. Updated -2 speed specifications throughout document and added note 3 to Table 27 advising designers to use the -2 speed specification update (v1.17) with the ISE 12.4 software patch. Added F_{CLKDIV} to Table 37 and Table 38. Updated note 2 in Table 39. Updated units for $T_{SMCKCSO}$ and T_{BPICCO} in Table 47. Updated -1L in Table 71. Removed Note 2: <i>Package delay information is available for these device/package combinations. This information can be used to deskew the package</i> from Table 79.
03/31/11	2.0	Production release of XC6SLX45 in the -1L speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. In Table 39, removed values in the -1L column and added note 3 as IODELAY2 only supports Tap0 for lower-power devices. Updated copyright page 1 and Notice of Disclaimer.
05/20/11	2.1	Production release of XC6SLX100 and XC6SLX150 in the specific speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. Updated Table 27 and Note 7 with changes per XCEN11012: Speed File Change for -3N Devices. Revised Switching Characteristics section for speed specifications: v1.18 for -3, -3N, and -2; including improvements in Table 73 through Table 77 and Table 81. Removed <i>Memory Controller Block</i> from the performance heading in Table 2 and revised Note 2. In Table 4, added Note 1 to C_{IN} and updated the description of R_{IN_TERM}. Updated Note 1 in Table 5. Updated Note 1 of Table 7. In Table 25, added and removed -1L specifications, increased the standard performance DDR3 specifications, removed the extended performance DDR3 row and updated Note 3 and Note 4. Clarified the introductory information for Table 28 and Table 30. In Table 32: Revised V_{MEAS} value for LVCMOS12; revised V_{REF} for LVDS_25, LVDS_33, BLVDS_25, MINI_LVDS_25, MINI_LVDS_33, RSDS_25, and RSDS_33; revised R_{REF} for BLVDS_25 and TMDS_33; and added Note 4 and Note 5. Updated Note 2 and Note 3 in Table 39. In Table 47, revised the values and description of T_{POR} including adding Note 3. Also in Table 47, augmented the description and added specifications for F_{RBCK} and removed XC6SLX4 from F_{MCCK} (maximum frequency, parallel mode (Master SelectMAP/BPI)). Added BUFGMUX to Table 48 title. Added Table 50. In Table 52, revised specifications for $T_{EXTFVAR}$ and $F_{INJITTER}$. In Table 54 removed the 5 MHz < CLKIN_FREQ_DLL parameter in the LOCK_DLL description. In both Table 56 and Table 57, removed the 5 MHz < F_{CLKIN} parameter in the LOCK_FX description. In Table 58, updated description for PSCLK_FREQ and PSCLK_PULSE. Revised title and symbol of Table 70, added new speed specifications for -1L, and added Note 2. Added Table 71.
07/11/11	2.2	Added the Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices to all appropriate tables while sometimes removing the XC6S nomenclature. Added expanded temperature range (Q) to all appropriate tables. Updated T_{SOL} packages in Table 1. Added R_{OUT_TERM} to Table 4. Updated Note 2 on Table 13. Production release of the XC6SLX4, XC6SLX9, XC6SLX16, XC6SLX25, XC6SLX75, XQ6SLX75, and XQ6SLX150 in Table 26 and Table 27 using ISE v13.2 software with -1L speed specification v1.07. Production release of the XA6SLX16, XA6SLX25T, XA6SLX45, XA6SLX45T, XQ6SLX75, XQ6SLX75T, XQ6SLX150, and XQ6SLX150T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices(1). Updated CS(G)484 from CSG484 throughout data sheet. Clarified Note 3 in Table 39.
08/08/11	2.3	Production release of the XA6SLX25, XA6SLX75, and XA6SLX75T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19.