

Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	3411
Number of Logic Elements/Cells	43661
Total RAM Bits	2138112
Number of I/O	296
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xc6slx45t-n3fgg484i">https://www.e-xfl.com/product-detail/xilinx/xc6slx45t-n3fgg484i</a>

## Quiescent Current

Typical values for quiescent supply current are specified at nominal voltage, 25°C junction temperatures ( $T_j$ ). Quiescent supply current is specified by speed grade for Spartan-6 devices. Xilinx recommends analyzing static power consumption using the XPOWER™ Estimator (XPE) tool (download at <http://www.xilinx.com/power>) for conditions other than those specified in Table 5.

*Table 5: Typical Quiescent Supply Current*

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
I <sub>CCINTQ</sub>	Quiescent V <sub>CCINT</sub> supply current	LX4	4.0	4.0	4.0	2.4	mA
		LX9	4.0	4.0	4.0	2.4	mA
		LX16	6.0	6.0	6.0	4.0	mA
		LX25	11.0	11.0	11.0	6.6	mA
		LX25T	11.0	11.0	11.0	N/A	mA
		LX45	15.0	15.0	15.0	9.0	mA
		LX45T	15.0	15.0	15.0	N/A	mA
		LX75	29.0	29.0	29.0	17.4	mA
		LX75T	29.0	29.0	29.0	N/A	mA
		LX100	36.0	36.0	36.0	21.6	mA
		LX100T	36.0	36.0	36.0	N/A	mA
		LX150	51.0	51.0	51.0	31.0	mA
		LX150T	51.0	51.0	51.0	N/A	mA
I <sub>CCOQ</sub>	Quiescent V <sub>CCO</sub> supply current	LX4	1.0	1.0	1.0	1.0	mA
		LX9	1.0	1.0	1.0	1.0	mA
		LX16	2.0	2.0	2.0	2.0	mA
		LX25	2.0	2.0	2.0	2.0	mA
		LX25T	2.0	2.0	2.0	N/A	mA
		LX45	3.0	3.0	3.0	3.0	mA
		LX45T	3.0	3.0	3.0	N/A	mA
		LX75	4.0	4.0	4.0	4.0	mA
		LX75T	4.0	4.0	4.0	N/A	mA
		LX100	5.0	5.0	5.0	5.0	mA
		LX100T	5.0	5.0	5.0	N/A	mA
		LX150	7.0	7.0	7.0	7.0	mA
		LX150T	7.0	7.0	7.0	N/A	mA

Table 5: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
I <sub>CCAUXQ</sub>	Quiescent V <sub>CCAUX</sub> supply current	LX4	2.5	2.5	2.5	2.5	mA
		LX9	2.5	2.5	2.5	2.5	mA
		LX16	3.0	3.0	3.0	3.0	mA
		LX25	4.0	4.0	4.0	4.0	mA
		LX25T	4.0	4.0	4.0	N/A	mA
		LX45	5.0	5.0	5.0	5.0	mA
		LX45T	5.0	5.0	5.0	N/A	mA
		LX75	7.0	7.0	7.0	7.0	mA
		LX75T	7.0	7.0	7.0	N/A	mA
		LX100	9.0	9.0	9.0	9.0	mA
		LX100T	9.0	9.0	9.0	N/A	mA
		LX150	12.0	12.0	12.0	12.0	mA
		LX150T	12.0	12.0	12.0	N/A	mA

**Notes:**

1. Typical values are specified at nominal voltage, 25°C junction temperatures (T<sub>j</sub>). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 25°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. Nominal V<sub>CCINT</sub> is 1.20V; use the XPE tool to calculate 1.23V values for the nominal V<sub>CCINT</sub> of the extended performance range.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 6: Power Supply Ramp Time

Symbol	Description	Speed Grade	Ramp Time	Units
V <sub>CCINTR</sub>	Internal supply voltage ramp time	-3, -3N, -2	0.20 to 50.0	ms
		-1L	0.20 to 40.0	ms
V <sub>CCO2</sub> <sup>(1)</sup>	Output drivers bank 2 supply voltage ramp time	All	0.20 to 50.0	ms
V <sub>CCAUXR</sub>	Auxiliary supply voltage ramp time	All	0.20 to 50.0	ms

**Notes:**

1. The minimum V<sub>CCO2</sub> for power-on reset and configuration is 1.65V.
2. Spartan-6 FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply. Use the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools to estimate current drain on these supplies. Spartan-6 devices do not have a required power-on sequence.

In [Table 9](#) and [Table 10](#), values for  $V_{IL}$  and  $V_{IH}$  are recommended input voltages. Values for  $I_{OL}$  and  $I_{OH}$  are guaranteed over the recommended operating conditions at the  $V_{OL}$  and  $V_{OH}$  test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum  $V_{CCO}$  with the respective  $V_{OL}$  and  $V_{OH}$  voltage levels shown. Other standards are sample tested.

**Table 9: Single-Ended I/O Standard DC Input and Output Levels**

I/O Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTTL	-0.5	0.8	2.0	4.1	0.4	2.4	Note 2	Note 2
LVC MOS33	-0.5	0.8	2.0	4.1	0.4	$V_{CCO} - 0.4$	Note 2	Note 2
LVC MOS25	-0.5	0.7	1.7	4.1	0.4	$V_{CCO} - 0.4$	Note 2	Note 2
LVC MOS18	-0.5	0.38	0.8	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS18 (-1L)	-0.5	0.33	0.71	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS18 JEDEC	-0.5	35% $V_{CCO}$	65% $V_{CCO}$	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS15	-0.5	0.38	0.8	4.1	25% $V_{CCO}$	75% $V_{CCO}$	Note 3	Note 3
LVC MOS15 (-1L)	-0.5	0.33	0.71	4.1	25% $V_{CCO}$	75% $V_{CCO}$	Note 3	Note 3
LVC MOS15 JEDEC	-0.5	35% $V_{CCO}$	65% $V_{CCO}$	4.1	25% $V_{CCO}$	75% $V_{CCO}$	Note 3	Note 3
LVC MOS12	-0.5	0.38	0.8	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
LVC MOS12 (-1L)	-0.5	0.33	0.71	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
LVC MOS12 JEDEC	-0.5	35% $V_{CCO}$	65% $V_{CCO}$	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
PCI33_3	-0.5	30% $V_{CCO}$	50% $V_{CCO}$	$V_{CCO} + 0.5$	10% $V_{CCO}$	90% $V_{CCO}$	1.5	-0.5
PCI66_3	-0.5	30% $V_{CCO}$	50% $V_{CCO}$	$V_{CCO} + 0.5$	10% $V_{CCO}$	90% $V_{CCO}$	1.5	-0.5
I2C	-0.5	25% $V_{CCO}$	70% $V_{CCO}$	4.1	20% $V_{CCO}$	-	3	-
SMBUS	-0.5	0.8	2.1	4.1	0.4	-	4	-
SDIO	-0.5	12.5% $V_{CCO}$	75% $V_{CCO}$	4.1	12.5% $V_{CCO}$	75% $V_{CCO}$	0.1	-0.1
MOBILE_DDR	-0.5	20% $V_{CCO}$	80% $V_{CCO}$	4.1	10% $V_{CCO}$	90% $V_{CCO}$	0.1	-0.1
HSTL_I	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	8	-8
HSTL_II	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	16	-16
HSTL_III	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	24	-8
HSTL_I_18	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	11	-11
HSTL_II_18	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	22	-22
HSTL_III_18	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	30	-11
SSTL3_I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	4.1	$V_{TT} - 0.6$	$V_{TT} + 0.6$	8	-8
SSTL3_II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	4.1	$V_{TT} - 0.8$	$V_{TT} + 0.8$	16	-16
SSTL2_I	-0.5	$V_{REF} - 0.15$	$V_{REF} + 0.15$	4.1	$V_{TT} - 0.61$	$V_{TT} + 0.61$	8.1	-8.1
SSTL2_II	-0.5	$V_{REF} - 0.15$	$V_{REF} + 0.15$	4.1	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	-16.2
SSTL18_I	-0.5	$V_{REF} - 0.125$	$V_{REF} + 0.125$	4.1	$V_{TT} - 0.47$	$V_{TT} + 0.47$	6.7	-6.7
SSTL18_II	-0.5	$V_{REF} - 0.125$	$V_{REF} + 0.125$	4.1	$V_{TT} - 0.60$	$V_{TT} + 0.60$	13.4	-13.4
SSTL15_II	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	$V_{TT} - 0.4$	$V_{TT} + 0.4$	13.4	-13.4

**Notes:**

1. Tested according to relevant specifications.
2. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
3. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
4. Using drive strengths of 2, 4, 6, 8, or 12 mA.
5. For more information, refer to [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 10: Differential I/O Standard DC Input and Output Levels

I/O Standard	V <sub>ID</sub>		V <sub>ICM</sub>		V <sub>OD</sub>		V <sub>OCM</sub>		V <sub>OH</sub>	V <sub>OL</sub>
	mV, Min	mV, Max	V, Min	V, Max	mV, Min	mV, Max	V, Min	V, Max	V, Min	V, Max
LVDS_33 <sup>(2)(3)</sup>	100	600	0.3	2.35	247	454	1.125	1.375	–	–
LVDS_25 <sup>(2)(3)</sup>	100	600	0.3	2.35	247	454	1.125	1.375	–	–
BLVDS_25 <sup>(2)(3)</sup>	100	–	0.3	2.35	240	460	Typical 50% V <sub>CCO</sub>		–	–
MINI_LVDS_33	200	600	0.3	1.95	300	600	1.0	1.4	–	–
MINI_LVDS_25	200	600	0.3	1.95	300	600	1.0	1.4	–	–
LVPECL_33 <sup>(2)(3)</sup>	100	1000	0.3	2.8 <sup>(1)</sup>	Inputs only					
LVPECL_25 <sup>(2)(3)</sup>	100	1000	0.3	1.95	Inputs only					
RSDS_33 <sup>(2)(3)</sup>	100	–	0.3	1.5	100	400	1.0	1.4	–	–
RSDS_25 <sup>(2)(3)</sup>	100	–	0.3	1.5	100	400	1.0	1.4	–	–
TMDS_33	150	1200	2.7	3.23 <sup>(1)</sup>	400	800	V <sub>CCO</sub> – 0.405	V <sub>CCO</sub> – 0.190	–	–
PPDS_33 <sup>(2)(3)</sup>	100	400	0.2	2.3	100	400	0.5	1.4	–	–
PPDS_25 <sup>(2)(3)</sup>	100	400	0.2	2.3	100	400	0.5	1.4	–	–
DISPLAY_PORT	190	1260	0.3	2.35	–	–	Typical 50% V <sub>CCO</sub>		–	–
DIFF_MOBILE_DDR	100	–	0.78	1.02	–	–	–	–	90% V <sub>CCO</sub>	10% V <sub>CCO</sub>
DIFF_HSTL_I	100	–	0.68	0.9	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_HSTL_II	100	–	0.68	0.9	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_HSTL_III	100	–	0.68	0.9	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_HSTL_I_18	100	–	0.8	1.1	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_HSTL_II_18	100	–	0.8	1.1	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_HSTL_III_18	100	–	0.8	1.1	–	–	–	–	V <sub>CCO</sub> – 0.4	0.4
DIFF_SSTL3_I	100	–	1.0	1.9	–	–	–	–	V <sub>TT</sub> + 0.6	V <sub>TT</sub> – 0.6
DIFF_SSTL3_II	100	–	1.0	1.9	–	–	–	–	V <sub>TT</sub> + 0.8	V <sub>TT</sub> – 0.8
DIFF_SSTL2_I	100	–	1.0	1.5	–	–	–	–	V <sub>TT</sub> + 0.61	V <sub>TT</sub> – 0.61
DIFF_SSTL2_II	100	–	1.0	1.5	–	–	–	–	V <sub>TT</sub> + 0.81	V <sub>TT</sub> – 0.81
DIFF_SSTL18_I	100	–	0.7	1.1	–	–	–	–	V <sub>TT</sub> + 0.47	V <sub>TT</sub> – 0.47
DIFF_SSTL18_II	100	–	0.7	1.1	–	–	–	–	V <sub>TT</sub> + 0.6	V <sub>TT</sub> – 0.6
DIFF_SSTL15_II	100	–	0.55	0.95	–	–	–	–	V <sub>TT</sub> + 0.4	V <sub>TT</sub> – 0.4

**Notes:**

1. LVPECL\_33 and TMDS\_33 maximum V<sub>ICM</sub> is the lower of V (maximum) or V<sub>CCAUX</sub> – (V<sub>ID</sub>/2)
2. When V<sub>CCAUX</sub> = 3.3V, the DCD can be higher than 5% for V<sub>ICM</sub> < 0.7V when using these I/O standards: LVDS\_25, LVDS\_33, BLVDS\_25, LVPECL\_25, LVPECL\_33, RSDS\_25, RSDS\_33, PPDS\_25, and PPDS\_33.
3. The -1L devices require V<sub>CCAUX</sub> = 2.5V when using the LVDS\_25, LVDS\_33, BLVDS\_25, LVPECL\_25, RSDS\_25, RSDS\_33, PPDS\_25, and PPDS\_33 I/O standards on inputs. LVPECL\_33 is not supported in the -1L devices.

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [Switching Characteristics, page 19](#).

Table 25: Interface Performances

Description	I/O Resource	Clock Buffer	Data Width	Speed Grade				Units
				-3	-3N	-2	-1L	
<b>Networking Applications<sup>(1)</sup></b>								
SDR LVDS transmitter or receiver	IOB SDR register	BUFG	–	400	400	375	250	Mb/s
DDR LVDS transmitter or receiver	ODDR2/IDDR2 register	2 BUFGs	–	800	800	750	500	Mb/s
SDR LVDS transmitter	OSERDES2	BUFPLL	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
DDR LVDS transmitter	OSERDES2	2 BUFIO2s	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
SDR LVDS receiver	ISERDES2 in RETIMED mode	BUFPLL	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
DDR LVDS receiver	ISERDES2 in RETIMED mode	2 BUFIO2s	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
<b>Memory Interfaces (Implemented using the Spartan-6 FPGA Memory Controller Block)<sup>(2)</sup></b>								
<b>Standard Performance (Standard V<sub>CCINT</sub>)</b>								
DDR				400	<a href="#">Note 4</a>	400	350	Mb/s
DDR2				667	<a href="#">Note 4</a>	625	400	Mb/s
DDR3				800	<a href="#">Note 4</a>	667	—	Mb/s
LPDDR (Mobile_DDR)				400	<a href="#">Note 4</a>	400	350	Mb/s
<b>Extended Performance (Requires Extended Performance V<sub>CCINT</sub>)<sup>(3)</sup></b>								
DDR2				800	<a href="#">Note 4</a>	667	—	Mb/s

**Notes:**

1. Refer to [XAPP1064](#), *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)* and [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.
2. Refer to [UG388](#), *Spartan-6 FPGA Memory Controller User Guide*.
3. Extended Memory Controller block performance for DDR2 can be achieved using the extended performance V<sub>CCINT</sub> range from [Table 2](#).
4. The LX4 device, all devices in the TQG144 and CPG196 packages, and the -3N speed grade do not support a Memory Controller Block.

## Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.20 for -3, -3N, and -2; and v1.08 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

### Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

The -1L speed grade refers to the lower-power Spartan-6 devices. The -3N speed grade refers to the Spartan-6 devices that do not support MCB functionality.

[Table 26](#) correlates the current status of each Spartan-6 device on a per speed grade basis.

## Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-6 devices.

Table 26: Spartan-6 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6SLX4 <sup>(1)</sup>			-3, -2, -1L
XC6SLX9			-3, -3N, -2, -1L
XC6SLX16			-3, -3N, -2, -1L
XC6SLX25			-3, -3N, -2, -1L
XC6SLX25T			-3, -3N, -2
XC6SLX45			-3, -3N, -2, -1L
XC6SLX45T			-3, -3N, -2
XC6SLX75			-3, -3N, -2, -1L
XC6SLX75T			-3, -3N, -2
XC6SLX100			-3, -3N, -2, -1L
XC6SLX100T			-3, -3N, -2
XC6SLX150			-3, -3N, -2, -1L
XC6SLX150T			-3, -3N, -2
XA6SLX4			-3, -2
XA6SLX9			-3, -2
XA6SLX16			-3, -2
XA6SLX25			-3, -2
XA6SLX25T			-3, -2
XA6SLX45			-3, -2
XA6SLX45T			-3, -2
XA6SLX75			-3, -2
XA6SLX75T			-3, -2
XA6SLX100			-2
XQ6SLX75			-2, -1L
XQ6SLX75T			-3, -2
XQ6SLX150			-2, -1L
XQ6SLX150T			-3, -2

### Notes:

1. The XC6SLX4 is not available in the -3N speed grade.

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T <sub>IOPI</sub>				T <sub>IOOP</sub>				T <sub>IOTP</sub>				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	
PPDS_33	1.17	1.29	1.42	1.68	1.57	1.71	1.91	2.43	3000	3000	3000	3000	ns
PPDS_25	1.01	1.13	1.26	1.56	1.68	1.82	2.02	2.47	3000	3000	3000	3000	ns
PCI33_3	1.07	1.19	1.32	1.57 <sup>(2)</sup>	3.51	3.65	3.85	4.38 <sup>(2)</sup>	3.51	3.65	3.85	4.38 <sup>(1)</sup>	ns
PCI66_3	1.07	1.19	1.32	1.57 <sup>(2)</sup>	3.53	3.67	3.87	4.39 <sup>(2)</sup>	3.53	3.67	3.87	4.39 <sup>(1)</sup>	ns
DISPLAY_PORT	1.02	1.14	1.27	1.56	3.15	3.29	3.49	4.08	3.15	3.29	3.49	4.08	ns
I2C	1.33	1.45	1.58	1.82	11.56	11.70	11.90	12.52	11.56	11.70	11.90	12.52	ns
SMBUS	1.33	1.45	1.58	1.82	11.56	11.70	11.90	12.52	11.56	11.70	11.90	12.52	ns
SDIO	1.36	1.48	1.61	1.84	2.64	2.78	2.98	3.60	2.64	2.78	2.98	3.60	ns
MOBILE_DDR	0.94	1.06	1.19	1.43	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns
HSTL_I	0.90	1.02	1.15	1.39	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
HSTL_II	0.91	1.03	1.16	1.40	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
HSTL_III	0.95	1.07	1.20	1.44	1.67	1.81	2.01	2.61	1.67	1.81	2.01	2.61	ns
HSTL_I_18	0.94	1.06	1.19	1.43	1.77	1.91	2.11	2.73	1.77	1.91	2.11	2.73	ns
HSTL_II_18	0.94	1.06	1.19	1.43	1.85	1.99	2.19	2.81	1.85	1.99	2.19	2.81	ns
HSTL_III_18	0.99	1.11	1.24	1.47	1.79	1.93	2.13	2.72	1.79	1.93	2.13	2.72	ns
SSTL3_I	1.58	1.70	1.83	2.16	1.83	1.97	2.17	2.72	1.83	1.97	2.17	2.72	ns
SSTL3_II	1.58	1.70	1.83	2.16	2.01	2.15	2.35	2.94	2.01	2.15	2.35	2.94	ns
SSTL2_I	1.30	1.42	1.55	1.87	1.77	1.91	2.11	2.69	1.77	1.91	2.11	2.69	ns
SSTL2_II	1.30	1.42	1.55	1.88	1.86	2.00	2.20	2.82	1.86	2.00	2.20	2.82	ns
SSTL18_I	0.92	1.04	1.17	1.41	1.63	1.77	1.97	2.59	1.63	1.77	1.97	2.59	ns
SSTL18_II	0.92	1.04	1.17	1.41	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
SSTL15_II	0.92	1.04	1.17	1.41	1.67	1.81	2.01	2.63	1.67	1.81	2.01	2.63	ns
DIFF_HSTL_I	0.94	1.06	1.19	1.46	1.77	1.91	2.11	2.62	1.77	1.91	2.11	2.62	ns
DIFF_HSTL_II	0.93	1.05	1.18	1.45	1.72	1.86	2.06	2.54	1.72	1.86	2.06	2.54	ns
DIFF_HSTL_III	0.93	1.05	1.18	1.46	1.69	1.83	2.03	2.53	1.69	1.83	2.03	2.53	ns
DIFF_HSTL_I_18	0.97	1.09	1.22	1.50	1.79	1.93	2.13	2.63	1.79	1.93	2.13	2.63	ns
DIFF_HSTL_II_18	0.97	1.09	1.22	1.49	1.69	1.83	2.03	2.51	1.69	1.83	2.03	2.51	ns
DIFF_HSTL_III_18	0.97	1.09	1.22	1.50	1.69	1.83	2.03	2.53	1.69	1.83	2.03	2.53	ns
DIFF_SSTL3_I	1.18	1.30	1.43	1.68	1.81	1.95	2.15	2.64	1.81	1.95	2.15	2.64	ns
DIFF_SSTL3_II	1.19	1.31	1.44	1.68	1.80	1.94	2.14	2.63	1.80	1.94	2.14	2.63	ns
DIFF_SSTL2_I	1.02	1.14	1.27	1.57	1.80	1.94	2.14	2.62	1.80	1.94	2.14	2.62	ns
DIFF_SSTL2_II	1.02	1.14	1.27	1.57	1.76	1.90	2.10	2.57	1.76	1.90	2.10	2.57	ns
DIFF_SSTL18_I	0.97	1.09	1.22	1.51	1.72	1.86	2.06	2.56	1.72	1.86	2.06	2.56	ns
DIFF_SSTL18_II	0.98	1.10	1.23	1.50	1.68	1.82	2.02	2.52	1.68	1.82	2.02	2.52	ns
DIFF_SSTL15_II	0.94	1.06	1.19	1.46	1.67	1.81	2.01	2.50	1.67	1.81	2.01	2.50	ns
DIFF_MOBILE_DDR	0.97	1.09	1.22	1.51	1.75	1.89	2.09	2.57	1.75	1.89	2.09	2.57	ns



### Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 4 and Figure 5.

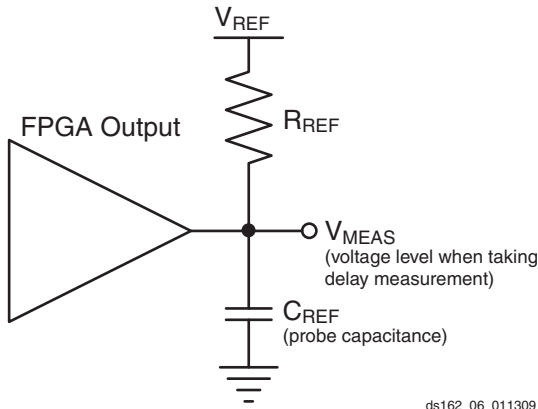


Figure 4: Single-Ended Test Setup

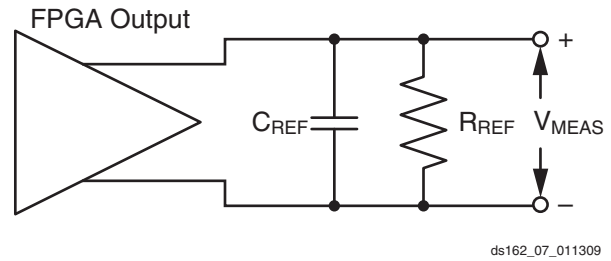


Figure 5: Differential Test Setup

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters  $V_{REF}$ ,  $R_{REF}$ ,  $C_{REF}$ , and  $V_{MEAS}$  fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 32.
2. Record the time to  $V_{MEAS}$ .
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to  $V_{MEAS}$ .
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 32: Output Delay Measurement Methodology

Description	I/O Standard Attribute	$R_{REF}$ ( $\Omega$ )	$C_{REF}^{(1)}$ (pF)	$V_{MEAS}$ (V)	$V_{REF}$ (V)
LVTTTL (Low-Voltage Transistor-Transistor Logic)	LVTTTL (all)	1M	0	1.4	0
LVC MOS (Low-Voltage CMOS), 3.3V	LVC MOS33	1M	0	1.65	0
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS, 1.2V	LVC MOS12	1M	0	0.6	0
PCI (Peripheral Component Interface) 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3 (rising edge)	25	10 <sup>(2)</sup>	0.94	0
	PCI33_3, PCI66_3 (falling edge)	25	10 <sup>(2)</sup>	2.03	3.3
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	$V_{REF}$	0.75
HSTL, Class II	HSTL_II	25	0	$V_{REF}$	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	$V_{REF}$	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	$V_{REF}$	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	$V_{REF}$	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	$V_{REF}$	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	$V_{REF}$	1.25

Table 32: Output Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	R <sub>REF</sub> (Ω)	C <sub>REF</sub> <sup>(1)</sup> (pF)	V <sub>MEAS</sub> (V)	V <sub>REF</sub> (V)
SSTL, Class II, 2.5V	SSTL2_II	25	0	V <sub>REF</sub>	1.25
SSTL, Class II, 1.5V	SSTL15_II	25	0	V <sub>REF</sub>	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	100	0	0 <sup>(3)</sup>	–
BLVDS (Bus LVDS), 2.5V	BLVDS_25	Note 4	0	0 <sup>(3)</sup>	–
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	100	0	0 <sup>(3)</sup>	–
RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RSDS_25, RSDS_33	100	0	0 <sup>(3)</sup>	–
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	Note 5	0	0 <sup>(3)</sup>	–
PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V	PPDS_25, PPDS_33	100	0	0 <sup>(3)</sup>	–

**Notes:**

1. C<sub>REF</sub> is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. The value given is the differential output voltage.
4. See the *BLVDS Output Termination* section in [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.
5. See the *TMDS\_33 Termination* section in [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.

## Simultaneously Switching Outputs

Due to package electrical parasitics, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. [Table 33](#) and [Table 34](#) provide guidelines for the recommended maximum allowable number of SSOs. These guidelines describe the maximum number of user I/O pins of an output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise for that particular signal standard. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of GND and power bounce.

For each device/package combination, [Table 33](#) provides the number of equivalent V<sub>CCO</sub>/GND pairs per bank. For each output signal standard and drive strength, [Table 34](#) recommends the maximum number of SSOs, switching in the same direction, allowed per V<sub>CCO</sub>/GND pair within an I/O bank. The guidelines are categorized by package style, slew rate, and output drive current. The number of SSOs are also specified by I/O bank. Multiply the appropriate numbers from each table to calculate the maximum number of SSOs allowed within an I/O bank. The guidelines assume that all pins within a bank use the same I/O standard. Exceeding these SSO guidelines can result in increased power or GND bounce, degraded signal integrity, or increased system jitter. For a given I/O standard, if the SSO limit per pair in [Table 34](#) is greater than the maximum I/O per pair in [Table 33](#), then there is no SSO limit for the exclusive use of that I/O standard.

The recommended maximum SSO values assume that the FPGA is soldered on a printed circuit board and that the board uses sound design practices. Due to the additional inductance introduced by the socket, the SSO values do not apply for FPGAs mounted in sockets. The SSO values assume that the V<sub>CCAUX</sub> is powered at 3.3V. Setting V<sub>CCAUX</sub> to 2.5V provides better SSO characteristics. For more detail, see [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 34: SSO Limit per V<sub>CC0</sub>/GND Pair (Cont'd)

V <sub>CC0</sub>	I/O Standard	Drive	Slew	SSO Limit per V <sub>CC0</sub> /GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
3.3V	LVCMOS33	2	Fast	42	46	42	44
			Slow	50	55	50	49
			QuietIO	60	68	60	60
		4	Fast	21	27	21	25
			Slow	32	37	32	32
			QuietIO	39	42	39	37
		6	Fast	14	19	14	17
			Slow	19	25	19	22
			QuietIO	29	30	29	25
		8	Fast	11	15	11	14
			Slow	15	20	15	18
			QuietIO	25	24	25	20
		12	Fast	1	3	1	1
			Slow	2	5	2	2
			QuietIO	4	9	4	7
		16	Fast	1	2	1	1
			Slow	1	5	1	1
			QuietIO	3	10	3	8
		24	Fast	1	2	1	1
			Slow	2	5	2	1
			QuietIO	7	9	7	7

## Input Serializer/Deserializer Switching Characteristics

Table 37: ISERDES2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
<b>Setup/Hold for Control Lines</b>						
$T_{ISCK\_BITSLIP} / T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.16/ -0.09	0.20/ -0.09	0.31/ -0.09	0.34/ -0.14	ns
$T_{ISCK\_CE} / T_{ISCKC\_CE}$	CE pin Setup/Hold with respect to CLK	0.71/ -0.47	0.71/ -0.42	0.97/ -0.42	1.39/ -0.71	ns
<b>Setup/Hold for Data Lines</b>						
$T_{ISDCK\_D} / T_{ISCKD\_D}$	D pin Setup/Hold with respect to CLK	0.24/ -0.15	0.25/ -0.05	0.29/ -0.05	0.09/ -0.05	ns
$T_{ISDCK\_DDL} / T_{ISCKD\_DDL}$	DDL pin Setup/Hold with respect to CLK (using IODELAY2)	-0.25/ 0.30	-0.25/ 0.42	-0.25/ 0.56	-0.54/ 0.67	ns
$T_{ISDCK\_D\_DDR} / T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	-0.03/ 0.04	-0.03/ 0.16	-0.03/ 0.18	-0.05/ 0.12	ns
$T_{ISDCK\_DDL\_DDR} / T_{ISCKD\_DDL\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY2)	-0.40/ 0.48	-0.40/ 0.53	-0.40/ 0.71	-0.71/ 0.86	ns
<b>Sequential Delays</b>						
$T_{ISCKO\_Q}$	CLKDIV to out at Q pin	1.30	1.44	2.02	2.22	ns
$F_{CLKDIV}$	CLKDIV maximum frequency	270	262.5	250	125	MHz

## Output Serializer/Deserializer Switching Characteristics

Table 38: OSERDES2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
<b>Setup/Hold</b>						
$T_{OSDCK\_D} / T_{OSCKD\_D}$	D input Setup/Hold with respect to CLKDIV	-0.03/ 1.02	-0.03/ 1.17	-0.03/ 1.27	-0.02/ 0.23	ns
$T_{OSDCK\_T} / T_{OSCKD\_T}^{(1)}$	T input Setup/Hold with respect to CLK	-0.05/ 1.03	-0.05/ 1.13	-0.05/ 1.23	-0.05/ 0.24	ns
$T_{OSCK\_OCE} / T_{OSCKC\_OCE}$	OCE input Setup/Hold with respect to CLK	0.12/ -0.03	0.15/ -0.03	0.24/ -0.03	0.28/ -0.17	ns
$T_{OSCK\_TCE} / T_{OSCKC\_TCE}$	TCE input Setup/Hold with respect to CLK	0.14/ -0.08	0.17/ -0.08	0.27/ -0.08	0.31/ -0.16	ns
<b>Sequential Delays</b>						
$T_{OSCKO\_OQ}$	Clock to out from CLK to OQ	0.94	1.11	1.51	1.89	ns
$T_{OSCKO\_TQ}$	Clock to out from CLK to TQ	0.94	1.11	1.51	1.91	ns
$F_{CLKDIV}$	CLKDIV maximum frequency	270	262.5	250	125	MHz

**Notes:**

- $T_{OSDCK\_T2} / T_{OSCKD\_T2}$  (T input setup/hold with respect to CLKDIV) are reported as  $T_{OSDCK\_T} / T_{OSCKD\_T}$  in TRACE report.

## Input/Output Delay Switching Characteristics

Table 39: IODELAY2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L <sup>(3)</sup>	
$T_{IODCCK\_CAL} / T_{IODCKC\_CAL}$	CAL pin Setup/Hold with respect to CK	0.28/ -0.13	0.33/ -0.13	0.48/ -0.13	N/A	ns
$T_{IODCCK\_CE} / T_{IODCKC\_CE}$	CE pin Setup/Hold with respect to CK	0.17/ -0.03	0.17/ -0.03	0.25/ -0.02	N/A	ns
$T_{IODCCK\_INC} / T_{IODCKC\_INC}$	INC pin Setup/Hold with respect to CK	0.10/ 0.02	0.12/ 0.03	0.18/ 0.06	N/A	ns
$T_{IODCCK\_RST} / T_{IODCKC\_RST}$	RST pin Setup/Hold with respect to CK	0.12/ -0.02	0.15/ -0.02	0.22/ -0.01	N/A	ns
$T_{TAP1}^{(2)}$	Maximum tap 1 delay	8	14	16	N/A	ps
$T_{TAP2}$	Maximum tap 2 delay	40	66	77	N/A	ps
$T_{TAP3}$	Maximum tap 3 delay	95	120	140	N/A	ps
$T_{TAP4}$	Maximum tap 4 delay	108	141	166	N/A	ps
$T_{TAP5}$	Maximum tap 5 delay	171	194	231	N/A	ps
$T_{TAP6}$	Maximum tap 6 delay	207	249	292	N/A	ps
$T_{TAP7}$	Maximum tap 7 delay	212	276	343	N/A	ps
$T_{TAP8}$	Maximum tap 8 delay	322	341	424	N/A	ps
$F_{MINCAL}$	Minimum allowed bit rate for calibration in variable mode: VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX, and DIFF_PHASE_DETECTOR.	188	188	188	N/A	Mb/s
$T_{IODDO\_IDATAIN}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	-
$T_{IODDO\_ODATAIN}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	-

**Notes:**

1. Delay depends on IODELAY2 tap setting. See TRACE report for actual values.
2. Maximum delay = integer (number of taps/8) ×  $T_{TAP8}$  +  $T_{TAPn}$  (where n equals the remainder). For minimum delay consult the TRACE setup and hold report. Minimum delay is typically greater than 30% of the maximum delay. Tap delays can vary by device and overall conditions. See TRACE report for actual values.
3. Spartan-6 -1L devices only support tap 0. See TRACE report for actual values.

Table 45: Device DNA Interface Port Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T <sub>DNASSU</sub>	Setup time on SHIFT before the rising edge of CLK	7				ns, Min
T <sub>DNASH</sub>	Hold time on SHIFT after the rising edge of CLK	1				ns, Min
T <sub>DNADSU</sub>	Setup time on DIN before the rising edge of CLK	7				ns, Min
T <sub>DNADH</sub>	Hold time on DIN after the rising edge of CLK	1				ns, Min
T <sub>DNARSU</sub>	Setup time on READ before the rising edge of CLK	7				ns, Min
		1,000				ns, Max
T <sub>DNARH</sub>	Hold time on READ after the rising edge of CLK	1				ns, Min
T <sub>DNADCKO</sub>	Clock-to-output delay on DOUT after rising edge of CLK	0.5				ns, Min
		6				ns, Max
T <sub>DNACLKF</sub> <sup>(2)</sup>	CLK frequency	2				MHz, Max
T <sub>DNACLKL</sub>	CLK Low time	50				ns, Min
T <sub>DNACLKH</sub>	CLK High time	50				ns, Min

**Notes:**

1. The minimum READ pulse width is 8 ns, the maximum READ pulse width is 1 μs.
2. Also applies to TCK when reading DNA through the boundary-scan port.

Table 46: Suspend Mode Switching Characteristics

Symbol	Description	Min	Max	Units
<b>Entering Suspend Mode</b>				
T <sub>SUSPENDHIGH_AWAKE</sub>	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter	2.5	14	ns
T <sub>SUSPENDFILTER</sub>	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled	31	430	ns
T <sub>SUSPEND_GWE</sub>	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior (without glitch filter)	–	15	ns
T <sub>SUSPEND_GTS</sub>	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements (without glitch filter)	–	15	ns
T <sub>SUSPEND_DISABLE</sub>	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled (without glitch filter)	–	1500	ns
<b>Exiting Suspend Mode</b>				
T <sub>SUSPENDLOW_AWAKE</sub>	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM or PLL lock time.	7	75	μs
T <sub>SUSPEND_ENABLE</sub>	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	7	41	μs
T <sub>AWAKE_GWE1</sub>	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using <b>sw_clk:InternalClock</b> and <b>sw_gwe_cycle:1</b> .	–	80	ns
T <sub>AWAKE_GWE512</sub>	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using <b>sw_clk:InternalClock</b> and <b>sw_gwe_cycle:512</b> .	–	20.5	μs
T <sub>AWAKE_GTS1</sub>	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using <b>sw_clk:InternalClock</b> and <b>sw_gts_cycle:1</b> .	–	80	ns
T <sub>AWAKE_GTS512</sub>	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using <b>sw_clk:InternalClock</b> and <b>sw_gts_cycle:512</b> .	–	20.5	μs
T <sub>SCP_AWAKE</sub>	Rising edge of SCP pins to rising edge of AWAKE pin	7	75	μs

Table 57: Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM\_CLKGEN)<sup>(1)</sup> (Cont'd)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
<b>Spread Spectrum</b>										
F <sub>CLKIN_FIXED_SPREAD_SPECTRUM</sub>	Frequency of the CLKIN input for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD/ CENTER_HIGH_SPREAD)	30	200	30	200	30	200	30	200	MHz
T <sub>CENTER_LOW_SPREAD</sub> <sup>(6)</sup>	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD)	Typical = $\frac{100}{\text{CLKFX\_DIVIDE}}$ Maximum = 250								ps
T <sub>CENTER_HIGH_SPREAD</sub> <sup>(6)</sup>	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_HIGH_SPREAD)	Typical = $\frac{240}{\text{CLKFX\_DIVIDE}}$ Maximum = 400								ps
F <sub>MOD_FIXED_SPREAD_SPECTRUM</sub> <sup>(6)</sup>	Average modulation frequency when using fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD / CENTER_HIGH_SPREAD)	Typical = F <sub>IN</sub> /1024								MHz

**Notes:**

1. The values in this table are based on the operating conditions described in Table 2 and Table 55.
2. For optimal jitter tolerance and a faster LOCK time, use the CLKIN\_PERIOD attribute.
3. Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
5. Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.
6. When using CENTER\_LOW\_SPREAD, CENTER\_HIGH\_SPREAD, the valid values for CLKFX\_MULTIPLY are limited to 2 through 32, and the valid values for CLKFX\_DIVIDE are limited to 1 through 4.

Table 58: Recommended Operating Conditions for the Phase-Shift Clock in Variable Phase Mode (DCM\_SP) or Dynamic Frequency Synthesis (DCM\_CLKGEN)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
<b>Operating Frequency Ranges</b>										
PSCLK_FREQ	Frequency for the PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) input.	1	167	1	167	1	167	1	100	MHz
<b>Input Pulse Requirements</b>										
PSCLK_PULSE	PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) pulse width as a percentage of the clock period.	40	60	40	60	40	60	40	60	%

## Spartan-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in [Table 63](#) through [Table 69](#). Values are expressed in nanoseconds unless otherwise noted.

**Table 63: Global Clock Input to Output Delay Without DCM or PLL**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>without</i> DCM or PLL							
T <sub>ICKOF</sub>	Global Clock and OUTFF <i>without</i> DCM or PLL	XC6SLX4	6.12	N/A	7.68	9.41	ns
		XC6SLX9	6.12	6.51	7.68	9.41	ns
		XC6SLX16	5.98	6.42	7.48	9.10	ns
		XC6SLX25	6.20	6.69	7.84	9.44	ns
		XC6SLX25T	6.20	6.69	7.84	N/A	ns
		XC6SLX45	6.37	6.88	8.10	9.61	ns
		XC6SLX45T	6.37	6.88	8.10	N/A	ns
		XC6SLX75	6.39	6.99	8.16	10.18	ns
		XC6SLX75T	6.39	6.99	8.16	N/A	ns
		XC6SLX100	6.59	7.18	8.41	10.31	ns
		XC6SLX100T	6.59	7.18	8.41	N/A	ns
		XC6SLX150	6.98	7.68	8.80	10.62	ns
		XC6SLX150T	6.98	7.68	8.80	N/A	ns
		XA6SLX4	6.44	N/A	7.68	N/A	ns
		XA6SLX9	6.44	N/A	7.68	N/A	ns
		XA6SLX16	6.30	N/A	7.48	N/A	ns
		XA6SLX25	6.52	N/A	7.84	N/A	ns
		XA6SLX25T	6.52	N/A	7.84	N/A	ns
		XA6SLX45	6.69	N/A	8.12	N/A	ns
		XA6SLX45T	6.69	N/A	8.12	N/A	ns
		XA6SLX75	6.89	N/A	8.16	N/A	ns
		XA6SLX75T	6.89	N/A	8.16	N/A	ns
		XA6SLX100	N/A	N/A	8.36	N/A	ns
XQ6SLX75	N/A	N/A	8.16	10.18	ns		
XQ6SLX75T	6.89	N/A	8.16	N/A	ns		
XQ6SLX150	N/A	N/A	8.80	10.62	ns		
XQ6SLX150T	7.61	N/A	8.80	N/A	ns		

**Notes:**

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.



Table 69: Global Clock Input to Output Delay With DCM and PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode.							
T <sub>ICKOFDCM0_PLL</sub>	Global Clock and OUTFF with DCM and PLL	XC6SLX4	5.58	N/A	7.42	8.54	ns
		XC6SLX9	5.58	6.19	7.42	8.54	ns
		XC6SLX16	5.50	6.06	7.05	8.24	ns
		XC6SLX25	5.57	6.04	7.02	8.33	ns
		XC6SLX25T	5.57	6.04	7.02	N/A	ns
		XC6SLX45	5.53	5.97	6.96	8.32	ns
		XC6SLX45T	5.53	5.97	6.96	N/A	ns
		XC6SLX75	5.55	6.00	6.99	8.54	ns
		XC6SLX75T	5.55	6.00	6.99	N/A	ns
		XC6SLX100	5.58	6.03	7.02	9.11	ns
		XC6SLX100T	5.62	6.03	7.02	N/A	ns
		XC6SLX150	5.32	5.70	6.41	8.26	ns
		XC6SLX150T	5.32	5.70	6.41	N/A	ns
		XA6SLX4	5.87	N/A	7.28	N/A	ns
		XA6SLX9	5.87	N/A	7.28	N/A	ns
		XA6SLX16	6.02	N/A	6.87	N/A	ns
		XA6SLX25	5.88	N/A	6.90	N/A	ns
		XA6SLX25T	5.88	N/A	7.00	N/A	ns
		XA6SLX45	5.82	N/A	6.81	N/A	ns
		XA6SLX45T	5.82	N/A	6.81	N/A	ns
		XA6SLX75	5.81	N/A	6.80	N/A	ns
		XA6SLX75T	5.81	N/A	6.80	N/A	ns
		XA6SLX100	N/A	N/A	6.88	N/A	ns
		XQ6SLX75	N/A	N/A	6.80	8.54	ns
XQ6SLX75T	5.81	N/A	6.80	N/A	ns		
XQ6SLX150	N/A	N/A	6.41	8.26	ns		
XQ6SLX150T	5.90	N/A	6.41	N/A	ns		

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 72: Global Clock Setup and Hold With DCM in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
<b>Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.<sup>(1)</sup></b>							
T <sub>PSDCM</sub> / T <sub>PHDCM</sub>	No Delay Global Clock and IFF <sup>(2)</sup> with DCM in System-Synchronous Mode	XC6SLX4	1.54/0.06	N/A	1.75/0.12	2.84/0.27	ns
		XC6SLX9	1.54/0.06	1.63/0.12	1.75/0.12	2.84/0.27	ns
		XC6SLX16	1.72/-0.18	1.87/-0.17	2.13/-0.17	2.31/0.26	ns
		XC6SLX25	1.70/-0.03	1.78/-0.02	2.00/-0.02	2.88/0.20	ns
		XC6SLX25T	1.70/0.07	1.78/0.08	2.00/0.08	N/A	ns
		XC6SLX45	1.74/-0.03	1.84/-0.02	2.02/-0.02	2.64/0.52	ns
		XC6SLX45T	1.74/-0.01	1.84/0.00	2.02/0.00	N/A	ns
		XC6SLX75	1.86/0.11	1.98/0.12	2.20/0.12	2.96/0.58	ns
		XC6SLX75T	1.86/0.11	1.98/0.12	2.20/0.12	N/A	ns
		XC6SLX100	1.64/0.07	1.72/0.08	1.97/0.08	2.70/0.99	ns
		XC6SLX100T	1.64/0.09	1.72/0.10	1.97/0.10	N/A	ns
		XC6SLX150	1.53/0.39	1.62/0.40	1.82/0.40	2.75/1.00	ns
		XC6SLX150T	1.53/0.39	1.62/0.40	1.82/0.40	N/A	ns
		XA6SLX4	1.65/0.16	N/A	1.75/0.26	N/A	ns
		XA6SLX9	1.65/0.16	N/A	1.75/0.26	N/A	ns
		XA6SLX16	1.88/0.02	N/A	2.13/0.03	N/A	ns
		XA6SLX25	1.80/0.16	N/A	2.05/0.17	N/A	ns
		XA6SLX25T	1.80/0.16	N/A	2.13/0.17	N/A	ns
		XA6SLX45	1.75/0.12	N/A	2.02/0.13	N/A	ns
		XA6SLX45T	1.75/0.12	N/A	2.02/0.13	N/A	ns
		XA6SLX75	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XA6SLX75T	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XA6SLX100	N/A	N/A	2.46/0.24	N/A	ns
		XQ6SLX75	N/A	N/A	2.20/0.12	2.96/0.58	ns
		XQ6SLX75T	1.87/0.11	N/A	2.20/0.12	N/A	ns
		XQ6SLX150	N/A	N/A	1.82/0.56	2.75/1.00	ns
XQ6SLX150T	1.65/0.55	N/A	1.82/0.56	N/A	ns		

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

## Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Spartan-6 FPGA source-synchronous transmitter and receiver data-valid windows.

Table 78: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device <sup>(1)</sup>	Speed Grade				Units
			-3	-3N	-2	-1L	
T <sub>DCD_CLK</sub>	Global Clock Tree Duty Cycle Distortion <sup>(2)</sup>	LX4	0.20	N/A	0.20	0.35	ns
		LX9	0.20	0.20	0.20	0.35	ns
		LX16	0.20	0.20	0.20	0.35	ns
		LX25	0.20	0.20	0.20	0.35	ns
		LX25T	0.20	0.20	0.20	N/A	ns
		LX45	0.20	0.20	0.20	0.35	ns
		LX45T	0.20	0.20	0.20	N/A	ns
		LX75	0.20	0.20	0.20	0.35	ns
		LX75T	0.20	0.20	0.20	N/A	ns
		LX100	0.20	0.20	0.20	0.35	ns
		LX100T	0.20	0.20	0.20	N/A	ns
		LX150	0.35	0.35	0.35	0.35	ns
		LX150T	0.35	0.35	0.35	N/A	ns
T <sub>CKSKEW</sub>	Global Clock Tree Skew <sup>(3)</sup>	LX4	0.25	N/A	0.25	0.29	ns
		LX9	0.25	0.25	0.25	0.29	ns
		LX16	0.15	0.15	0.15	0.22	ns
		LX25	0.26	0.26	0.26	0.41	ns
		LX25T	0.26	0.26	0.26	N/A	ns
		LX45	0.20	0.20	0.20	0.28	ns
		LX45T	0.20	0.20	0.20	N/A	ns
		LX75	0.56	0.56	0.56	0.50	ns
		LX75T	0.56	0.56	0.56	N/A	ns
		XC6SLX100 <sup>(4)</sup>	0.22	0.22	0.22	0.21	ns
		XA6SLX100 <sup>(4)</sup>	N/A	N/A	0.43	N/A	ns
		LX100T	0.22	0.22	0.22	N/A	ns
		LX150	0.48	0.48	0.48	0.35	ns
LX150T	0.48	0.48	0.48	N/A	ns		
T <sub>DCD_BUFIO2</sub>	I/O clock tree duty cycle distortion	LX devices	0.25	0.25	0.25	0.50	ns
		LXT devices	0.25	0.25	0.25	N/A	ns

Table 79: Package Skew (Cont'd)

Symbol	Description	Device	Package <sup>(2)</sup>	Value	Units
T <sub>PKGSKEW</sub>	Package Skew <sup>(1)</sup>	LX45	CSG324	70	ps
			CS(G)484	99	ps
			FG(G)484	109	ps
			FG(G)676	138	ps
		LX45T	CSG324	75	ps
			CS(G)484	100	ps
			FG(G)484	95	ps
		LX75	CS(G)484	101	ps
			FG(G)484	107	ps
			FG(G)676	161	ps
			LX75T	CS(G)484	107
		FG(G)484		110	ps
		FG(G)676		134	ps
		LX100	CS(G)484	95	ps
			FG(G)484	155	ps
			FG(G)676	144	ps
		LX100T	CS(G)484	88	ps
			FG(G)484	111	ps
			FG(G)676	147	ps
			FG(G)900	134	ps
		LX150	CS(G)484	84	ps
			FG(G)484	103	ps
			FG(G)676	115	ps
			FG(G)900	121	ps
LX150T	CS(G)484	83	ps		
	FG(G)484	88	ps		
	FG(G)676	141	ps		
	FG(G)900	120	ps		

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from Pad to Ball.
2. Some of the devices are available in both Pb and Pb-free (additional G) packages as standard ordering options. See [DS160: Spartan-6 Family Overview](#) for more information.

Table 80: Sample Window

Symbol	Description	Device <sup>(1)</sup>	Speed Grade				Units
			-3	-3N	-2	-1L	
T <sub>SAMP</sub>	Sampling Error at Receiver Pins <sup>(2)</sup>	All	510	510	530	740	ps
T <sub>SAMP_BUFIO2</sub>	Sampling Error at Receiver Pins using BUFIO2 <sup>(3)</sup>	All	430	430	450	590	ps

Notes:

1. LXT devices are not available with a -1L speed grade.
2. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
  - CLK0 DCM jitter
  - DCM accuracy (phase offset)
  - DCM phase shift resolution
 These measurements do not include package or clock tree skew.
3. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO2 clock network and IODELAY2 to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Date	Version	Description of Revisions
01/10/11	1.11	<p>Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v12.4 software with speed specification v1.15 for the -4, -3, -3N, and -2 speed grades. Added note 3 to <a href="#">Table 27</a>. Also updated the -1L speed grade requirements to ISE v12.4 software with speed specification v1.06. Revised -3N definition throughout the document.</p> <p>Added note 4 to <a href="#">Table 2</a> and updated note 5. Added information on <math>V_{CCINT}</math> to note 1 in <a href="#">Table 5</a>. Updated Networking Applications -3 values in <a href="#">Table 25</a> to match improvements made in ISE v12.4. In <a href="#">Table 28</a>, added note 1 and revised the <math>T_{IOTP}</math> values for LVDS_33, LVDS_25, MINI_LVDS_33, MINI_LVDS_25, RSDS_33, RSDS_25, TMDS_33, PPDS_33, and PPDS_25. Added note 3 to <a href="#">Table 55</a>.</p>
02/11/11	1.12	<p>As described in <a href="#">XCN11008: Product Discontinuation Notice For Spartan-6 LXT -4 Devices</a>, the -4 speed specifications have been discontinued. As outlined in page 2 of the XCN, designers currently using -4 speed specifications should rerun timing analysis using the new -3 speed specifications before moving to a replacement device.</p> <p>Updated the networking applications section of <a href="#">Table 25</a>. Updated -2 speed specifications throughout document and added note 3 to <a href="#">Table 27</a> advising designers to use the -2 speed specification update (v1.17) with the ISE 12.4 software patch. Added <math>F_{CLKDIV}</math> to <a href="#">Table 37</a> and <a href="#">Table 38</a>. Updated note 2 in <a href="#">Table 39</a>. Updated units for <math>T_{SMCKCSO}</math> and <math>T_{BPICCO}</math> in <a href="#">Table 47</a>. Updated -1L in <a href="#">Table 71</a>. Removed Note 2: <i>Package delay information is available for these device/package combinations. This information can be used to deskew the package</i> from <a href="#">Table 79</a>.</p>
03/31/11	2.0	<p>Production release of XC6SLX45 in the -1L speed grades listed in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v13.1 software with -1L speed specification v1.06.</p> <p>In <a href="#">Table 39</a>, removed values in the -1L column and added note 3 as IODELAY2 only supports Tap0 for lower-power devices. Updated copyright <a href="#">page 1</a> and <a href="#">Notice of Disclaimer</a>.</p>
05/20/11	2.1	<p>Production release of XC6SLX100 and XC6SLX150 in the specific speed grades listed in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v13.1 software with -1L speed specification v1.06. Updated <a href="#">Table 27</a> and <a href="#">Note 7</a> with changes per <a href="#">XCN11012: Speed File Change for -3N Devices</a>. Revised <a href="#">Switching Characteristics</a> section for speed specifications: v1.18 for -3, -3N, and -2; including improvements in <a href="#">Table 73</a> through <a href="#">Table 77</a> and <a href="#">Table 81</a>.</p> <p>Removed <i>Memory Controller Block</i> from the performance heading in <a href="#">Table 2</a> and revised <a href="#">Note 2</a>. In <a href="#">Table 4</a>, added <a href="#">Note 1</a> to <math>C_{IN}</math> and updated the description of <math>R_{IN\_TERM}</math>. Updated <a href="#">Note 1</a> in <a href="#">Table 5</a>. Updated <a href="#">Note 1</a> of <a href="#">Table 7</a>. In <a href="#">Table 25</a>, added and removed -1L specifications, increased the standard performance DDR3 specifications, removed the extended performance DDR3 row and updated <a href="#">Note 3</a> and <a href="#">Note 4</a>. Clarified the introductory information for <a href="#">Table 28</a> and <a href="#">Table 30</a>.</p> <p>In <a href="#">Table 32</a>: Revised <math>V_{MEAS}</math> value for LVCMOS12; revised <math>V_{REF}</math> for LVDS_25, LVDS_33, BLVDS_25, MINI_LVDS_25, MINI_LVDS_33, RSDS_25, and RSDS_33; revised <math>R_{REF}</math> for BLVDS_25 and TMDS_33; and added <a href="#">Note 4</a> and <a href="#">Note 5</a>. Updated <a href="#">Note 2</a> and <a href="#">Note 3</a> in <a href="#">Table 39</a>.</p> <p>In <a href="#">Table 47</a>, revised the values and description of <math>T_{POR}</math> including adding <a href="#">Note 3</a>. Also in <a href="#">Table 47</a>, augmented the description and added specifications for <math>F_{RBCK}</math> and removed XC6SLX4 from <math>F_{MCCK}</math> (maximum frequency, parallel mode (Master Select/MAPI/BPI)). Added BUFGMUX to <a href="#">Table 48</a> title. Added <a href="#">Table 50</a>.</p> <p>In <a href="#">Table 52</a>, revised specifications for <math>T_{EXTFVAR}</math> and <math>F_{INJITTER}</math>. In <a href="#">Table 54</a> removed the 5 MHz &lt; <math>CLKIN\_FREQ\_DLL</math> parameter in the LOCK_DLL description. In both <a href="#">Table 56</a> and <a href="#">Table 57</a>, removed the 5 MHz &lt; <math>F_{CLKIN}</math> parameter in the LOCK_FX description. In <a href="#">Table 58</a>, updated description for PSCLK_FREQ and PSCLK_PULSE.</p> <p>Revised title and symbol of <a href="#">Table 70</a>, added new speed specifications for -1L, and added <a href="#">Note 2</a>. Added <a href="#">Table 71</a>.</p>
07/11/11	2.2	<p>Added the Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices to all appropriate tables while sometimes removing the XC6S nomenclature. Added expanded temperature range (Q) to all appropriate tables. Updated <math>T_{SOL}</math> packages in <a href="#">Table 1</a>. Added <math>R_{OUT\_TERM}</math> to <a href="#">Table 4</a>. Updated <a href="#">Note 2</a> on <a href="#">Table 13</a>.</p> <p>Production release of the XC6SLX4, XC6SLX9, XC6SLX16, XC6SLX25, XC6SLX75, XQ6SLX75, and XQ6SLX150 in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v13.2 software with -1L speed specification v1.07.</p> <p>Production release of the XA6SLX16, XA6SLX25T, XA6SLX45, XA6SLX45T, XQ6SLX75, XQ6SLX75T, XQ6SLX150, and XQ6SLX150T in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v13.2 software with -2 and -3 speed specification v1.19.</p> <p>Added <a href="#">Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices(1)</a>. Updated CS(G)484 from CSG484 throughout data sheet. Clarified <a href="#">Note 3</a> in <a href="#">Table 39</a>.</p>
08/08/11	2.3	<p>Production release of the XA6SLX25, XA6SLX75, and XA6SLX75T in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v13.2 software with -2 and -3 speed specification v1.19.</p>