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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	5831
Number of Logic Elements/Cells	74637
Total RAM Bits	3170304
Number of I/O	328
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA, CSPBGA
Supplier Device Package	484-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx75-2csg484c

Table 4: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.8	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin for commercial (C) and industrial (I) devices	–10	–	10	μA
	V_{REF} leakage current per pin for expanded (Q) devices	–15	–	15	μA
I_L	Input or output leakage current per pin (sample-tested) for commercial (C) and industrial (I) devices	–10	–	10	μA
	Input or output leakage current per pin (sample-tested) for expanded (Q) devices	–15	–	15	μA
I_{HS}	Leakage current on pins during hot socketing with FPGA unpowered	–20	–	20	μA
	All pins except PROGRAM_B, DONE, and JTAG pins when HSWAPEN = 1 PROGRAM_B, DONE, and JTAG pins, or other pins when HSWAPEN = 0	$I_{HS} + I_{RPU}$			μA
$C_{IN}^{(1)}$	Die input capacitance at the pad	–	–	10	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 3.3V$ or $V_{CCAUX} = 3.3V$	200	–	500	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 2.5V$ or $V_{CCAUX} = 2.5V$	120	–	350	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.8V$	60	–	200	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.5V$	40	–	150	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.2V$	12	–	100	μA
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = V_{CCO}$, $V_{CCAUX} = 3.3V$	200	–	550	μA
	Pad pull-down (when selected) @ $V_{IN} = V_{CCO}$, $V_{CCAUX} = 2.5V$	140	–	400	μA
$I_{BATT}^{(2)}$	Battery supply current	–	–	150	nA
$R_{DT}^{(3)}$	Resistance of optional input differential termination circuit, $V_{CCAUX} = 3.3V$	–	100	–	Ω
$R_{IN_TERM}^{(5)}$	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for commercial (C) and industrial (I) devices	23	25	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for expanded (Q) devices	20	25	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for commercial (C) and industrial (I) devices	39	50	72	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for expanded (Q) devices	32	50	74	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for commercial (C) and industrial (I) devices	56	75	109	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for expanded (Q) devices	47	75	115	Ω
R_{OUT_TERM}	Thevenin equivalent resistance of programmable output termination (UNTUNED_25)	11	25	52	Ω
	Thevenin equivalent resistance of programmable output termination (UNTUNED_50)	21	50	96	Ω
	Thevenin equivalent resistance of programmable output termination (UNTUNED_75)	29	75	145	Ω

Notes:

1. The C_{IN} measurement represents the die capacitance at the pad, not including the package.
2. Maximum value specified for worst case process at 25°C. LX75, LX75T, LX100, LX100T, LX150, and LX150T only.
3. Refer to IBIS models for R_{DT} variation and for values at $V_{CCAUX} = 2.5V$. IBIS values for R_{DT} are valid for all temperature ranges.
4. V_{CCO2} is not required for data retention. The minimum V_{CCO2} for power-on reset and configuration is 1.65V.
5. Termination resistance to a $V_{CCO}/2$ level.

SelectIO™ Interface DC Input and Output Levels

Table 7: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

I/O Standard	V _{CCO} for Drivers ⁽¹⁾			V _{REF} for Inputs		
	V, Min	V, Nom	V, Max	V, Min	V, Nom	V, Max
LVTTTL	3.0	3.3	3.45	V _{REF} is not used for these I/O standards		
LVC MOS33	3.0	3.3	3.45			
LVC MOS25	2.3	2.5	2.7			
LVC MOS18	1.65	1.8	1.95			
LVC MOS18_JEDEC	1.65	1.8	1.95			
LVC MOS15	1.4	1.5	1.6			
LVC MOS15_JEDEC	1.4	1.5	1.6			
LVC MOS12	1.1	1.2	1.3			
LVC MOS12_JEDEC	1.1	1.2	1.3			
PCI33_3 ⁽²⁾	3.0	3.3	3.45			
PCI66_3 ⁽²⁾	3.0	3.3	3.45			
I2C	2.7	3.0	3.45			
SMBUS	2.7	3.0	3.45			
SDIO	3.0	3.3	3.45			
MOBILE_DDR	1.7	1.8	1.9			
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_II	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_III	1.4	1.5	1.6	–	0.9	–
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–
HSTL_III_18	1.7	1.8	1.9	–	1.1	–
SSTL3_I	3.0	3.3	3.45	1.3	1.5	1.7
SSTL3_II	3.0	3.3	3.45	1.3	1.5	1.7
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38
SSTL18_I	1.7	1.8	1.9	0.833	0.9	0.969
SSTL18_II	1.7	1.8	1.9	0.833	0.9	0.969
SSTL15_II	1.425	1.5	1.575	0.69	0.75	0.81

Notes:

- V_{CCO} range required when using I/O standard for an output. Also required for MOBILE_DDR, PCI33_3, LVC MOS18_JEDEC, LVC MOS15_JEDEC, and LVC MOS12_JEDEC inputs, and for LVC MOS25 inputs when V_{CCAUX} = 3.3V.
- For PCI systems, the transmitter and receiver should have common supplies for V_{CCO}.

In Table 9 and Table 10, values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: Single-Ended I/O Standard DC Input and Output Levels

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTTL	−0.5	0.8	2.0	4.1	0.4	2.4	Note 2	Note 2
LVC MOS33	−0.5	0.8	2.0	4.1	0.4	$V_{CCO} - 0.4$	Note 2	Note 2
LVC MOS25	−0.5	0.7	1.7	4.1	0.4	$V_{CCO} - 0.4$	Note 2	Note 2
LVC MOS18	−0.5	0.38	0.8	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS18 (−1L)	−0.5	0.33	0.71	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS18_JEDEC	−0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS15	−0.5	0.38	0.8	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVC MOS15 (−1L)	−0.5	0.33	0.71	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVC MOS15_JEDEC	−0.5	35% V_{CCO}	65% V_{CCO}	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVC MOS12	−0.5	0.38	0.8	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
LVC MOS12 (−1L)	−0.5	0.33	0.71	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
LVC MOS12_JEDEC	−0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
PCI33_3	−0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	1.5	−0.5
PCI66_3	−0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	1.5	−0.5
I2C	−0.5	25% V_{CCO}	70% V_{CCO}	4.1	20% V_{CCO}	—	3	—
SMBUS	−0.5	0.8	2.1	4.1	0.4	—	4	—
SDIO	−0.5	12.5% V_{CCO}	75% V_{CCO}	4.1	12.5% V_{CCO}	75% V_{CCO}	0.1	−0.1
MOBILE_DDR	−0.5	20% V_{CCO}	80% V_{CCO}	4.1	10% V_{CCO}	90% V_{CCO}	0.1	−0.1
HSTL_I	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	8	−8
HSTL_II	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	16	−16
HSTL_III	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	24	−8
HSTL_I_18	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	11	−11
HSTL_II_18	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	22	−22
HSTL_III_18	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	30	−11
SSTL3_I	−0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	4.1	$V_{TT} - 0.6$	$V_{TT} + 0.6$	8	−8
SSTL3_II	−0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	4.1	$V_{TT} - 0.8$	$V_{TT} + 0.8$	16	−16
SSTL2_I	−0.5	$V_{REF} - 0.15$	$V_{REF} + 0.15$	4.1	$V_{TT} - 0.61$	$V_{TT} + 0.61$	8.1	−8.1
SSTL2_II	−0.5	$V_{REF} - 0.15$	$V_{REF} + 0.15$	4.1	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	−16.2
SSTL18_I	−0.5	$V_{REF} - 0.125$	$V_{REF} + 0.125$	4.1	$V_{TT} - 0.47$	$V_{TT} + 0.47$	6.7	−6.7
SSTL18_II	−0.5	$V_{REF} - 0.125$	$V_{REF} + 0.125$	4.1	$V_{TT} - 0.60$	$V_{TT} + 0.60$	13.4	−13.4
SSTL15_II	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	$V_{TT} - 0.4$	$V_{TT} + 0.4$	13.4	−13.4

Notes:

1. Tested according to relevant specifications.
2. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
3. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
4. Using drive strengths of 2, 4, 6, 8, or 12 mA.
5. For more information, refer to [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 10: Differential I/O Standard DC Input and Output Levels

I/O Standard	V _{ID}		V _{ICM}		V _{OD}		V _{OCM}		V _{OH}	V _{OL}
	mV, Min	mV, Max	V, Min	V, Max	mV, Min	mV, Max	V, Min	V, Max	V, Min	V, Max
LVDS_33 ⁽²⁾⁽³⁾	100	600	0.3	2.35	247	454	1.125	1.375	–	–
LVDS_25 ⁽²⁾⁽³⁾	100	600	0.3	2.35	247	454	1.125	1.375	–	–
BLVDS_25 ⁽²⁾⁽³⁾	100	–	0.3	2.35	240	460	Typical 50% V _{CCO}		–	–
MINI_LVDS_33	200	600	0.3	1.95	300	600	1.0	1.4	–	–
MINI_LVDS_25	200	600	0.3	1.95	300	600	1.0	1.4	–	–
LVPECL_33 ⁽²⁾⁽³⁾	100	1000	0.3	2.8 ⁽¹⁾	Inputs only					
LVPECL_25 ⁽²⁾⁽³⁾	100	1000	0.3	1.95	Inputs only					
RSDS_33 ⁽²⁾⁽³⁾	100	–	0.3	1.5	100	400	1.0	1.4	–	–
RSDS_25 ⁽²⁾⁽³⁾	100	–	0.3	1.5	100	400	1.0	1.4	–	–
TMDS_33	150	1200	2.7	3.23 ⁽¹⁾	400	800	V _{CCO} – 0.405	V _{CCO} – 0.190	–	–
PPDS_33 ⁽²⁾⁽³⁾	100	400	0.2	2.3	100	400	0.5	1.4	–	–
PPDS_25 ⁽²⁾⁽³⁾	100	400	0.2	2.3	100	400	0.5	1.4	–	–
DISPLAY_PORT	190	1260	0.3	2.35	–	–	Typical 50% V _{CCO}		–	–
DIFF_MOBILE_DDR	100	–	0.78	1.02	–	–	–	–	90% V _{CCO}	10% V _{CCO}
DIFF_HSTL_I	100	–	0.68	0.9	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_HSTL_II	100	–	0.68	0.9	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_HSTL_III	100	–	0.68	0.9	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_HSTL_I_18	100	–	0.8	1.1	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_HSTL_II_18	100	–	0.8	1.1	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_HSTL_III_18	100	–	0.8	1.1	–	–	–	–	V _{CCO} – 0.4	0.4
DIFF_SSTL3_I	100	–	1.0	1.9	–	–	–	–	V _{TT} + 0.6	V _{TT} – 0.6
DIFF_SSTL3_II	100	–	1.0	1.9	–	–	–	–	V _{TT} + 0.8	V _{TT} – 0.8
DIFF_SSTL2_I	100	–	1.0	1.5	–	–	–	–	V _{TT} + 0.61	V _{TT} – 0.61
DIFF_SSTL2_II	100	–	1.0	1.5	–	–	–	–	V _{TT} + 0.81	V _{TT} – 0.81
DIFF_SSTL18_I	100	–	0.7	1.1	–	–	–	–	V _{TT} + 0.47	V _{TT} – 0.47
DIFF_SSTL18_II	100	–	0.7	1.1	–	–	–	–	V _{TT} + 0.6	V _{TT} – 0.6
DIFF_SSTL15_II	100	–	0.55	0.95	–	–	–	–	V _{TT} + 0.4	V _{TT} – 0.4

Notes:

1. LVPECL_33 and TMDS_33 maximum V_{ICM} is the lower of V (maximum) or V_{CCAUX} – (V_{ID}/2)
2. When V_{CCAUX} = 3.3V, the DCD can be higher than 5% for V_{ICM} < 0.7V when using these I/O standards: LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, LVPECL_33, RSDS_25, RSDS_33, PPDS_25, and PPDS_33.
3. The -1L devices require V_{CCAUX} = 2.5V when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.

GTP Transceiver DC Input and Output Levels

Table 16 summarizes the DC output specifications of the GTP transceivers in Spartan-6 FPGAs. Figure 1 shows the single-ended output voltage swing. Figure 2 shows the peak-to-peak differential output voltage.

Consult [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#) for further details.

Table 16: GTP Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled	140	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTTRX = 1.2V	–400	–	MGTAVTTRX	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTTRX = 1.2V	–	3/4 MGTAVTTRX	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
V_{SEOUT}	Single-ended output voltage swing ⁽¹⁾		–	–	500	mV
$V_{CMOUTDC}$	Common mode output voltage	Equation based	$MGTAVTTTX - V_{SEOUT}/2$			mV
R_{IN}	Differential input resistance		80	100	130	Ω
R_{OUT}	Differential output resistance		80	100	130	Ω
T_{OSKEW}	Transmitter output skew		–	–	15	ps
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		75	100	200	nF

Notes:

- The output swing and preemphasis levels are programmable using the attributes discussed in [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#) and can result in values lower than reported in this table.
- Other values can be used as appropriate to conform to specific protocols and standards.

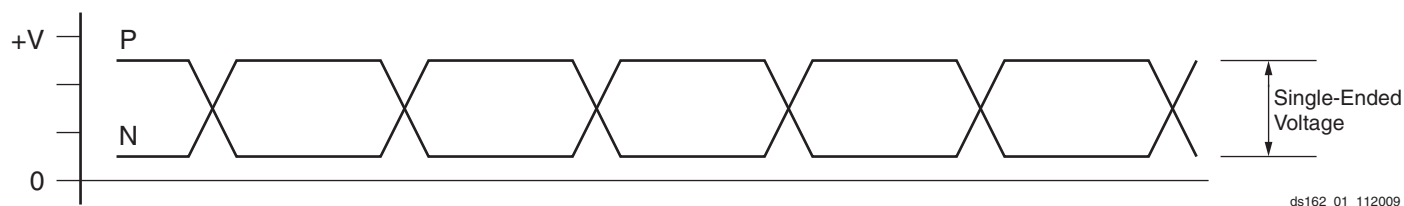


Figure 1: Single-Ended Peak-to-Peak Voltage

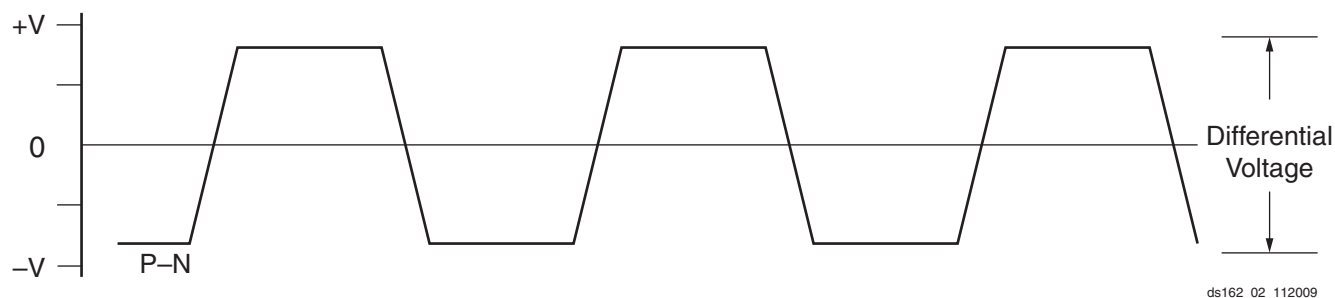


Figure 2: Differential Peak-to-Peak Voltage

Table 17 summarizes the DC specifications of the clock input of the GTP transceiver. Consult [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#) for further details.

Table 23: GTP Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units	
T _{RXELECIDLE}	Time for RXELECIDLE to respond to loss or restoration of data		–	75	–	ns	
R _{XOVBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV	
R _{XSST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	0	ppm	
R _{XRL}	Run length (CID)	Internal AC capacitor bypassed	–	–	150	UI	
R _{XPMTOL}	Data/REFCLK PPM offset tolerance	CDR 2 nd -order loop disabled	–200	–	200	ppm	
		CDR 2 nd -order loop enabled	PLL_RXDIVSEL_OUT = 1	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 2	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 4	–1000	–	1000	ppm
SJ Jitter Tolerance ⁽²⁾							
JT_SJ _{3.125}	Sinusoidal Jitter ⁽³⁾	3.125 Gb/s	0.4	–	–	UI	
JT_SJ _{2.5}	Sinusoidal Jitter ⁽³⁾	2.5 Gb/s	0.4	–	–	UI	
JT_SJ _{1.62}	Sinusoidal Jitter ⁽³⁾	1.62 Gb/s	0.5	–	–	UI	
JT_SJ _{1.25}	Sinusoidal Jitter ⁽³⁾	1.25 Gb/s	0.5	–	–	UI	
JT_SJ ₆₁₄	Sinusoidal Jitter ⁽³⁾	614 Mb/s	0.5	–	–	UI	
SJ Jitter Tolerance with Stressed Eye ⁽²⁾⁽⁵⁾							
JT_TJSE _{3.125}	Total Jitter with stressed eye ⁽⁴⁾	3.125 Gb/s	0.65	–	–	UI	
JT_SJSE _{3.125}	Sinusoidal Jitter with stressed eye	3.125 Gb/s	0.1	–	–	UI	
JT_TJSE _{2.7}	Total Jitter with stressed eye ⁽⁴⁾	2.7 Gb/s	0.65	–	–	UI	
JT_SJSE _{2.7}	Sinusoidal Jitter with stressed eye	2.7 Gb/s	0.1	–	–	UI	

Notes:

- Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
- All jitter values are based on a Bit Error Ratio of 1e⁻¹².
- Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
- Composed of 0.37 UI DJ in the form of ISI and 0.18 UI RJ.
- Measured using PRBS7 data pattern.

Endpoint Block for PCI Express Designs Switching Characteristics

The Endpoint block for PCI Express is available in the Spartan-6 LXT devices. Consult the [Spartan-6 FPGA Integrated Endpoint Block for PCI Express](#) for further information.

Table 24: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
F _{PCIEUSER}	User clock maximum frequency	62.5	62.5	62.5	N/A	MHz

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVC MOS12, Fast, 2 mA	0.91	1.03	1.16	1.51	3.46	3.60	3.80	4.44	3.46	3.60	3.80	4.44	ns
LVC MOS12, Fast, 4 mA	0.91	1.03	1.16	1.51	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVC MOS12, Fast, 6 mA	0.91	1.03	1.16	1.51	1.79	1.93	2.13	2.75	1.79	1.93	2.13	2.75	ns
LVC MOS12, Fast, 8 mA	0.91	1.03	1.16	1.51	1.68	1.82	2.02	2.64	1.68	1.82	2.02	2.64	ns
LVC MOS12, Fast, 12 mA	0.91	1.03	1.16	1.51	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
LVC MOS12_JEDEC, QUIETIO, 2 mA	1.50	1.62	1.75	1.88	6.39	6.53	6.73	7.31	6.39	6.53	6.73	7.31	ns
LVC MOS12_JEDEC, QUIETIO, 4 mA	1.50	1.62	1.75	1.88	4.98	5.12	5.32	5.88	4.98	5.12	5.32	5.88	ns
LVC MOS12_JEDEC, QUIETIO, 6 mA	1.50	1.62	1.75	1.88	4.67	4.81	5.01	5.54	4.67	4.81	5.01	5.54	ns
LVC MOS12_JEDEC, QUIETIO, 8 mA	1.50	1.62	1.75	1.88	4.23	4.37	4.57	5.22	4.23	4.37	4.57	5.22	ns
LVC MOS12_JEDEC, QUIETIO, 12 mA	1.50	1.62	1.75	1.88	3.99	4.13	4.33	4.94	3.99	4.13	4.33	4.94	ns
LVC MOS12_JEDEC, Slow, 2 mA	1.50	1.62	1.75	1.88	5.00	5.14	5.34	5.90	5.00	5.14	5.34	5.90	ns
LVC MOS12_JEDEC, Slow, 4 mA	1.50	1.62	1.75	1.88	2.85	2.99	3.19	3.80	2.85	2.99	3.19	3.80	ns
LVC MOS12_JEDEC, Slow, 6 mA	1.50	1.62	1.75	1.88	2.76	2.90	3.10	3.72	2.76	2.90	3.10	3.72	ns
LVC MOS12_JEDEC, Slow, 8 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVC MOS12_JEDEC, Slow, 12 mA	1.50	1.62	1.75	1.88	2.09	2.23	2.43	3.05	2.09	2.23	2.43	3.05	ns
LVC MOS12_JEDEC, Fast, 2 mA	1.50	1.62	1.75	1.88	3.46	3.60	3.80	4.42	3.46	3.60	3.80	4.42	ns
LVC MOS12_JEDEC, Fast, 4 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns
LVC MOS12_JEDEC, Fast, 6 mA	1.50	1.62	1.75	1.88	1.79	1.93	2.13	2.76	1.79	1.93	2.13	2.76	ns
LVC MOS12_JEDEC, Fast, 8 mA	1.50	1.62	1.75	1.88	1.69	1.83	2.03	2.65	1.69	1.83	2.03	2.65	ns
LVC MOS12_JEDEC, Fast, 12 mA	1.50	1.62	1.75	1.88	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns

Notes:

1. The -1L values listed in this table are also applicable to the Spartan-6Q devices.
2. Devices with a -1L speed grade do not support Xilinx PCI IP.

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS15, QUIETIO, 2 mA	1.05	1.23	5.63	5.83	5.63	5.83	ns
LVC MOS15, QUIETIO, 4 mA	1.05	1.23	4.75	4.95	4.75	4.95	ns
LVC MOS15, QUIETIO, 6 mA	1.05	1.23	4.21	4.41	4.21	4.41	ns
LVC MOS15, QUIETIO, 8 mA	1.05	1.23	4.05	4.25	4.05	4.25	ns
LVC MOS15, QUIETIO, 12 mA	1.05	1.23	3.74	3.94	3.74	3.94	ns
LVC MOS15, QUIETIO, 16 mA	1.05	1.23	3.52	3.72	3.52	3.72	ns
LVC MOS15, Slow, 2 mA	1.05	1.23	4.32	4.52	4.32	4.52	ns
LVC MOS15, Slow, 4 mA	1.05	1.23	3.58	3.78	3.58	3.78	ns
LVC MOS15, Slow, 6 mA	1.05	1.23	2.45	2.65	2.45	2.65	ns
LVC MOS15, Slow, 8 mA	1.05	1.23	2.46	2.66	2.46	2.66	ns
LVC MOS15, Slow, 12 mA	1.05	1.23	2.17	2.37	2.17	2.37	ns
LVC MOS15, Slow, 16 mA	1.05	1.23	2.15	2.35	2.15	2.35	ns
LVC MOS15, Fast, 2 mA	1.05	1.23	3.43	3.63	3.43	3.63	ns
LVC MOS15, Fast, 4 mA	1.05	1.23	2.42	2.62	2.42	2.62	ns
LVC MOS15, Fast, 6 mA	1.05	1.23	1.92	2.12	1.92	2.12	ns
LVC MOS15, Fast, 8 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVC MOS15, Fast, 12 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVC MOS15, Fast, 16 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVC MOS15_JEDEC, QUIETIO, 2 mA	1.10	1.28	5.64	5.84	5.64	5.84	ns
LVC MOS15_JEDEC, QUIETIO, 4 mA	1.10	1.28	4.75	4.95	4.75	4.95	ns
LVC MOS15_JEDEC, QUIETIO, 6 mA	1.10	1.28	4.21	4.41	4.21	4.41	ns
LVC MOS15_JEDEC, QUIETIO, 8 mA	1.10	1.28	4.06	4.26	4.06	4.26	ns
LVC MOS15_JEDEC, QUIETIO, 12 mA	1.10	1.28	3.75	3.95	3.75	3.95	ns
LVC MOS15_JEDEC, QUIETIO, 16 mA	1.10	1.28	3.53	3.73	3.53	3.73	ns
LVC MOS15_JEDEC, Slow, 2 mA	1.10	1.28	4.32	4.52	4.32	4.52	ns
LVC MOS15_JEDEC, Slow, 4 mA	1.10	1.28	3.56	3.76	3.56	3.76	ns
LVC MOS15_JEDEC, Slow, 6 mA	1.10	1.28	2.44	2.64	2.44	2.64	ns
LVC MOS15_JEDEC, Slow, 8 mA	1.10	1.28	2.47	2.67	2.47	2.67	ns
LVC MOS15_JEDEC, Slow, 12 mA	1.10	1.28	2.15	2.35	2.15	2.35	ns
LVC MOS15_JEDEC, Slow, 16 mA	1.10	1.28	2.15	2.35	2.15	2.35	ns
LVC MOS15_JEDEC, Fast, 2 mA	1.10	1.28	3.43	3.63	3.43	3.63	ns
LVC MOS15_JEDEC, Fast, 4 mA	1.10	1.28	2.42	2.62	2.42	2.62	ns
LVC MOS15_JEDEC, Fast, 6 mA	1.10	1.28	1.92	2.12	1.92	2.12	ns
LVC MOS15_JEDEC, Fast, 8 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVC MOS15_JEDEC, Fast, 12 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVC MOS15_JEDEC, Fast, 16 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVC MOS12, QUIETIO, 2 mA	0.98	1.16	6.54	6.74	6.54	6.74	ns
LVC MOS12, QUIETIO, 4 mA	0.98	1.16	5.12	5.32	5.12	5.32	ns

Table 32: Output Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	R_{REF} (Ω)	$C_{REF}^{(1)}$ (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
SSTL, Class II, 1.5V	SSTL15_II	25	0	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	100	0	0 ⁽³⁾	—
BLVDS (Bus LVDS), 2.5V	BLVDS_25	Note 4	0	0 ⁽³⁾	—
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	100	0	0 ⁽³⁾	—
RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RSDS_25, RSDS_33	100	0	0 ⁽³⁾	—
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	Note 5	0	0 ⁽³⁾	—
PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V	PPDS_25, PPDS_33	100	0	0 ⁽³⁾	—

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. The value given is the differential output voltage.
4. See the *BLVDS Output Termination* section in [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.
5. See the *TMDS_33 Termination* section in [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.

Simultaneously Switching Outputs

Due to package electrical parasitics, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. [Table 33](#) and [Table 34](#) provide guidelines for the recommended maximum allowable number of SSOs. These guidelines describe the maximum number of user I/O pins of an output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise for that particular signal standard. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of GND and power bounce.

For each device/package combination, [Table 33](#) provides the number of equivalent V_{CCO} /GND pairs per bank. For each output signal standard and drive strength, [Table 34](#) recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO} /GND pair within an I/O bank. The guidelines are categorized by package style, slew rate, and output drive current. The number of SSOs are also specified by I/O bank. Multiply the appropriate numbers from each table to calculate the maximum number of SSOs allowed within an I/O bank. The guidelines assume that all pins within a bank use the same I/O standard. Exceeding these SSO guidelines can result in increased power or GND bounce, degraded signal integrity, or increased system jitter. For a given I/O standard, if the SSO limit per pair in [Table 34](#) is greater than the maximum I/O per pair in [Table 33](#), then there is no SSO limit for the exclusive use of that I/O standard.

The recommended maximum SSO values assume that the FPGA is soldered on a printed circuit board and that the board uses sound design practices. Due to the additional inductance introduced by the socket, the SSO values do not apply for FPGAs mounted in sockets. The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics. For more detail, see [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

V _{CCO}	I/O Standard	Drive	Slew	SSO Limit per V _{CCO} /GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
1.5V	LVCMOS15, LVCMOS15_JEDEC	2	Fast	33	40	33	41
			Slow	57	62	57	56
			QuietIO	70	67	70	66
		4	Fast	19	21	19	21
			Slow	30	30	30	24
			QuietIO	38	33	38	30
		6	Fast	14	16	14	16
			Slow	18	19	18	17
			QuietIO	27	24	27	21
		8	Fast	11	13	11	12
			Slow	16	16	16	14
			QuietIO	23	20	23	17
		12	Fast	N/A	5	N/A	4
			Slow	N/A	8	N/A	5
			QuietIO	N/A	10	N/A	9
		16	Fast	N/A	5	N/A	4
			Slow	N/A	8	N/A	8
			QuietIO	N/A	10	N/A	9
	HSTL_I			9	10	9	10
	HSTL_II			N/A	5	N/A	6
	HSTL_III			7	9	7	9
	DIFF_HSTL_I			27	30	27	30
	DIFF_HSTL_II			N/A	15	N/A	18
	DIFF_HSTL_III			21	27	21	27
	SSTL_15_II ⁽³⁾			N/A	5	N/A	4
	DIFF_SSTL_15_II ⁽³⁾			N/A	15	N/A	12

CLB Switching Characteristics (SLICEM Only)

Table 40: CLB Switching Characteristics (SLICEM Only)

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT inputs to A to D outputs	0.21	0.26	0.26	0.46	ns, Max
	An – Dn LUT inputs through F7AMUX/F7BMUX to AMUX/CMUX output	0.37	0.43	0.43	0.77	ns, Max
T _{OPAB}	An – Dn LUT inputs through F7AMUX or F7BMUX and F8MUX to BMUX output	0.37	0.46	0.46	0.84	ns, Max
T _{ITO}	An – Dn LUT inputs through latch to AQ – DQ outputs	0.82	0.95	0.95	1.64	ns, Max
T _{TITO_LOGIC}	An – Dn LUT inputs to AQ – DQ outputs (latch as logic)	0.82	0.95	0.95	1.64	ns, Max
T _{OPCYA}	An LUT inputs to COUT output	0.38	0.48	0.48	0.69	ns, Max
T _{OPCYB}	Bn LUT inputs to COUT output	0.38	0.49	0.49	0.71	ns, Max
T _{OPCYC}	Cn LUT inputs to COUT output	0.28	0.33	0.33	0.55	ns, Max
T _{OPCYD}	Dn LUT inputs to COUT output	0.28	0.35	0.35	0.52	ns, Max
T _{AXCY}	AX input to COUT output	0.21	0.26	0.26	0.36	ns, Max
T _{BXCy}	BX input to COUT output	0.13	0.16	0.16	0.18	ns, Max
T _{CXCy}	CX input to COUT output	0.10	0.12	0.12	0.09	ns, Max
T _{DXCy}	DX input to COUT output	0.09	0.11	0.11	0.09	ns, Max
T _{BYP}	CIN input to COUT output	0.08	0.10	0.10	0.06	ns, Max
T _{CINA}	CIN input to AMUX output	0.21	0.22	0.22	0.47	ns, Max
T _{CINB}	CIN input to BMUX output	0.30	0.31	0.31	0.57	ns, Max
T _{CINC}	CIN input to CMUX output	0.29	0.31	0.31	0.58	ns, Max
T _{CIND}	CIN input to DMUX output	0.31	0.32	0.32	0.68	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.45	0.53	0.53	0.74	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{DICK} /T _{CKDI}	AX – DX input to CLK on A – D flip-flops	0.42/ 0.28	0.47/ 0.39	0.47/ 0.39	0.90/ 0.56	ns, Min
T _{CECK} /T _{CKCE}	CE input to CLK on A – D flip-flops	0.31/ –0.07	0.37/ –0.07	0.37/ –0.07	0.59/ –0.27	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D flip-flops for XC devices	0.41/ 0.02	0.42/ 0.02	0.42/ 0.02	0.68/ –0.29	ns, Min
	SR input to CLK on A – D flip-flops for XA and XQ devices	0.41/ 0.02	N/A	0.44/ 0.02	0.68/ –0.29	ns, Min
T _{CINCK} /T _{CKCIN}	CIN input to CLK on A – D flip-flops	0.31/ –0.17	0.31/ –0.13	0.31/ –0.13	0.81/ –0.42	ns, Min
Set/Reset						
T _{RPW}	SR input minimum pulse width	0.41	0.48	0.48	1.37	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.60	0.70	0.70	0.88	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.60	0.65	0.65	0.90	ns, Max
F _{TOG}	Toggle frequency (for export control)	862	806	667	500	MHz

DSP48A1 Switching Characteristics

Table 44: DSP48A1 Switching Characteristics

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-3	-3N	-2	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock									
$T_{\text{DSPDCK_A_A1REG}}/$ $T_{\text{DSPCKD_A_A1REG}}$	A input to A1 register CLK	N/A	N/A	N/A	0.15/ 0.09	0.17/ 0.09	0.17/ 0.09	0.32/ 0.09	ns
$T_{\text{DSPDCK_D_B1REG}}/$ $T_{\text{DSPCKD_D_B1REG}}$	D input to B1 register CLK	Yes	N/A	N/A	1.90/ -0.07	1.95/ -0.07	1.95/ -0.07	2.82/ -0.07	ns
$T_{\text{DSPDCK_C_CREG}}/$ $T_{\text{DSPCKD_C_CREG}}$	C input to C register CLK for XC devices	N/A	N/A	N/A	0.11/ 0.15	0.13/ 0.15	0.13/ 0.15	0.24/ 0.09	ns
	C input to C register CLK for XA and XQ devices				0.11/ 0.19	N/A	0.13/ 0.23	0.24/ 0.09	
$T_{\text{DSPDCK_D_DREG}}/$ $T_{\text{DSPCKD_D_DREG}}$	D input to D register CLK for XC devices	N/A	N/A	N/A	0.09/ 0.15	0.10/ 0.15	0.10/ 0.15	0.19/ 0.12	ns
	D input to D register CLK for XA and XQ devices				0.09/ 0.23	N/A	0.10/ 0.27	0.19/ 0.12	
$T_{\text{DSPDCK_OPMODE_B1REG}}/$ $T_{\text{DSPCKD_OPMODE_B1REG}}$	OPMODE input to B1 register CLK	Yes	N/A	N/A	1.97/ 0.01	2.00/ 0.01	2.00/ 0.01	2.85/ 0.01	ns
$T_{\text{DSPDCK_OPMODE_OPMODEREG}}/$ $T_{\text{DSPCKD_OPMODE_OPMODEREG}}$	OPMODE input to OPMODE register CLK for XC devices	N/A	N/A	N/A	0.18/ 0.12	0.21/ 0.12	0.21/ 0.12	0.40/ 0.12	ns
	OPMODE input to OPMODE register CLK for XA and XQ devices				0.18/ 0.16	N/A	0.21/ 0.22	0.40/ 0.12	
Setup and Hold Times of Data Pins to the Pipeline Register Clock									
$T_{\text{DSPDCK_A_MREG}}/$ $T_{\text{DSPCKD_A_MREG}}$	A input to M register CLK	N/A	Yes	N/A	3.06/ -0.40	3.51/ -0.40	3.51/ -0.40	3.97/ -0.40	ns
$T_{\text{DSPDCK_B_MREG}}/$ $T_{\text{DSPCKD_B_MREG}}$	B input to M register CLK	Yes	Yes	N/A	3.96/ -0.68	4.58/ -0.68	4.58/ -0.68	7.00/ -0.68	ns
$T_{\text{DSPDCK_D_MREG}}/$ $T_{\text{DSPCKD_D_MREG}}$	D input to M register CLK	Yes	Yes	N/A	4.23/ -0.56	4.80/ -0.56	4.80/ -0.56	6.84/ -0.56	ns
$T_{\text{DSPDCK_OPMODE_MREG}}/$ $T_{\text{DSPCKD_OPMODE_MREG}}$	OPMODE to M register CLK	Yes	Yes	N/A	4.18/ -0.48	4.80/ -0.48	4.80/ -0.48	6.88/ -0.48	ns
		No	Yes	N/A	2.37/ -0.48	2.70/ -0.48	2.70/ -0.48	4.28/ -0.48	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock									
$T_{\text{DSPDCK_A_PREG}}/$ $T_{\text{DSPCKD_A_PREG}}$	A input to P register CLK	N/A	Yes	Yes	4.32/ -0.76	5.06/ -0.76	5.06/ -0.76	7.52/ -0.76	ns
$T_{\text{DSPDCK_B_PREG}}/$ $T_{\text{DSPCKD_B_PREG}}$	B input to P register CLK	Yes	Yes	Yes	5.87/ -0.59	6.87/ -0.59	6.87/ -0.59	10.55/ -0.59	ns
		No	Yes	Yes	4.14/ -0.93	4.68/ -0.93	4.68/ -0.93	8.12/ -0.93	ns
$T_{\text{DSPDCK_C_PREG}}/$ $T_{\text{DSPCKD_C_PREG}}$	C input to P register CLK	N/A	N/A	Yes	2.20/ -0.23	2.25/ -0.23	2.25/ -0.23	3.27/ -0.23	ns
$T_{\text{DSPDCK_D_PREG}}/$ $T_{\text{DSPCKD_D_PREG}}$	D input to P register CLK	Yes	Yes	Yes	5.90/ -0.92	6.91/ -0.92	6.91/ -0.92	10.39/ -0.92	ns

Table 54: Switching Characteristics for the Delay-Locked Loop (DLL)⁽¹⁾ (Cont'd)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
LOCK_DLL ⁽³⁾	When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. CLKIN_FREQ_DLL < 50 MHz.	–	5	–	5	–	5	–	5	ms
	When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. CLKIN_FREQ_DLL > 50 MHz	–	0.60	–	0.60	–	0.60	–	0.60	ms
Delay Lines										
DCM_DELAY_STEP ⁽⁵⁾	Finest delay resolution, averaged over all steps.	10	40	10	40	10	40	10	40	ps

Notes:

1. The values in this table are based on the operating conditions described in Table 2 and Table 53.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster LOCK time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, this data sheet specifies a maximum jitter of $\pm(1\% \text{ of CLKIN period} + 150 \text{ ps})$. Assuming that the CLKIN frequency is 100 MHz, the equivalent CLKIN period is 10 ns. Since 1% of 10 ns is 0.1 ns or 100 ps, the maximum jitter is $\pm(100 \text{ ps} + 150 \text{ ps}) = \pm250 \text{ ps}$.
5. A typical delay step size is 23 ps.
6. The timing analysis tools use the CLK_FEEDBACK = 1X condition for the CLKIN_CLKFB_PHASE value (reported as phase error). When using CLK_FEEDBACK = 2X, add 100 ps to the phase error for the CLKIN_CLKFB_PHASE value (as shown in this table).

Table 55: Recommended Operating Conditions for the Digital Frequency Synthesizer (DFS)⁽¹⁾

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Input Frequency Ranges ⁽²⁾										
CLKIN_FREQ_FX	Frequency for the CLKIN input. Also described as F _{CLKIN} .	0.5	375 ⁽³⁾	0.5	375 ⁽³⁾	0.5	333 ⁽³⁾	0.5	200 ⁽³⁾	MHz
Input Clock Jitter Tolerance ⁽⁴⁾										
CLKIN_CYC_JITT_FX_LF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: FCLKFX < 150 MHz.	–	±300	–	±300	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: FCLKFX > 150 MHz.	–	±150	–	±150	–	±150	–	±150	ps
CLKIN_PER_JITT_FX	Period jitter at the CLKIN input.	–	±1	–	±1	–	±1	–	±1	ns

Notes:

1. DFS specifications apply when using either of the DFS outputs (CLKFX or CLKFX180).
2. When using both DFS and DLL outputs on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 53.
3. The CLKIN_DIVIDE_BY_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the F_{MAX} (see Table 48 and Table 49 for BUFG and BUFGIO limits).
4. CLKIN input jitter beyond these limits can cause the DCM to lose LOCK.

Table 59: Switching Characteristics for the Phase-Shift Clock in Variable Phase Mode⁽¹⁾

Symbol	Description	Amount of Phase Shift	Units
Phase Shifting Range			
MAX_STEPS ⁽²⁾	When CLKIN < 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period.	$\pm(\text{INTEGER}(10 \times (\text{TCLKIN} - 3 \text{ ns})))$	steps
	When CLKIN ≥ 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period.	$\pm(\text{INTEGER}(15 \times (\text{TCLKIN} - 3 \text{ ns})))$	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting.	$\pm(\text{MAX_STEPS} \times \text{DCM_DELAY_STEP_MIN})$	ps
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	$\pm(\text{MAX_STEPS} \times \text{DCM_DELAY_STEP_MAX})$	ps

Notes:

1. The values in this table are based on the operating conditions described in Table 53 and Table 58.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM has no initial fixed-phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the end of Table 54.

Table 60: Miscellaneous DCM Timing Parameters⁽¹⁾

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	3	–	CLKIN cycles

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFXDV, CLKFX180) are unaffected.

Table 61: Frequency Synthesis

Attribute	Min	Max
CLKFX_MULTIPLY (DCM_SP)	2	32
CLKFX_DIVIDE (DCM_SP)	1	32
CLKDV_DIVIDE (DCM_SP)	1.5	16
CLKFX_MULTIPLY (DCM_CLKGEN)	2	256
CLKFX_DIVIDE (DCM_CLKGEN)	1	256
CLKFXDV_DIVIDE (DCM_CLKGEN)	2	32

Table 62: DCM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T _{DMCK_PSEN} /T _{DMCKC_PSEN}	PSEN Setup/Hold	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	ns
T _{DMCK_PSINCDEC} /T _{DMCKC_PSINCDEC}	PSINCDEC Setup/Hold	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	1.50/ 0.00	ns
T _{DMCKO_PSDONE}	Clock to out of PSDONE	1.50	1.50	1.50	1.50	ns

Table 64: Global Clock Input to Output Delay With DCM in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in System-Synchronous Mode.							
T _{ICKOFDCM}	Global Clock and OUTFF <i>with</i> DCM	XC6SLX4	4.23	N/A	6.11	6.60	ns
		XC6SLX9	4.23	5.17	6.11	6.60	ns
		XC6SLX16	4.28	4.57	5.34	6.36	ns
		XC6SLX25	3.95	4.18	4.59	6.91	ns
		XC6SLX25T	3.95	4.18	4.59	N/A	ns
		XC6SLX45	4.37	4.70	5.50	6.85	ns
		XC6SLX45T	4.37	4.70	5.50	N/A	ns
		XC6SLX75	3.90	4.23	4.77	6.31	ns
		XC6SLX75T	3.90	4.23	4.77	N/A	ns
		XC6SLX100	3.86	4.16	4.66	7.25	ns
		XC6SLX100T	3.90	4.16	4.66	N/A	ns
		XC6SLX150	4.03	4.33	4.83	6.63	ns
		XC6SLX150T	4.03	4.33	4.83	N/A	ns
		XA6SLX4	4.55	N/A	6.11	N/A	ns
		XA6SLX9	4.55	N/A	6.11	N/A	ns
		XA6SLX16	4.62	N/A	5.33	N/A	ns
		XA6SLX25	4.27	N/A	4.59	N/A	ns
		XA6SLX25T	4.27	N/A	4.69	N/A	ns
		XA6SLX45	4.69	N/A	5.50	N/A	ns
		XA6SLX45T	4.69	N/A	5.50	N/A	ns
		XA6SLX75	4.22	N/A	4.77	N/A	ns
		XA6SLX75T	4.22	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.34	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	6.31	ns
		XQ6SLX75T	4.22	N/A	4.77	N/A	ns
		XQ6SLX150	N/A	N/A	4.96	6.63	ns
		XQ6SLX150T	4.62	N/A	4.96	N/A	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
- DCM output jitter is already included in the timing calculation.

Table 74: Global Clock Setup and Hold With PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.(1)							
T _{PSPLL} / T _{PHPLL}	No Delay Global Clock and IFF(2) with PLL in System-Synchronous Mode	XC6SLX4	1.37/0.25	N/A	1.52/0.41	2.07/0.69	ns
		XC6SLX9	1.37/0.21	1.48/0.21	1.52/0.26	2.07/0.69	ns
		XC6SLX16	1.33/−0.03	1.53/−0.02	1.60/−0.02	1.57/0.48	ns
		XC6SLX25	1.65/0.28	1.71/0.28	1.91/0.28	2.44/0.76	ns
		XC6SLX25T	1.65/0.28	1.71/0.28	1.91/0.28	N/A	ns
		XC6SLX45	1.55/0.18	1.64/0.18	1.75/0.18	2.02/0.90	ns
		XC6SLX45T	1.55/0.18	1.64/0.18	1.75/0.18	N/A	ns
		XC6SLX75	1.77/0.21	1.89/0.21	2.13/0.21	2.46/0.53	ns
		XC6SLX75T	1.77/0.21	1.89/0.21	2.13/0.21	N/A	ns
		XC6SLX100	1.44/0.32	1.52/0.32	1.70/0.32	1.78/0.86	ns
		XC6SLX100T	1.44/0.32	1.52/0.32	1.70/0.32	N/A	ns
		XC6SLX150	1.39/0.49	1.48/0.49	1.67/0.49	1.94/0.94	ns
		XC6SLX150T	1.39/0.49	1.48/0.49	1.67/0.49	N/A	ns
		XA6SLX4	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX9	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX16	1.89/−0.08	N/A	1.72/−0.08	N/A	ns
		XA6SLX25	1.85/0.16	N/A	2.08/0.16	N/A	ns
		XA6SLX25T	1.85/0.16	N/A	2.17/0.16	N/A	ns
		XA6SLX45	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX45T	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX75	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX100	N/A	N/A	2.34/0.14	N/A	ns
		XQ6SLX75	N/A	N/A	2.25/0.06	2.46/0.53	ns
		XQ6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XQ6SLX150	N/A	N/A	1.79/0.37	1.94/0.94	ns
		XQ6SLX150T	1.43/0.37	N/A	1.79/0.37	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 75: Global Clock Setup and Hold With PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard. ⁽¹⁾							
T _{PSPLL0} / T _{PHPLL0}	No Delay Global Clock and IFF ⁽²⁾ with PLL in Source-Synchronous Mode	XC6SLX4	0.47/1.08	N/A	0.47/1.60	1.15/1.68	ns
		XC6SLX9	0.47/1.08	0.47/1.35	0.47/1.60	1.15/1.68	ns
		XC6SLX16	0.37/0.75	0.37/0.82	0.51/0.94	0.57/1.31	ns
		XC6SLX25	0.69/1.06	0.69/1.06	0.69/1.06	1.86/1.67	ns
		XC6SLX25T	0.69/1.06	0.69/1.06	0.69/1.06	N/A	ns
		XC6SLX45	0.57/1.05	0.65/1.10	0.65/1.18	1.02/1.65	ns
		XC6SLX45T	0.57/1.06	0.65/1.10	0.65/1.18	N/A	ns
		XC6SLX75	0.86/1.04	0.87/1.04	0.90/1.04	1.34/1.55	ns
		XC6SLX75T	0.86/1.04	0.87/1.04	0.90/1.04	N/A	ns
		XC6SLX100	0.53/1.13	0.54/1.13	0.55/1.13	0.89/2.39	ns
		XC6SLX100T	0.53/1.13	0.54/1.13	0.55/1.13	N/A	ns
		XC6SLX150	0.50/1.31	0.51/1.31	0.52/1.31	1.02/1.72	ns
		XC6SLX150T	0.50/1.31	0.51/1.31	0.52/1.31	N/A	ns
		XA6SLX4	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX9	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX16	0.92/0.69	N/A	0.63/0.82	N/A	ns
		XA6SLX25	0.99/0.94	N/A	0.96/0.94	N/A	ns
		XA6SLX25T	0.99/0.94	N/A	1.04/0.94	N/A	ns
		XA6SLX45	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX45T	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX75	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX100	N/A	N/A	1.25/0.96	N/A	ns
		XQ6SLX75	N/A	N/A	1.02/0.89	1.34/1.55	ns
		XQ6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XQ6SLX150	N/A	N/A	0.63/1.19	1.02/1.72	ns
		XQ6SLX150T	0.60/1.19	N/A	0.63/1.19	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 78: Duty Cycle Distortion and Clock-Tree Skew (Cont'd)

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{BUFIOSKEW}	I/O clock tree skew across one clock region	LX4	0.06	N/A	0.06	0.07	ns
		LX9	0.06	0.06	0.06	0.07	ns
		LX16	0.06	0.06	0.06	0.07	ns
		LX25	0.06	0.06	0.06	0.07	ns
		LX25T	0.06	0.06	0.06	N/A	ns
		LX45	0.06	0.06	0.06	0.07	ns
		LX45T	0.06	0.06	0.06	N/A	ns
		LX75	0.06	0.06	0.06	0.07	ns
		LX75T	0.06	0.06	0.06	N/A	ns
		LX100	0.06	0.06	0.06	0.07	ns
		LX100T	0.06	0.06	0.06	N/A	ns
		LX150	0.06	0.06	0.06	0.07	ns
		LX150T	0.06	0.06	0.06	N/A	ns

Notes:

1. LXT devices are not available with a -1L speed grade. The LX4 is not available in -3N speed grade.
2. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
3. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
4. The T_{CKSKEW} is 0.43 ns for the XA6SLX100 device using a -2 speed grade and 0.22 ns for the XC6SLX100 devices using the -2 speed grade.

Table 79: Package Skew

Symbol	Description	Device	Package ⁽²⁾	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	LX4	TQG144	N/A	ps
			CPG196	23	ps
			CSG225	58	ps
		LX9	TQG144	N/A	ps
			CPG196	23	ps
			CSG225	58	ps
			FT(G)256	88	ps
			CSG324	64	ps
		LX16	CPG196	19	ps
			CSG225	70	ps
			FT(G)256	71	ps
			CSG324	54	ps
		LX25	FT(G)256	90	ps
			CSG324	61	ps
			FG(G)484	84	ps
		LX25T	CSG324	48	ps
			FG(G)484	112	ps

Table 81: Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out Using BUFIO2 (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Pin-to-Pin Clock-to-Out Using BUFIO2							
T _{ICKO} FCS	OFF clock-to-out using BUFIO2 clock	XC6SLX4	5.51	N/A	6.95	8.45	ns
		XC6SLX9	5.51	5.89	6.95	8.45	ns
		XC6SLX16	5.31	5.70	6.67	8.21	ns
		XC6SLX25	5.53	6.00	7.02	8.72	ns
		XC6SLX25T	5.53	6.00	7.02	N/A	ns
		XC6SLX45	5.76	6.18	7.22	8.77	ns
		XC6SLX45T	5.76	6.18	7.22	N/A	ns
		XC6SLX75	5.94	6.46	7.57	9.72	ns
		XC6SLX75T	5.94	6.46	7.57	N/A	ns
		XC6SLX100	6.09	6.53	7.60	9.66	ns
		XC6SLX100T	6.09	6.53	7.60	N/A	ns
		XC6SLX150	6.29	6.69	7.81	9.94	ns
		XC6SLX150T	6.29	6.69	7.81	N/A	ns
		XA6SLX4	5.83	N/A	6.95	N/A	ns
		XA6SLX9	5.83	N/A	6.95	N/A	ns
		XA6SLX16	5.65	N/A	6.68	N/A	ns
		XA6SLX25	5.85	N/A	7.03	N/A	ns
		XA6SLX25T	5.85	N/A	7.03	N/A	ns
		XA6SLX45	6.07	N/A	7.25	N/A	ns
		XA6SLX45T	6.07	N/A	7.25	N/A	ns
		XA6SLX75	6.26	N/A	7.57	N/A	ns
		XA6SLX75T	6.26	N/A	7.57	N/A	ns
		XA6SLX100	N/A	N/A	7.48	N/A	ns
		XQ6SLX75	N/A	N/A	7.57	9.72	ns
		XQ6SLX75T	6.26	N/A	7.57	N/A	ns
		XQ6SLX150	N/A	N/A	7.81	9.94	ns
		XQ6SLX150T	6.62	N/A	7.81	N/A	ns

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