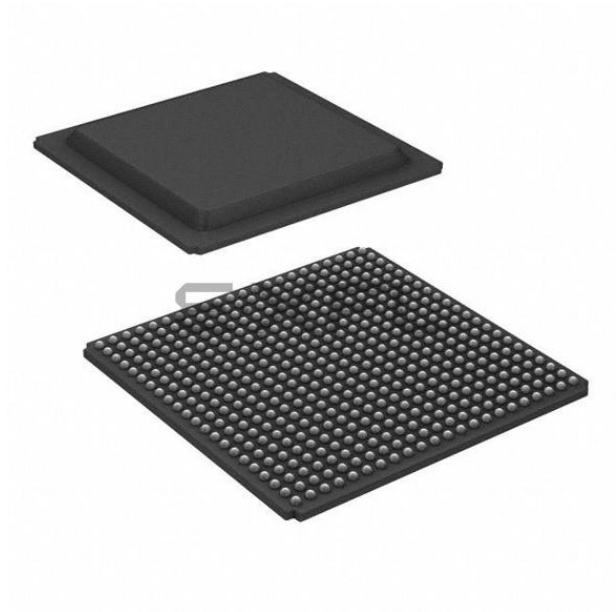
# AMD Xilinx - XC6SLX75-2FG484I Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 5831 |
| Number of Logic Elements/Cells | 74637 |
| Total RAM Bits | 3170304 |
| Number of I/O | 280 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc6slx75-2fg484i |

*Table 5:* **Typical Quiescent Supply Current *(Cont'd)***

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current | LX4 | 2.5 | 2.5 | 2.5 | 2.5 | mA |
| | | LX9 | 2.5 | 2.5 | 2.5 | 2.5 | mA |
| | | LX16 | 3.0 | 3.0 | 3.0 | 3.0 | mA |
| | | LX25 | 4.0 | 4.0 | 4.0 | 4.0 | mA |
| | | LX25T | 4.0 | 4.0 | 4.0 | N/A | mA |
| | | LX45 | 5.0 | 5.0 | 5.0 | 5.0 | mA |
| | | LX45T | 5.0 | 5.0 | 5.0 | N/A | mA |
| | | LX75 | 7.0 | 7.0 | 7.0 | 7.0 | mA |
| | | LX75T | 7.0 | 7.0 | 7.0 | N/A | mA |
| | | LX100 | 9.0 | 9.0 | 9.0 | 9.0 | mA |
| | | LX100T | 9.0 | 9.0 | 9.0 | N/A | mA |
| | | LX150 | 12.0 | 12.0 | 12.0 | 12.0 | mA |
| | | LX150T | 12.0 | 12.0 | 12.0 | N/A | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C junction temperatures (Tj). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 25°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. Nominal $V_{CCINT}$ is 1.20V; use the XPE tool to calculate 1.23V values for the nominal $V_{CCINT}$ of the extended performance range.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

*Table 6:* **Power Supply Ramp Time**

| Symbol | Description | Speed Grade | Ramp Time | Units |
|---|---|---|---|---|
| $V_{CCINTR}$ | Internal supply voltage ramp time | -3, -3N, -2 | 0.20 to 50.0 | ms |
| | | -1L | 0.20 to 40.0 | ms |
| $V_{CCO2}$(1) | Output drivers bank 2 supply voltage ramp time | All | 0.20 to 50.0 | ms |
| $V_{CCAUXR}$ | Auxiliary supply voltage ramp time | All | 0.20 to 50.0 | ms |

**Notes:**

1. The minimum $V_{CCO2}$ for power-on reset and configuration is 1.65V.
2. Spartan-6 FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply. Use the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools to estimate current drain on these supplies. Spartan-6 devices do not have a required power-on sequence.

## SelectIO™ Interface DC Input and Output Levels

*Table 7:* **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

| I/O Standard | $V_{CCO}$ for Drivers[1] | | | $V_{REF}$ for Inputs | | |
|---|---|---|---|---|---|---|
| | V, Min | V, Nom | V, Max | V, Min | V, Nom | V, Max |
| LVTTL | 3.0 | 3.3 | 3.45 | $V_{REF}$ is not used for these I/O standards | | |
| LVCMOS33 | 3.0 | 3.3 | 3.45 | | | |
| LVCMOS25 | 2.3 | 2.5 | 2.7 | | | |
| LVCMOS18 | 1.65 | 1.8 | 1.95 | | | |
| LVCMOS18_JEDEC | 1.65 | 1.8 | 1.95 | | | |
| LVCMOS15 | 1.4 | 1.5 | 1.6 | | | |
| LVCMOS15_JEDEC | 1.4 | 1.5 | 1.6 | | | |
| LVCMOS12 | 1.1 | 1.2 | 1.3 | | | |
| LVCMOS12_JEDEC | 1.1 | 1.2 | 1.3 | | | |
| PCI33_3[2] | 3.0 | 3.3 | 3.45 | | | |
| PCI66_3[2] | 3.0 | 3.3 | 3.45 | | | |
| I2C | 2.7 | 3.0 | 3.45 | | | |
| SMBUS | 2.7 | 3.0 | 3.45 | | | |
| SDIO | 3.0 | 3.3 | 3.45 | | | |
| MOBILE_DDR | 1.7 | 1.8 | 1.9 | | | |
| HSTL_I | 1.4 | 1.5 | 1.6 | 0.68 | 0.75 | 0.9 |
| HSTL_II | 1.4 | 1.5 | 1.6 | 0.68 | 0.75 | 0.9 |
| HSTL_III | 1.4 | 1.5 | 1.6 | – | 0.9 | – |
| HSTL_I_18 | 1.7 | 1.8 | 1.9 | 0.8 | 0.9 | 1.1 |
| HSTL_II_18 | 1.7 | 1.8 | 1.9 | – | 0.9 | – |
| HSTL_III_18 | 1.7 | 1.8 | 1.9 | – | 1.1 | – |
| SSTL3_I | 3.0 | 3.3 | 3.45 | 1.3 | 1.5 | 1.7 |
| SSTL3_II | 3.0 | 3.3 | 3.45 | 1.3 | 1.5 | 1.7 |
| SSTL2_I | 2.3 | 2.5 | 2.7 | 1.13 | 1.25 | 1.38 |
| SSTL2_II | 2.3 | 2.5 | 2.7 | 1.13 | 1.25 | 1.38 |
| SSTL18_I | 1.7 | 1.8 | 1.9 | 0.833 | 0.9 | 0.969 |
| SSTL18_II | 1.7 | 1.8 | 1.9 | 0.833 | 0.9 | 0.969 |
| SSTL15_II | 1.425 | 1.5 | 1.575 | 0.69 | 0.75 | 0.81 |

**Notes:**

1. $V_{CCO}$ range required when using I/O standard for an output. Also required for MOBILE_DDR, PCI33_3, LVCMOS18_JEDEC, LVCMOS15_JEDEC, and LVCMOS12_JEDEC inputs, and for LVCMOS25 inputs when $V_{CCAUX}$ = 3.3V.
2. For PCI systems, the transmitter and receiver should have common supplies for $V_{CCO}$.

*Table 8:* **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

| I/O Standard | $V_{CCO}$ for Drivers | | |
|---|---|---|---|
| | V, Min | V, Nom | V, Max |
| LVDS_33 | 3.0 | 3.3 | 3.45 |
| LVDS_25 | 2.25 | 2.5 | 2.75 |
| BLVDS_25 | 2.25 | 2.5 | 2.75 |
| MINI_LVDS_33 | 3.0 | 3.3 | 3.45 |
| MINI_LVDS_25 | 2.25 | 2.5 | 2.75 |
| LVPECL_33(1) | N/A–Inputs Only | | |
| LVPECL_25 | N/A–Inputs Only | | |
| RSDS_33 | 3.0 | 3.3 | 3.45 |
| RSDS_25 | 2.25 | 2.5 | 2.75 |
| TMDS_33(1) | 3.14 | 3.3 | 3.45 |
| PPDS_33 | 3.0 | 3.3 | 3.45 |
| PPDS_25 | 2.25 | 2.5 | 2.75 |
| DISPLAY_PORT | 2.3 | 2.5 | 2.7 |
| DIFF_MOBILE_DDR | 1.7 | 1.8 | 1.9 |
| DIFF_HSTL_I | 1.4 | 1.5 | 1.6 |
| DIFF_HSTL_II | 1.4 | 1.5 | 1.6 |
| DIFF_HSTL_III | 1.4 | 1.5 | 1.6 |
| DIFF_HSTL_I_18 | 1.7 | 1.8 | 1.9 |
| DIFF_HSTL_II_18 | 1.7 | 1.8 | 1.9 |
| DIFF_HSTL_III_18 | 1.7 | 1.8 | 1.9 |
| DIFF_SSTL3_I | 3.0 | 3.3 | 3.45 |
| DIFF_SSTL3_II | 3.0 | 3.3 | 3.45 |
| DIFF_SSTL2_I | 2.3 | 2.5 | 2.7 |
| DIFF_SSTL2_II | 2.3 | 2.5 | 2.7 |
| DIFF_SSTL18_I | 1.7 | 1.8 | 1.9 |
| DIFF_SSTL18_II | 1.7 | 1.8 | 1.9 |
| DIFF_SSTL15_II | 1.425 | 1.5 | 1.575 |

**Notes:**

1. LVPECL_33 and TMDS_33 inputs require $V_{CCAUX}$ = 3.3V nominal.

*Table 10:* **Differential I/O Standard DC Input and Output Levels**

| I/O Standard | $V_{ID}$ | | $V_{ICM}$ | | $V_{OD}$ | | $V_{OCM}$ | | $V_{OH}$ | $V_{OL}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| | mV, Min | mV, Max | V, Min | V, Max | mV, Min | mV, Max | V, Min | V, Max | V, Min | V, Max |
| LVDS_33[2][3] | 100 | 600 | 0.3 | 2.35 | 247 | 454 | 1.125 | 1.375 | – | – |
| LVDS_25[2][3] | 100 | 600 | 0.3 | 2.35 | 247 | 454 | 1.125 | 1.375 | – | – |
| BLVDS_25[2][3] | 100 | – | 0.3 | 2.35 | 240 | 460 | Typical 50% $V_{CCO}$ | | – | – |
| MINI_LVDS_33 | 200 | 600 | 0.3 | 1.95 | 300 | 600 | 1.0 | 1.4 | – | – |
| MINI_LVDS_25 | 200 | 600 | 0.3 | 1.95 | 300 | 600 | 1.0 | 1.4 | – | – |
| LVPECL_33[2][3] | 100 | 1000 | 0.3 | 2.8[1] | Inputs only | | | | | |
| LVPECL_25[2][3] | 100 | 1000 | 0.3 | 1.95 | Inputs only | | | | | |
| RSDS_33[2][3] | 100 | – | 0.3 | 1.5 | 100 | 400 | 1.0 | 1.4 | – | – |
| RSDS_25[2][3] | 100 | – | 0.3 | 1.5 | 100 | 400 | 1.0 | 1.4 | – | – |
| TMDS_33 | 150 | 1200 | 2.7 | 3.23[1] | 400 | 800 | $V_{CCO}$ – 0.405 | $V_{CCO}$ – 0.190 | – | – |
| PPDS_33[2][3] | 100 | 400 | 0.2 | 2.3 | 100 | 400 | 0.5 | 1.4 | – | – |
| PPDS_25[2][3] | 100 | 400 | 0.2 | 2.3 | 100 | 400 | 0.5 | 1.4 | – | – |
| DISPLAY_PORT | 190 | 1260 | 0.3 | 2.35 | – | – | Typical 50% $V_{CCO}$ | | – | – |
| DIFF_MOBILE_DDR | 100 | – | 0.78 | 1.02 | – | – | – | – | 90% $V_{CCO}$ | 10% $V_{CCO}$ |
| DIFF_HSTL_I | 100 | – | 0.68 | 0.9 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_HSTL_II | 100 | – | 0.68 | 0.9 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_HSTL_III | 100 | – | 0.68 | 0.9 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_HSTL_I_18 | 100 | – | 0.8 | 1.1 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_HSTL_II_18 | 100 | – | 0.8 | 1.1 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_HSTL_III_18 | 100 | – | 0.8 | 1.1 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_SSTL3_I | 100 | – | 1.0 | 1.9 | – | – | – | – | $V_{TT}$ + 0.6 | $V_{TT}$ – 0.6 |
| DIFF_SSTL3_II | 100 | – | 1.0 | 1.9 | – | – | – | – | $V_{TT}$ + 0.8 | $V_{TT}$ – 0.8 |
| DIFF_SSTL2_I | 100 | – | 1.0 | 1.5 | – | – | – | – | $V_{TT}$ + 0.61 | $V_{TT}$ – 0.61 |
| DIFF_SSTL2_II | 100 | – | 1.0 | 1.5 | – | – | – | – | $V_{TT}$ + 0.81 | $V_{TT}$ – 0.81 |
| DIFF_SSTL18_I | 100 | – | 0.7 | 1.1 | – | – | – | – | $V_{TT}$ + 0.47 | $V_{TT}$ – 0.47 |
| DIFF_SSTL18_II | 100 | – | 0.7 | 1.1 | – | – | – | – | $V_{TT}$ + 0.6 | $V_{TT}$ – 0.6 |
| DIFF_SSTL15_II | 100 | – | 0.55 | 0.95 | – | – | – | – | $V_{TT}$ + 0.4 | $V_{TT}$ – 0.4 |

**Notes:**

1. LVPECL_33 and TMDS_33 maximum $V_{ICM}$ is the lower of V (maximum) or $V_{CCAUX}$ – ($V_{ID}$/2)
2. When $V_{CCAUX}$ = 3.3V, the DCD can be higher than 5% for $V_{ICM}$ < 0.7V when using these I/O standards: LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, LVPECL_33, RSDS_25, RSDS_33, PPDS_25, and PPDS_33.
3. The -1L devices require $V_{CCAUX}$ = 2.5V when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.

*Table 21:* **GTP Transceiver User Clock Switching Characteristics(1)**

| Symbol | Description | Conditions | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| $F_{TXOUT}$ | TXOUTCLK maximum frequency | | 320 | 320 | 270 | N/A | MHz |
| $F_{RXREC}$ | RXRECCLK maximum frequency | | 320 | 320 | 270 | N/A | MHz |
| $T_{RX}$ | RXUSRCLK maximum frequency | | 320 | 320 | 270 | N/A | MHz |
| $T_{RX2}$ | RXUSRCLK2 maximum frequency | 1 byte interface | 156.25 | 156.25 | 125 | N/A | MHz |
| | | 2 byte interface | 160 | 160 | 125 | N/A | MHz |
| | | 4 byte interface | 80 | 80 | 67.5 | N/A | MHz |
| $T_{TX}$ | TXUSRCLK maximum frequency | | 320 | 320 | 270 | N/A | MHz |
| $T_{TX2}$ | TXUSRCLK2 maximum frequency | 1 byte interface | 156.25 | 156.25 | 125 | N/A | MHz |
| | | 2 byte interface | 160 | 160 | 125 | N/A | MHz |
| | | 4 byte interface | 80 | 80 | 67.5 | N/A | MHz |

**Notes:**
1. Clocking must be implemented as described in UG386: *Spartan-6 FPGA GTP Transceivers User Guide*.

*Table 22:* **GTP Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{RTX}$ | TX Rise time | 20%–80% | – | 140 | – | ps |
| $T_{FTX}$ | TX Fall time | 80%–20% | – | 120 | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | – | – | 400 | ps |
| $V_{TXOOBVDPP}$ | Electrical idle amplitude | | – | – | 20 | mV |
| $T_{TXOOBTRANSITION}$ | Electrical idle transition time | | – | – | 50 | ns |
| $T_{J3.125}$ | Total Jitter(2) | 3.125 Gb/s | – | – | 0.35 | UI |
| $D_{J3.125}$ | Deterministic Jitter(2) | | – | – | 0.15 | UI |
| $T_{J2.5}$ | Total Jitter(2) | 2.5 Gb/s | – | – | 0.33 | UI |
| $D_{J2.5}$ | Deterministic Jitter(2) | | – | – | 0.15 | UI |
| $T_{J1.62}$ | Total Jitter(2) | 1.62 Gb/s | – | – | 0.20 | UI |
| $D_{J1.62}$ | Deterministic Jitter(2) | | – | – | 0.10 | UI |
| $T_{J1.25}$ | Total Jitter(2) | 1.25 Gb/s | – | – | 0.20 | UI |
| $D_{J1.25}$ | Deterministic Jitter(2) | | – | – | 0.10 | UI |
| $T_{J614}$ | Total Jitter(2) | 614 Mb/s | – | – | 0.10 | UI |
| $D_{J614}$ | Deterministic Jitter(2) | | – | – | 0.05 | UI |

**Notes:**
1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP transceiver sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics, page 19.

*Table 25:* **Interface Performances**

| Description | I/O Resource | Clock Buffer | Data Width | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | -3 | -3N | -2 | -1L | |
| **Networking Applications(1)** | | | | | | | | |
| SDR LVDS transmitter or receiver | IOB SDR register | BUFG | – | 400 | 400 | 375 | 250 | Mb/s |
| DDR LVDS transmitter or receiver | ODDR2/IDDR2 register | 2 BUFGs | – | 800 | 800 | 750 | 500 | Mb/s |
| SDR LVDS transmitter | OSERDES2 | BUFPLL | 2 | 500 | 500 | 500 | 250 | Mb/s |
| | | | 3 | 750 | 750 | 750 | 375 | Mb/s |
| | | | 4-8 | 1080 | 1050 | 950 | 500 | Mb/s |
| DDR LVDS transmitter | OSERDES2 | 2 BUFIO2s | 2 | 500 | 500 | 500 | 250 | Mb/s |
| | | | 3 | 750 | 750 | 750 | 375 | Mb/s |
| | | | 4-8 | 1080 | 1050 | 950 | 500 | Mb/s |
| SDR LVDS receiver | ISERDES2 in RETIMED mode | BUFPLL | 2 | 500 | 500 | 500 | — | Mb/s |
| | | | 3 | 750 | 750 | 750 | — | Mb/s |
| | | | 4-8 | 1080 | 1050 | 950 | — | Mb/s |
| DDR LVDS receiver | ISERDES2 in RETIMED mode | 2 BUFIO2s | 2 | 500 | 500 | 500 | — | Mb/s |
| | | | 3 | 750 | 750 | 750 | — | Mb/s |
| | | | 4-8 | 1080 | 1050 | 950 | — | Mb/s |
| **Memory Interfaces (Implemented using the Spartan-6 FPGA Memory Controller Block)(2)** | | | | | | | | |
| **Standard Performance (Standard $V_{CCINT}$)** | | | | | | | | |
| DDR | | | | 400 | Note 4 | 400 | 350 | Mb/s |
| DDR2 | | | | 667 | Note 4 | 625 | 400 | Mb/s |
| DDR3 | | | | 800 | Note 4 | 667 | — | Mb/s |
| LPDDR (Mobile_DDR) | | | | 400 | Note 4 | 400 | 350 | Mb/s |
| **Extended Performance (Requires Extended Performance $V_{CCINT}$)(3)** | | | | | | | | |
| DDR2 | | | | 800 | Note 4 | 667 | — | Mb/s |

**Notes:**

1. Refer to XAPP1064, *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)* and UG381, *Spartan-6 FPGA SelectIO Resources User Guide.*
2. Refer to UG388, *Spartan-6 FPGA Memory Controller User Guide*.
3. Extended Memory Controller block performance for DDR2 can be achieved using the extended performance $V_{CCINT}$ range from Table 2.
4. The LX4 device, all devices in the TQG144 and CPG196 packages, and the -3N speed grade do not support a Memory Controller Block.

## Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 27 lists the production released Spartan-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE® software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

*Table 27:* **Spartan-6 Device Production Software and Speed Specification Release(1)**

| Device | Speed Grade Designations(2) | | | |
|---|---|---|---|---|
| | -3(3) | -3N | -2(4) | -1L |
| XC6SLX4 | ISE 12.4 v1.15 | N/A | ISE 12.3 v1.12(5) | ISE 13.2 v1.07 |
| XC6SLX9 | ISE 12.4 v1.15 | ISE 13.1 Update v1.18(7) | ISE 12.3 v1.12(5) | ISE 13.2 v1.07 |
| XC6SLX16 | ISE 12.1 v1.08 | ISE 13.1 Update v1.18(7) | ISE 11.5 v1.06 | ISE 13.2 v1.07 |
| XC6SLX25 | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | ISE 13.2 v1.07 |
| XC6SLX25T | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | N/A |
| XC6SLX45 | ISE 12.1 v1.08 | ISE 13.1 Update v1.18(7) | ISE 11.5 v1.07 | ISE 13.1 v1.06 |
| XC6SLX45T | ISE 12.1 v1.08 | ISE 13.1 Update v1.18(7) | ISE 12.1 v1.08 | N/A |
| XC6SLX75 | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | ISE 13.2 v1.07 |
| XC6SLX75T | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | N/A |
| XC6SLX100 | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | ISE 13.1 v1.06 |
| XC6SLX100T | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | N/A |
| XC6SLX150 | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | ISE 13.1 v1.06 |
| XC6SLX150T | ISE 12.2 v1.11(6) | ISE 13.1 Update v1.18(7) | ISE 12.2 v1.11(6) | N/A |
| XA6SLX4 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX9 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX16 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX25 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX25T | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX45 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX45T | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX75 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX75T | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX100 | N/A | N/A | ISE 13.3 v1.20 | N/A |

*Table 28:* **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -3N | -2 | -1L[1] | -3 | -3N | -2 | -1L[1] | -3 | -3N | -2 | -1L[1] | |
| LVTTL, QUIETIO, 2 mA | 1.35 | 1.47 | 1.60 | 1.82 | 5.39 | 5.53 | 5.73 | 6.37 | 5.39 | 5.53 | 5.73 | 6.37 | ns |
| LVTTL, QUIETIO, 4 mA | 1.35 | 1.47 | 1.60 | 1.82 | 4.29 | 4.43 | 4.63 | 5.22 | 4.29 | 4.43 | 4.63 | 5.22 | ns |
| LVTTL, QUIETIO, 6 mA | 1.35 | 1.47 | 1.60 | 1.82 | 3.75 | 3.89 | 4.09 | 4.69 | 3.75 | 3.89 | 4.09 | 4.69 | ns |
| LVTTL, QUIETIO, 8 mA | 1.35 | 1.47 | 1.60 | 1.82 | 3.23 | 3.37 | 3.57 | 4.20 | 3.23 | 3.37 | 3.57 | 4.20 | ns |
| LVTTL, QUIETIO, 12 mA | 1.35 | 1.47 | 1.60 | 1.82 | 3.28 | 3.42 | 3.62 | 4.22 | 3.28 | 3.42 | 3.62 | 4.22 | ns |
| LVTTL, QUIETIO, 16 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.94 | 3.08 | 3.28 | 3.92 | 2.94 | 3.08 | 3.28 | 3.92 | ns |
| LVTTL, QUIETIO, 24 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.69 | 2.83 | 3.03 | 3.67 | 2.69 | 2.83 | 3.03 | 3.67 | ns |
| LVTTL, Slow, 2 mA | 1.35 | 1.47 | 1.60 | 1.82 | 4.36 | 4.50 | 4.70 | 5.30 | 4.36 | 4.50 | 4.70 | 5.30 | ns |
| LVTTL, Slow, 4 mA | 1.35 | 1.47 | 1.60 | 1.82 | 3.17 | 3.31 | 3.51 | 4.16 | 3.17 | 3.31 | 3.51 | 4.16 | ns |
| LVTTL, Slow, 6 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.76 | 2.90 | 3.10 | 3.75 | 2.76 | 2.90 | 3.10 | 3.75 | ns |
| LVTTL, Slow, 8 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.59 | 2.73 | 2.93 | 3.55 | 2.59 | 2.73 | 2.93 | 3.55 | ns |
| LVTTL, Slow, 12 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.58 | 2.72 | 2.92 | 3.54 | 2.58 | 2.72 | 2.92 | 3.54 | ns |
| LVTTL, Slow, 16 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.39 | 2.53 | 2.73 | 3.40 | 2.39 | 2.53 | 2.73 | 3.40 | ns |
| LVTTL, Slow, 24 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.28 | 2.42 | 2.62 | 3.24 | 2.28 | 2.42 | 2.62 | 3.24 | ns |
| LVTTL, Fast, 2 mA | 1.35 | 1.47 | 1.60 | 1.82 | 3.78 | 3.92 | 4.12 | 4.74 | 3.78 | 3.92 | 4.12 | 4.74 | ns |
| LVTTL, Fast, 4 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.49 | 2.63 | 2.83 | 3.45 | 2.49 | 2.63 | 2.83 | 3.45 | ns |
| LVTTL, Fast, 6 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.44 | 2.58 | 2.78 | 3.40 | 2.44 | 2.58 | 2.78 | 3.40 | ns |
| LVTTL, Fast, 8 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.32 | 2.46 | 2.66 | 3.28 | 2.32 | 2.46 | 2.66 | 3.28 | ns |
| LVTTL, Fast, 12 mA | 1.35 | 1.47 | 1.60 | 1.82 | 1.83 | 1.97 | 2.17 | 2.79 | 1.83 | 1.97 | 2.17 | 2.79 | ns |
| LVTTL, Fast, 16 mA | 1.35 | 1.47 | 1.60 | 1.82 | 1.83 | 1.97 | 2.17 | 2.79 | 1.83 | 1.97 | 2.17 | 2.79 | ns |
| LVTTL, Fast, 24 mA | 1.35 | 1.47 | 1.60 | 1.82 | 1.83 | 1.97 | 2.17 | 2.79 | 1.83 | 1.97 | 2.17 | 2.79 | ns |
| LVCMOS33, QUIETIO, 2 mA | 1.34 | 1.46 | 1.59 | 1.82 | 5.40 | 5.54 | 5.74 | 6.37 | 5.40 | 5.54 | 5.74 | 6.37 | ns |
| LVCMOS33, QUIETIO, 4 mA | 1.34 | 1.46 | 1.59 | 1.82 | 4.03 | 4.17 | 4.37 | 5.01 | 4.03 | 4.17 | 4.37 | 5.01 | ns |
| LVCMOS33, QUIETIO, 6 mA | 1.34 | 1.46 | 1.59 | 1.82 | 3.51 | 3.65 | 3.85 | 4.47 | 3.51 | 3.65 | 3.85 | 4.47 | ns |
| LVCMOS33, QUIETIO, 8 mA | 1.34 | 1.46 | 1.59 | 1.82 | 3.37 | 3.51 | 3.71 | 4.33 | 3.37 | 3.51 | 3.71 | 4.33 | ns |
| LVCMOS33, QUIETIO, 12 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.94 | 3.08 | 3.28 | 3.93 | 2.94 | 3.08 | 3.28 | 3.93 | ns |
| LVCMOS33, QUIETIO, 16 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.77 | 2.91 | 3.11 | 3.78 | 2.77 | 2.91 | 3.11 | 3.78 | ns |
| LVCMOS33, QUIETIO, 24 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.59 | 2.73 | 2.93 | 3.58 | 2.59 | 2.73 | 2.93 | 3.58 | ns |
| LVCMOS33, Slow, 2 mA | 1.34 | 1.46 | 1.59 | 1.82 | 4.37 | 4.51 | 4.71 | 5.28 | 4.37 | 4.51 | 4.71 | 5.28 | ns |
| LVCMOS33, Slow, 4 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.98 | 3.12 | 3.32 | 3.94 | 2.98 | 3.12 | 3.32 | 3.94 | ns |
| LVCMOS33, Slow, 6 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.58 | 2.72 | 2.92 | 3.61 | 2.58 | 2.72 | 2.92 | 3.61 | ns |
| LVCMOS33, Slow, 8 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.65 | 2.79 | 2.99 | 3.61 | 2.65 | 2.79 | 2.99 | 3.61 | ns |
| LVCMOS33, Slow, 12 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.39 | 2.53 | 2.73 | 3.31 | 2.39 | 2.53 | 2.73 | 3.31 | ns |
| LVCMOS33, Slow, 16 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.31 | 2.45 | 2.65 | 3.27 | 2.31 | 2.45 | 2.65 | 3.27 | ns |
| LVCMOS33, Slow, 24 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.28 | 2.42 | 2.62 | 3.24 | 2.28 | 2.42 | 2.62 | 3.24 | ns |
| LVCMOS33, Fast, 2 mA | 1.34 | 1.46 | 1.59 | 1.82 | 3.76 | 3.90 | 4.10 | 4.70 | 3.76 | 3.90 | 4.10 | 4.70 | ns |
| LVCMOS33, Fast, 4 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.48 | 2.62 | 2.82 | 3.44 | 2.48 | 2.62 | 2.82 | 3.44 | ns |
| LVCMOS33, Fast, 6 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.32 | 2.46 | 2.66 | 3.28 | 2.32 | 2.46 | 2.66 | 3.28 | ns |

*Table 29:* **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices[1] *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | $T_{IOOP}$ | | $T_{IOTP}$ | | Units |
|---|---|---|---|---|---|---|---|
| | Speed Grade | | Speed Grade | | Speed Grade | | |
| | -3 | -2 | -3 | -2 | -3 | -2 | |
| LVCMOS15, QUIETIO, 2 mA | 1.05 | 1.23 | 5.63 | 5.83 | 5.63 | 5.83 | ns |
| LVCMOS15, QUIETIO, 4 mA | 1.05 | 1.23 | 4.75 | 4.95 | 4.75 | 4.95 | ns |
| LVCMOS15, QUIETIO, 6 mA | 1.05 | 1.23 | 4.21 | 4.41 | 4.21 | 4.41 | ns |
| LVCMOS15, QUIETIO, 8 mA | 1.05 | 1.23 | 4.05 | 4.25 | 4.05 | 4.25 | ns |
| LVCMOS15, QUIETIO, 12 mA | 1.05 | 1.23 | 3.74 | 3.94 | 3.74 | 3.94 | ns |
| LVCMOS15, QUIETIO, 16 mA | 1.05 | 1.23 | 3.52 | 3.72 | 3.52 | 3.72 | ns |
| LVCMOS15, Slow, 2 mA | 1.05 | 1.23 | 4.32 | 4.52 | 4.32 | 4.52 | ns |
| LVCMOS15, Slow, 4 mA | 1.05 | 1.23 | 3.58 | 3.78 | 3.58 | 3.78 | ns |
| LVCMOS15, Slow, 6 mA | 1.05 | 1.23 | 2.45 | 2.65 | 2.45 | 2.65 | ns |
| LVCMOS15, Slow, 8 mA | 1.05 | 1.23 | 2.46 | 2.66 | 2.46 | 2.66 | ns |
| LVCMOS15, Slow, 12 mA | 1.05 | 1.23 | 2.17 | 2.37 | 2.17 | 2.37 | ns |
| LVCMOS15, Slow, 16 mA | 1.05 | 1.23 | 2.15 | 2.35 | 2.15 | 2.35 | ns |
| LVCMOS15, Fast, 2 mA | 1.05 | 1.23 | 3.43 | 3.63 | 3.43 | 3.63 | ns |
| LVCMOS15, Fast, 4 mA | 1.05 | 1.23 | 2.42 | 2.62 | 2.42 | 2.62 | ns |
| LVCMOS15, Fast, 6 mA | 1.05 | 1.23 | 1.92 | 2.12 | 1.92 | 2.12 | ns |
| LVCMOS15, Fast, 8 mA | 1.05 | 1.23 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVCMOS15, Fast, 12 mA | 1.05 | 1.23 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVCMOS15, Fast, 16 mA | 1.05 | 1.23 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVCMOS15_JEDEC, QUIETIO, 2 mA | 1.10 | 1.28 | 5.64 | 5.84 | 5.64 | 5.84 | ns |
| LVCMOS15_JEDEC, QUIETIO, 4 mA | 1.10 | 1.28 | 4.75 | 4.95 | 4.75 | 4.95 | ns |
| LVCMOS15_JEDEC, QUIETIO, 6 mA | 1.10 | 1.28 | 4.21 | 4.41 | 4.21 | 4.41 | ns |
| LVCMOS15_JEDEC, QUIETIO, 8 mA | 1.10 | 1.28 | 4.06 | 4.26 | 4.06 | 4.26 | ns |
| LVCMOS15_JEDEC, QUIETIO, 12 mA | 1.10 | 1.28 | 3.75 | 3.95 | 3.75 | 3.95 | ns |
| LVCMOS15_JEDEC, QUIETIO, 16 mA | 1.10 | 1.28 | 3.53 | 3.73 | 3.53 | 3.73 | ns |
| LVCMOS15_JEDEC, Slow, 2 mA | 1.10 | 1.28 | 4.32 | 4.52 | 4.32 | 4.52 | ns |
| LVCMOS15_JEDEC, Slow, 4 mA | 1.10 | 1.28 | 3.56 | 3.76 | 3.56 | 3.76 | ns |
| LVCMOS15_JEDEC, Slow, 6 mA | 1.10 | 1.28 | 2.44 | 2.64 | 2.44 | 2.64 | ns |
| LVCMOS15_JEDEC, Slow, 8 mA | 1.10 | 1.28 | 2.47 | 2.67 | 2.47 | 2.67 | ns |
| LVCMOS15_JEDEC, Slow, 12 mA | 1.10 | 1.28 | 2.15 | 2.35 | 2.15 | 2.35 | ns |
| LVCMOS15_JEDEC, Slow, 16 mA | 1.10 | 1.28 | 2.15 | 2.35 | 2.15 | 2.35 | ns |
| LVCMOS15_JEDEC, Fast, 2 mA | 1.10 | 1.28 | 3.43 | 3.63 | 3.43 | 3.63 | ns |
| LVCMOS15_JEDEC, Fast, 4 mA | 1.10 | 1.28 | 2.42 | 2.62 | 2.42 | 2.62 | ns |
| LVCMOS15_JEDEC, Fast, 6 mA | 1.10 | 1.28 | 1.92 | 2.12 | 1.92 | 2.12 | ns |
| LVCMOS15_JEDEC, Fast, 8 mA | 1.10 | 1.28 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVCMOS15_JEDEC, Fast, 12 mA | 1.10 | 1.28 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVCMOS15_JEDEC, Fast, 16 mA | 1.10 | 1.28 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVCMOS12, QUIETIO, 2 mA | 0.98 | 1.16 | 6.54 | 6.74 | 6.54 | 6.74 | ns |
| LVCMOS12, QUIETIO, 4 mA | 0.98 | 1.16 | 5.12 | 5.32 | 5.12 | 5.32 | ns |

# I/O Standard Measurement Methodology

## Input Delay Measurements

Table 31 shows the test setup parameters used for measuring input delay.

*Table 31:* **Input Delay Measurement Methodology**

| Description | I/O Standard Attribute | $V_L$[1] | $V_H$[1] | $V_{MEAS}$[3][4] | $V_{REF}$[2][4] |
|---|---|---|---|---|---|
| LVTTL (Low-Voltage Transistor-Transistor Logic) | LVTTL | 0 | 3.0 | 1.4 | – |
| LVCMOS (Low-Voltage CMOS), 3.3V | LVCMOS33 | 0 | 3.3 | 1.65 | – |
| LVCMOS, 2.5V | LVCMOS25 | 0 | 2.5 | 1.25 | – |
| LVCMOS, 1.8V | LVCMOS18 | 0 | 1.8 | 0.9 | – |
| LVCMOS, 1.5V | LVCMOS15 | 0 | 1.5 | 0.75 | – |
| LVCMOS, 1.2V | LVCMOS12 | 0 | 1.2 | 0.6 | – |
| PCI (Peripheral Component Interface), 33 MHz and 66 MHz, 3.3V | PCI33_3, PCI66_3 | Per PCI Specification | | | – |
| HSTL (High-Speed Transceiver Logic), Class I & II | HSTL_I, HSTL_II | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.75 |
| HSTL, Class III | HSTL_III | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| HSTL, Class I & II, 1.8V | HSTL_I_18, HSTL_II_18 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| HSTL, Class III 1.8V | HSTL_III_18 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 1.1 |
| SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V | SSTL3_I, SSTL3_II | $V_{REF}$ – 0.75 | $V_{REF}$ + 0.75 | $V_{REF}$ | 1.5 |
| SSTL, Class I & II, 2.5V | SSTL2_I, SSTL2_II | $V_{REF}$ – 0.75 | $V_{REF}$ + 0.75 | $V_{REF}$ | 1.25 |
| SSTL, Class I & II, 1.8V | SSTL18_I, SSTL18_II | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| SSTL, Class II, 1.5V | SSTL15_II | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 0.75 |
| LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V | LVDS_25, LVDS_33 | 1.25 – 0.125 | 1.25 + 0.125 | 0[5] | – |
| LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V & 3.3V | LVPECL_25, LVPECL_33 | 1.2 – 0.3 | 1.2 + 0.3 | 0[5] | – |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | 1.3 – 0.125 | 1.3 + 0.125 | 0[5] | – |
| Mini-LVDS, 2.5V & 3.3V | MINI_LVDS_25, MINI_LVDS_33 | 1.2 – 0.125 | 1.2 + 0.125 | 0[5] | – |
| RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V | RSDS_25, RSDS_33 | 1.2 – 0.1 | 1.2 + 0.1 | 0[5] | – |
| TMDS (Transition Minimized Differential Signaling), 3.3V | TMDS_33 | 3.0 – 0.1 | 3.0 + 0.1 | 0[5] | – |
| PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V | PPDS_25, PPDS_33 | 1.25 – 0.1 | 1.25 + 0.1 | 0[5] | – |

**Notes:**
1. Input waveform switches between $V_L$ and $V_H$.
2. Measurements are made at typical, minimum, and maximum $V_{REF}$ values. Reported delays reflect worst case of these measurements. $V_{REF}$ values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the $V_{REF}$ / $V_{MEAS}$ parameters found in IBIS models and/or noted in Figure 4.
5. The value given is the differential input voltage.

*Table 32:* **Output Delay Measurement Methodology *(Cont'd)***

| Description | I/O Standard Attribute | $R_{REF}$ (Ω) | $C_{REF}$[1] (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| SSTL, Class II, 2.5V | SSTL2_II | 25 | 0 | $V_{REF}$ | 1.25 |
| SSTL, Class II, 1.5V | SSTL15_II | 25 | 0 | $V_{REF}$ | 0.75 |
| LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V | LVDS_25, LVDS_33 | 100 | 0 | 0[3] | – |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | Note 4 | 0 | 0[3] | – |
| Mini-LVDS, 2.5V & 3.3V | MINI_LVDS_25, MINI_LVDS_33 | 100 | 0 | 0[3] | – |
| RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V | RSDS_25, RSDS_33 | 100 | 0 | 0[3] | – |
| TMDS (Transition Minimized Differential Signaling), 3.3V | TMDS_33 | Note 5 | 0 | 0[3] | – |
| PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V | PPDS_25, PPDS_33 | 100 | 0 | 0[3] | – |

**Notes:**
1. $C_{REF}$ is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. The value given is the differential output voltage.
4. See the *BLVDS Output Termination* section in UG381, *Spartan-6 FPGA SelectIO Resources User Guide*.
5. See the *TMDS_33 Termination* section in UG381, *Spartan-6 FPGA SelectIO Resources User Guide*.

## Simultaneously Switching Outputs

Due to package electrical parasitics, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. Table 33 and Table 34 provide guidelines for the recommended maximum allowable number of SSOs. These guidelines describe the maximum number of user I/O pins of an output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise for that particular signal standard. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of GND and power bounce.

For each device/package combination, Table 33 provides the number of equivalent $V_{CCO}$/GND pairs per bank. For each output signal standard and drive strength, Table 34 recommends the maximum number of SSOs, switching in the same direction, allowed per $V_{CCO}$/GND pair within an I/O bank. The guidelines are categorized by package style, slew rate, and output drive current. The number of SSOs are also specified by I/O bank. Multiply the appropriate numbers from each table to calculate the maximum number of SSOs allowed within an I/O bank. The guidelines assume that all pins within a bank use the same I/O standard. Exceeding these SSO guidelines can result in increased power or GND bounce, degraded signal integrity, or increased system jitter. For a given I/O standard, if the SSO limit per pair in Table 34 is greater than the maximum I/O per pair in Table 33, then there is no SSO limit for the exclusive use of that I/O standard.

The recommended maximum SSO values assume that the FPGA is soldered on a printed circuit board and that the board uses sound design practices. Due to the additional inductance introduced by the socket, the SSO values do not apply for FPGAs mounted in sockets. The SSO values assume that the $V_{CCAUX}$ is powered at 3.3V. Setting $V_{CCAUX}$ to 2.5V provides better SSO characteristics. For more detail, see UG381: *Spartan-6 FPGA SelectIO Resources User Guide*.

*Table 34:* **SSO Limit per $V_{CCO}$/GND Pair**

| $V_{CCO}$ | I/O Standard | Drive | Slew | SSO Limit per $V_{CCO}$/GND Pair | | | |
|---|---|---|---|---|---|---|---|
| | | | | All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324 | | All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324 | |
| | | | | Bank 0/2 | Bank 1/3 | Bank 0/2 | Bank 1/3/4/5 |
| 1.2V | LVCMOS12, LVCMOS12_JEDEC | 2 | Fast | 30 (1) | 35 | 30 | 35 |
| | | | Slow | 51 | 55 | 51 | 52 |
| | | | QuietIO | 71 | 58 | 71 | 70 |
| | | 4 | Fast | 17 | 17 | 17 | 19 |
| | | | Slow | 23 | 25 | 23 | 22 |
| | | | QuietIO | 35 | 32 | 35 | 32 |
| | | 6 | Fast | 13 | 15 | 13 | 14 |
| | | | Slow | 19 | 20 | 19 | 17 |
| | | | QuietIO | 26 | 24 | 26 | 24 |
| | | 8 | Fast | N/A | 12 | N/A | 12 |
| | | | Slow | N/A | 15 | N/A | 13 |
| | | | QuietIO | N/A | 20 | N/A | 19 |
| | | 12 | Fast | N/A | 5 | N/A | 4 |
| | | | Slow | N/A | 8 | N/A | 5 |
| | | | QuietIO | N/A | 11 | N/A | 10 |

*Table 34:* **SSO Limit per $V_{CCO}$/GND Pair *(Cont'd)***

| $V_{CCO}$ | I/O Standard | Drive | Slew | SSO Limit per $V_{CCO}$/GND Pair | | | |
|---|---|---|---|---|---|---|---|
| | | | | All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324 | | All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324 | |
| | | | | Bank 0/2 | Bank 1/3 | Bank 0/2 | Bank 1/3/4/5 |
| Various | LVDS_33 | | | 16 | N/A | 16 | N/A |
| | LVDS_25 | | | 20 | N/A | 20 | N/A |
| | BLVDS_25 | | | 20 | 48 | 20 | 20 |
| | MINI_LVDS_33 | | | 13 | N/A | 13 | N/A |
| | MINI_LVDS_25 | | | 18 | N/A | 18 | N/A |
| | RSDS_33 | | | 12 | N/A | 12 | N/A |
| | RSDS_25 | | | 15 | N/A | 15 | N/A |
| | TMDS_33 | | | 83 | N/A | 83 | N/A |
| | PPDS_33 | | | 12 | N/A | 12 | N/A |
| | PPDS_25 | | | 16 | N/A | 16 | N/A |
| | DISPLAY_PORT | | | 42 | 40 | 42 | 30 |
| | I2C | | | 47 | 55 | 47 | 42 |
| | SMBUS | | | 44 | 52 | 44 | 40 |

**Notes:**

1. SSO limits greater than the number of I/O per $V_{CCO}$/GND pair (Table 33) indicate No Limit for the given I/O standard. They are provided in this table to calculate limits when using multiple I/O standards in a bank.
2. Not available (N/A) indicates that the I/O standard is not available in the given bank.
3. When used with the MCB, these signals are exempt from SSO analysis due to the known activity of the MCB switching patterns. SSO performance is validated for all MCB instances. MCB outputs can, in some cases, exceed the SSO limits.

## Input/Output Logic Switching Characteristics

*Table 35:* **ILOGIC2 Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| **Setup/Hold** | | | | | | |
| $T_{ICE0CK}/T_{ICKCE0}$ | CE0 pin Setup/Hold with respect to CLK | 0.56/ –0.30 | 0.56/ –0.25 | 0.79/ –0.22 | 1.21/ –0.52 | ns |
| $T_{ISRCK}/T_{ICKSR}$ | SR pin Setup/Hold with respect to CLK | 0.74/ –0.23 | 0.74/ –0.22 | 0.98/ –0.20 | 1.31/ –0.45 | ns |
| $T_{IDOCK}/T_{IOCKD}$ | D pin Setup/Hold with respect to CLK without Delay | 1.19/ –0.83 | 1.36/ –0.83 | 1.73/ –0.83 | 2.18/ –1.77 | ns |
| $T_{IDOCKD}/T_{IOCKDD}$ | DDLY pin Setup/Hold with respect to CLK (using IODELAY2) | 0.31/ 0.00 | 0.47/ 0.00 | 0.54/ 0.00 | 0.63/ –0.39 | ns |
| **Combinatorial** | | | | | | |
| $T_{IDI}$ | D pin to O pin propagation delay, no Delay | 0.95 | 1.28 | 1.53 | 2.25 | ns |
| $T_{IDID}$ | DDLY pin to O pin propagation delay (using IODELAY2) | 0.23 | 0.39 | 0.44 | 0.74 | ns |
| **Sequential Delays** | | | | | | |
| $T_{IDLO}$ | D pin to Q pin using flip-flop as a latch without Delay | 1.56 | 1.86 | 2.39 | 3.49 | ns |
| $T_{IDLOD}$ | DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY2) | 0.68 | 0.97 | 1.20 | 1.94 | ns |
| $T_{ICKQ}$ | CLK to Q outputs for XC devices | 1.03 | 1.24 | 1.43 | 2.11 | ns |
| | CLK to Q outputs for XA and XQ devices | 1.38 | N/A | 1.78 | 2.11 | ns |
| $T_{RQ\_ILOGIC2}$ | SR pin to Q outputs | 1.81 | 1.81 | 2.50 | 3.05 | ns |

*Table 36:* **OLOGIC2 Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| **Setup/Hold** | | | | | | |
| $T_{ODCK}/T_{OCKD}$ | D1/D2 pins Setup/Hold with respect to CLK | 0.81/ –0.05 | 0.86/ –0.05 | 1.18/ 0.00 | 1.73/ –0.27 | ns |
| $T_{OOCECK}/T_{OCKOCE}$ | OCE pin Setup/Hold with respect to CLK | 0.75/ –0.10 | 0.75/ –0.10 | 1.01/ –0.05 | 1.66/ –0.23 | ns |
| $T_{OSRCK}/T_{OCKSR}$ | SR pin Setup/Hold with respect to CLK | 0.70/ –0.28 | 0.79/ –0.28 | 1.03/ –0.23 | 1.39/ –0.47 | ns |
| $T_{OTCK}/T_{OCKT}$ | T1/T2 pins Setup/Hold with respect to CLK | 0.24/ –0.08 | 0.56/ –0.06 | 0.83/ –0.01 | 0.99/ –0.19 | ns |
| $T_{OTCECK}/T_{OCKTCE}$ | TCE pin Setup/Hold with respect to CLK | 0.58/ –0.06 | 0.72/ –0.06 | 1.18/ –0.01 | 1.51/ –0.13 | ns |
| **Sequential Delays** | | | | | | |
| $T_{OCKQ}$ | CLK to OQ/TQ out for XC devices | 0.48 | 0.51 | 0.74 | 0.74 | ns |
| | CLK to OQ/TQ out for XA and XQ devices | 0.85 | N/A | 1.16 | 0.74 | ns |
| $T_{RQ\_OLOGIC2}$ | SR pin to OQ/TQ out | 1.81 | 1.81 | 2.50 | 3.05 | ns |

## CLB Switching Characteristics (SLICEM Only)

*Table 40:* **CLB Switching Characteristics (SLICEM Only)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| **Combinatorial Delays** | | | | | | |
| $T_{ILO}$ | An – Dn LUT inputs to A to D outputs | 0.21 | 0.26 | 0.26 | 0.46 | ns, Max |
| | An – Dn LUT inputs through F7AMUX/F7BMUX to AMUX/CMUX output | 0.37 | 0.43 | 0.43 | 0.77 | ns, Max |
| $T_{OPAB}$ | An – Dn LUT inputs through F7AMUX or F7BMUX and F8MUX to BMUX output | 0.37 | 0.46 | 0.46 | 0.84 | ns, Max |
| $T_{ITO}$ | An – Dn LUT inputs through latch to AQ – DQ outputs | 0.82 | 0.95 | 0.95 | 1.64 | ns, Max |
| $T_{TITO\_LOGIC}$ | An – Dn LUT inputs to AQ – DQ outputs (latch as logic) | 0.82 | 0.95 | 0.95 | 1.64 | ns, Max |
| $T_{OPCYA}$ | An LUT inputs to COUT output | 0.38 | 0.48 | 0.48 | 0.69 | ns, Max |
| $T_{OPCYB}$ | Bn LUT inputs to COUT output | 0.38 | 0.49 | 0.49 | 0.71 | ns, Max |
| $T_{OPCYC}$ | Cn LUT inputs to COUT output | 0.28 | 0.33 | 0.33 | 0.55 | ns, Max |
| $T_{OPCYD}$ | Dn LUT inputs to COUT output | 0.28 | 0.35 | 0.35 | 0.52 | ns, Max |
| $T_{AXCY}$ | AX input to COUT output | 0.21 | 0.26 | 0.26 | 0.36 | ns, Max |
| $T_{BXCY}$ | BX input to COUT output | 0.13 | 0.16 | 0.16 | 0.18 | ns, Max |
| $T_{CXCY}$ | CX input to COUT output | 0.10 | 0.12 | 0.12 | 0.09 | ns, Max |
| $T_{DXCY}$ | DX input to COUT output | 0.09 | 0.11 | 0.11 | 0.09 | ns, Max |
| $T_{BYP}$ | CIN input to COUT output | 0.08 | 0.10 | 0.10 | 0.06 | ns, Max |
| $T_{CINA}$ | CIN input to AMUX output | 0.21 | 0.22 | 0.22 | 0.47 | ns, Max |
| $T_{CINB}$ | CIN input to BMUX output | 0.30 | 0.31 | 0.31 | 0.57 | ns, Max |
| $T_{CINC}$ | CIN input to CMUX output | 0.29 | 0.31 | 0.31 | 0.58 | ns, Max |
| $T_{CIND}$ | CIN input to DMUX output | 0.31 | 0.32 | 0.32 | 0.68 | ns, Max |
| **Sequential Delays** | | | | | | |
| $T_{CKO}$ | Clock to AQ – DQ outputs | 0.45 | 0.53 | 0.53 | 0.74 | ns, Max |
| **Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK** | | | | | | |
| $T_{DICK}/T_{CKDI}$ | AX – DX input to CLK on A – D flip-flops | 0.42/ 0.28 | 0.47/ 0.39 | 0.47/ 0.39 | 0.90/ 0.56 | ns, Min |
| $T_{CECK}/T_{CKCE}$ | CE input to CLK on A – D flip-flops | 0.31/ –0.07 | 0.37/ –0.07 | 0.37/ –0.07 | 0.59/ –0.27 | ns, Min |
| $T_{SRCK}/T_{CKSR}$ | SR input to CLK on A – D flip-flops for XC devices | 0.41/ 0.02 | 0.42/ 0.02 | 0.42/ 0.02 | 0.68/ –0.29 | ns, Min |
| | SR input to CLK on A – D flip-flops for XA and XQ devices | 0.41/ 0.02 | N/A | 0.44/ 0.02 | 0.68/ –0.29 | ns, Min |
| $T_{CINCK}/T_{CKCIN}$ | CIN input to CLK on A – D flip-flops | 0.31/ –0.17 | 0.31/ –0.13 | 0.31/ –0.13 | 0.81/ –0.42 | ns, Min |
| **Set/Reset** | | | | | | |
| $T_{RPW}$ | SR input minimum pulse width | 0.41 | 0.48 | 0.48 | 1.37 | ns, Min |
| $T_{RQ}$ | Delay from SR input to AQ – DQ flip-flops | 0.60 | 0.70 | 0.70 | 0.88 | ns, Max |
| $T_{CEO}$ | Delay from CE input to AQ – DQ flip-flops | 0.60 | 0.65 | 0.65 | 0.90 | ns, Max |
| $F_{TOG}$ | Toggle frequency (for export control) | 862 | 806 | 667 | 500 | MHz |

*Table 52:* **PLL Specification *(Cont'd)***

| Symbol | Description | Device[1] | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| $F_{INMIN}$ | Minimum Input Clock Frequency | LX devices | 19 | 19 | 19 | 19 | MHz |
| | | LXT devices | 19 | 19 | 19 | N/A | MHz |
| $F_{INJITTER}$ | Maximum Input Clock Period Jitter: 19–200 MHz | All | 1 ns Maximum | | | | |
| | Maximum Input Clock Period Jitter: > 200 MHz | All | <20% of clock input period Maximum | | | | |
| $F_{INDUTY}$ | Allowable Input Duty Cycle: 19—199 MHz | All | 25/75 | | | | % |
| | Allowable Input Duty Cycle: 200—299 MHz | All | 35/65 | | | | % |
| | Allowable Input Duty Cycle: > 300 MHz | All | 45/55 | | | | % |
| $F_{VCOMIN}$ | Minimum PLL VCO Frequency | LX devices | 400 | 400 | 400 | 400 | MHz |
| | | LXT devices | 400 | 400 | 400 | N/A | MHz |
| $F_{VCOMAX}$ | Maximum PLL VCO Frequency | LX devices | 1080 | 1050 | 1000 | 1000 | MHz |
| | | LXT devices | 1080 | 1050 | 1000 | N/A | MHz |
| $F_{BANDWIDTH}$ | Low PLL Bandwidth at Typical[3] | All | 1 | 1 | 1 | 1 | MHz |
| | High PLL Bandwidth at Typical[3] | All | 4 | 4 | 4 | 4 | MHz |
| $T_{STAPHAOFFSET}$ | Static Phase Offset of the PLL Outputs | All | 0.12 | 0.12 | 0.12 | 0.15 | ns |
| $T_{OUTJITTER}$ | PLL Output Jitter[3] | All | Note 2 | | | | |
| $T_{OUTDUTY}$ | PLL Output Clock Duty Cycle Precision[4] | All | 0.15 | 0.15 | 0.20 | 0.25 | ns |
| $T_{LOCKMAX}$ | PLL Maximum Lock Time | All | 100 | 100 | 100 | 100 | µs |
| $F_{OUTMAX}$ | PLL Maximum Output Frequency for BUFGMUX | LX devices | 400 | 400 | 375 | 250 | MHz |
| | | LXT devices | 400 | 400 | 375 | N/A | MHz |
| | PLL Maximum Output Frequency for BUFPLL | LX devices | 1080 | 1050 | 950 | 500 | MHz |
| | | LXT devices | 1080 | 1050 | 950 | N/A | MHz |
| $F_{OUTMIN}$ | PLL Minimum Output Frequency[5] | All | 3.125 | 3.125 | 3.125 | 3.125 | MHz |
| $T_{EXTFDVAR}$ | External Clock Feedback Variation: 19–200 MHz | All | 1 ns Maximum | | | | |
| | External Clock Feedback Variation: > 200 MHz | All | < 20% of clock input period Maximum | | | | |
| $RST_{MINPULSE}$ | Minimum Reset Pulse Width | All | 5 | 5 | 5 | 5 | ns |
| $F_{PFDMAX}$[5] | Maximum Frequency at the Phase Frequency Detector | LX devices | 500 | 500 | 400 | 300 | MHz |
| | | LXT devices | 500 | 500 | 400 | N/A | MHz |
| $F_{PFDMIN}$ | Minimum Frequency at the Phase Frequency Detector | LX devices | 19 | 19 | 19 | 19 | MHz |
| | | LXT devices | 19 | 19 | 19 | N/A | MHz |
| $T_{FBDELAY}$ | Maximum Delay in the Feedback Path | All | 3 ns Max or one CLKIN cycle | | | | |

**Notes:**

1. LXT devices are not available with a -1L speed grade.
2. Values for this parameter are available in the Clocking Wizard.
3. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When using CLK_FEEDBACK = CLKOUT0 with BUFIO2 feedback, the feedback frequency will be higher than the phase frequency detector frequency. $F_{PFDMAX} = F_{CLKFB}$ / CLKFBOUT_MULT

## Spartan-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 70 through Table 77. Values are expressed in nanoseconds unless otherwise noted.

*Table 70:* **Global Clock Setup and Hold Without DCM or PLL (No Delay)**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)** | | | | | | | |
| $T_{PSND}$/ $T_{PHND}$ | No Delay Global Clock and IFF(3) without DCM or PLL | XC6SLX4 | 0.10/1.56 | N/A | 0.10/1.83 | 0.07/2.54 | ns |
| | | XC6SLX9 | 0.10/1.56 | 0.10/1.57 | 0.10/1.84 | 0.07/2.54 | ns |
| | | XC6SLX16 | 0.12/1.42 | 0.12/1.48 | 0.12/1.64 | 0.13/2.19 | ns |
| | | XC6SLX25 | 0.18/1.64 | 0.18/1.75 | 0.18/1.99 | 0.11/2.57 | ns |
| | | XC6SLX25T | 0.18/1.64 | 0.18/1.75 | 0.18/1.99 | N/A | ns |
| | | XC6SLX45 | –0.08/1.80 | –0.08/1.95 | –0.08/2.27 | –0.17/2.74 | ns |
| | | XC6SLX45T | –0.08/1.80 | –0.08/1.95 | –0.08/2.27 | N/A | ns |
| | | XC6SLX75 | 0.13/1.81 | 0.13/2.06 | 0.13/2.27 | –0.12/3.30 | ns |
| | | XC6SLX75T | 0.13/1.81 | 0.13/2.06 | 0.13/2.27 | N/A | ns |
| | | XC6SLX100 | –0.14/2.03 | –0.14/2.24 | –0.14/2.56 | –0.17/3.44 | ns |
| | | XC6SLX100T | –0.14/2.03 | –0.14/2.24 | –0.14/2.56 | N/A | ns |
| | | XC6SLX150 | –0.24/2.42 | –0.24/2.74 | –0.24/2.95 | –0.60/3.75 | ns |
| | | XC6SLX150T | –0.24/2.42 | –0.24/2.74 | –0.24/2.95 | N/A | ns |
| | | XA6SLX4 | 0.10/1.57 | N/A | 0.10/1.84 | N/A | ns |
| | | XA6SLX9 | 0.10/1.57 | N/A | 0.10/1.84 | N/A | ns |
| | | XA6SLX16 | 0.12/1.43 | N/A | 0.12/1.64 | N/A | ns |
| | | XA6SLX25 | 0.18/1.65 | N/A | 0.18/1.99 | N/A | ns |
| | | XA6SLX25T | 0.18/1.65 | N/A | 0.18/1.99 | N/A | ns |
| | | XA6SLX45 | –0.08/1.82 | N/A | –0.08/2.27 | N/A | ns |
| | | XA6SLX45T | –0.08/1.82 | N/A | –0.08/2.27 | N/A | ns |
| | | XA6SLX75 | 0.13/2.02 | N/A | 0.13/2.32 | N/A | ns |
| | | XA6SLX75T | 0.13/2.02 | N/A | 0.13/2.32 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 0.10/2.51 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 0.13/2.32 | –0.12/3.30 | ns |
| | | XQ6SLX75T | 0.13/2.02 | N/A | 0.13/2.32 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | –0.24/2.95 | –0.60/3.75 | ns |
| | | XQ6SLX150T | –0.24/2.74 | N/A | –0.24/2.95 | N/A | ns |

**Notes:**
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.

*Table 79:* **Package Skew *(Cont'd)***

| Symbol | Description | Device | Package[2] | Value | Units |
|---|---|---|---|---|---|
| $T_{PKGSKEW}$ | Package Skew[1] | LX45 | CSG324 | 70 | ps |
| | | | CS(G)484 | 99 | ps |
| | | | FG(G)484 | 109 | ps |
| | | | FG(G)676 | 138 | ps |
| | | LX45T | CSG324 | 75 | ps |
| | | | CS(G)484 | 100 | ps |
| | | | FG(G)484 | 95 | ps |
| | | LX75 | CS(G)484 | 101 | ps |
| | | | FG(G)484 | 107 | ps |
| | | | FG(G)676 | 161 | ps |
| | | LX75T | CS(G)484 | 107 | ps |
| | | | FG(G)484 | 110 | ps |
| | | | FG(G)676 | 134 | ps |
| | | LX100 | CS(G)484 | 95 | ps |
| | | | FG(G)484 | 155 | ps |
| | | | FG(G)676 | 144 | ps |
| | | LX100T | CS(G)484 | 88 | ps |
| | | | FG(G)484 | 111 | ps |
| | | | FG(G)676 | 147 | ps |
| | | | FG(G)900 | 134 | ps |
| | | LX150 | CS(G)484 | 84 | ps |
| | | | FG(G)484 | 103 | ps |
| | | | FG(G)676 | 115 | ps |
| | | | FG(G)900 | 121 | ps |
| | | LX150T | CS(G)484 | 83 | ps |
| | | | FG(G)484 | 88 | ps |
| | | | FG(G)676 | 141 | ps |
| | | | FG(G)900 | 120 | ps |

**Notes:**
1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from Pad to Ball.
2. Some of the devices are available in both Pb and Pb-free (additional G) packages as standard ordering options. See DS160: *Spartan-6 Family Overview* for more information.

*Table 80:* **Sample Window**

| Symbol | Description | Device[1] | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| $T_{SAMP}$ | Sampling Error at Receiver Pins[2] | All | 510 | 510 | 530 | 740 | ps |
| $T_{SAMP\_BUFIO2}$ | Sampling Error at Receiver Pins using BUFIO2[3] | All | 430 | 430 | 450 | 590 | ps |

**Notes:**
1. LXT devices are not available with a -1L speed grade.
2. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 DCM jitter
   - DCM accuracy (phase offset)
   - DCM phase shift resolution

   These measurements do not include package or clock tree skew.
3. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO2 clock network and IODELAY2 to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

| Date | Version | Description of Revisions |
|---|---|---|
| 01/10/11 | 1.11 | Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.4 software with speed specification v1.15 for the -4, -3, -3N, and -2 speed grades. Added note 3 to Table 27. Also updated the -1L speed grade requirements to ISE v12.4 software with speed specification v1.06. Revised -3N definition throughout the document.<br>Added note 4 to Table 2 and updated note 5. Added information on $V_{CCINT}$ to note 1 in Table 5. Updated Networking Applications -3 values in Table 25 to match improvements made in ISE v12.4. In Table 28, added note 1 and revised the $T_{IOTP}$ values for LVDS_33, LVDS_25, MINI_LVDS_33, MINI_LVDS_25, RSDS_33, RSDS_25, TMDS_33. PPDS_33, and PPDS_25. Added note 3 to Table 55. |
| 02/11/11 | 1.12 | As described in XCN11008: *Product Discontinuation Notice For Spartan-6 LXT -4 Devices*, the -4 speed specifications have been discontinued. As outlined in page 2 of the XCN, designers currently using -4 speed specifications should rerun timing analysis using the new -3 speed specifications before moving to a replacement device.<br>Updated the networking applications section of Table 25. Updated -2 speed specifications throughout document and added note 3 to Table 27 advising designers to use the -2 speed specification update (v1.17) with the ISE 12.4 software patch. Added $F_{CLKDIV}$ to Table 37 and Table 38. Updated note 2 in Table 39. Updated units for $T_{SMCKCSO}$ and $T_{BPICCO}$ in Table 47. Updated -1L in Table 71. Removed Note 2: *Package delay information is available for these device/package combinations. This information can be used to deskew the package* from Table 79. |
| 03/31/11 | 2.0 | Production release of XC6SLX45 in the -1L speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06.<br>In Table 39, removed values in the -1L column and added note 3 as IODELAY2 only supports Tap0 for lower-power devices. Updated copyright page 1 and Notice of Disclaimer. |
| 05/20/11 | 2.1 | Production release of XC6SLX100 and XC6SLX150 in the specific speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. Updated Table 27 and Note 7 with changes per XCN11012: *Speed File Change for -3N Devices*. Revised Switching Characteristics section for speed specifications: v1.18 for -3, -3N, and -2; including improvements in Table 73 through Table 77 and Table 81.<br>Removed *Memory Controller Block* from the performance heading in Table 2 and revised Note 2. In Table 4, added Note 1 to $C_{IN}$ and updated the description of $R_{IN\_TERM}$. Updated Note 1 in Table 5. Updated Note 1 of Table 7. In Table 25, added and removed -1L specifications, increased the standard performance DDR3 specifications, removed the extended performance DDR3 row and updated Note 3 and Note 4. Clarified the introductory information for Table 28 and Table 30.<br>In Table 32: Revised $V_{MEAS}$ value for LVCMOS12; revised $V_{REF}$ for LVDS_25, LVDS_33, BLVDS_25,MINI_LVDS_25, MINI_LVDS_33, RSDS_25, and RSDS_33; revised $R_{REF}$ for BLVDS_25 and TMDS_33; and added Note 4 and Note 5. Updated Note 2 and Note 3 in Table 39.<br>In Table 47, revised the values and description of $T_{POR}$ including adding Note 3. Also in Table 47, augmented the description and added specifications for $F_{RBCCK}$ and removed XC6SLX4 from $F_{MCCK}$ (maximum frequency, parallel mode (Master SelectMAP/BPI). Added BUFGMUX to Table 48 title. Added Table 50.<br>In Table 52, revised specifications for $T_{EXTFDVAR}$ and $F_{INJITTER}$. In Table 54 removed the 5 MHz < CLKIN_FREQ_DLL parameter in the LOCK_DLL description. In both Table 56 and Table 57, removed the 5 MHz < $F_{CLKIN}$ parameter in the LOCK_FX description. In Table 58, updated description for PSCLK_FREQ and PSCLK_PULSE.<br>Revised title and symbol of Table 70, added new speed specifications for -1L, and added Note 2. Added Table 71. |
| 07/11/11 | 2.2 | Added the Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices to all appropriate tables while sometimes removing the XC6S nomenclature. Added expanded temperature range (Q) to all appropriate tables. Updated $T_{SOL}$ packages in Table 1. Added $R_{OUT\_TERM}$ to Table 4. Updated Note 2 on Table 13.<br>Production release of the XC6SLX4, XC6SLX9, XC6SLX16, XC6SLX25, XC6SLX75, XQ6SLX75, and XQ6SLX150 in Table 26 and Table 27 using ISE v13.2 software with -1L speed specification v1.07.<br>Production release of the XA6SLX16, XA6SLX25T, XA6SLX45, XA6SLX45T, XQ6SLX75, XQ6SLX75T, XQ6SLX150, and XQ6SLX150T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19.<br>Added Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices(1). Updated CS(G)484 from CSG484 throughout data sheet. Clarified Note 3 in Table 39. |
| 08/08/11 | 2.3 | Production release of the XA6SLX25, XA6SLX75, and XA6SLX75T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. |

| Date | Version | Description of Revisions |
|---|---|---|
| 09/14/11 | 2.4 | Production release of the XA6SLX4 and XA6SLX9 devices in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added production released version of the XA6SLX100 to Table 26 and Table 27 using ISE v13.3 software with -2 speed specification v1.20.<br><br>Updated $R_{OUT\_TERM}$ description in Table 4. Fixed the LVPECL $V_H$ error in Table 31. Updated introduction in Simultaneously Switching Outputs. Added the XA6SLX100 to Table 63 through Table 78, and Table 81. Added Note 4 to Table 78 because the $T_{CKSKEW}$ for the XC6SLX100 is not the same as the $T_{CKSKEW}$ for the XA6SLX100.<br><br>Revised the revision history for version 1.6 dated 06/24/10. Removed the parenthetical statement about the -3N speed grade: (specifications are identical to the -3 speed grade). |
| 10/17/11 | 3.0 | Changed the data sheet from Preliminary Product Specification to Product Specification.<br>Updated the Switching Characteristics, page 19 speed specification version ISE v13.3 software to -2 and -3 speed specification v1.20 and -1L speed specification of v1.08. Also updated Note 1 in Table 27.<br>In Table 43, *Block RAM Switching Characteristics*, the $F_{MAX}$ value for the -2 speed grade has been changed from 260 MHz to 280 MHz.<br>In Table 54, *Switching Characteristics for the DLL*, a Note 6 was added and linked to CLKIN_CLKFB_PHASE. |