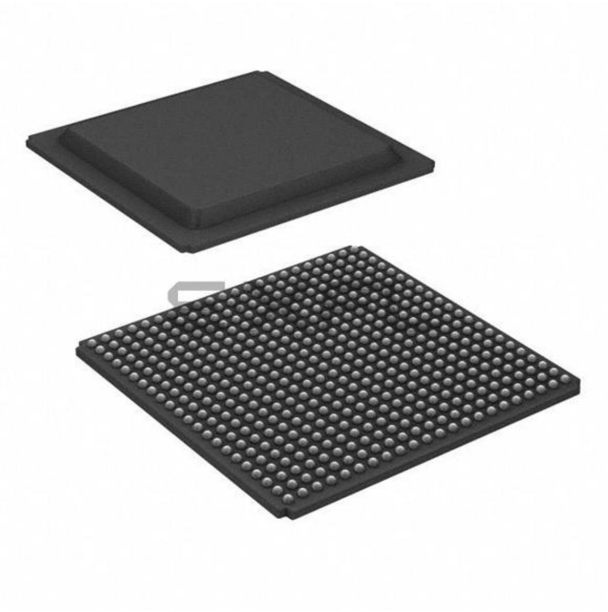
AMD Xilinx - XC6SLX75-L1FGG484C Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	5831
Number of Logic Elements/Cells	74637
Total RAM Bits	3170304
Number of I/O	280
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx75-l1fgg484c

Table 2: **Recommended Operating Conditions**(1)

Symbol	Description			Min	Typ	Max	Units
V_{CCINT}	Internal supply voltage relative to GND	-3, -3N, -2	Standard performance(2)	1.14	1.2	1.26	V
		-3, -2	Extended performance(2)	1.2	1.23	1.26	V
		-1L	Standard performance(2)	0.95	1.0	1.05	V
V_{CCAUX}(3)(4)	Auxiliary supply voltage relative to GND	V_{CCAUX} = 2.5V(5)		2.375	2.5	2.625	V
		V_{CCAUX} = 3.3V		3.15	3.3	3.45	V
V_{CCO}(6)(7)(8)	Output supply voltage relative to GND			1.1	–	3.45	V
V_{IN}	Input voltage relative to GND	All I/O standards (except PCI)	Commercial temperature (C)	–0.5	–	4.0	V
			Industrial temperature (I)	–0.5	–	3.95	V
			Expanded (Q) temperature	–0.5	–	3.95	V
		PCI I/O standard(9)		–0.5	–	V_{CCO} + 0.5	V
I_{IN}(10)	Maximum current through pin using PCI I/O standard when forward biasing the clamp diode.(9)		Commercial (C) and Industrial temperature (I)	–	–	10	mA
			Expanded (Q) temperature	–	–	7	mA
V_{BATT}(11)	Battery voltage relative to GND, T_j = 0°C to +85°C (LX75, LX75T, LX100, LX100T, LX150, and LX150T only)			1.0	–	3.6	V
T_j	Junction temperature operating range	Commercial (C) range		0	–	85	°C
		Industrial temperature (I) range		–40	–	100	°C
		Expanded (Q) temperature range		–40	–	125	°C

Notes:

1. All voltages are relative to ground.
2. See *Interface Performances for Memory Interfaces* in Table 25. The extended performance range is specified for designs not using the standard V_{CCINT} voltage range. The standard V_{CCINT} voltage range is used for:
   - Designs that do not use an MCB
   - LX4 devices
   - Devices in the TQG144 or CPG196 packages
   - Devices with the -3N speed grade
3. Recommended maximum voltage droop for V_{CCAUX} is 10 mV/ms.
4. During configuration, if V_{CCO_2} is 1.8V, then V_{CCAUX} must be 2.5V.
5. The -1L devices require V_{CCAUX} = 2.5V when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.
6. Configuration data is retained even if V_{CCO} drops to 0V.
7. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
8. For PCI systems, the transmitter and receiver should have common supplies for V_{CCO}.
9. Devices with a -1L speed grade do not support Xilinx PCI IP.
10. Do not exceed a total of 100 mA per bank.
11. V_{BATT} is required to maintain the battery backed RAM (BBR) AES key when V_{CCAUX} is not applied. Once V_{CCAUX} is applied, V_{BATT} can be unconnected. When BBR is not used, Xilinx recommends connecting to V_{CCAUX} or GND. However, V_{BATT} can be unconnected.

Table 4: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description		Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)		0.8	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)		2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin for commercial (C) and industrial (I) devices		–10	–	10	µA
	V_{REF} leakage current per pin for expanded (Q) devices		–15	–	15	µA
I_L	Input or output leakage current per pin (sample-tested) for commercial (C) and industrial (I) devices		–10	–	10	µA
	Input or output leakage current per pin (sample-tested) for expanded (Q) devices		–15	–	15	µA
I_{HS}	Leakage current on pins during hot socketing with FPGA unpowered	All pins except PROGRAM_B, DONE, and JTAG pins when HSWAPEN = 1	–20	–	20	µA
		PROGRAM_B, DONE, and JTAG pins, or other pins when HSWAPEN = 0	$I_{HS} + I_{RPU}$			µA
C_{IN}(1)	Die input capacitance at the pad		–	–	10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V or V_{CCAUX} = 3.3V		200	–	500	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V or V_{CCAUX} = 2.5V		120	–	350	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V		60	–	200	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V		40	–	150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V		12	–	100	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = V_{CCO}, V_{CCAUX} = 3.3V		200	–	550	µA
	Pad pull-down (when selected) @ V_{IN} = V_{CCO}, V_{CCAUX} = 2.5V		140	–	400	µA
I_{BATT}(2)	Battery supply current		–	–	150	nA
R_{DT}(3)	Resistance of optional input differential termination circuit, V_{CCAUX} = 3.3V		–	100	–	Ω
R_{IN_TERM}(5)	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for commercial (C) and industrial (I) devices		23	25	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for expanded (Q) devices		20	25	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for commercial (C) and industrial (I) devices		39	50	72	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for expanded (Q) devices		32	50	74	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for commercial (C) and industrial (I) devices		56	75	109	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for expanded (Q) devices		47	75	115	Ω
R_{OUT_TERM}	Thevenin equivalent resistance of programmable output termination (UNTUNED_25)		11	25	52	Ω
	Thevenin equivalent resistance of programmable output termination (UNTUNED_50)		21	50	96	Ω
	Thevenin equivalent resistance of programmable output termination (UNTUNED_75)		29	75	145	Ω

Notes:

1. The C_{IN} measurement represents the die capacitance at the pad, not including the package.
2. Maximum value specified for worst case process at 25°C. LX75, LX75T, LX100, LX100T, LX150, and LX150T only.
3. Refer to IBIS models for R_{DT} variation and for values at V_{CCAUX} = 2.5V. IBIS values for R_{DT} are valid for all temperature ranges.
4. V_{CCO2} is not required for data retention. The minimum V_{CCO2} for power-on reset and configuration is 1.65V.
5. Termination resistance to a $V_{CCO}/2$ level.

Table 8: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

I/O Standard	V_{CCO} for Drivers		
	V, Min	V, Nom	V, Max
LVDS_33	3.0	3.3	3.45
LVDS_25	2.25	2.5	2.75
BLVDS_25	2.25	2.5	2.75
MINI_LVDS_33	3.0	3.3	3.45
MINI_LVDS_25	2.25	2.5	2.75
LVPECL_33(1)	N/A–Inputs Only		
LVPECL_25	N/A–Inputs Only		
RSDS_33	3.0	3.3	3.45
RSDS_25	2.25	2.5	2.75
TMDS_33(1)	3.14	3.3	3.45
PPDS_33	3.0	3.3	3.45
PPDS_25	2.25	2.5	2.75
DISPLAY_PORT	2.3	2.5	2.7
DIFF_MOBILE_DDR	1.7	1.8	1.9
DIFF_HSTL_I	1.4	1.5	1.6
DIFF_HSTL_II	1.4	1.5	1.6
DIFF_HSTL_III	1.4	1.5	1.6
DIFF_HSTL_I_18	1.7	1.8	1.9
DIFF_HSTL_II_18	1.7	1.8	1.9
DIFF_HSTL_III_18	1.7	1.8	1.9
DIFF_SSTL3_I	3.0	3.3	3.45
DIFF_SSTL3_II	3.0	3.3	3.45
DIFF_SSTL2_I	2.3	2.5	2.7
DIFF_SSTL2_II	2.3	2.5	2.7
DIFF_SSTL18_I	1.7	1.8	1.9
DIFF_SSTL18_II	1.7	1.8	1.9
DIFF_SSTL15_II	1.425	1.5	1.575

Notes:

1. LVPECL_33 and TMDS_33 inputs require V_{CCAUX} = 3.3V nominal.

Table 10: **Differential I/O Standard DC Input and Output Levels**

I/O Standard	V_{ID}		V_{ICM}		V_{OD}		V_{OCM}		V_{OH}	V_{OL}
	mV, Min	mV, Max	V, Min	V, Max	mV, Min	mV, Max	V, Min	V, Max	V, Min	V, Max
LVDS_33(2)(3)	100	600	0.3	2.35	247	454	1.125	1.375	–	–
LVDS_25(2)(3)	100	600	0.3	2.35	247	454	1.125	1.375	–	–
BLVDS_25(2)(3)	100	–	0.3	2.35	240	460	Typical 50% V_{CCO}		–	–
MINI_LVDS_33	200	600	0.3	1.95	300	600	1.0	1.4	–	–
MINI_LVDS_25	200	600	0.3	1.95	300	600	1.0	1.4	–	–
LVPECL_33(2)(3)	100	1000	0.3	2.8(1)	Inputs only					
LVPECL_25(2)(3)	100	1000	0.3	1.95	Inputs only					
RSDS_33(2)(3)	100	–	0.3	1.5	100	400	1.0	1.4	–	–
RSDS_25(2)(3)	100	–	0.3	1.5	100	400	1.0	1.4	–	–
TMDS_33	150	1200	2.7	3.23(1)	400	800	$V_{CCO} - 0.405$	$V_{CCO} - 0.190$	–	–
PPDS_33(2)(3)	100	400	0.2	2.3	100	400	0.5	1.4	–	–
PPDS_25(2)(3)	100	400	0.2	2.3	100	400	0.5	1.4	–	–
DISPLAY_PORT	190	1260	0.3	2.35	–	–	Typical 50% V_{CCO}		–	–
DIFF_MOBILE_DDR	100	–	0.78	1.02	–	–	–	–	90% V_{CCO}	10% V_{CCO}
DIFF_HSTL_I	100	–	0.68	0.9	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_II	100	–	0.68	0.9	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_III	100	–	0.68	0.9	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_I_18	100	–	0.8	1.1	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_II_18	100	–	0.8	1.1	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_III_18	100	–	0.8	1.1	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_SSTL3_I	100	–	1.0	1.9	–	–	–	–	$V_{TT} + 0.6$	$V_{TT} - 0.6$
DIFF_SSTL3_II	100	–	1.0	1.9	–	–	–	–	$V_{TT} + 0.8$	$V_{TT} - 0.8$
DIFF_SSTL2_I	100	–	1.0	1.5	–	–	–	–	$V_{TT} + 0.61$	$V_{TT} - 0.61$
DIFF_SSTL2_II	100	–	1.0	1.5	–	–	–	–	$V_{TT} + 0.81$	$V_{TT} - 0.81$
DIFF_SSTL18_I	100	–	0.7	1.1	–	–	–	–	$V_{TT} + 0.47$	$V_{TT} - 0.47$
DIFF_SSTL18_II	100	–	0.7	1.1	–	–	–	–	$V_{TT} + 0.6$	$V_{TT} - 0.6$
DIFF_SSTL15_II	100	–	0.55	0.95	–	–	–	–	$V_{TT} + 0.4$	$V_{TT} - 0.4$

Notes:

1. LVPECL_33 and TMDS_33 maximum V_{ICM} is the lower of V (maximum) or $V_{CCAUX} - (V_{ID}/2)$
2. When $V_{CCAUX} = 3.3V$, the DCD can be higher than 5% for $V_{ICM} < 0.7V$ when using these I/O standards: LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, LVPECL_33, RSDS_25, RSDS_33, PPDS_25, and PPDS_33.
3. The -1L devices require $V_{CCAUX} = 2.5V$ when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.

Table 23: **GTP Transceiver Receiver Switching Characteristics**

Symbol	Description			Min	Typ	Max	Units
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data			–	75	–	ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak			60	–	150	mV
R_{XSST}	Receiver spread-spectrum tracking(1)		Modulated @ 33 KHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)	Internal AC capacitor bypassed		–	–	150	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	CDR 2nd-order loop disabled		–200	–	200	ppm
		CDR 2nd-order loop enabled	PLL_RXDIVSEL_OUT = 1	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 2	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 4	–1000	–	1000	ppm
SJ Jitter Tolerance(2)							
$JT\_SJ_{3.125}$	Sinusoidal Jitter(3)		3.125 Gb/s	0.4	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(3)		2.5 Gb/s	0.4	–	–	UI
$JT\_SJ_{1.62}$	Sinusoidal Jitter(3)		1.62 Gb/s	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(3)		1.25 Gb/s	0.5	–	–	UI
JT_SJ_{614}	Sinusoidal Jitter(3)		614 Mb/s	0.5	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)(5)							
$JT\_TJSE_{3.125}$	Total Jitter with stressed eye(4)		3.125 Gb/s	0.65	–	–	UI
$JT\_SJSE_{3.125}$	Sinusoidal Jitter with stressed eye		3.125 Gb/s	0.1	–	–	UI
$JT\_TJSE_{2.7}$	Total Jitter with stressed eye(4)		2.7 Gb/s	0.65	–	–	UI
$JT\_SJSE_{2.7}$	Sinusoidal Jitter with stressed eye		2.7 Gb/s	0.1	–	–	UI

Notes:

1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a Bit Error Ratio of $1e^{-12}$.
3. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
4. Composed of 0.37 UI DJ in the form of ISI and 0.18 UI RJ.
5. Measured using PRBS7 data pattern.

Endpoint Block for PCI Express Designs Switching Characteristics

The Endpoint block for PCI Express is available in the Spartan-6 LXT devices. Consult the Spartan-6 FPGA Integrated Endpoint Block for PCI Express for further information.

Table 24: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
$F_{PCIEUSER}$	User clock maximum frequency	62.5	62.5	62.5	N/A	MHz

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L(1)	-3	-3N	-2	-1L(1)	-3	-3N	-2	-1L(1)	
PPDS_33	1.17	1.29	1.42	1.68	1.57	1.71	1.91	2.43	3000	3000	3000	3000	ns
PPDS_25	1.01	1.13	1.26	1.56	1.68	1.82	2.02	2.47	3000	3000	3000	3000	ns
PCI33_3	1.07	1.19	1.32	1.57(2)	3.51	3.65	3.85	4.38(2)	3.51	3.65	3.85	4.38(1)	ns
PCI66_3	1.07	1.19	1.32	1.57(2)	3.53	3.67	3.87	4.39(2)	3.53	3.67	3.87	4.39(1)	ns
DISPLAY_PORT	1.02	1.14	1.27	1.56	3.15	3.29	3.49	4.08	3.15	3.29	3.49	4.08	ns
I2C	1.33	1.45	1.58	1.82	11.56	11.70	11.90	12.52	11.56	11.70	11.90	12.52	ns
SMBUS	1.33	1.45	1.58	1.82	11.56	11.70	11.90	12.52	11.56	11.70	11.90	12.52	ns
SDIO	1.36	1.48	1.61	1.84	2.64	2.78	2.98	3.60	2.64	2.78	2.98	3.60	ns
MOBILE_DDR	0.94	1.06	1.19	1.43	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns
HSTL_I	0.90	1.02	1.15	1.39	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
HSTL_II	0.91	1.03	1.16	1.40	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
HSTL_III	0.95	1.07	1.20	1.44	1.67	1.81	2.01	2.61	1.67	1.81	2.01	2.61	ns
HSTL_I _18	0.94	1.06	1.19	1.43	1.77	1.91	2.11	2.73	1.77	1.91	2.11	2.73	ns
HSTL_II _18	0.94	1.06	1.19	1.43	1.85	1.99	2.19	2.81	1.85	1.99	2.19	2.81	ns
HSTL_III _18	0.99	1.11	1.24	1.47	1.79	1.93	2.13	2.72	1.79	1.93	2.13	2.72	ns
SSTL3_I	1.58	1.70	1.83	2.16	1.83	1.97	2.17	2.72	1.83	1.97	2.17	2.72	ns
SSTL3_II	1.58	1.70	1.83	2.16	2.01	2.15	2.35	2.94	2.01	2.15	2.35	2.94	ns
SSTL2_I	1.30	1.42	1.55	1.87	1.77	1.91	2.11	2.69	1.77	1.91	2.11	2.69	ns
SSTL2_II	1.30	1.42	1.55	1.88	1.86	2.00	2.20	2.82	1.86	2.00	2.20	2.82	ns
SSTL18_I	0.92	1.04	1.17	1.41	1.63	1.77	1.97	2.59	1.63	1.77	1.97	2.59	ns
SSTL18_II	0.92	1.04	1.17	1.41	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
SSTL15_II	0.92	1.04	1.17	1.41	1.67	1.81	2.01	2.63	1.67	1.81	2.01	2.63	ns
DIFF_HSTL_I	0.94	1.06	1.19	1.46	1.77	1.91	2.11	2.62	1.77	1.91	2.11	2.62	ns
DIFF_HSTL_II	0.93	1.05	1.18	1.45	1.72	1.86	2.06	2.54	1.72	1.86	2.06	2.54	ns
DIFF_HSTL_III	0.93	1.05	1.18	1.46	1.69	1.83	2.03	2.53	1.69	1.83	2.03	2.53	ns
DIFF_HSTL_I_18	0.97	1.09	1.22	1.50	1.79	1.93	2.13	2.63	1.79	1.93	2.13	2.63	ns
DIFF_HSTL_II_18	0.97	1.09	1.22	1.49	1.69	1.83	2.03	2.51	1.69	1.83	2.03	2.51	ns
DIFF_HSTL_III_18	0.97	1.09	1.22	1.50	1.69	1.83	2.03	2.53	1.69	1.83	2.03	2.53	ns
DIFF_SSTL3_I	1.18	1.30	1.43	1.68	1.81	1.95	2.15	2.64	1.81	1.95	2.15	2.64	ns
DIFF_SSTL3_II	1.19	1.31	1.44	1.68	1.80	1.94	2.14	2.63	1.80	1.94	2.14	2.63	ns
DIFF_SSTL2_I	1.02	1.14	1.27	1.57	1.80	1.94	2.14	2.62	1.80	1.94	2.14	2.62	ns
DIFF_SSTL2_II	1.02	1.14	1.27	1.57	1.76	1.90	2.10	2.57	1.76	1.90	2.10	2.57	ns
DIFF_SSTL18_I	0.97	1.09	1.22	1.51	1.72	1.86	2.06	2.56	1.72	1.86	2.06	2.56	ns
DIFF_SSTL18_II	0.98	1.10	1.23	1.50	1.68	1.82	2.02	2.52	1.68	1.82	2.02	2.52	ns
DIFF_SSTL15_II	0.94	1.06	1.19	1.46	1.67	1.81	2.01	2.50	1.67	1.81	2.01	2.50	ns
DIFF_MOBILE_DDR	0.97	1.09	1.22	1.51	1.75	1.89	2.09	2.57	1.75	1.89	2.09	2.57	ns

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L(1)	-3	-3N	-2	-1L(1)	-3	-3N	-2	-1L(1)	
LVCMOS12, Fast, 2 mA	0.91	1.03	1.16	1.51	3.46	3.60	3.80	4.44	3.46	3.60	3.80	4.44	ns
LVCMOS12, Fast, 4 mA	0.91	1.03	1.16	1.51	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVCMOS12, Fast, 6 mA	0.91	1.03	1.16	1.51	1.79	1.93	2.13	2.75	1.79	1.93	2.13	2.75	ns
LVCMOS12, Fast, 8 mA	0.91	1.03	1.16	1.51	1.68	1.82	2.02	2.64	1.68	1.82	2.02	2.64	ns
LVCMOS12, Fast, 12 mA	0.91	1.03	1.16	1.51	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
LVCMOS12_JEDEC, QUIETIO, 2 mA	1.50	1.62	1.75	1.88	6.39	6.53	6.73	7.31	6.39	6.53	6.73	7.31	ns
LVCMOS12_JEDEC, QUIETIO, 4 mA	1.50	1.62	1.75	1.88	4.98	5.12	5.32	5.88	4.98	5.12	5.32	5.88	ns
LVCMOS12_JEDEC, QUIETIO, 6 mA	1.50	1.62	1.75	1.88	4.67	4.81	5.01	5.54	4.67	4.81	5.01	5.54	ns
LVCMOS12_JEDEC, QUIETIO, 8 mA	1.50	1.62	1.75	1.88	4.23	4.37	4.57	5.22	4.23	4.37	4.57	5.22	ns
LVCMOS12_JEDEC, QUIETIO, 12 mA	1.50	1.62	1.75	1.88	3.99	4.13	4.33	4.94	3.99	4.13	4.33	4.94	ns
LVCMOS12_JEDEC, Slow, 2 mA	1.50	1.62	1.75	1.88	5.00	5.14	5.34	5.90	5.00	5.14	5.34	5.90	ns
LVCMOS12_JEDEC, Slow, 4 mA	1.50	1.62	1.75	1.88	2.85	2.99	3.19	3.80	2.85	2.99	3.19	3.80	ns
LVCMOS12_JEDEC, Slow, 6 mA	1.50	1.62	1.75	1.88	2.76	2.90	3.10	3.72	2.76	2.90	3.10	3.72	ns
LVCMOS12_JEDEC, Slow, 8 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVCMOS12_JEDEC, Slow, 12 mA	1.50	1.62	1.75	1.88	2.09	2.23	2.43	3.05	2.09	2.23	2.43	3.05	ns
LVCMOS12_JEDEC, Fast, 2 mA	1.50	1.62	1.75	1.88	3.46	3.60	3.80	4.42	3.46	3.60	3.80	4.42	ns
LVCMOS12_JEDEC, Fast, 4 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns
LVCMOS12_JEDEC, Fast, 6 mA	1.50	1.62	1.75	1.88	1.79	1.93	2.13	2.76	1.79	1.93	2.13	2.76	ns
LVCMOS12_JEDEC, Fast, 8 mA	1.50	1.62	1.75	1.88	1.69	1.83	2.03	2.65	1.69	1.83	2.03	2.65	ns
LVCMOS12_JEDEC, Fast, 12 mA	1.50	1.62	1.75	1.88	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns

Notes:

1. The -1L values listed in this table are also applicable to the Spartan-6Q devices.
2. Devices with a -1L speed grade do not support Xilinx PCI IP.

Table 29: **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices[(1)] *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVCMOS33, Slow, 6 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVCMOS33, Slow, 8 mA	1.41	1.59	2.79	2.99	2.79	2.99	ns
LVCMOS33, Slow, 12 mA	1.41	1.59	2.53	2.73	2.53	2.73	ns
LVCMOS33, Slow, 16 mA	1.41	1.59	2.45	2.65	2.45	2.65	ns
LVCMOS33, Slow, 24 mA	1.41	1.59	2.42	2.62	2.42	2.62	ns
LVCMOS33, Fast, 2 mA	1.41	1.59	4.05	4.25	4.05	4.25	ns
LVCMOS33, Fast, 4 mA	1.41	1.59	2.66	2.86	2.66	2.86	ns
LVCMOS33, Fast, 6 mA	1.41	1.59	2.46	2.66	2.46	2.66	ns
LVCMOS33, Fast, 8 mA	1.41	1.59	2.21	2.41	2.21	2.41	ns
LVCMOS33, Fast, 12 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVCMOS33, Fast, 16 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVCMOS33, Fast, 24 mA	1.41	1.59	1.80	2.00	1.80	2.00	ns
LVCMOS25, QUIETIO, 2 mA	0.89	1.07	5.00	5.20	5.00	5.20	ns
LVCMOS25, QUIETIO, 4 mA	0.89	1.07	3.85	4.05	3.85	4.05	ns
LVCMOS25, QUIETIO, 6 mA	0.89	1.07	3.60	3.80	3.60	3.80	ns
LVCMOS25, QUIETIO, 8 mA	0.89	1.07	3.34	3.54	3.34	3.54	ns
LVCMOS25, QUIETIO, 12 mA	0.89	1.07	2.98	3.18	2.98	3.18	ns
LVCMOS25, QUIETIO, 16 mA	0.89	1.07	2.79	2.99	2.79	2.99	ns
LVCMOS25, QUIETIO, 24 mA	0.89	1.07	2.64	2.84	2.64	2.84	ns
LVCMOS25, Slow, 2 mA	0.89	1.07	3.96	4.16	3.96	4.16	ns
LVCMOS25, Slow, 4 mA	0.89	1.07	2.96	3.16	2.96	3.16	ns
LVCMOS25, Slow, 6 mA	0.89	1.07	2.88	3.08	2.88	3.08	ns
LVCMOS25, Slow, 8 mA	0.89	1.07	2.63	2.83	2.63	2.83	ns
LVCMOS25, Slow, 12 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVCMOS25, Slow, 16 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVCMOS25, Slow, 24 mA	0.89	1.07	2.15	2.35	2.15	2.35	ns
LVCMOS25, Fast, 2 mA	0.89	1.07	3.52	3.72	3.52	3.72	ns
LVCMOS25, Fast, 4 mA	0.89	1.07	2.43	2.63	2.43	2.63	ns
LVCMOS25, Fast, 6 mA	0.89	1.07	2.23	2.43	2.23	2.43	ns
LVCMOS25, Fast, 8 mA	0.89	1.07	2.16	2.36	2.16	2.36	ns
LVCMOS25, Fast, 12 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVCMOS25, Fast, 16 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVCMOS25, Fast, 24 mA	0.89	1.07	1.70	1.90	1.70	1.90	ns
LVCMOS18, QUIETIO, 2 mA	1.25	1.43	6.11	6.31	6.11	6.31	ns
LVCMOS18, QUIETIO, 4 mA	1.25	1.43	4.88	5.08	4.88	5.08	ns
LVCMOS18, QUIETIO, 6 mA	1.25	1.43	4.20	4.40	4.20	4.40	ns
LVCMOS18, QUIETIO, 8 mA	1.25	1.43	3.86	4.06	3.86	4.06	ns
LVCMOS18, QUIETIO, 12 mA	1.25	1.43	3.49	3.69	3.49	3.69	ns

Table 29: **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices[(1)](#) *(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVCMOS15, QUIETIO, 2 mA	1.05	1.23	5.63	5.83	5.63	5.83	ns
LVCMOS15, QUIETIO, 4 mA	1.05	1.23	4.75	4.95	4.75	4.95	ns
LVCMOS15, QUIETIO, 6 mA	1.05	1.23	4.21	4.41	4.21	4.41	ns
LVCMOS15, QUIETIO, 8 mA	1.05	1.23	4.05	4.25	4.05	4.25	ns
LVCMOS15, QUIETIO, 12 mA	1.05	1.23	3.74	3.94	3.74	3.94	ns
LVCMOS15, QUIETIO, 16 mA	1.05	1.23	3.52	3.72	3.52	3.72	ns
LVCMOS15, Slow, 2 mA	1.05	1.23	4.32	4.52	4.32	4.52	ns
LVCMOS15, Slow, 4 mA	1.05	1.23	3.58	3.78	3.58	3.78	ns
LVCMOS15, Slow, 6 mA	1.05	1.23	2.45	2.65	2.45	2.65	ns
LVCMOS15, Slow, 8 mA	1.05	1.23	2.46	2.66	2.46	2.66	ns
LVCMOS15, Slow, 12 mA	1.05	1.23	2.17	2.37	2.17	2.37	ns
LVCMOS15, Slow, 16 mA	1.05	1.23	2.15	2.35	2.15	2.35	ns
LVCMOS15, Fast, 2 mA	1.05	1.23	3.43	3.63	3.43	3.63	ns
LVCMOS15, Fast, 4 mA	1.05	1.23	2.42	2.62	2.42	2.62	ns
LVCMOS15, Fast, 6 mA	1.05	1.23	1.92	2.12	1.92	2.12	ns
LVCMOS15, Fast, 8 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVCMOS15, Fast, 12 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVCMOS15, Fast, 16 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVCMOS15_JEDEC, QUIETIO, 2 mA	1.10	1.28	5.64	5.84	5.64	5.84	ns
LVCMOS15_JEDEC, QUIETIO, 4 mA	1.10	1.28	4.75	4.95	4.75	4.95	ns
LVCMOS15_JEDEC, QUIETIO, 6 mA	1.10	1.28	4.21	4.41	4.21	4.41	ns
LVCMOS15_JEDEC, QUIETIO, 8 mA	1.10	1.28	4.06	4.26	4.06	4.26	ns
LVCMOS15_JEDEC, QUIETIO, 12 mA	1.10	1.28	3.75	3.95	3.75	3.95	ns
LVCMOS15_JEDEC, QUIETIO, 16 mA	1.10	1.28	3.53	3.73	3.53	3.73	ns
LVCMOS15_JEDEC, Slow, 2 mA	1.10	1.28	4.32	4.52	4.32	4.52	ns
LVCMOS15_JEDEC, Slow, 4 mA	1.10	1.28	3.56	3.76	3.56	3.76	ns
LVCMOS15_JEDEC, Slow, 6 mA	1.10	1.28	2.44	2.64	2.44	2.64	ns
LVCMOS15_JEDEC, Slow, 8 mA	1.10	1.28	2.47	2.67	2.47	2.67	ns
LVCMOS15_JEDEC, Slow, 12 mA	1.10	1.28	2.15	2.35	2.15	2.35	ns
LVCMOS15_JEDEC, Slow, 16 mA	1.10	1.28	2.15	2.35	2.15	2.35	ns
LVCMOS15_JEDEC, Fast, 2 mA	1.10	1.28	3.43	3.63	3.43	3.63	ns
LVCMOS15_JEDEC, Fast, 4 mA	1.10	1.28	2.42	2.62	2.42	2.62	ns
LVCMOS15_JEDEC, Fast, 6 mA	1.10	1.28	1.92	2.12	1.92	2.12	ns
LVCMOS15_JEDEC, Fast, 8 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVCMOS15_JEDEC, Fast, 12 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVCMOS15_JEDEC, Fast, 16 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVCMOS12, QUIETIO, 2 mA	0.98	1.16	6.54	6.74	6.54	6.74	ns
LVCMOS12, QUIETIO, 4 mA	0.98	1.16	5.12	5.32	5.12	5.32	ns

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 4 and Figure 5.

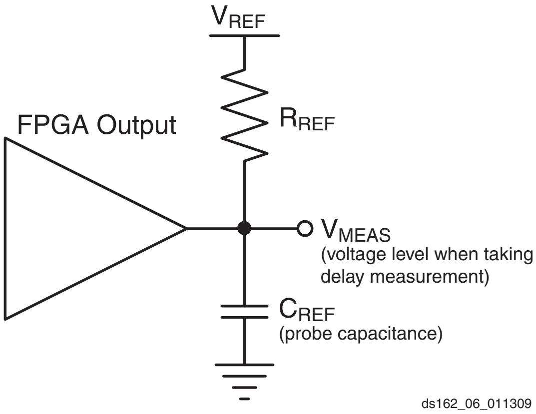

Figure 4: **Single-Ended Test Setup**

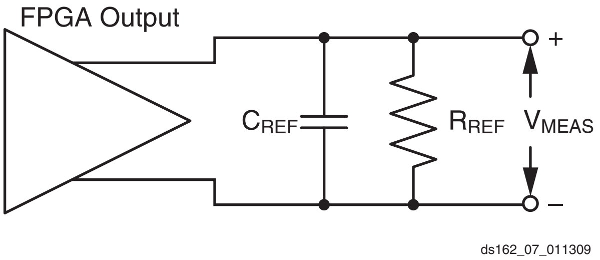

Figure 5: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 32.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 32: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[(1)] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.4	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
PCI (Peripheral Component Interface) 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3 (rising edge)	25	10[(2)]	0.94	0
	PCI33_3, PCI66_3 (falling edge)	25	10[(2)]	2.03	3.3
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25

Table 32: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[(1)] (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
SSTL, Class II, 1.5V	SSTL15_II	25	0	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	100	0	0(3)	–
BLVDS (Bus LVDS), 2.5V	BLVDS_25	Note 4	0	0(3)	–
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	100	0	0(3)	–
RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RSDS_25, RSDS_33	100	0	0(3)	–
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	Note 5	0	0(3)	–
PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V	PPDS_25, PPDS_33	100	0	0(3)	–

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. The value given is the differential output voltage.
4. See the *BLVDS Output Termination* section in UG381, *Spartan-6 FPGA SelectIO Resources User Guide*.
5. See the *TMDS_33 Termination* section in UG381, *Spartan-6 FPGA SelectIO Resources User Guide*.

Simultaneously Switching Outputs

Due to package electrical parasitics, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. Table 33 and Table 34 provide guidelines for the recommended maximum allowable number of SSOs. These guidelines describe the maximum number of user I/O pins of an output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise for that particular signal standard. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of GND and power bounce.

For each device/package combination, Table 33 provides the number of equivalent V_{CCO}/GND pairs per bank. For each output signal standard and drive strength, Table 34 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines are categorized by package style, slew rate, and output drive current. The number of SSOs are also specified by I/O bank. Multiply the appropriate numbers from each table to calculate the maximum number of SSOs allowed within an I/O bank. The guidelines assume that all pins within a bank use the same I/O standard. Exceeding these SSO guidelines can result in increased power or GND bounce, degraded signal integrity, or increased system jitter. For a given I/O standard, if the SSO limit per pair in Table 34 is greater than the maximum I/O per pair in Table 33, then there is no SSO limit for the exclusive use of that I/O standard.

The recommended maximum SSO values assume that the FPGA is soldered on a printed circuit board and that the board uses sound design practices. Due to the additional inductance introduced by the socket, the SSO values do not apply for FPGAs mounted in sockets. The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics. For more detail, see UG381: *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 34: **SSO Limit per V_{CCO}/GND Pair** ***(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
1.8V	LVCMOS18, LVCMOS18_JEDEC	2	Fast	39	46	39	47
			Slow	65	75	65	74
			QuietIO	80	80	80	85
		4	Fast	22	25	22	25
			Slow	38	36	38	29
			QuietIO	45	40	45	35
		6	Fast	16	18	16	17
			Slow	27	25	27	19
			QuietIO	30	28	30	23
		8	Fast	13	15	13	14
			Slow	16	18	16	16
			QuietIO	25	22	25	18
		12	Fast	5	7	5	5
			Slow	7	8	7	6
			QuietIO	11	10	11	8
		16	Fast	4	5	4	4
			Slow	7	8	7	5
			QuietIO	11	10	11	8
		24	Fast	N/A	5	N/A	3
			Slow	N/A	8	N/A	8
			QuietIO	N/A	10	N/A	8
	HSTL_I_18			9	10	9	9
	HSTL_II_18			N/A	5	N/A	6
	HSTL_III_18			9	10	9	11
	DIFF_HSTL_I_18			27	30	27	27
	DIFF_HSTL_II_18			N/A	15	N/A	18
	DIFF_HSTL_III_18			27	30	27	33
	MOBILE_DDR (3)			12	14	12	14
	DIFF_MOBILE_DDR (3)			36	42	36	42
	SSTL_18_I (3)			9	10	9	10
	SSTL_18_II (3)			N/A	5	N/A	4
	DIFF_SSTL_18_I (3)			27	30	27	30
	DIFF_SSTL_18_II (3)			N/A	15	N/A	12

Input Serializer/Deserializer Switching Characteristics

Table 37: **ISERDES2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold for Control Lines						
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.16/ –0.09	0.20/ –0.09	0.31/ –0.09	0.34/ –0.14	ns
T_{ISCCK_CE} / T_{ISCKC_CE}	CE pin Setup/Hold with respect to CLK	0.71/ –0.47	0.71/ –0.42	0.97/ –0.42	1.39/ –0.71	ns
Setup/Hold for Data Lines						
T_{ISDCK_D} /T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.24/ –0.15	0.25/ –0.05	0.29/ –0.05	0.09/ –0.05	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	–0.25/ 0.30	–0.25/ 0.42	–0.25/ 0.56	–0.54/ 0.67	ns
$T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	–0.03/ 0.04	–0.03/ 0.16	–0.03/ 0.18	–0.05/ 0.12	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY2)	–0.40/ 0.48	–0.40/ 0.53	–0.40/ 0.71	–0.71/ 0.86	ns
Sequential Delays						
T_{ISCKO_Q}	CLKDIV to out at Q pin	1.30	1.44	2.02	2.22	ns
F_{CLKDIV}	CLKDIV maximum frequency	270	262.5	250	125	MHz

Output Serializer/Deserializer Switching Characteristics

Table 38: **OSERDES2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	–0.03/ 1.02	–0.03/ 1.17	–0.03/ 1.27	–0.02/ 0.23	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	–0.05/ 1.03	–0.05/ 1.13	–0.05/ 1.23	–0.05/ 0.24	ns
T_{OSCCK_OCE}/T_{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.12/ –0.03	0.15/ –0.03	0.24/ –0.03	0.28/ –0.17	ns
T_{OSCCK_TCE}/T_{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.14/ –0.08	0.17/ –0.08	0.27/ –0.08	0.31/ –0.16	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.94	1.11	1.51	1.89	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.94	1.11	1.51	1.91	ns
F_{CLKDIV}	CLKDIV maximum frequency	270	262.5	250	125	MHz

Notes:

1. T_{OSDCK_T2}/T_{OSCKD_T2} (T input setup/hold with respect to CLKDIV) are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

DSP48A1 Switching Characteristics

Table 44: **DSP48A1 Switching Characteristics**

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-3	-3N	-2	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock									
$T_{DSPDCK\_A\_A1REG}$/ $T_{DSPCKD\_A\_A1REG}$	A input to A1 register CLK	N/A	N/A	N/A	0.15/ 0.09	0.17/ 0.09	0.17/ 0.09	0.32/ 0.09	ns
$T_{DSPDCK\_D\_B1REG}$/ $T_{DSPCKD\_D\_B1REG}$	D input to B1 register CLK	Yes	N/A	N/A	1.90/ –0.07	1.95/ –0.07	1.95/ –0.07	2.82/ –0.07	ns
$T_{DSPDCK\_C\_CREG}$/ $T_{DSPCKD\_C\_CREG}$	C input to C register CLK for XC devices	N/A	N/A	N/A	0.11/ 0.15	0.13/ 0.15	0.13/ 0.15	0.24/ 0.09	ns
	C input to C register CLK for XA and XQ devices				0.11/ 0.19	N/A	0.13/ 0.23	0.24/ 0.09	
$T_{DSPDCK\_D\_DREG}$/ $T_{DSPCKD\_D\_DREG}$	D input to D register CLK for XC devices	N/A	N/A	N/A	0.09/ 0.15	0.10/ 0.15	0.10/ 0.15	0.19/ 0.12	ns
	D input to D register CLK for XA and XQ devices				0.09/ 0.23	N/A	0.10/ 0.27	0.19/ 0.12	
$T_{DSPDCK\_OPMODE\_B1REG}$/ $T_{DSPCKD\_OPMODE\_B1REG}$	OPMODE input to B1 register CLK	Yes	N/A	N/A	1.97/ 0.01	2.00/ 0.01	2.00/ 0.01	2.85/ 0.01	ns
$T_{DSPDCK\_OPMODE\_OPMODEREG}$/ $T_{DSPCKD\_OPMODE\_OPMODEREG}$	OPMODE input to OPMODE register CLK for XC devices	N/A	N/A	N/A	0.18/ 0.12	0.21/ 0.12	0.21/ 0.12	0.40/ 0.12	ns
	OPMODE input to OPMODE register CLK for XA and XQ devices				0.18/ 0.16	N/A	0.21/ 0.22	0.40/ 0.12	
Setup and Hold Times of Data Pins to the Pipeline Register Clock									
$T_{DSPDCK\_A\_MREG}$/ $T_{DSPCKD\_A\_MREG}$	A input to M register CLK	N/A	Yes	N/A	3.06/ –0.40	3.51/ –0.40	3.51/ –0.40	3.97/ –0.40	ns
$T_{DSPDCK\_B\_MREG}$/ $T_{DSPCKD\_B\_MREG}$	B input to M register CLK	Yes	Yes	N/A	3.96/ –0.68	4.58/ –0.68	4.58/ –0.68	7.00/ –0.68	ns
$T_{DSPDCK\_D\_MREG}$/ $T_{DSPCKD\_D\_MREG}$	D input to M register CLK	Yes	Yes	N/A	4.23/ –0.56	4.80/ –0.56	4.80/ –0.56	6.84/ –0.56	ns
$T_{DSPDCK\_OPMODE\_MREG}$/ $T_{DSPCKD\_OPMODE\_MREG}$	OPMODE to M register CLK	Yes	Yes	N/A	4.18/ –0.48	4.80/ –0.48	4.80/ –0.48	6.88/ –0.48	ns
		No	Yes	N/A	2.37/ –0.48	2.70/ –0.48	2.70/ –0.48	4.28/ –0.48	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock									
$T_{DSPDCK\_A\_PREG}$/ $T_{DSPCKD\_A\_PREG}$	A input to P register CLK	N/A	Yes	Yes	4.32/ –0.76	5.06/ –0.76	5.06/ –0.76	7.52/ –0.76	ns
$T_{DSPDCK\_B\_PREG}$/ $T_{DSPCKD\_B\_PREG}$	B input to P register CLK	Yes	Yes	Yes	5.87/ –0.59	6.87/ –0.59	6.87/ –0.59	10.55/ –0.59	ns
		No	Yes	Yes	4.14/ –0.93	4.68/ –0.93	4.68/ –0.93	8.12/ –0.93	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK	N/A	N/A	Yes	2.20/ –0.23	2.25/ –0.23	2.25/ –0.23	3.27/ –0.23	ns
$T_{DSPDCK\_D\_PREG}$/ $T_{DSPCKD\_D\_PREG}$	D input to P register CLK	Yes	Yes	Yes	5.90/ –0.92	6.91/ –0.92	6.91/ –0.92	10.39/ –0.92	ns

Table 47: **Configuration Switching Characteristics[1] *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
BPI Master Flash Mode Programming Switching[4]						
T_{BPICCO}[5]	A[25:0], FCS_B, FOE_B, FWE_B, LDC outputs valid after CCLK falling edge	15	15	15	20	ns, Max
T_{BPICCK}	Master BPI CCLK (output) delay	10/100	10/100	10/100	10/130	µs, Min/Max
T_{BPIDCC}/T_{BPICCD}	Setup/Hold on D[15:0] data input pins	5.0/1.0	5.0/1.0	5.0/1.0	6.0/2.0	ns, Min
SPI Master Flash Mode Programming Switching[6]						
$T_{SPIDCC}/T_{SPIDCCD}$	DIN, MISO0, MISO1, MISO2, MISO3, Setup/Hold before/after the rising CCLK edge	5.0/1.0	5.0/1.0	5.0/1.0	7.0/1.0	ns, Min
T_{SPICCK}	Master SPI CCLK (output) delay	0.4/7.0	0.4/7.0	0.4/7.0	0.4/10.0	µs, Min/Max
T_{SPICCM}	MOSI clock to out	13	13	13	19	ns, Max
$T_{SPICCFC}$	CSO_B clock to out	16	16	16	26	ns, Max
CCLK Output (Master Modes)						
T_{MCCKL}	Master CCLK clock duty cycle Low	40/60				%, Min/Max
T_{MCCKH}	Master CCLK clock duty cycle High	40/60				%, Min/Max
F_{MCCK}	Maximum frequency, serial mode (Master Serial/SPI) All devices	40	40	40	30	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T	40	40	40	25	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x8 mode, LX150, and LX150T	40	40	40	20	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x16 mode	35	35	35	20	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode	±50	±50	±50	±50	%
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time	5	5	5	8	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	5	5	5	8	ns, Min
USERCCLK Input						
$T_{USERCCLKL}$	USERCCLK clock minimum Low time	12	12	12	16	ns, Min
$T_{USERCCLKH}$	USERCCLK clock minimum High time	12	12	12	16	ns, Min
$F_{USERCCLK}$	Maximum USERCCLK frequency	40	40	40	30	MHz, Max

Notes:

1. Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
2. To support longer delays in configuration, use the design solutions described in UG380: *Spartan-6 FPGA Configuration User Guide*.
3. Table 6 specifies the power supply ramp time.
4. BPI mode is not supported in:
    - LX4, LX25, or LX25T devices
    - LX9 devices in the TQG144 package
    - LX9 or LX16 devices in the CPG196 package.
5. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
6. Defense-grade Spartan-6Q -2Q devices configure in single default SPI Master (x1) mode at T_j = –55°C. During operation and when using all other configuration functions, the minimum operating temperature is –40°C.

Table 57: **Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)[1]**

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges (DCM_CLKGEN)										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz
CLKOUT_FREQ_FXDV	Frequency for the CLKFXDV output	0.15625	187.5	0.15625	187.5	0.15625	166.5	0.15625	100	MHz
Output Clock Jitter[2][3]										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKOUT_PER_JITT_FXDV	Period jitter at the CLKFXDV output.	Typical = ±[0.2% of CLKFX period + 100]								ps
CLKFX_FREEZE_VAR	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX > 50 MHz	Maximum = ±3% of CLKFX period								ps
	CLKFX period change in free running oscillator mode at the same temperature. FCLKFX < 50 MHz	Maximum = ±5% of CLKFX period								ps
CLKFX_FREEZE_TEMP_SLOPE	CLKFX period will change in free_oscillator mode over temperature. Add to CLKFX_FREEZE_VAR to determine total CLKFX period change. Percentage change for CLKFX period over 1°C.	Maximum = 0.1								%/°C
Duty Cycle[4][5]										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
CLKOUT_DUTY_CYCLE_FXDV	Duty cycle precision for the CLKFXDV outputs, including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±[1% of CLKFX period + 350]								ps
Lock Time										
LOCK_FX[2]	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX, CLKFX180, and CLKFXDV signals are valid. Lock time requires CLKFX_DIVIDE < F_{IN}/(0.50 MHz) when: F_{CLKIN} < 50 MHz	–	50	–	50	–	50	–	50	ms
	when: F_{CLKIN} > 50 MHz	–	5	–	5	–	5	–	5	ms

Table 73: **Global Clock Setup and Hold With DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSDCM0}/ T_{PHDCM0}	No Delay Global Clock and IFF(2) with DCM in Source-Synchronous Mode	XC6SLX4	0.71/0.65	N/A	0.72/1.22	1.58/1.18	ns
		XC6SLX9	0.71/0.69	0.71/1.19	0.72/1.36	1.58/1.18	ns
		XC6SLX16	0.86/0.52	0.92/0.57	1.04/0.60	1.02/1.06	ns
		XC6SLX25	0.84/0.58	0.90/0.59	1.01/0.59	1.58/1.07	ns
		XC6SLX25T	0.84/0.58	0.90/0.59	1.01/0.59	N/A	ns
		XC6SLX45	0.85/0.70	0.90/0.76	0.98/0.79	1.34/1.34	ns
		XC6SLX45T	0.85/0.70	0.90/0.76	0.98/0.79	N/A	ns
		XC6SLX75	1.00/0.62	1.06/0.63	1.15/0.63	1.65/1.46	ns
		XC6SLX75T	1.00/0.71	1.06/0.72	1.15/0.72	N/A	ns
		XC6SLX100	0.81/0.68	0.81/0.69	0.94/0.69	1.42/2.07	ns
		XC6SLX100T	0.81/0.68	0.81/0.69	0.94/0.69	N/A	ns
		XC6SLX150	0.68/0.98	0.69/0.99	0.79/0.99	1.45/1.60	ns
		XC6SLX150T	0.68/0.98	0.69/0.99	0.79/0.99	N/A	ns
		XA6SLX4	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX9	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX16	1.01/0.56	N/A	1.04/0.60	N/A	ns
		XA6SLX25	0.94/0.76	N/A	1.06/0.77	N/A	ns
		XA6SLX25T	0.94/0.76	N/A	1.14/0.77	N/A	ns
		XA6SLX45	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX45T	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX75	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX100	N/A	N/A	1.37/0.75	N/A	ns
		XQ6SLX75	N/A	N/A	1.15/0.72	1.65/1.46	ns
		XQ6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XQ6SLX150	N/A	N/A	0.79/1.15	1.45/1.60	ns
		XQ6SLX150T	0.73/1.15	N/A	0.79/1.15	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 78: Duty Cycle Distortion and Clock-Tree Skew *(Cont'd)*

Symbol	Description	Device[1]	Speed Grade				Units
			-3	-3N	-2	-1L	
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	LX4	0.06	N/A	0.06	0.07	ns
		LX9	0.06	0.06	0.06	0.07	ns
		LX16	0.06	0.06	0.06	0.07	ns
		LX25	0.06	0.06	0.06	0.07	ns
		LX25T	0.06	0.06	0.06	N/A	ns
		LX45	0.06	0.06	0.06	0.07	ns
		LX45T	0.06	0.06	0.06	N/A	ns
		LX75	0.06	0.06	0.06	0.07	ns
		LX75T	0.06	0.06	0.06	N/A	ns
		LX100	0.06	0.06	0.06	0.07	ns
		LX100T	0.06	0.06	0.06	N/A	ns
		LX150	0.06	0.06	0.06	0.07	ns
		LX150T	0.06	0.06	0.06	N/A	ns

Notes:

1. LXT devices are not available with a -1L speed grade. The LX4 is not available in -3N speed grade.
2. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
3. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
4. The T_{CKSKEW} is 0.43 ns for the XA6SLX100 device using a -2 speed grade and 0.22 ns for the XC6SLX100 devices using the -2 speed grade.

Table 79: Package Skew

Symbol	Description	Device	Package[2]	Value	Units
$T_{PKGSKEW}$	Package Skew[1]	LX4	TQG144	N/A	ps
			CPG196	23	ps
			CSG225	58	ps
		LX9	TQG144	N/A	ps
			CPG196	23	ps
			CSG225	58	ps
			FT(G)256	88	ps
			CSG324	64	ps
		LX16	CPG196	19	ps
			CSG225	70	ps
			FT(G)256	71	ps
			CSG324	54	ps
		LX25	FT(G)256	90	ps
			CSG324	61	ps
			FG(G)484	84	ps
		LX25T	CSG324	48	ps
			FG(G)484	112	ps

Table 79: **Package Skew *(Cont'd)***

Symbol	Description	Device	Package[2]	Value	Units
$T_{PKGSKEW}$	Package Skew[1]	LX45	CSG324	70	ps
			CS(G)484	99	ps
			FG(G)484	109	ps
			FG(G)676	138	ps
		LX45T	CSG324	75	ps
			CS(G)484	100	ps
			FG(G)484	95	ps
		LX75	CS(G)484	101	ps
			FG(G)484	107	ps
			FG(G)676	161	ps
		LX75T	CS(G)484	107	ps
			FG(G)484	110	ps
			FG(G)676	134	ps
		LX100	CS(G)484	95	ps
			FG(G)484	155	ps
			FG(G)676	144	ps
		LX100T	CS(G)484	88	ps
			FG(G)484	111	ps
			FG(G)676	147	ps
			FG(G)900	134	ps
		LX150	CS(G)484	84	ps
			FG(G)484	103	ps
			FG(G)676	115	ps
			FG(G)900	121	ps
		LX150T	CS(G)484	83	ps
			FG(G)484	88	ps
			FG(G)676	141	ps
			FG(G)900	120	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from Pad to Ball.
2. Some of the devices are available in both Pb and Pb-free (additional G) packages as standard ordering options. See DS160: *Spartan-6 Family Overview* for more information.

Table 80: **Sample Window**

Symbol	Description	Device[1]	Speed Grade				Units
			-3	-3N	-2	-1L	
T_{SAMP}	Sampling Error at Receiver Pins[2]	All	510	510	530	740	ps
T_{SAMP_BUFIO2}	Sampling Error at Receiver Pins using BUFIO2[3]	All	430	430	450	590	ps

Notes:

1. LXT devices are not available with a -1L speed grade.
2. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 DCM jitter
   - DCM accuracy (phase offset)
   - DCM phase shift resolution

   These measurements do not include package or clock tree skew.
3. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO2 clock network and IODELAY2 to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 81: **Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out Using BUFIO2**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO2							
T_{PSCS}/T_{PHCS}	IFF setup/hold using BUFIO2 clock	XC6SLX4	0.57/0.94	N/A	0.95/1.12	0.27/1.56	ns
		XC6SLX9	0.40/0.95	0.50/0.96	0.60/1.12	0.27/1.56	ns
		XC6SLX16	0.48/0.74	0.55/0.75	0.69/0.83	1.27/1.31	ns
		XC6SLX25	0.28/1.02	0.28/1.12	0.28/1.24	0.15/1.78	ns
		XC6SLX25T	0.28/1.02	0.28/1.12	0.28/1.24	N/A	ns
		XC6SLX45	0.42/1.19	0.44/1.29	0.50/1.40	0.12/1.83	ns
		XC6SLX45T	0.42/1.19	0.44/1.29	0.50/1.40	N/A	ns
		XC6SLX75	0.38/1.48	0.38/1.63	0.38/1.84	0.05/2.78	ns
		XC6SLX75T	0.38/1.48	0.38/1.63	0.38/1.84	N/A	ns
		XC6SLX100	0.06/1.48	0.06/1.63	0.06/1.87	–0.03/2.72	ns
		XC6SLX100T	0.06/1.48	0.06/1.63	0.06/1.87	N/A	ns
		XC6SLX150	0.04/1.73	0.04/1.75	0.04/1.98	–0.08/3.07	ns
		XC6SLX150T	0.04/1.73	0.04/1.75	0.04/1.98	N/A	ns
		XA6SLX4	0.64/0.96	N/A	0.97/1.12	N/A	ns
		XA6SLX9	0.44/0.99	N/A	0.62/1.16	N/A	ns
		XA6SLX16	0.50/0.78	N/A	0.69/0.83	N/A	ns
		XA6SLX25	0.28/1.04	N/A	0.28/1.25	N/A	ns
		XA6SLX25T	0.28/1.04	N/A	0.28/1.25	N/A	ns
		XA6SLX45	0.43/1.21	N/A	0.50/1.40	N/A	ns
		XA6SLX45T	0.43/1.21	N/A	0.50/1.40	N/A	ns
		XA6SLX75	0.38/1.49	N/A	0.38/1.84	N/A	ns
		XA6SLX75T	0.38/1.49	N/A	0.38/1.84	N/A	ns
		XA6SLX100	N/A	N/A	1.01/1.63	N/A	ns
		XQ6SLX75	N/A	N/A	0.38/1.84	0.05/2.78	ns
		XQ6SLX75T	0.38/1.49	N/A	0.38/1.84	N/A	ns
		XQ6SLX150	N/A	N/A	0.04/1.98	–0.08/3.07	ns
		XQ6SLX150T	0.04/1.75	N/A	0.04/1.98	N/A	ns