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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	715
Number of Logic Elements/Cells	9152
Total RAM Bits	589824
Number of I/O	186
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx9-2ft256c

Table 4: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.8	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin for commercial (C) and industrial (I) devices	–10	–	10	μA
	V_{REF} leakage current per pin for expanded (Q) devices	–15	–	15	μA
I_L	Input or output leakage current per pin (sample-tested) for commercial (C) and industrial (I) devices	–10	–	10	μA
	Input or output leakage current per pin (sample-tested) for expanded (Q) devices	–15	–	15	μA
I_{HS}	Leakage current on pins during hot socketing with FPGA unpowered	–20	–	20	μA
	All pins except PROGRAM_B, DONE, and JTAG pins when HSWAPEN = 1 PROGRAM_B, DONE, and JTAG pins, or other pins when HSWAPEN = 0	$I_{HS} + I_{RPU}$			μA
$C_{IN}^{(1)}$	Die input capacitance at the pad	–	–	10	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 3.3V$ or $V_{CCAUX} = 3.3V$	200	–	500	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 2.5V$ or $V_{CCAUX} = 2.5V$	120	–	350	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.8V$	60	–	200	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.5V$	40	–	150	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.2V$	12	–	100	μA
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = V_{CCO}$, $V_{CCAUX} = 3.3V$	200	–	550	μA
	Pad pull-down (when selected) @ $V_{IN} = V_{CCO}$, $V_{CCAUX} = 2.5V$	140	–	400	μA
$I_{BATT}^{(2)}$	Battery supply current	–	–	150	nA
$R_{DT}^{(3)}$	Resistance of optional input differential termination circuit, $V_{CCAUX} = 3.3V$	–	100	–	Ω
$R_{IN_TERM}^{(5)}$	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for commercial (C) and industrial (I) devices	23	25	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for expanded (Q) devices	20	25	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for commercial (C) and industrial (I) devices	39	50	72	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for expanded (Q) devices	32	50	74	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for commercial (C) and industrial (I) devices	56	75	109	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for expanded (Q) devices	47	75	115	Ω
R_{OUT_TERM}	Thevenin equivalent resistance of programmable output termination (UNTUNED_25)	11	25	52	Ω
	Thevenin equivalent resistance of programmable output termination (UNTUNED_50)	21	50	96	Ω
	Thevenin equivalent resistance of programmable output termination (UNTUNED_75)	29	75	145	Ω

Notes:

- The C_{IN} measurement represents the die capacitance at the pad, not including the package.
- Maximum value specified for worst case process at 25°C. LX75, LX75T, LX100, LX100T, LX150, and LX150T only.
- Refer to IBIS models for R_{DT} variation and for values at $V_{CCAUX} = 2.5V$. IBIS values for R_{DT} are valid for all temperature ranges.
- V_{CCO2} is not required for data retention. The minimum V_{CCO2} for power-on reset and configuration is 1.65V.
- Termination resistance to a $V_{CCO}/2$ level.

SelectIO™ Interface DC Input and Output Levels

Table 7: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

I/O Standard	V _{CCO} for Drivers ⁽¹⁾			V _{REF} for Inputs		
	V, Min	V, Nom	V, Max	V, Min	V, Nom	V, Max
LVTTTL	3.0	3.3	3.45	V _{REF} is not used for these I/O standards		
LVC MOS33	3.0	3.3	3.45			
LVC MOS25	2.3	2.5	2.7			
LVC MOS18	1.65	1.8	1.95			
LVC MOS18_JEDEC	1.65	1.8	1.95			
LVC MOS15	1.4	1.5	1.6			
LVC MOS15_JEDEC	1.4	1.5	1.6			
LVC MOS12	1.1	1.2	1.3			
LVC MOS12_JEDEC	1.1	1.2	1.3			
PCI33_3 ⁽²⁾	3.0	3.3	3.45			
PCI66_3 ⁽²⁾	3.0	3.3	3.45			
I2C	2.7	3.0	3.45			
SMBUS	2.7	3.0	3.45			
SDIO	3.0	3.3	3.45			
MOBILE_DDR	1.7	1.8	1.9			
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_II	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_III	1.4	1.5	1.6	–	0.9	–
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–
HSTL_III_18	1.7	1.8	1.9	–	1.1	–
SSTL3_I	3.0	3.3	3.45	1.3	1.5	1.7
SSTL3_II	3.0	3.3	3.45	1.3	1.5	1.7
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38
SSTL18_I	1.7	1.8	1.9	0.833	0.9	0.969
SSTL18_II	1.7	1.8	1.9	0.833	0.9	0.969
SSTL15_II	1.425	1.5	1.575	0.69	0.75	0.81

Notes:

1. V_{CCO} range required when using I/O standard for an output. Also required for MOBILE_DDR, PCI33_3, LVC MOS18_JEDEC, LVC MOS15_JEDEC, and LVC MOS12_JEDEC inputs, and for LVC MOS25 inputs when V_{CCAUX} = 3.3V.
2. For PCI systems, the transmitter and receiver should have common supplies for V_{CCO}.

eFUSE Read Endurance

Table 11 lists the minimum guaranteed number of read cycle operations for Device DNA and for the AES eFUSE key. For more information, see [UG380: Spartan-6 FPGA Configuration User Guide](#).

Table 11: eFUSE Read Endurance

Symbol	Description	Speed Grade				Units (Min)
		-3	-3N	-2	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTP Transceiver Specifications

GTP transceivers are available in the Spartan-6 LXT devices. See [DS160: Spartan-6 Family Overview](#) for more information.

GTP Transceiver DC Characteristics

Table 12: Absolute Maximum Ratings for GTP Transceivers⁽¹⁾

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	-0.5	1.32	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	-0.5	1.32	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	-0.5	1.32	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	-0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	-0.5	1.32	V
V _{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	-0.5	1.32	V
V _{MGTREFCLK}	Reference clock absolute input voltage	-0.5	1.32	V

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 13: Recommended Operating Conditions for GTP Transceivers⁽¹⁾⁽²⁾⁽³⁾

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTTX	Analog supply voltage for the GTP transmitter termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVTTRX	Analog supply voltage for the GTP receiver termination circuit relative to GND	1.14	1.20	1.26	V
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND	1.14	1.20	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom)	1.14	1.20	1.26	V

Notes:

- Each voltage listed requires the filter circuit described in [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#).
- Voltages are specified for the temperature range of T_j = -40°C to +125°C.
- The voltage level of MGTAVCCPLL must not exceed the voltage level of MGTAVCC +10mV. The voltage level of MGTAVCC must not exceed the voltage level of MGTAVCCPLL.

Table 14: GTP Transceiver Current Supply (per Lane)

Symbol	Description	Typ ⁽¹⁾	Max	Units
I _{MGTAVCC}	GTP transceiver internal analog supply current	40.4	Note 2	mA
I _{MGTAVTTTX}	GTP transmitter termination supply current	27.4		mA
I _{MGTAVTTRX}	GTP receiver termination supply current	13.6		mA
I _{MGTAVCCPLL}	GTP transmitter and receiver PLL supply current	28.7		mA
R _{MGTRREF}	Precision reference resistor for internal calibration termination	50.0 ± 1% tolerance		Ω

Notes:

- Typical values are specified at nominal voltage, 25°C, with a 2.5 Gb/s line rate, with a shared PLL use mode.
- Values for currents of other transceiver configurations and conditions can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 15: GTP Transceiver Quiescent Supply Current (per Lane)⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

Symbol	Description	Typ ⁽⁵⁾	Max	Units
I _{MGTAVCCQ}	Quiescent MGTAVCC supply current	1.7	Note 2	mA
I _{MGTAVTTTXQ}	Quiescent MGTAVTTTX supply current	0.1		mA
I _{MGTAVTTRXQ}	Quiescent MGTAVTTRX supply current	1.2		mA
I _{MGTAVCCPLLQ}	Quiescent MGTAVCCPLL supply current	1.0		mA

Notes:

- Device powered and unconfigured.
- Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
- GTP transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTP transceivers.
- Does not include power-up MGTAVTTRCAL supply current during device configuration.
- Typical values are specified at nominal voltage, 25°C.

Table 23: GTP Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units	
T _{RXELECIDLE}	Time for RXELECIDLE to respond to loss or restoration of data		–	75	–	ns	
R _{XOVBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV	
R _{XSST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	0	ppm	
R _{XRL}	Run length (CID)	Internal AC capacitor bypassed	–	–	150	UI	
R _{XPMTOL}	Data/REFCLK PPM offset tolerance	CDR 2 nd -order loop disabled	–200	–	200	ppm	
		CDR 2 nd -order loop enabled	PLL_RXDIVSEL_OUT = 1	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 2	–2000	–	2000	ppm
			PLL_RXDIVSEL_OUT = 4	–1000	–	1000	ppm
SJ Jitter Tolerance ⁽²⁾							
JT_SJ _{3.125}	Sinusoidal Jitter ⁽³⁾	3.125 Gb/s	0.4	–	–	UI	
JT_SJ _{2.5}	Sinusoidal Jitter ⁽³⁾	2.5 Gb/s	0.4	–	–	UI	
JT_SJ _{1.62}	Sinusoidal Jitter ⁽³⁾	1.62 Gb/s	0.5	–	–	UI	
JT_SJ _{1.25}	Sinusoidal Jitter ⁽³⁾	1.25 Gb/s	0.5	–	–	UI	
JT_SJ ₆₁₄	Sinusoidal Jitter ⁽³⁾	614 Mb/s	0.5	–	–	UI	
SJ Jitter Tolerance with Stressed Eye ⁽²⁾⁽⁵⁾							
JT_TJSE _{3.125}	Total Jitter with stressed eye ⁽⁴⁾	3.125 Gb/s	0.65	–	–	UI	
JT_SJSE _{3.125}	Sinusoidal Jitter with stressed eye	3.125 Gb/s	0.1	–	–	UI	
JT_TJSE _{2.7}	Total Jitter with stressed eye ⁽⁴⁾	2.7 Gb/s	0.65	–	–	UI	
JT_SJSE _{2.7}	Sinusoidal Jitter with stressed eye	2.7 Gb/s	0.1	–	–	UI	

Notes:

- Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
- All jitter values are based on a Bit Error Ratio of 1e⁻¹².
- Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
- Composed of 0.37 UI DJ in the form of ISI and 0.18 UI RJ.
- Measured using PRBS7 data pattern.

Endpoint Block for PCI Express Designs Switching Characteristics

The Endpoint block for PCI Express is available in the Spartan-6 LXT devices. Consult the [Spartan-6 FPGA Integrated Endpoint Block for PCI Express](#) for further information.

Table 24: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
F _{PCIEUSER}	User clock maximum frequency	62.5	62.5	62.5	N/A	MHz

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVC MOS15, Slow, 8 mA	0.98	1.10	1.23	1.79	2.30	2.44	2.64	3.25	2.30	2.44	2.64	3.25	ns
LVC MOS15, Slow, 12 mA	0.98	1.10	1.23	1.79	2.03	2.17	2.37	2.99	2.03	2.17	2.37	2.99	ns
LVC MOS15, Slow, 16 mA	0.98	1.10	1.23	1.79	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVC MOS15, Fast, 2 mA	0.98	1.10	1.23	1.79	3.29	3.43	3.63	4.24	3.29	3.43	3.63	4.24	ns
LVC MOS15, Fast, 4 mA	0.98	1.10	1.23	1.79	2.27	2.41	2.61	3.22	2.27	2.41	2.61	3.22	ns
LVC MOS15, Fast, 6 mA	0.98	1.10	1.23	1.79	1.78	1.92	2.12	2.74	1.78	1.92	2.12	2.74	ns
LVC MOS15, Fast, 8 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.69	1.73	1.87	2.07	2.69	ns
LVC MOS15, Fast, 12 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.64	1.73	1.87	2.07	2.64	ns
LVC MOS15, Fast, 16 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.64	1.73	1.87	2.07	2.64	ns
LVC MOS15_JEDEC, QUIETIO, 2 mA	1.03	1.15	1.28	1.49	5.49	5.63	5.83	6.37	5.49	5.63	5.83	6.37	ns
LVC MOS15_JEDEC, QUIETIO, 4 mA	1.03	1.15	1.28	1.49	4.61	4.75	4.95	5.51	4.61	4.75	4.95	5.51	ns
LVC MOS15_JEDEC, QUIETIO, 6 mA	1.03	1.15	1.28	1.49	4.07	4.21	4.41	4.97	4.07	4.21	4.41	4.97	ns
LVC MOS15_JEDEC, QUIETIO, 8 mA	1.03	1.15	1.28	1.49	3.92	4.06	4.26	4.81	3.92	4.06	4.26	4.81	ns
LVC MOS15_JEDEC, QUIETIO, 12 mA	1.03	1.15	1.28	1.49	3.54	3.68	3.88	4.51	3.54	3.68	3.88	4.51	ns
LVC MOS15_JEDEC, QUIETIO, 16 mA	1.03	1.15	1.28	1.49	3.33	3.47	3.67	4.31	3.33	3.47	3.67	4.31	ns
LVC MOS15_JEDEC, Slow, 2 mA	1.03	1.15	1.28	1.49	4.18	4.32	4.52	5.13	4.18	4.32	4.52	5.13	ns
LVC MOS15_JEDEC, Slow, 4 mA	1.03	1.15	1.28	1.49	3.42	3.56	3.76	4.35	3.42	3.56	3.76	4.35	ns
LVC MOS15_JEDEC, Slow, 6 mA	1.03	1.15	1.28	1.49	2.29	2.43	2.63	3.25	2.29	2.43	2.63	3.25	ns
LVC MOS15_JEDEC, Slow, 8 mA	1.03	1.15	1.28	1.49	2.30	2.44	2.64	3.26	2.30	2.44	2.64	3.26	ns
LVC MOS15_JEDEC, Slow, 12 mA	1.03	1.15	1.28	1.49	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVC MOS15_JEDEC, Slow, 16 mA	1.03	1.15	1.28	1.49	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVC MOS15_JEDEC, Fast, 2 mA	1.03	1.15	1.28	1.49	3.28	3.42	3.62	4.22	3.28	3.42	3.62	4.22	ns
LVC MOS15_JEDEC, Fast, 4 mA	1.03	1.15	1.28	1.49	2.27	2.41	2.61	3.23	2.27	2.41	2.61	3.23	ns
LVC MOS15_JEDEC, Fast, 6 mA	1.03	1.15	1.28	1.49	1.78	1.92	2.12	2.74	1.78	1.92	2.12	2.74	ns
LVC MOS15_JEDEC, Fast, 8 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.69	1.73	1.87	2.07	2.69	ns
LVC MOS15_JEDEC, Fast, 12 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.63	1.73	1.87	2.07	2.63	ns
LVC MOS15_JEDEC, Fast, 16 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.63	1.73	1.87	2.07	2.63	ns
LVC MOS12, QUIETIO, 2 mA	0.91	1.03	1.16	1.51	6.40	6.54	6.74	7.30	6.40	6.54	6.74	7.30	ns
LVC MOS12, QUIETIO, 4 mA	0.91	1.03	1.16	1.51	4.98	5.12	5.32	5.90	4.98	5.12	5.32	5.90	ns
LVC MOS12, QUIETIO, 6 mA	0.91	1.03	1.16	1.51	4.65	4.79	4.99	5.55	4.65	4.79	4.99	5.55	ns
LVC MOS12, QUIETIO, 8 mA	0.91	1.03	1.16	1.51	4.23	4.37	4.57	5.21	4.23	4.37	4.57	5.21	ns
LVC MOS12, QUIETIO, 12 mA	0.91	1.03	1.16	1.51	3.98	4.12	4.32	4.94	3.98	4.12	4.32	4.94	ns
LVC MOS12, Slow, 2 mA	0.91	1.03	1.16	1.51	4.98	5.12	5.32	5.91	4.98	5.12	5.32	5.91	ns
LVC MOS12, Slow, 4 mA	0.91	1.03	1.16	1.51	2.84	2.98	3.18	3.81	2.84	2.98	3.18	3.81	ns
LVC MOS12, Slow, 6 mA	0.91	1.03	1.16	1.51	2.77	2.91	3.11	3.72	2.77	2.91	3.11	3.72	ns
LVC MOS12, Slow, 8 mA	0.91	1.03	1.16	1.51	2.34	2.48	2.68	3.31	2.34	2.48	2.68	3.31	ns
LVC MOS12, Slow, 12 mA	0.91	1.03	1.16	1.51	2.08	2.22	2.42	3.06	2.08	2.22	2.42	3.06	ns

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVC MOS12, Fast, 2 mA	0.91	1.03	1.16	1.51	3.46	3.60	3.80	4.44	3.46	3.60	3.80	4.44	ns
LVC MOS12, Fast, 4 mA	0.91	1.03	1.16	1.51	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVC MOS12, Fast, 6 mA	0.91	1.03	1.16	1.51	1.79	1.93	2.13	2.75	1.79	1.93	2.13	2.75	ns
LVC MOS12, Fast, 8 mA	0.91	1.03	1.16	1.51	1.68	1.82	2.02	2.64	1.68	1.82	2.02	2.64	ns
LVC MOS12, Fast, 12 mA	0.91	1.03	1.16	1.51	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
LVC MOS12_JEDEC, QUIETIO, 2 mA	1.50	1.62	1.75	1.88	6.39	6.53	6.73	7.31	6.39	6.53	6.73	7.31	ns
LVC MOS12_JEDEC, QUIETIO, 4 mA	1.50	1.62	1.75	1.88	4.98	5.12	5.32	5.88	4.98	5.12	5.32	5.88	ns
LVC MOS12_JEDEC, QUIETIO, 6 mA	1.50	1.62	1.75	1.88	4.67	4.81	5.01	5.54	4.67	4.81	5.01	5.54	ns
LVC MOS12_JEDEC, QUIETIO, 8 mA	1.50	1.62	1.75	1.88	4.23	4.37	4.57	5.22	4.23	4.37	4.57	5.22	ns
LVC MOS12_JEDEC, QUIETIO, 12 mA	1.50	1.62	1.75	1.88	3.99	4.13	4.33	4.94	3.99	4.13	4.33	4.94	ns
LVC MOS12_JEDEC, Slow, 2 mA	1.50	1.62	1.75	1.88	5.00	5.14	5.34	5.90	5.00	5.14	5.34	5.90	ns
LVC MOS12_JEDEC, Slow, 4 mA	1.50	1.62	1.75	1.88	2.85	2.99	3.19	3.80	2.85	2.99	3.19	3.80	ns
LVC MOS12_JEDEC, Slow, 6 mA	1.50	1.62	1.75	1.88	2.76	2.90	3.10	3.72	2.76	2.90	3.10	3.72	ns
LVC MOS12_JEDEC, Slow, 8 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.30	2.35	2.49	2.69	3.30	ns
LVC MOS12_JEDEC, Slow, 12 mA	1.50	1.62	1.75	1.88	2.09	2.23	2.43	3.05	2.09	2.23	2.43	3.05	ns
LVC MOS12_JEDEC, Fast, 2 mA	1.50	1.62	1.75	1.88	3.46	3.60	3.80	4.42	3.46	3.60	3.80	4.42	ns
LVC MOS12_JEDEC, Fast, 4 mA	1.50	1.62	1.75	1.88	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns
LVC MOS12_JEDEC, Fast, 6 mA	1.50	1.62	1.75	1.88	1.79	1.93	2.13	2.76	1.79	1.93	2.13	2.76	ns
LVC MOS12_JEDEC, Fast, 8 mA	1.50	1.62	1.75	1.88	1.69	1.83	2.03	2.65	1.69	1.83	2.03	2.65	ns
LVC MOS12_JEDEC, Fast, 12 mA	1.50	1.62	1.75	1.88	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns

Notes:

1. The -1L values listed in this table are also applicable to the Spartan-6Q devices.
2. Devices with a -1L speed grade do not support Xilinx PCI IP.

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

I/O Standard	T _{IOPI}		T _{IOOP}		T _{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS18, QUIETIO, 16 mA	1.25	1.43	3.34	3.54	3.34	3.54	ns
LVC MOS18, QUIETIO, 24 mA	1.25	1.43	3.18	3.38	3.18	3.38	ns
LVC MOS18, Slow, 2 mA	1.25	1.43	4.79	4.99	4.79	4.99	ns
LVC MOS18, Slow, 4 mA	1.25	1.43	3.84	4.04	3.84	4.04	ns
LVC MOS18, Slow, 6 mA	1.25	1.43	3.17	3.37	3.17	3.37	ns
LVC MOS18, Slow, 8 mA	1.25	1.43	2.37	2.57	2.37	2.57	ns
LVC MOS18, Slow, 12 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns
LVC MOS18, Slow, 16 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns
LVC MOS18, Slow, 24 mA	1.25	1.43	2.13	2.33	2.13	2.33	ns
LVC MOS18, Fast, 2 mA	1.25	1.43	3.78	3.98	3.78	3.98	ns
LVC MOS18, Fast, 4 mA	1.25	1.43	2.54	2.74	2.54	2.74	ns
LVC MOS18, Fast, 6 mA	1.25	1.43	2.02	2.22	2.02	2.22	ns
LVC MOS18, Fast, 8 mA	1.25	1.43	1.95	2.15	1.95	2.15	ns
LVC MOS18, Fast, 12 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns
LVC MOS18, Fast, 16 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns
LVC MOS18, Fast, 24 mA	1.25	1.43	1.85	2.05	1.85	2.05	ns
LVC MOS18_JEDEC, QUIETIO, 2 mA	1.01	1.19	6.09	6.29	6.09	6.29	ns
LVC MOS18_JEDEC, QUIETIO, 4 mA	1.01	1.19	4.89	5.09	4.89	5.09	ns
LVC MOS18_JEDEC, QUIETIO, 6 mA	1.01	1.19	4.20	4.40	4.20	4.40	ns
LVC MOS18_JEDEC, QUIETIO, 8 mA	1.01	1.19	3.87	4.07	3.87	4.07	ns
LVC MOS18_JEDEC, QUIETIO, 12 mA	1.01	1.19	3.49	3.69	3.49	3.69	ns
LVC MOS18_JEDEC, QUIETIO, 16 mA	1.01	1.19	3.34	3.54	3.34	3.54	ns
LVC MOS18_JEDEC, QUIETIO, 24 mA	1.01	1.19	3.17	3.37	3.17	3.37	ns
LVC MOS18_JEDEC, Slow, 2 mA	1.01	1.19	4.79	4.99	4.79	4.99	ns
LVC MOS18_JEDEC, Slow, 4 mA	1.01	1.19	3.84	4.04	3.84	4.04	ns
LVC MOS18_JEDEC, Slow, 6 mA	1.01	1.19	3.18	3.38	3.18	3.38	ns
LVC MOS18_JEDEC, Slow, 8 mA	1.01	1.19	2.37	2.57	2.37	2.57	ns
LVC MOS18_JEDEC, Slow, 12 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns
LVC MOS18_JEDEC, Slow, 16 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns
LVC MOS18_JEDEC, Slow, 24 mA	1.01	1.19	2.13	2.33	2.13	2.33	ns
LVC MOS18_JEDEC, Fast, 2 mA	1.01	1.19	3.75	3.95	3.75	3.95	ns
LVC MOS18_JEDEC, Fast, 4 mA	1.01	1.19	2.54	2.74	2.54	2.74	ns
LVC MOS18_JEDEC, Fast, 6 mA	1.01	1.19	2.02	2.22	2.02	2.22	ns
LVC MOS18_JEDEC, Fast, 8 mA	1.01	1.19	1.94	2.14	1.94	2.14	ns
LVC MOS18_JEDEC, Fast, 12 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns
LVC MOS18_JEDEC, Fast, 16 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns
LVC MOS18_JEDEC, Fast, 24 mA	1.01	1.19	1.86	2.06	1.86	2.06	ns

Table 32: Output Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	R_{REF} (Ω)	$C_{REF}^{(1)}$ (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
SSTL, Class II, 1.5V	SSTL15_II	25	0	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	100	0	0 ⁽³⁾	—
BLVDS (Bus LVDS), 2.5V	BLVDS_25	Note 4	0	0 ⁽³⁾	—
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	100	0	0 ⁽³⁾	—
RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RSDS_25, RSDS_33	100	0	0 ⁽³⁾	—
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	Note 5	0	0 ⁽³⁾	—
PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V	PPDS_25, PPDS_33	100	0	0 ⁽³⁾	—

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. The value given is the differential output voltage.
4. See the *BLVDS Output Termination* section in [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.
5. See the *TMDS_33 Termination* section in [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.

Simultaneously Switching Outputs

Due to package electrical parasitics, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. [Table 33](#) and [Table 34](#) provide guidelines for the recommended maximum allowable number of SSOs. These guidelines describe the maximum number of user I/O pins of an output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise for that particular signal standard. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of GND and power bounce.

For each device/package combination, [Table 33](#) provides the number of equivalent V_{CCO} /GND pairs per bank. For each output signal standard and drive strength, [Table 34](#) recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO} /GND pair within an I/O bank. The guidelines are categorized by package style, slew rate, and output drive current. The number of SSOs are also specified by I/O bank. Multiply the appropriate numbers from each table to calculate the maximum number of SSOs allowed within an I/O bank. The guidelines assume that all pins within a bank use the same I/O standard. Exceeding these SSO guidelines can result in increased power or GND bounce, degraded signal integrity, or increased system jitter. For a given I/O standard, if the SSO limit per pair in [Table 34](#) is greater than the maximum I/O per pair in [Table 33](#), then there is no SSO limit for the exclusive use of that I/O standard.

The recommended maximum SSO values assume that the FPGA is soldered on a printed circuit board and that the board uses sound design practices. Due to the additional inductance introduced by the socket, the SSO values do not apply for FPGAs mounted in sockets. The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics. For more detail, see [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

V _{CCO}	I/O Standard	Drive	Slew	SSO Limit per V _{CCO} /GND Pair					
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324			
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5		
2.5V	LVCMOS25	2	Fast	38	43	38	43		
			Slow	46	52	46	48		
			QuietIO	57	64	57	59		
		4	Fast	21	24	21	23		
			Slow	26	31	26	27		
			QuietIO	33	32	33	30		
		6	Fast	15	17	15	16		
			Slow	19	22	19	19		
			QuietIO	25	23	25	19		
		8	Fast	12	15	12	14		
			Slow	15	18	15	16		
			QuietIO	21	19	21	16		
		12	Fast	1	3	1	1		
			Slow	2	7	2	4		
			QuietIO	3	8	3	8		
		16	Fast	1	3	1	1		
			Slow	3	7	3	3		
			QuietIO	4	9	4	8		
		24	Fast	N/A	3	N/A	1		
			Slow	N/A	5	N/A	2		
			QuietIO	N/A	8	N/A	6		
		SSTL_2_I ⁽³⁾				10	11	10	11
		SSTL_2_II ⁽³⁾				N/A	7	N/A	7
		DIFF_SSTL_2_I ⁽³⁾				30	33	30	33
	DIFF_SSTL_2_II ⁽³⁾				N/A	21	N/A	24	

Input/Output Logic Switching Characteristics

Table 35: ILOGIC2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T _{ICE0CK} /T _{ICKCE0}	CE0 pin Setup/Hold with respect to CLK	0.56/ −0.30	0.56/ −0.25	0.79/ −0.22	1.21/ −0.52	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.74/ −0.23	0.74/ −0.22	0.98/ −0.20	1.31/ −0.45	ns
T _{IDOCK} /T _{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	1.19/ −0.83	1.36/ −0.83	1.73/ −0.83	2.18/ −1.77	ns
T _{IDOCKD} /T _{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	0.31/ 0.00	0.47/ 0.00	0.54/ 0.00	0.63/ −0.39	ns
Combinatorial						
T _{IDI}	D pin to O pin propagation delay, no Delay	0.95	1.28	1.53	2.25	ns
T _{IDID}	DDLY pin to O pin propagation delay (using IODELAY2)	0.23	0.39	0.44	0.74	ns
Sequential Delays						
T _{IDLO}	D pin to Q pin using flip-flop as a latch without Delay	1.56	1.86	2.39	3.49	ns
T _{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY2)	0.68	0.97	1.20	1.94	ns
T _{ICKQ}	CLK to Q outputs for XC devices	1.03	1.24	1.43	2.11	ns
	CLK to Q outputs for XA and XQ devices	1.38	N/A	1.78	2.11	ns
T _{RQ_ILOGIC2}	SR pin to Q outputs	1.81	1.81	2.50	3.05	ns

Table 36: OLOGIC2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T _{ODCK} /T _{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.81/ −0.05	0.86/ −0.05	1.18/ 0.00	1.73/ −0.27	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.75/ −0.10	0.75/ −0.10	1.01/ −0.05	1.66/ −0.23	ns
T _{OSRCK} /T _{OCKSR}	SR pin Setup/Hold with respect to CLK	0.70/ −0.28	0.79/ −0.28	1.03/ −0.23	1.39/ −0.47	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.24/ −0.08	0.56/ −0.06	0.83/ −0.01	0.99/ −0.19	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.58/ −0.06	0.72/ −0.06	1.18/ −0.01	1.51/ −0.13	ns
Sequential Delays						
T _{OCKQ}	CLK to OQ/TQ out for XC devices	0.48	0.51	0.74	0.74	ns
	CLK to OQ/TQ out for XA and XQ devices	0.85	N/A	1.16	0.74	ns
T _{RQ_OLOGIC2}	SR pin to OQ/TQ out	1.81	1.81	2.50	3.05	ns

Input/Output Delay Switching Characteristics

Table 39: IODELAY2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L ⁽³⁾	
$T_{\text{IODCCK_CAL}} / T_{\text{IODCKC_CAL}}$	CAL pin Setup/Hold with respect to CK	0.28/ -0.13	0.33/ -0.13	0.48/ -0.13	N/A	ns
$T_{\text{IODCCK_CE}} / T_{\text{IODCKC_CE}}$	CE pin Setup/Hold with respect to CK	0.17/ -0.03	0.17/ -0.03	0.25/ -0.02	N/A	ns
$T_{\text{IODCCK_INC}} / T_{\text{IODCKC_INC}}$	INC pin Setup/Hold with respect to CK	0.10/ 0.02	0.12/ 0.03	0.18/ 0.06	N/A	ns
$T_{\text{IODCCK_RST}} / T_{\text{IODCKC_RST}}$	RST pin Setup/Hold with respect to CK	0.12/ -0.02	0.15/ -0.02	0.22/ -0.01	N/A	ns
$T_{\text{TAP1}}^{(2)}$	Maximum tap 1 delay	8	14	16	N/A	ps
T_{TAP2}	Maximum tap 2 delay	40	66	77	N/A	ps
T_{TAP3}	Maximum tap 3 delay	95	120	140	N/A	ps
T_{TAP4}	Maximum tap 4 delay	108	141	166	N/A	ps
T_{TAP5}	Maximum tap 5 delay	171	194	231	N/A	ps
T_{TAP6}	Maximum tap 6 delay	207	249	292	N/A	ps
T_{TAP7}	Maximum tap 7 delay	212	276	343	N/A	ps
T_{TAP8}	Maximum tap 8 delay	322	341	424	N/A	ps
F_{MINCAL}	Minimum allowed bit rate for calibration in variable mode: VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX, and DIFF_PHASE_DETECTOR.	188	188	188	N/A	Mb/s
$T_{\text{IODDO_IDATAIN}}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	—
$T_{\text{IODDO_ODATAIN}}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	—

Notes:

- Delay depends on IODELAY2 tap setting. See TRACE report for actual values.
- Maximum delay = integer (number of taps/8) $\times$ T_{TAP8} + T_{TAPn} (where n equals the remainder). For minimum delay consult the TRACE setup and hold report. Minimum delay is typically greater than 30% of the maximum delay. Tap delays can vary by device and overall conditions. See TRACE report for actual values.
- Spartan-6 -1L devices only support tap 0. See TRACE report for actual values.

Block RAM Switching Characteristics

Table 43: Block RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Block RAM Clock to Out Delays						
T _{RCKO_DO}	Clock CLK to DOUT output (without output register) ⁽¹⁾	1.85	2.10	2.10	3.50	ns, Max
T _{RCKO_DO_REG}	Clock CLK to DOUT output (with output register) ⁽²⁾	1.60	1.75	1.75	2.30	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{RCCK_ADDR} /T _{RCKC_ADDR}	ADDR inputs for XC devices ⁽³⁾	0.35/ 0.10	0.40/ 0.12	0.40/ 0.12	0.50/ 0.15	ns, Min
	ADDR inputs for XA and XQ devices ⁽³⁾	0.35/ 0.17	N/A	0.40/ 0.17	0.50/ 0.15	ns, Min
T _{RDCK_DI} /T _{RCKD_DI}	DIN inputs ⁽⁴⁾	0.30/ 0.10	0.30/ 0.10	0.30/ 0.10	0.40/ 0.15	ns, Min
T _{RCCK_EN} /T _{RCKC_EN}	Block RAM Enable (EN) input	0.22/ 0.05	0.25/ 0.06	0.25/ 0.06	0.44/ 0.10	ns, Min
T _{RCCK_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.20/ 0.10	0.20/ 0.10	0.20/ 0.10	0.28/ 0.15	ns, Min
T _{RCCK_WE} /T _{RCKC_WE}	Write Enable (WE) input	0.25/ 0.10	0.33/ 0.10	0.33/ 0.10	0.28/ 0.15	ns, Min
Maximum Frequency						
F _{MAX}	Block RAM in all modes	320	280	280	150	MHz

Notes:

- T_{RCKO_DO} includes T_{RCKO_DOA} and T_{RCKO_DOPA} as well as the B port equivalent timing parameters.
- $T_{RCKO_DO_REG}$ includes $T_{RCKO_DOA_REG}$ and $T_{RCKO_DOPA_REG}$ as well as the B port equivalent timing parameters.
- The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
- T_{RDCK_DI} includes both A and B inputs as well as the parity inputs of A and B.

Table 52: PLL Specification (Cont'd)

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
F _{INMIN}	Minimum Input Clock Frequency	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
F _{INJITTER}	Maximum Input Clock Period Jitter: 19–200 MHz	All	1 ns Maximum				
	Maximum Input Clock Period Jitter: > 200 MHz	All	<20% of clock input period Maximum				
F _{INDUTY}	Allowable Input Duty Cycle: 19—199 MHz	All	25/75				%
	Allowable Input Duty Cycle: 200—299 MHz	All	35/65				%
	Allowable Input Duty Cycle: > 300 MHz	All	45/55				%
F _{VCOMIN}	Minimum PLL VCO Frequency	LX devices	400	400	400	400	MHz
		LXT devices	400	400	400	N/A	MHz
F _{VCOMAX}	Maximum PLL VCO Frequency	LX devices	1080	1050	1000	1000	MHz
		LXT devices	1080	1050	1000	N/A	MHz
F _{BANDWIDTH}	Low PLL Bandwidth at Typical ⁽³⁾	All	1	1	1	1	MHz
	High PLL Bandwidth at Typical ⁽³⁾	All	4	4	4	4	MHz
T _{STAPHAOFFSET}	Static Phase Offset of the PLL Outputs	All	0.12	0.12	0.12	0.15	ns
T _{OUTJITTER}	PLL Output Jitter ⁽³⁾	All	Note 2				
T _{OUTDUTY}	PLL Output Clock Duty Cycle Precision ⁽⁴⁾	All	0.15	0.15	0.20	0.25	ns
T _{LOCKMAX}	PLL Maximum Lock Time	All	100	100	100	100	μs
F _{OUTMAX}	PLL Maximum Output Frequency for BUFGMUX	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz
	PLL Maximum Output Frequency for BUFPLL	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz
F _{OUTMIN}	PLL Minimum Output Frequency ⁽⁵⁾	All	3.125	3.125	3.125	3.125	MHz
T _{EXTFDVAR}	External Clock Feedback Variation: 19–200 MHz	All	1 ns Maximum				
	External Clock Feedback Variation: > 200 MHz	All	< 20% of clock input period Maximum				
RST _{MINPULSE}	Minimum Reset Pulse Width	All	5	5	5	5	ns
F _{PFDMAX} ⁽⁵⁾	Maximum Frequency at the Phase Frequency Detector	LX devices	500	500	400	300	MHz
		LXT devices	500	500	400	N/A	MHz
F _{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
T _{FBDELAY}	Maximum Delay in the Feedback Path	All	3 ns Max or one CLKIN cycle				

Notes:

1. LXT devices are not available with a -1L speed grade.
2. Values for this parameter are available in the Clocking Wizard.
3. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When using CLK_FEEDBACK = CLKOUT0 with BUFIO2 feedback, the feedback frequency will be higher than the phase frequency detector frequency. $F_{PFDMAX} = F_{CLKFB} / CLKFBOUT_MULT$

Table 57: Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)⁽¹⁾ (Cont'd)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Spread Spectrum										
F _{CLKIN_FIXED_SPREAD_SPECTRUM}	Frequency of the CLKIN input for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD/ CENTER_HIGH_SPREAD)	30	200	30	200	30	200	30	200	MHz
T _{CENTER_LOW_SPREAD} ⁽⁶⁾	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD)	Typical = $\frac{100}{\text{CLKFX_DIVIDE}}$ Maximum = 250								ps
T _{CENTER_HIGH_SPREAD} ⁽⁶⁾	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM= CENTER_HIGH_SPREAD)	Typical = $\frac{240}{\text{CLKFX_DIVIDE}}$ Maximum = 400								ps
F _{MOD_FIXED_SPREAD_SPECTRUM} ⁽⁶⁾	Average modulation frequency when using fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD / CENTER_HIGH_SPREAD)	Typical = F _{IN} /1024								MHz

Notes:

- The values in this table are based on the operating conditions described in Table 2 and Table 55.
- For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
- Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
- The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
- Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of $\pm(1\% \text{ of CLKFX period} + 200 \text{ ps})$. Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is $\pm(100 \text{ ps} + 200 \text{ ps}) = \pm 300 \text{ ps}$.
- When using CENTER_LOW_SPREAD, CENTER_HIGH_SPREAD, the valid values for CLKFX_MULTIPLY are limited to 2 through 32, and the valid values for CLKFX_DIVIDE are limited to 1 through 4.

Table 58: Recommended Operating Conditions for the Phase-Shift Clock in Variable Phase Mode (DCM_SP) or Dynamic Frequency Synthesis (DCM_CLKGEN)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Operating Frequency Ranges										
PSCLK_FREQ	Frequency for the PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) input.	1	167	1	167	1	167	1	100	MHz
Input Pulse Requirements										
PSCLK_PULSE	PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) pulse width as a percentage of the clock period.	40	60	40	60	40	60	40	60	%

Table 65: Global Clock Input to Output Delay With DCM in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in Source-Synchronous Mode.							
T _{ICKOFDCM_0}	Global Clock and OUTFF <i>with</i> DCM	XC6SLX4	5.03	N/A	7.21	8.05	ns
		XC6SLX9	5.03	6.13	7.21	8.05	ns
		XC6SLX16	5.08	5.51	6.44	7.96	ns
		XC6SLX25	4.81	5.13	5.69	7.94	ns
		XC6SLX25T	4.81	5.13	5.69	N/A	ns
		XC6SLX45	5.26	5.69	6.63	7.92	ns
		XC6SLX45T	5.26	5.69	6.63	N/A	ns
		XC6SLX75	4.77	5.18	5.88	7.95	ns
		XC6SLX75T	4.77	5.18	5.88	N/A	ns
		XC6SLX100	4.72	5.11	5.76	8.59	ns
		XC6SLX100T	4.76	5.11	5.76	N/A	ns
		XC6SLX150	4.90	5.30	5.93	7.93	ns
		XC6SLX150T	4.90	5.30	5.93	N/A	ns
		XA6SLX4	5.35	N/A	7.21	N/A	ns
		XA6SLX9	5.35	N/A	7.21	N/A	ns
		XA6SLX16	5.42	N/A	6.44	N/A	ns
		XA6SLX25	5.13	N/A	5.69	N/A	ns
		XA6SLX25T	5.13	N/A	5.79	N/A	ns
		XA6SLX45	5.58	N/A	6.63	N/A	ns
		XA6SLX45T	5.58	N/A	6.63	N/A	ns
		XA6SLX75	5.09	N/A	5.87	N/A	ns
		XA6SLX75T	5.09	N/A	5.87	N/A	ns
		XA6SLX100	N/A	N/A	6.44	N/A	ns
		XQ6SLX75	N/A	N/A	5.87	7.95	ns
		XQ6SLX75T	5.09	N/A	5.87	N/A	ns
		XQ6SLX150	N/A	N/A	6.06	7.93	ns
		XQ6SLX150T	5.50	N/A	6.06	N/A	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
- DCM output jitter is already included in the timing calculation.

Table 74: Global Clock Setup and Hold With PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.(1)							
T _{PSPLL} / T _{PHPLL}	No Delay Global Clock and IFF(2) with PLL in System-Synchronous Mode	XC6SLX4	1.37/0.25	N/A	1.52/0.41	2.07/0.69	ns
		XC6SLX9	1.37/0.21	1.48/0.21	1.52/0.26	2.07/0.69	ns
		XC6SLX16	1.33/−0.03	1.53/−0.02	1.60/−0.02	1.57/0.48	ns
		XC6SLX25	1.65/0.28	1.71/0.28	1.91/0.28	2.44/0.76	ns
		XC6SLX25T	1.65/0.28	1.71/0.28	1.91/0.28	N/A	ns
		XC6SLX45	1.55/0.18	1.64/0.18	1.75/0.18	2.02/0.90	ns
		XC6SLX45T	1.55/0.18	1.64/0.18	1.75/0.18	N/A	ns
		XC6SLX75	1.77/0.21	1.89/0.21	2.13/0.21	2.46/0.53	ns
		XC6SLX75T	1.77/0.21	1.89/0.21	2.13/0.21	N/A	ns
		XC6SLX100	1.44/0.32	1.52/0.32	1.70/0.32	1.78/0.86	ns
		XC6SLX100T	1.44/0.32	1.52/0.32	1.70/0.32	N/A	ns
		XC6SLX150	1.39/0.49	1.48/0.49	1.67/0.49	1.94/0.94	ns
		XC6SLX150T	1.39/0.49	1.48/0.49	1.67/0.49	N/A	ns
		XA6SLX4	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX9	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX16	1.89/−0.08	N/A	1.72/−0.08	N/A	ns
		XA6SLX25	1.85/0.16	N/A	2.08/0.16	N/A	ns
		XA6SLX25T	1.85/0.16	N/A	2.17/0.16	N/A	ns
		XA6SLX45	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX45T	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX75	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX100	N/A	N/A	2.34/0.14	N/A	ns
		XQ6SLX75	N/A	N/A	2.25/0.06	2.46/0.53	ns
		XQ6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XQ6SLX150	N/A	N/A	1.79/0.37	1.94/0.94	ns
		XQ6SLX150T	1.43/0.37	N/A	1.79/0.37	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 79: Package Skew (Cont'd)

Symbol	Description	Device	Package ⁽²⁾	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	LX45	CSG324	70	ps
			CS(G)484	99	ps
			FG(G)484	109	ps
			FG(G)676	138	ps
		LX45T	CSG324	75	ps
			CS(G)484	100	ps
			FG(G)484	95	ps
		LX75	CS(G)484	101	ps
			FG(G)484	107	ps
			FG(G)676	161	ps
		LX75T	CS(G)484	107	ps
			FG(G)484	110	ps
			FG(G)676	134	ps
		LX100	CS(G)484	95	ps
			FG(G)484	155	ps
			FG(G)676	144	ps
		LX100T	CS(G)484	88	ps
			FG(G)484	111	ps
			FG(G)676	147	ps
			FG(G)900	134	ps
		LX150	CS(G)484	84	ps
			FG(G)484	103	ps
			FG(G)676	115	ps
			FG(G)900	121	ps
		LX150T	CS(G)484	83	ps
			FG(G)484	88	ps
			FG(G)676	141	ps
			FG(G)900	120	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from Pad to Ball.
- Some of the devices are available in both Pb and Pb-free (additional G) packages as standard ordering options. See [DS160: Spartan-6 Family Overview](#) for more information.

Table 80: Sample Window

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{SAMP}	Sampling Error at Receiver Pins ⁽²⁾	All	510	510	530	740	ps
T _{SAMP_BUFIO2}	Sampling Error at Receiver Pins using BUFIO2 ⁽³⁾	All	430	430	450	590	ps

Notes:

- LXT devices are not available with a -1L speed grade.
- This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 DCM jitter
 - DCM accuracy (phase offset)
 - DCM phase shift resolution
These measurements do not include package or clock tree skew.
- This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO2 clock network and IODELAY2 to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
08/26/09	1.1	Added V_{FS} to Table 1 and Table 2 . Added R_{FUSE} to Table 2 . Added XC6SLX75 and XC6SLX75T to V_{BATT} and I_{BATT} in Table 1 , Table 2 , and Table 4 . Corrected the quiescent supply current for the XC6SLX4 in Table 5 . Updated Table 11 . Removed DV_{PPIN} from Figure 2 . Removed $F_{PCIECORE}$ from Table 24 and added values to $F_{PCIEUSER}$. Added more networking applications to Table 25 . Updated values for $T_{SUSPENDLOW_AWAKE}$, $T_{SUSPEND_ENABLE}$, and T_{SCP_AWAKE} in Table 46 . Numerous changes to Table 47 , page 54 including the addition of new values to various specifications, revising the $T_{SMCKCSO}$ description, and changing the units of T_{POR} . Also, removed <i>Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK</i> section from Table 47 and updated all the notes. In Table 52 , added to F_{INMAX} , revised F_{OUTMAX} , and removed PLL Maximum Output Frequency for BUFIO2. Revised values for DCM_DELAY_STEP in Table 54 . Updated CLKIN_FREQ_FX values in Table 55 .
01/04/10	1.2	Added -4 speed grade to entire document. Updated speed specification of -4, -3, -2 speed grades to version 1.03. Added -1L speed grade numbers per speed specification 1.00. Updated T_{SOL} in Table 1 . Added -1L rows for LVCMOS12, LVCMOS15, and LVCMOS18 in Table 9 . Revised much of the detail in GTP Transceiver Specifications in Table 12 through Table 23 . Added -2 data to Table 25 . Updated F_{MAX} in Table 44 . Updated descriptions for T_{DNACKL} and T_{DNACKH} in Table 45 and revised values for all parameters. Removed $T_{INITADDR}$ from Table 47 and added new data. Updated values in Table 48 through Table 62 . Added Table 51 (BUFPLL) and Table 57 (DCM_CLKGEN). Removed $T_{LOCKMAX}$ note from Table 52 . Updated note 3 in Table 53 . In Table 79 : removed XC6SLX75CSG324 and XC6SLX75TCSG324; added XC6SLX75FG(G)484 and XC6SLX75FG(G)484.
02/22/10	1.3	Production release of XC6SLX16 -2 speed grade devices. The changes to Table 26 and Table 27 includes updating this data sheet to the data in ISE v11.5 software with speed specification v1.06. Updated maximum of V_{IN} and V_{TS} and note 2 in Table 1 . In Table 2 , changed V_{IN} , added I_{IN} and note 5, revised notes 1, 6, and 7, and added note 8 to R_{FUSE} . In Table 4 , removed previous note 1 and added data to I_{RPU} , I_{RPD} , and I_{BATT} , changed C_{IN} , added R_{DT} and R_{IN_TERM} , and added note 2 and 3. Updated V_{CCO2} in Table 6 . Added Table 7 and Table 8 . Removed PCI66_3 from Table 9 . Updated PCI33_3 and I2C in Table 9 . Updated the description of Table 11 . Completely updated Table 25 . Updated Table 28 including adding values for PCI33_3. Updated V_{REF} value for HSTL_III_18 in Table 31 . Updates missing V_{REF} values in Table 32 . Added Simultaneously Switching Outputs , page 36 . Removed T_{GSRQ} and T_{RPW} from Table 35 and Table 36 . Also removed T_{DOQ} from Table 36 . Removed T_{ISDO_DO} and note 1 from Table 37 . Removed T_{OSCK_S} and combinatorial section from Table 38 . In Table 39 , removed T_{IODDO_T} and added new tap parameters and note 2. In Table 40 , Table 41 , and Table 42 , made typographical edits and removed notes. Removed clock CLK section in Table 41 . Removed clock CLK section and T_{REG_MUX} and T_{REG_M31} in Table 42 . Added block RAM F_{MAX} values to Table 43 . Updated values and added note 2 to Table 45 . Added values to Table 46 and removed note 1. Numerous changes to Table 47 . Completely updated Table 57 . Revised data in Table 62 . Removed note 3 from Table 71 . Added values to Table 79 . Added data to Table 80 and Table 81 .
03/10/10	1.4	Production release of XC6SLX45 -2 speed grade devices, which includes changes to Table 26 and Table 27 updating this data sheet to the data in ISE v11.5 software with speed specification v1.07. Fixed R_{IN_TERM} description in Table 4 . Added PCI66_3 to Table 7 and replaced note 1. Corrected note 1 and the V, Max for TMDS_33 in Table 8 . In Table 10 , added note 1 to LVPECL_33 and TMDS_33. Also updated specifications for TMDS_33. Updated the GTP Transceiver Specifications section including adding values to Table 16 , Table 17 , and Table 20 through Table 23 . Added PCI66_3 back into Table 9 , Table 28 , Table 31 , Table 32 , and Table 34 . Updated note 3 on Table 32 . In Table 34 , corrected some typographical errors and fixed SSO limits for bank1/3 in FG(G)484 package. Corrected T_{OSCK_OCE} in Table 38 . In Table 57 , updated CLKFX_FREEZE_VAR and CLKFX_FREEZE_TEMP_SLOPE and added typical values to $T_{CENTER_LOW_SPREAD}$ and $T_{CENTER_HIGH_SPREAD}$. Updated and added values to Table 63 through Table 78 , and Table 81 . In Table 79 , revised the XC6SLX16-CSG324 and the XC6SLX45-CSG484 and FG(G)484 values.

Date	Version	Description of Revisions
06/14/10	1.5	In Table 2, added note 5 and added temperature range to V_{FS} and R_{FUSE}. Removed speed grade delineation, revised I_{RPD} description, and updated note 2 in Table 4. Added note 2 to Table 7. Added $DIFF_MOBILE_DDR$ to Table 8 and Table 10. Added note 4 to Table 15. Changed minimum DV_{PPIN} in Table 16. Updated $F_{GTPDRCLK}$ in Table 19. Increased maximum T_{LLSKEW} in Table 22. Updated descriptions and added data to Table 23. Removed note 1 and added new data to the Networking Applications section in Table 25. Updated Table 26 and Table 27 to the data in ISE v12.1 software with speed specification v1.08. In Table 28, added $DIFF_MOBILE_DDR$ and updated -4 speed grade data. Updated the maximum I/O pairs per bank in Table 33. Updated note 2 on Table 39. Revised the F_{MAX} in Table 44. In Table 47, updated description for $T_{SMCKCSO}$, revised values for T_{POR} and added Min value, added $T_{BPIICCK}$ and $T_{SPIICCK}$. Also in Table 47, added device dependencies to F_{SMCKCK} and F_{RBCKCK}. Updated and added data to Table 63 through Table 78, and Table 81. In Table 79, added data on the XC6SLX45-FG(G)676 and revised the XC6SLX45T and XC6SLX150T values. The following changes to this specification are addressed in the product change notice XC6SLX45-FG(G)676, <i>MCB Performance and JTAG Revision Code for Spartan-6 LX16 and LX45 FPGAs</i>. In Table 2, revised the V_{CCINT} to add the memory controller block extended performance specifications. In Table 25, changed the standard specifications and added extended performance specifications for the memory controller block and note 2. Added note 4 and updated values in Table 34.
06/24/10	1.6	Production release of XC6SLX45T (-2 and -3 speed grades), XC6SLX16 and XC6SLX45 (-3 speed grade) devices which includes changes to Table 26 and Table 27 (ISE v12.1 software with speed specification v1.08). Added the -3N speed grade, which designates Spartan-6 devices that do not support MCB functionality. This includes changes to Table 2 (note 2), Table 25 (note 4), and Switching Characteristics (Table 26). Updated Simultaneously Switching Outputs discussion. Added -3 speed grade values for T_{TAP} and F_{MINCAL} values in Table 39. In Table 40, updated T_{RPW} (-2 and -3 speed grade) values and F_{TOG} (-3 speed grade) values. In Table 48, updated T_{GIO} (-2 and -3 speed grade) values. Updated -3 values in spread spectrum section of Table 57.
07/16/10	1.7	Production release of specific devices listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 4 advising designers of the patch which contains v1.11. Also updated the -1L speed specification to v1.04. Updated numerous -4 and -1L values. Added -4 T_{TAP} values and F_{MINCAL} to Table 39. Revised T_{CINCK}/T_{CKCIN} in Table 40. In Table 41, revised T_{SHCKO}. In Table 42, revised T_{REQ}. Added new -1L values to Table 47. Added and updated values in Table 79.
07/26/10	1.8	Production release of XC6SLX25, XC6SLX25T, XC6SLX100 and XC6SLX100T in the specific speed grades listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 7 to Table 2 and moved V_{FS} and R_{FUSE} to a new Table 3. Added I_{HS} and note 4 to Table 4. Added note 1 to Table 28. Added and updated SSO limits per V_{CCO}/GND pairs in Table 34. Added note 3 to Table 47. In Table 54, removed -1L specifications for $CLKOUT_PER_JITT_DV1/2$ and revised $CLKIN_CLKFB_PHASE$ and $CLKOUT_PHASE_DLL$ values. Updated note 3 in both Table 56 and Table 57.
08/23/10	1.9	Updated values for $F_{GTPRANGE1}$, $F_{GTPRANGE2}$, and $F_{GPLLMIN}$ in Table 18. Revised -3 and -4 values in Table 21. Removed the -1L speed grade readback support restriction and note 3 in Table 47.
11/05/10	1.10	Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.3 software with speed specification v1.12 for the -2 speed grade available in the 12.3 <i>Speed Files Patch</i>. Added note 3 advising designers of the patch which contains v1.12. In Table 2, added note 4. In Table 4, added note 2. In Table 10, added notes 2 and 3. In Table 44, added note 2. In Table 47, updated symbol for $T_{SMWCKCK}/T_{SMCKCKW}$, changed -1L values for $T_{USERCCLKH}$ and $T_{USERCCLKL}$, and added and revised the modes for F_{MCKCK} and F_{SMCKCK}. In Table 53, redefined and expanded description for $CLKIN_FREQ_DLL$ and rewrote note 3. Updated title of Table 58. Also in Table 78, revised T_{DCD_CLK} for XC6SLX150 and XC6SLX150T. Changed description of T_{PSFD}/T_{PHFD} in Table 71. For the -1L speed grade, updated data sheet to ISE 12.3 software with speed specification v1.05 which revised the values in the following tables: Table 25, Table 28, Table 35, Table 36, Table 37, Table 40 through Table 43, Table 48 through Table 56, Table 62 through Table 78, Table 80, and Table 81. Updated Notice of Disclaimer.