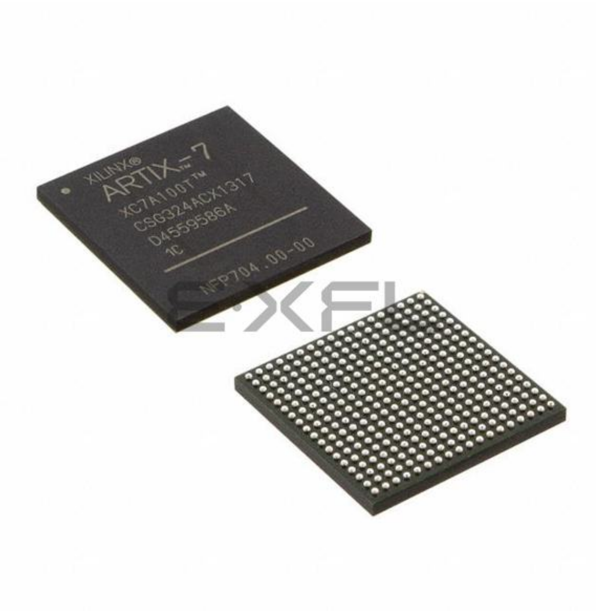
AMD Xilinx - XC6SLX9-3CSG324I Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	715
Number of Logic Elements/Cells	9152
Total RAM Bits	589824
Number of I/O	200
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	324-LFBGA, CSPBGA
Supplier Device Package	324-CSPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx9-3csg324i

Table 4: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.8	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin for commercial (C) and industrial (I) devices	–10	–	10	µA
	V_{REF} leakage current per pin for expanded (Q) devices	–15	–	15	µA
I_L	Input or output leakage current per pin (sample-tested) for commercial (C) and industrial (I) devices	–10	–	10	µA
	Input or output leakage current per pin (sample-tested) for expanded (Q) devices	–15	–	15	µA
I_{HS}	Leakage current on pins during hot socketing with FPGA unpowered All pins except PROGRAM_B, DONE, and JTAG pins when HSWAPEN = 1	–20	–	20	µA
	PROGRAM_B, DONE, and JTAG pins, or other pins when HSWAPEN = 0	$I_{HS} + I_{RPU}$			µA
C_{IN}(1)	Die input capacitance at the pad	–	–	10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V or V_{CCAUX} = 3.3V	200	–	500	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V or V_{CCAUX} = 2.5V	120	–	350	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	60	–	200	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	40	–	150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	12	–	100	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = V_{CCO}, V_{CCAUX} = 3.3V	200	–	550	µA
	Pad pull-down (when selected) @ V_{IN} = V_{CCO}, V_{CCAUX} = 2.5V	140	–	400	µA
I_{BATT}(2)	Battery supply current	–	–	150	nA
R_{DT}(3)	Resistance of optional input differential termination circuit, V_{CCAUX} = 3.3V	–	100	–	Ω
R_{IN_TERM}(5)	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for commercial (C) and industrial (I) devices	23	25	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for expanded (Q) devices	20	25	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for commercial (C) and industrial (I) devices	39	50	72	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for expanded (Q) devices	32	50	74	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for commercial (C) and industrial (I) devices	56	75	109	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for expanded (Q) devices	47	75	115	Ω
R_{OUT_TERM}	Thevenin equivalent resistance of programmable output termination (UNTUNED_25)	11	25	52	Ω
	Thevenin equivalent resistance of programmable output termination (UNTUNED_50)	21	50	96	Ω
	Thevenin equivalent resistance of programmable output termination (UNTUNED_75)	29	75	145	Ω

Notes:

1. The C_{IN} measurement represents the die capacitance at the pad, not including the package.
2. Maximum value specified for worst case process at 25°C. LX75, LX75T, LX100, LX100T, LX150, and LX150T only.
3. Refer to IBIS models for R_{DT} variation and for values at V_{CCAUX} = 2.5V. IBIS values for R_{DT} are valid for all temperature ranges.
4. V_{CCO2} is not required for data retention. The minimum V_{CCO2} for power-on reset and configuration is 1.65V.
5. Termination resistance to a $V_{CCO}/2$ level.

Table 10: **Differential I/O Standard DC Input and Output Levels**

I/O Standard	V_{ID}		V_{ICM}		V_{OD}		V_{OCM}		V_{OH}	V_{OL}
	mV, Min	mV, Max	V, Min	V, Max	mV, Min	mV, Max	V, Min	V, Max	V, Min	V, Max
LVDS_33(2)(3)	100	600	0.3	2.35	247	454	1.125	1.375	–	–
LVDS_25(2)(3)	100	600	0.3	2.35	247	454	1.125	1.375	–	–
BLVDS_25(2)(3)	100	–	0.3	2.35	240	460	Typical 50% V_{CCO}		–	–
MINI_LVDS_33	200	600	0.3	1.95	300	600	1.0	1.4	–	–
MINI_LVDS_25	200	600	0.3	1.95	300	600	1.0	1.4	–	–
LVPECL_33(2)(3)	100	1000	0.3	2.8(1)	Inputs only					
LVPECL_25(2)(3)	100	1000	0.3	1.95	Inputs only					
RSDS_33(2)(3)	100	–	0.3	1.5	100	400	1.0	1.4	–	–
RSDS_25(2)(3)	100	–	0.3	1.5	100	400	1.0	1.4	–	–
TMDS_33	150	1200	2.7	3.23(1)	400	800	V_{CCO} – 0.405	V_{CCO} – 0.190	–	–
PPDS_33(2)(3)	100	400	0.2	2.3	100	400	0.5	1.4	–	–
PPDS_25(2)(3)	100	400	0.2	2.3	100	400	0.5	1.4	–	–
DISPLAY_PORT	190	1260	0.3	2.35	–	–	Typical 50% V_{CCO}		–	–
DIFF_MOBILE_DDR	100	–	0.78	1.02	–	–	–	–	90% V_{CCO}	10% V_{CCO}
DIFF_HSTL_I	100	–	0.68	0.9	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II	100	–	0.68	0.9	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III	100	–	0.68	0.9	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_I_18	100	–	0.8	1.1	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II_18	100	–	0.8	1.1	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	100	–	0.8	1.1	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL3_I	100	–	1.0	1.9	–	–	–	–	V_{TT} + 0.6	V_{TT} – 0.6
DIFF_SSTL3_II	100	–	1.0	1.9	–	–	–	–	V_{TT} + 0.8	V_{TT} – 0.8
DIFF_SSTL2_I	100	–	1.0	1.5	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61
DIFF_SSTL2_II	100	–	1.0	1.5	–	–	–	–	V_{TT} + 0.81	V_{TT} – 0.81
DIFF_SSTL18_I	100	–	0.7	1.1	–	–	–	–	V_{TT} + 0.47	V_{TT} – 0.47
DIFF_SSTL18_II	100	–	0.7	1.1	–	–	–	–	V_{TT} + 0.6	V_{TT} – 0.6
DIFF_SSTL15_II	100	–	0.55	0.95	–	–	–	–	V_{TT} + 0.4	V_{TT} – 0.4

Notes:

1. LVPECL_33 and TMDS_33 maximum V_{ICM} is the lower of V (maximum) or V_{CCAUX} – (V_{ID}/2)
2. When V_{CCAUX} = 3.3V, the DCD can be higher than 5% for V_{ICM} < 0.7V when using these I/O standards: LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, LVPECL_33, RSDS_25, RSDS_33, PPDS_25, and PPDS_33.
3. The -1L devices require V_{CCAUX} = 2.5V when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.

GTP Transceiver DC Input and Output Levels

Table 16 summarizes the DC output specifications of the GTP transceivers in Spartan-6 FPGAs. Figure 1 shows the single-ended output voltage swing. Figure 2 shows the peak-to-peak differential output voltage.

Consult UG386: *Spartan-6 FPGA GTP Transceivers User Guide* for further details.

Table 16: **GTP Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled	140	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTTRX = 1.2V	–400	–	MGTAVTTRX	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTTRX = 1.2V	–	3/4 MGTAVTTRX	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage[1]	Transmitter output swing is set to maximum setting	–	–	1000	mV
V_{SEOUT}	Single-ended output voltage swing[1]		–	–	500	mV
$V_{CMOUTDC}$	Common mode output voltage	Equation based	MGTAVTTTX – $V_{SEOUT}/2$			mV
R_{IN}	Differential input resistance		80	100	130	Ω
R_{OUT}	Differential output resistance		80	100	130	Ω
T_{OSKEW}	Transmitter output skew		–	–	15	ps
C_{EXT}	Recommended external AC coupling capacitor[2]		75	100	200	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG386: *Spartan-6 FPGA GTP Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

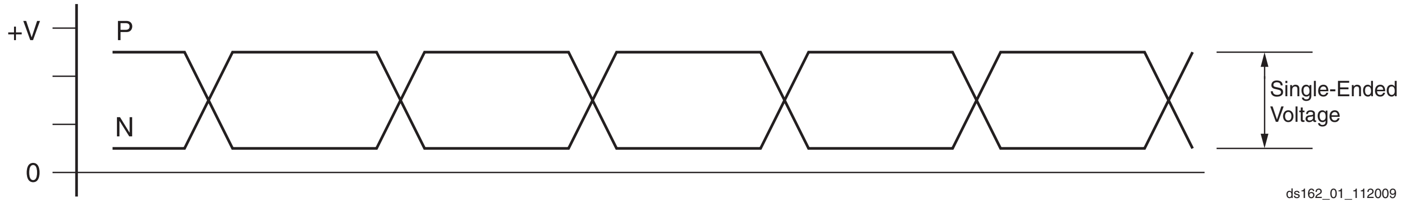

Figure 1: **Single-Ended Peak-to-Peak Voltage**

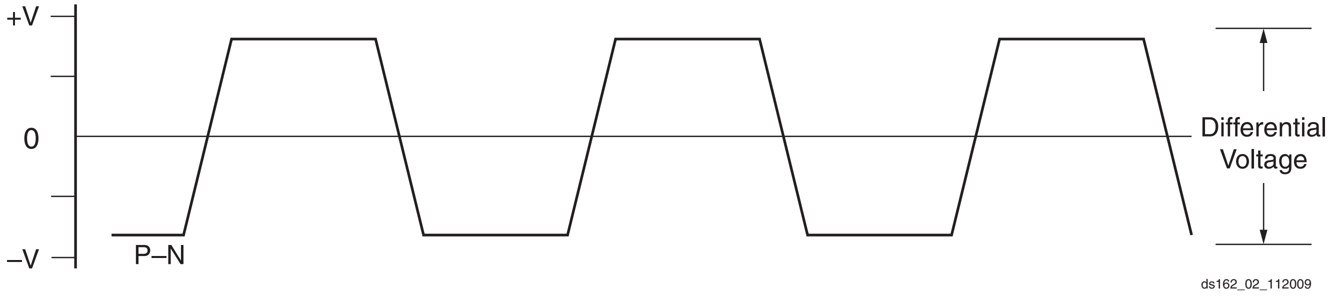

Figure 2: **Differential Peak-to-Peak Voltage**

Table 17 summarizes the DC specifications of the clock input of the GTP transceiver. Consult UG386: *Spartan-6 FPGA GTP Transceivers User Guide* for further details.

Table 17: **GTP Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	200	800	2000	mV
R_{IN}	Differential input resistance	80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult UG386: *Spartan-6 FPGA GTP Transceivers User Guide* for further information.

Table 18: **GTP Transceiver Performance**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
F_{GTPMAX}	Maximum GTP transceiver data rate	3.2	3.2	2.7	N/A	Gb/s
$F_{GTPRANGE1}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 1	1.88 to 3.2	1.88 to 3.2	1.88 to 2.7	N/A	Gb/s
$F_{GTPRANGE2}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 2	0.94 to 1.62	0.94 to 1.62	0.94 to 1.62	N/A	Gb/s
$F_{GTPRANGE3}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 4	0.6 to 0.81	0.6 to 0.81	0.6 to 0.81	N/A	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	1.62	1.62	1.62	N/A	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	0.94	0.94	0.94	N/A	GHz

Table 19: **GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
$F_{GTPDRPCLK}$	GTP transceiver DCLK (DRP clock) maximum frequency	125	125	100	N/A	MHz

Table 20: **GTP Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All LXT Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	160	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	µs

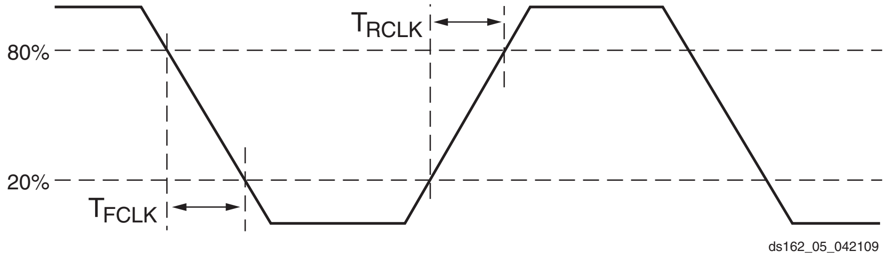

Figure 3: **Reference Clock Timing Parameters**

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics, page 19.

Table 25: **Interface Performances**

Description	I/O Resource	Clock Buffer	Data Width	Speed Grade				Units
				-3	-3N	-2	-1L	
Networking Applications(1)								
SDR LVDS transmitter or receiver	IOB SDR register	BUFG	–	400	400	375	250	Mb/s
DDR LVDS transmitter or receiver	ODDR2/IDDR2 register	2 BUFGs	–	800	800	750	500	Mb/s
SDR LVDS transmitter	OSERDES2	BUFPLL	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
DDR LVDS transmitter	OSERDES2	2 BUFIO2s	2	500	500	500	250	Mb/s
			3	750	750	750	375	Mb/s
			4-8	1080	1050	950	500	Mb/s
SDR LVDS receiver	ISERDES2 in RETIMED mode	BUFPLL	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
DDR LVDS receiver	ISERDES2 in RETIMED mode	2 BUFIO2s	2	500	500	500	—	Mb/s
			3	750	750	750	—	Mb/s
			4-8	1080	1050	950	—	Mb/s
Memory Interfaces (Implemented using the Spartan-6 FPGA Memory Controller Block)(2)								
Standard Performance (Standard V_{CCINT})								
DDR				400	Note 4	400	350	Mb/s
DDR2				667	Note 4	625	400	Mb/s
DDR3				800	Note 4	667	—	Mb/s
LPDDR (Mobile_DDR)				400	Note 4	400	350	Mb/s
Extended Performance (Requires Extended Performance V_{CCINT})(3)								
DDR2				800	Note 4	667	—	Mb/s

Notes:

1. Refer to XAPP1064, *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)* and UG381, *Spartan-6 FPGA SelectIO Resources User Guide.*
2. Refer to UG388, *Spartan-6 FPGA Memory Controller User Guide*.
3. Extended Memory Controller block performance for DDR2 can be achieved using the extended performance V_{CCINT} range from Table 2.
4. The LX4 device, all devices in the TQG144 and CPG196 packages, and the -3N speed grade do not support a Memory Controller Block.

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices** ***(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	
LVCMOS33, Fast, 8 mA	1.34	1.46	1.59	1.82	2.07	2.21	2.41	3.03	2.07	2.21	2.41	3.03	ns
LVCMOS33, Fast, 12 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns
LVCMOS33, Fast, 16 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns
LVCMOS33, Fast, 24 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns
LVCMOS25, QUIETIO, 2 mA	0.82	0.94	1.07	1.31	4.81	4.95	5.15	5.79	4.81	4.95	5.15	5.79	ns
LVCMOS25, QUIETIO, 4 mA	0.82	0.94	1.07	1.31	3.70	3.84	4.04	4.66	3.70	3.84	4.04	4.66	ns
LVCMOS25, QUIETIO, 6 mA	0.82	0.94	1.07	1.31	3.46	3.60	3.80	4.38	3.46	3.60	3.80	4.38	ns
LVCMOS25, QUIETIO, 8 mA	0.82	0.94	1.07	1.31	3.20	3.34	3.54	4.12	3.20	3.34	3.54	4.12	ns
LVCMOS25, QUIETIO, 12 mA	0.82	0.94	1.07	1.31	2.83	2.97	3.17	3.75	2.83	2.97	3.17	3.75	ns
LVCMOS25, QUIETIO, 16 mA	0.82	0.94	1.07	1.31	2.64	2.78	2.98	3.64	2.64	2.78	2.98	3.64	ns
LVCMOS25, QUIETIO, 24 mA	0.82	0.94	1.07	1.31	2.45	2.59	2.79	3.42	2.45	2.59	2.79	3.42	ns
LVCMOS25, Slow, 2 mA	0.82	0.94	1.07	1.31	3.78	3.92	4.12	4.76	3.78	3.92	4.12	4.76	ns
LVCMOS25, Slow, 4 mA	0.82	0.94	1.07	1.31	2.79	2.93	3.13	3.73	2.79	2.93	3.13	3.73	ns
LVCMOS25, Slow, 6 mA	0.82	0.94	1.07	1.31	2.73	2.87	3.07	3.66	2.73	2.87	3.07	3.66	ns
LVCMOS25, Slow, 8 mA	0.82	0.94	1.07	1.31	2.48	2.62	2.82	3.42	2.48	2.62	2.82	3.42	ns
LVCMOS25, Slow, 12 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.95	2.01	2.15	2.35	2.95	ns
LVCMOS25, Slow, 16 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.95	2.01	2.15	2.35	2.95	ns
LVCMOS25, Slow, 24 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.94	2.01	2.15	2.35	2.94	ns
LVCMOS25, Fast, 2 mA	0.82	0.94	1.07	1.31	3.35	3.49	3.69	4.31	3.35	3.49	3.69	4.31	ns
LVCMOS25, Fast, 4 mA	0.82	0.94	1.07	1.31	2.25	2.39	2.59	3.22	2.25	2.39	2.59	3.22	ns
LVCMOS25, Fast, 6 mA	0.82	0.94	1.07	1.31	2.09	2.23	2.43	3.05	2.09	2.23	2.43	3.05	ns
LVCMOS25, Fast, 8 mA	0.82	0.94	1.07	1.31	2.02	2.16	2.36	2.98	2.02	2.16	2.36	2.98	ns
LVCMOS25, Fast, 12 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns
LVCMOS25, Fast, 16 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns
LVCMOS25, Fast, 24 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns
LVCMOS18, QUIETIO, 2 mA	1.18	1.30	1.43	2.04	5.92	6.06	6.26	6.80	5.92	6.06	6.26	6.80	ns
LVCMOS18, QUIETIO, 4 mA	1.18	1.30	1.43	2.04	4.74	4.88	5.08	5.63	4.74	4.88	5.08	5.63	ns
LVCMOS18, QUIETIO, 6 mA	1.18	1.30	1.43	2.04	4.05	4.19	4.39	4.96	4.05	4.19	4.39	4.96	ns
LVCMOS18, QUIETIO, 8 mA	1.18	1.30	1.43	2.04	3.71	3.85	4.05	4.63	3.71	3.85	4.05	4.63	ns
LVCMOS18, QUIETIO, 12 mA	1.18	1.30	1.43	2.04	3.35	3.49	3.69	4.27	3.35	3.49	3.69	4.27	ns
LVCMOS18, QUIETIO, 16 mA	1.18	1.30	1.43	2.04	3.20	3.34	3.54	4.14	3.20	3.34	3.54	4.14	ns
LVCMOS18, QUIETIO, 24 mA	1.18	1.30	1.43	2.04	2.96	3.10	3.30	3.98	2.96	3.10	3.30	3.98	ns
LVCMOS18, Slow, 2 mA	1.18	1.30	1.43	2.04	4.62	4.76	4.96	5.54	4.62	4.76	4.96	5.54	ns
LVCMOS18, Slow, 4 mA	1.18	1.30	1.43	2.04	3.69	3.83	4.03	4.60	3.69	3.83	4.03	4.60	ns
LVCMOS18, Slow, 6 mA	1.18	1.30	1.43	2.04	3.00	3.14	3.34	3.94	3.00	3.14	3.34	3.94	ns
LVCMOS18, Slow, 8 mA	1.18	1.30	1.43	2.04	2.19	2.33	2.53	3.17	2.19	2.33	2.53	3.17	ns
LVCMOS18, Slow, 12 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18, Slow, 16 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns

Table 29: **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices**[(1)] ***(Cont'd)***

I/O Standard	T_{IOPI}		T_{IOOP}		T_{IOTP}		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVCMOS15, QUIETIO, 2 mA	1.05	1.23	5.63	5.83	5.63	5.83	ns
LVCMOS15, QUIETIO, 4 mA	1.05	1.23	4.75	4.95	4.75	4.95	ns
LVCMOS15, QUIETIO, 6 mA	1.05	1.23	4.21	4.41	4.21	4.41	ns
LVCMOS15, QUIETIO, 8 mA	1.05	1.23	4.05	4.25	4.05	4.25	ns
LVCMOS15, QUIETIO, 12 mA	1.05	1.23	3.74	3.94	3.74	3.94	ns
LVCMOS15, QUIETIO, 16 mA	1.05	1.23	3.52	3.72	3.52	3.72	ns
LVCMOS15, Slow, 2 mA	1.05	1.23	4.32	4.52	4.32	4.52	ns
LVCMOS15, Slow, 4 mA	1.05	1.23	3.58	3.78	3.58	3.78	ns
LVCMOS15, Slow, 6 mA	1.05	1.23	2.45	2.65	2.45	2.65	ns
LVCMOS15, Slow, 8 mA	1.05	1.23	2.46	2.66	2.46	2.66	ns
LVCMOS15, Slow, 12 mA	1.05	1.23	2.17	2.37	2.17	2.37	ns
LVCMOS15, Slow, 16 mA	1.05	1.23	2.15	2.35	2.15	2.35	ns
LVCMOS15, Fast, 2 mA	1.05	1.23	3.43	3.63	3.43	3.63	ns
LVCMOS15, Fast, 4 mA	1.05	1.23	2.42	2.62	2.42	2.62	ns
LVCMOS15, Fast, 6 mA	1.05	1.23	1.92	2.12	1.92	2.12	ns
LVCMOS15, Fast, 8 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVCMOS15, Fast, 12 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVCMOS15, Fast, 16 mA	1.05	1.23	1.87	2.07	1.87	2.07	ns
LVCMOS15_JEDEC, QUIETIO, 2 mA	1.10	1.28	5.64	5.84	5.64	5.84	ns
LVCMOS15_JEDEC, QUIETIO, 4 mA	1.10	1.28	4.75	4.95	4.75	4.95	ns
LVCMOS15_JEDEC, QUIETIO, 6 mA	1.10	1.28	4.21	4.41	4.21	4.41	ns
LVCMOS15_JEDEC, QUIETIO, 8 mA	1.10	1.28	4.06	4.26	4.06	4.26	ns
LVCMOS15_JEDEC, QUIETIO, 12 mA	1.10	1.28	3.75	3.95	3.75	3.95	ns
LVCMOS15_JEDEC, QUIETIO, 16 mA	1.10	1.28	3.53	3.73	3.53	3.73	ns
LVCMOS15_JEDEC, Slow, 2 mA	1.10	1.28	4.32	4.52	4.32	4.52	ns
LVCMOS15_JEDEC, Slow, 4 mA	1.10	1.28	3.56	3.76	3.56	3.76	ns
LVCMOS15_JEDEC, Slow, 6 mA	1.10	1.28	2.44	2.64	2.44	2.64	ns
LVCMOS15_JEDEC, Slow, 8 mA	1.10	1.28	2.47	2.67	2.47	2.67	ns
LVCMOS15_JEDEC, Slow, 12 mA	1.10	1.28	2.15	2.35	2.15	2.35	ns
LVCMOS15_JEDEC, Slow, 16 mA	1.10	1.28	2.15	2.35	2.15	2.35	ns
LVCMOS15_JEDEC, Fast, 2 mA	1.10	1.28	3.43	3.63	3.43	3.63	ns
LVCMOS15_JEDEC, Fast, 4 mA	1.10	1.28	2.42	2.62	2.42	2.62	ns
LVCMOS15_JEDEC, Fast, 6 mA	1.10	1.28	1.92	2.12	1.92	2.12	ns
LVCMOS15_JEDEC, Fast, 8 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVCMOS15_JEDEC, Fast, 12 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVCMOS15_JEDEC, Fast, 16 mA	1.10	1.28	1.87	2.07	1.87	2.07	ns
LVCMOS12, QUIETIO, 2 mA	0.98	1.16	6.54	6.74	6.54	6.74	ns
LVCMOS12, QUIETIO, 4 mA	0.98	1.16	5.12	5.32	5.12	5.32	ns

Table 34: **SSO Limit per V_{CCO}/GND Pair**

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
1.2V	LVCMOS12, LVCMOS12_JEDEC	2	Fast	30 (1)	35	30	35
			Slow	51	55	51	52
			QuietIO	71	58	71	70
		4	Fast	17	17	17	19
			Slow	23	25	23	22
			QuietIO	35	32	35	32
		6	Fast	13	15	13	14
			Slow	19	20	19	17
			QuietIO	26	24	26	24
		8	Fast	N/A	12	N/A	12
			Slow	N/A	15	N/A	13
			QuietIO	N/A	20	N/A	19
		12	Fast	N/A	5	N/A	4
			Slow	N/A	8	N/A	5
			QuietIO	N/A	11	N/A	10

Table 34: **SSO Limit per V_{CCO}/GND Pair *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
2.5V	LVCMOS25	2	Fast	38	43	38	43
			Slow	46	52	46	48
			QuietIO	57	64	57	59
		4	Fast	21	24	21	23
			Slow	26	31	26	27
			QuietIO	33	32	33	30
		6	Fast	15	17	15	16
			Slow	19	22	19	19
			QuietIO	25	23	25	19
		8	Fast	12	15	12	14
			Slow	15	18	15	16
			QuietIO	21	19	21	16
		12	Fast	1	3	1	1
			Slow	2	7	2	4
			QuietIO	3	8	3	8
		16	Fast	1	3	1	1
			Slow	3	7	3	3
			QuietIO	4	9	4	8
		24	Fast	N/A	3	N/A	1
			Slow	N/A	5	N/A	2
			QuietIO	N/A	8	N/A	6
	SSTL_2_I (3)			10	11	10	11
	SSTL_2_II (3)			N/A	7	N/A	7
	DIFF_SSTL_2_I (3)			30	33	30	33
	DIFF_SSTL_2_II (3)			N/A	21	N/A	24

Table 34: **SSO Limit per V_{CCO}/GND Pair *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
3.3V	LVTTL	2	Fast	53	65	53	62
			Slow	70	80	70	73
			QuietIO	79	89	79	91
		4	Fast	23	30	23	27
			Slow	34	41	34	37
			QuietIO	44	49	44	46
		6	Fast	16	21	16	20
			Slow	21	28	21	25
			QuietIO	34	39	34	34
		8	Fast	12	16	12	15
			Slow	16	22	16	19
			QuietIO	27	28	27	24
		12	Fast	1	3	1	1
			Slow	2	5	2	4
			QuietIO	2	10	2	8
		16	Fast	1	3	1	1
			Slow	1	7	1	2
			QuietIO	3	11	3	8
		24	Fast	1	2	1	1
			Slow	2	5	2	2
			QuietIO	8	9	8	8
	PCI33_3			18	19	18	19
	PCI66_3			18	19	18	19
	SSTL_3_I			5	8	5	8
	SSTL_3_II			3	5	3	3
	DIFF_SSTL_3_I			15	24	15	24
	DIFF_SSTL_3_II			9	15	9	9
	SDIO			17	18	17	15

Table 34: **SSO Limit per V_{CCO}/GND Pair *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
Various	LVDS_33			16	N/A	16	N/A
	LVDS_25			20	N/A	20	N/A
	BLVDS_25			20	48	20	20
	MINI_LVDS_33			13	N/A	13	N/A
	MINI_LVDS_25			18	N/A	18	N/A
	RSDS_33			12	N/A	12	N/A
	RSDS_25			15	N/A	15	N/A
	TMDS_33			83	N/A	83	N/A
	PPDS_33			12	N/A	12	N/A
	PPDS_25			16	N/A	16	N/A
	DISPLAY_PORT			42	40	42	30
	I2C			47	55	47	42
	SMBUS			44	52	44	40

Notes:

1. SSO limits greater than the number of I/O per V_{CCO}/GND pair (Table 33) indicate No Limit for the given I/O standard. They are provided in this table to calculate limits when using multiple I/O standards in a bank.
2. Not available (N/A) indicates that the I/O standard is not available in the given bank.
3. When used with the MCB, these signals are exempt from SSO analysis due to the known activity of the MCB switching patterns. SSO performance is validated for all MCB instances. MCB outputs can, in some cases, exceed the SSO limits.

Input/Output Delay Switching Characteristics

Table 39: **IODELAY2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L(3)	
T_{IODCCK_CAL} / T_{IODCKC_CAL}	CAL pin Setup/Hold with respect to CK	0.28/ –0.13	0.33/ –0.13	0.48/ –0.13	N/A	ns
T_{IODCCK_CE} / T_{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.17/ –0.03	0.17/ –0.03	0.25/ –0.02	N/A	ns
T_{IODCCK_INC}/ T_{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.10/ 0.02	0.12/ 0.03	0.18/ 0.06	N/A	ns
T_{IODCCK_RST}/ T_{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.12/ –0.02	0.15/ –0.02	0.22/ –0.01	N/A	ns
T_{TAP1}(2)	Maximum tap 1 delay	8	14	16	N/A	ps
T_{TAP2}	Maximum tap 2 delay	40	66	77	N/A	ps
T_{TAP3}	Maximum tap 3 delay	95	120	140	N/A	ps
T_{TAP4}	Maximum tap 4 delay	108	141	166	N/A	ps
T_{TAP5}	Maximum tap 5 delay	171	194	231	N/A	ps
T_{TAP6}	Maximum tap 6 delay	207	249	292	N/A	ps
T_{TAP7}	Maximum tap 7 delay	212	276	343	N/A	ps
T_{TAP8}	Maximum tap 8 delay	322	341	424	N/A	ps
F_{MINCAL}	Minimum allowed bit rate for calibration in variable mode: VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX, and DIFF_PHASE_DETECTOR.	188	188	188	N/A	Mb/s
$T_{IODDO\_IDATAIN}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	–
$T_{IODDO\_ODATAIN}$	Propagation delay through IODELAY2	Note 1	Note 1	Note 1	Note 3	–

Notes:

1. Delay depends on IODELAY2 tap setting. See TRACE report for actual values.
2. Maximum delay = integer (number of taps/8) × T_{TAP8} + T_{TAPn} (where n equals the remainder). For minimum delay consult the TRACE setup and hold report. Minimum delay is typically greater than 30% of the maximum delay. Tap delays can vary by device and overall conditions. See TRACE report for actual values.
3. Spartan-6 -1L devices only support tap 0. See TRACE report for actual values.

Block RAM Switching Characteristics

Table 43: **Block RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Block RAM Clock to Out Delays						
T_{RCKO_DO}	Clock CLK to DOUT output (without output register)(1)	1.85	2.10	2.10	3.50	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register)(2)	1.60	1.75	1.75	2.30	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs for XC devices(3)	0.35/ 0.10	0.40/ 0.12	0.40/ 0.12	0.50/ 0.15	ns, Min
	ADDR inputs for XA and XQ devices(3)	0.35/ 0.17	N/A	0.40/ 0.17	0.50/ 0.15	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs(4)	0.30/ 0.10	0.30/ 0.10	0.30/ 0.10	0.40/ 0.15	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.22/ 0.05	0.25/ 0.06	0.25/ 0.06	0.44/ 0.10	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.20/ 0.10	0.20/ 0.10	0.20/ 0.10	0.28/ 0.15	ns, Min
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input	0.25/ 0.10	0.33/ 0.10	0.33/ 0.10	0.28/ 0.15	ns, Min
Maximum Frequency						
F_{MAX}	Block RAM in all modes	320	280	280	150	MHz

Notes:

1. T_{RCKO_DO} includes T_{RCKO_DOA} and T_{RCKO_DOPA} as well as the B port equivalent timing parameters.
2. $T_{RCKO\_DO\_REG}$ includes $T_{RCKO\_DOA\_REG}$ and $T_{RCKO\_DOPA\_REG}$ as well as the B port equivalent timing parameters.
3. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
4. T_{RDCK_DI} includes both A and B inputs as well as the parity inputs of A and B.

Clock Buffers and Networks

Table 48: **Global Clock Switching Characteristics (BUFGMUX)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T_{GSI}	S pin Setup to I0/I1 inputs	LX devices	0.25	0.31	0.48	0.48	ns
		LXT devices	0.25	0.31	0.48	N/A	ns
T_{GIO}	BUFGMUX delay from I0/I1 to O	LX devices	0.21	0.21	0.21	0.21	ns
		LXT devices	0.21	0.21	0.21	N/A	ns
Maximum Frequency							
F_{MAX}	Global clock tree (BUFGMUX)	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 49: **Input/Output Clock Switching Characteristics (BUFIO2)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T_{BUFCKO_O}	Clock to out delay from I to O	LX devices	0.67	0.82	1.09	1.50	ns
		LXT devices	0.67	0.82	1.09	N/A	ns
Maximum Frequency							
F_{MAX}	I/O clock tree (BUFIO2)	LX devices	540	525	500	300	MHz
		LXT devices	540	525	500	N/A	MHz

Table 50: **Input/Output Clock Switching Characteristics (BUFIO2FB)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
Maximum Frequency							
F_{MAX}	I/O clock tree (BUFIO2FB)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

Table 51: **Input/Output Clock Switching Characteristics (BUFPLL)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
Maximum Frequency							
F_{MAX}	BUFPLL clock tree (BUFPLL)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

PLL Switching Characteristics

Table 52: **PLL Specification**

Symbol	Description	Device[(1)]	Speed Grade				Units
			-3	-3N	-2	-1L	
F_{INMAX}	Maximum Input Clock Frequency from I/O Clock	LX devices	540	525	450	300	MHz
		LXT devices	540	525	450	N/A	MHz
	Maximum Input Clock Frequency from Global Clock	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 52: **PLL Specification *(Cont'd)***

Symbol	Description	Device[1]	Speed Grade				Units
			-3	-3N	-2	-1L	
F_{INMIN}	Minimum Input Clock Frequency	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter: 19–200 MHz	All	1 ns Maximum				
	Maximum Input Clock Period Jitter: > 200 MHz	All	<20% of clock input period Maximum				
F_{INDUTY}	Allowable Input Duty Cycle: 19—199 MHz	All	25/75				%
	Allowable Input Duty Cycle: 200—299 MHz	All	35/65				%
	Allowable Input Duty Cycle: > 300 MHz	All	45/55				%
F_{VCOMIN}	Minimum PLL VCO Frequency	LX devices	400	400	400	400	MHz
		LXT devices	400	400	400	N/A	MHz
F_{VCOMAX}	Maximum PLL VCO Frequency	LX devices	1080	1050	1000	1000	MHz
		LXT devices	1080	1050	1000	N/A	MHz
$F_{BANDWIDTH}$	Low PLL Bandwidth at Typical[3]	All	1	1	1	1	MHz
	High PLL Bandwidth at Typical[3]	All	4	4	4	4	MHz
$T_{STAPHAOFFSET}$	Static Phase Offset of the PLL Outputs	All	0.12	0.12	0.12	0.15	ns
$T_{OUTJITTER}$	PLL Output Jitter[3]	All	Note 2				
$T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision[4]	All	0.15	0.15	0.20	0.25	ns
$T_{LOCKMAX}$	PLL Maximum Lock Time	All	100	100	100	100	μs
F_{OUTMAX}	PLL Maximum Output Frequency for BUFGMUX	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz
	PLL Maximum Output Frequency for BUFPLL	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz
F_{OUTMIN}	PLL Minimum Output Frequency[5]	All	3.125	3.125	3.125	3.125	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation: 19–200 MHz	All	1 ns Maximum				
	External Clock Feedback Variation: > 200 MHz	All	< 20% of clock input period Maximum				
$RST_{MINPULSE}$	Minimum Reset Pulse Width	All	5	5	5	5	ns
F_{PFDMAX}[5]	Maximum Frequency at the Phase Frequency Detector	LX devices	500	500	400	300	MHz
		LXT devices	500	500	400	N/A	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	LX devices	19	19	19	19	MHz
		LXT devices	19	19	19	N/A	MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	All	3 ns Max or one CLKIN cycle				

Notes:

1. LXT devices are not available with a -1L speed grade.
2. Values for this parameter are available in the Clocking Wizard.
3. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When using CLK_FEEDBACK = CLKOUT0 with BUFIO2 feedback, the feedback frequency will be higher than the phase frequency detector frequency. $F_{PFDMAX} = F_{CLKFB}$ / CLKFBOUT_MULT

Table 65: **Global Clock Input to Output Delay With DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in Source-Synchronous Mode.							
$T_{ICKOFDCM\_0}$	Global Clock and OUTFF *with* DCM	XC6SLX4	5.03	N/A	7.21	8.05	ns
		XC6SLX9	5.03	6.13	7.21	8.05	ns
		XC6SLX16	5.08	5.51	6.44	7.96	ns
		XC6SLX25	4.81	5.13	5.69	7.94	ns
		XC6SLX25T	4.81	5.13	5.69	N/A	ns
		XC6SLX45	5.26	5.69	6.63	7.92	ns
		XC6SLX45T	5.26	5.69	6.63	N/A	ns
		XC6SLX75	4.77	5.18	5.88	7.95	ns
		XC6SLX75T	4.77	5.18	5.88	N/A	ns
		XC6SLX100	4.72	5.11	5.76	8.59	ns
		XC6SLX100T	4.76	5.11	5.76	N/A	ns
		XC6SLX150	4.90	5.30	5.93	7.93	ns
		XC6SLX150T	4.90	5.30	5.93	N/A	ns
		XA6SLX4	5.35	N/A	7.21	N/A	ns
		XA6SLX9	5.35	N/A	7.21	N/A	ns
		XA6SLX16	5.42	N/A	6.44	N/A	ns
		XA6SLX25	5.13	N/A	5.69	N/A	ns
		XA6SLX25T	5.13	N/A	5.79	N/A	ns
		XA6SLX45	5.58	N/A	6.63	N/A	ns
		XA6SLX45T	5.58	N/A	6.63	N/A	ns
		XA6SLX75	5.09	N/A	5.87	N/A	ns
		XA6SLX75T	5.09	N/A	5.87	N/A	ns
		XA6SLX100	N/A	N/A	6.44	N/A	ns
		XQ6SLX75	N/A	N/A	5.87	7.95	ns
		XQ6SLX75T	5.09	N/A	5.87	N/A	ns
		XQ6SLX150	N/A	N/A	6.06	7.93	ns
		XQ6SLX150T	5.50	N/A	6.06	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 69: **Global Clock Input to Output Delay With DCM and PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode.							
$T_{ICKOFDCM0\_PLL}$	Global Clock and OUTFF with DCM and PLL	XC6SLX4	5.58	N/A	7.42	8.54	ns
		XC6SLX9	5.58	6.19	7.42	8.54	ns
		XC6SLX16	5.50	6.06	7.05	8.24	ns
		XC6SLX25	5.57	6.04	7.02	8.33	ns
		XC6SLX25T	5.57	6.04	7.02	N/A	ns
		XC6SLX45	5.53	5.97	6.96	8.32	ns
		XC6SLX45T	5.53	5.97	6.96	N/A	ns
		XC6SLX75	5.55	6.00	6.99	8.54	ns
		XC6SLX75T	5.55	6.00	6.99	N/A	ns
		XC6SLX100	5.58	6.03	7.02	9.11	ns
		XC6SLX100T	5.62	6.03	7.02	N/A	ns
		XC6SLX150	5.32	5.70	6.41	8.26	ns
		XC6SLX150T	5.32	5.70	6.41	N/A	ns
		XA6SLX4	5.87	N/A	7.28	N/A	ns
		XA6SLX9	5.87	N/A	7.28	N/A	ns
		XA6SLX16	6.02	N/A	6.87	N/A	ns
		XA6SLX25	5.88	N/A	6.90	N/A	ns
		XA6SLX25T	5.88	N/A	7.00	N/A	ns
		XA6SLX45	5.82	N/A	6.81	N/A	ns
		XA6SLX45T	5.82	N/A	6.81	N/A	ns
		XA6SLX75	5.81	N/A	6.80	N/A	ns
		XA6SLX75T	5.81	N/A	6.80	N/A	ns
		XA6SLX100	N/A	N/A	6.88	N/A	ns
		XQ6SLX75	N/A	N/A	6.80	8.54	ns
		XQ6SLX75T	5.81	N/A	6.80	N/A	ns
		XQ6SLX150	N/A	N/A	6.41	8.26	ns
		XQ6SLX150T	5.90	N/A	6.41	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 73: **Global Clock Setup and Hold With DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.[1]							
T_{PSDCM0}/ T_{PHDCM0}	No Delay Global Clock and IFF[2] with DCM in Source-Synchronous Mode	XC6SLX4	0.71/0.65	N/A	0.72/1.22	1.58/1.18	ns
		XC6SLX9	0.71/0.69	0.71/1.19	0.72/1.36	1.58/1.18	ns
		XC6SLX16	0.86/0.52	0.92/0.57	1.04/0.60	1.02/1.06	ns
		XC6SLX25	0.84/0.58	0.90/0.59	1.01/0.59	1.58/1.07	ns
		XC6SLX25T	0.84/0.58	0.90/0.59	1.01/0.59	N/A	ns
		XC6SLX45	0.85/0.70	0.90/0.76	0.98/0.79	1.34/1.34	ns
		XC6SLX45T	0.85/0.70	0.90/0.76	0.98/0.79	N/A	ns
		XC6SLX75	1.00/0.62	1.06/0.63	1.15/0.63	1.65/1.46	ns
		XC6SLX75T	1.00/0.71	1.06/0.72	1.15/0.72	N/A	ns
		XC6SLX100	0.81/0.68	0.81/0.69	0.94/0.69	1.42/2.07	ns
		XC6SLX100T	0.81/0.68	0.81/0.69	0.94/0.69	N/A	ns
		XC6SLX150	0.68/0.98	0.69/0.99	0.79/0.99	1.45/1.60	ns
		XC6SLX150T	0.68/0.98	0.69/0.99	0.79/0.99	N/A	ns
		XA6SLX4	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX9	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX16	1.01/0.56	N/A	1.04/0.60	N/A	ns
		XA6SLX25	0.94/0.76	N/A	1.06/0.77	N/A	ns
		XA6SLX25T	0.94/0.76	N/A	1.14/0.77	N/A	ns
		XA6SLX45	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX45T	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX75	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX100	N/A	N/A	1.37/0.75	N/A	ns
		XQ6SLX75	N/A	N/A	1.15/0.72	1.65/1.46	ns
		XQ6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XQ6SLX150	N/A	N/A	0.79/1.15	1.45/1.60	ns
		XQ6SLX150T	0.73/1.15	N/A	0.79/1.15	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 75: **Global Clock Setup and Hold With PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSPLL0}/ T_{PHPLL0}	No Delay Global Clock and IFF(2) with PLL in Source-Synchronous Mode	XC6SLX4	0.47/1.08	N/A	0.47/1.60	1.15/1.68	ns
		XC6SLX9	0.47/1.08	0.47/1.35	0.47/1.60	1.15/1.68	ns
		XC6SLX16	0.37/0.75	0.37/0.82	0.51/0.94	0.57/1.31	ns
		XC6SLX25	0.69/1.06	0.69/1.06	0.69/1.06	1.86/1.67	ns
		XC6SLX25T	0.69/1.06	0.69/1.06	0.69/1.06	N/A	ns
		XC6SLX45	0.57/1.05	0.65/1.10	0.65/1.18	1.02/1.65	ns
		XC6SLX45T	0.57/1.06	0.65/1.10	0.65/1.18	N/A	ns
		XC6SLX75	0.86/1.04	0.87/1.04	0.90/1.04	1.34/1.55	ns
		XC6SLX75T	0.86/1.04	0.87/1.04	0.90/1.04	N/A	ns
		XC6SLX100	0.53/1.13	0.54/1.13	0.55/1.13	0.89/2.39	ns
		XC6SLX100T	0.53/1.13	0.54/1.13	0.55/1.13	N/A	ns
		XC6SLX150	0.50/1.31	0.51/1.31	0.52/1.31	1.02/1.72	ns
		XC6SLX150T	0.50/1.31	0.51/1.31	0.52/1.31	N/A	ns
		XA6SLX4	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX9	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX16	0.92/0.69	N/A	0.63/0.82	N/A	ns
		XA6SLX25	0.99/0.94	N/A	0.96/0.94	N/A	ns
		XA6SLX25T	0.99/0.94	N/A	1.04/0.94	N/A	ns
		XA6SLX45	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX45T	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX75	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX100	N/A	N/A	1.25/0.96	N/A	ns
		XQ6SLX75	N/A	N/A	1.02/0.89	1.34/1.55	ns
		XQ6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XQ6SLX150	N/A	N/A	0.63/1.19	1.02/1.72	ns
		XQ6SLX150T	0.60/1.19	N/A	0.63/1.19	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 79: **Package Skew *(Cont'd)***

Symbol	Description	Device	Package[2]	Value	Units
$T_{PKGSKEW}$	Package Skew[1]	LX45	CSG324	70	ps
			CS(G)484	99	ps
			FG(G)484	109	ps
			FG(G)676	138	ps
		LX45T	CSG324	75	ps
			CS(G)484	100	ps
			FG(G)484	95	ps
		LX75	CS(G)484	101	ps
			FG(G)484	107	ps
			FG(G)676	161	ps
		LX75T	CS(G)484	107	ps
			FG(G)484	110	ps
			FG(G)676	134	ps
		LX100	CS(G)484	95	ps
			FG(G)484	155	ps
			FG(G)676	144	ps
		LX100T	CS(G)484	88	ps
			FG(G)484	111	ps
			FG(G)676	147	ps
			FG(G)900	134	ps
		LX150	CS(G)484	84	ps
			FG(G)484	103	ps
			FG(G)676	115	ps
			FG(G)900	121	ps
		LX150T	CS(G)484	83	ps
			FG(G)484	88	ps
			FG(G)676	141	ps
			FG(G)900	120	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from Pad to Ball.
2. Some of the devices are available in both Pb and Pb-free (additional G) packages as standard ordering options. See DS160: *Spartan-6 Family Overview* for more information.

Table 80: **Sample Window**

Symbol	Description	Device[1]	Speed Grade				Units
			-3	-3N	-2	-1L	
T_{SAMP}	Sampling Error at Receiver Pins[2]	All	510	510	530	740	ps
T_{SAMP_BUFIO2}	Sampling Error at Receiver Pins using BUFIO2[3]	All	430	430	450	590	ps

Notes:

1. LXT devices are not available with a -1L speed grade.
2. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 DCM jitter
   - DCM accuracy (phase offset)
   - DCM phase shift resolution

   These measurements do not include package or clock tree skew.
3. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO2 clock network and IODELAY2 to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.