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### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### **Details**

Product Status	Active
Number of LABs/CLBs	715
Number of Logic Elements/Cells	9152
Total RAM Bits	589824
Number of I/O	102
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xc6slx9-3tqg144c">https://www.e-xfl.com/product-detail/xilinx/xc6slx9-3tqg144c</a>

Table 1: Absolute Maximum Ratings<sup>(1)</sup> (Cont'd)

Symbol	Description				Units	
$V_{IN}$ and $V_{TS}$ <sup>(3)</sup>	I/O input voltage or voltage applied to 3-state output, relative to GND <sup>(4)</sup>	All user and dedicated I/Os	Commercial	DC	-0.60 to 4.10	V
				20% overshoot duration	-0.75 to 4.25	V
				8% overshoot duration <sup>(5)</sup>	-0.75 to 4.40	V
			Industrial	DC	-0.60 to 3.95	V
				20% overshoot duration	-0.75 to 4.15	V
				4% overshoot duration <sup>(5)</sup>	-0.75 to 4.40	V
			Expanded (Q)	DC	-0.60 to 3.95	V
				20% overshoot duration	-0.75 to 4.15	V
				4% overshoot duration <sup>(5)</sup>	-0.75 to 4.40	V
		Restricted to maximum of 100 user I/Os	Commercial	20% overshoot duration	-0.75 to 4.35	V
				15% overshoot duration <sup>(5)</sup>	-0.75 to 4.40	V
				10% overshoot duration	-0.75 to 4.45	V
			Industrial	20% overshoot duration	-0.75 to 4.25	V
				10% overshoot duration	-0.75 to 4.35	V
				8% overshoot duration <sup>(5)</sup>	-0.75 to 4.40	V
Expanded (Q)	20% overshoot duration	-0.75 to 4.25	V			
	10% overshoot duration	-0.75 to 4.35	V			
	8% overshoot duration <sup>(5)</sup>	-0.75 to 4.40	V			
$T_{STG}$	Storage temperature (ambient)				-65 to 150	°C
$T_{SOL}$	Maximum soldering temperature <sup>(6)</sup> (TQG144, CPG196, CSG225, CSG324, CSG484, and FTG256)				+260	°C
	Maximum soldering temperature <sup>(6)</sup> (Pb-free packages: FGG484, FGG676, and FGG900)				+250	°C
	Maximum soldering temperature <sup>(6)</sup> (Pb packages: CS484, FT256, FG484, FG676, and FG900)				+220	°C
$T_j$	Maximum junction temperature <sup>(6)</sup>				+125	°C

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When programming eFUSE,  $V_{FS} \leq V_{CCAUX}$ . Requires up to 40 mA current. For read mode,  $V_{FS}$  can be between GND and 3.45 V.
3. I/O absolute maximum limit applied to DC and AC signals. Overshoot duration is the percentage of a data period that the I/O is stressed beyond 3.45V.
4. For I/O operation, refer to [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.
5. Maximum percent overshoot duration to meet 4.40V maximum.
6. For soldering guidelines and thermal considerations, see [UG385](#): *Spartan-6 FPGA Packaging and Pinout Specification*.

## SelectIO™ Interface DC Input and Output Levels

Table 7: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

I/O Standard	V <sub>CCO</sub> for Drivers <sup>(1)</sup>			V <sub>REF</sub> for Inputs		
	V, Min	V, Nom	V, Max	V, Min	V, Nom	V, Max
LVTTTL	3.0	3.3	3.45	V <sub>REF</sub> is not used for these I/O standards		
LVC MOS33	3.0	3.3	3.45			
LVC MOS25	2.3	2.5	2.7			
LVC MOS18	1.65	1.8	1.95			
LVC MOS18_JEDEC	1.65	1.8	1.95			
LVC MOS15	1.4	1.5	1.6			
LVC MOS15_JEDEC	1.4	1.5	1.6			
LVC MOS12	1.1	1.2	1.3			
LVC MOS12_JEDEC	1.1	1.2	1.3			
PCI33_3 <sup>(2)</sup>	3.0	3.3	3.45			
PCI66_3 <sup>(2)</sup>	3.0	3.3	3.45			
I2C	2.7	3.0	3.45			
SMBUS	2.7	3.0	3.45			
SDIO	3.0	3.3	3.45			
MOBILE_DDR	1.7	1.8	1.9			
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_II	1.4	1.5	1.6	0.68	0.75	0.9
HSTL_III	1.4	1.5	1.6	–	0.9	–
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–
HSTL_III_18	1.7	1.8	1.9	–	1.1	–
SSTL3_I	3.0	3.3	3.45	1.3	1.5	1.7
SSTL3_II	3.0	3.3	3.45	1.3	1.5	1.7
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38
SSTL18_I	1.7	1.8	1.9	0.833	0.9	0.969
SSTL18_II	1.7	1.8	1.9	0.833	0.9	0.969
SSTL15_II	1.425	1.5	1.575	0.69	0.75	0.81

### Notes:

1. V<sub>CCO</sub> range required when using I/O standard for an output. Also required for MOBILE\_DDR, PCI33\_3, LVC MOS18\_JEDEC, LVC MOS15\_JEDEC, and LVC MOS12\_JEDEC inputs, and for LVC MOS25 inputs when V<sub>CCAUX</sub> = 3.3V.
2. For PCI systems, the transmitter and receiver should have common supplies for V<sub>CCO</sub>.

Table 8: Recommended Operating Conditions for User I/Os Using Differential Signal Standards

I/O Standard	V <sub>CCO</sub> for Drivers		
	V, Min	V, Nom	V, Max
LVDS_33	3.0	3.3	3.45
LVDS_25	2.25	2.5	2.75
BLVDS_25	2.25	2.5	2.75
MINI_LVDS_33	3.0	3.3	3.45
MINI_LVDS_25	2.25	2.5	2.75
LVPECL_33 <sup>(1)</sup>	N/A—Inputs Only		
LVPECL_25	N/A—Inputs Only		
RSDS_33	3.0	3.3	3.45
RSDS_25	2.25	2.5	2.75
TMDS_33 <sup>(1)</sup>	3.14	3.3	3.45
PPDS_33	3.0	3.3	3.45
PPDS_25	2.25	2.5	2.75
DISPLAY_PORT	2.3	2.5	2.7
DIFF_MOBILE_DDR	1.7	1.8	1.9
DIFF_HSTL_I	1.4	1.5	1.6
DIFF_HSTL_II	1.4	1.5	1.6
DIFF_HSTL_III	1.4	1.5	1.6
DIFF_HSTL_I_18	1.7	1.8	1.9
DIFF_HSTL_II_18	1.7	1.8	1.9
DIFF_HSTL_III_18	1.7	1.8	1.9
DIFF_SSTL3_I	3.0	3.3	3.45
DIFF_SSTL3_II	3.0	3.3	3.45
DIFF_SSTL2_I	2.3	2.5	2.7
DIFF_SSTL2_II	2.3	2.5	2.7
DIFF_SSTL18_I	1.7	1.8	1.9
DIFF_SSTL18_II	1.7	1.8	1.9
DIFF_SSTL15_II	1.425	1.5	1.575

**Notes:**

1. LVPECL\_33 and TMDS\_33 inputs require V<sub>CCAUX</sub> = 3.3V nominal.

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T <sub>IOPI</sub>				T <sub>IOOP</sub>				T <sub>IOTP</sub>				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	-3	-3N	-2	-1L <sup>(1)</sup>	
LVC MOS15, Slow, 8 mA	0.98	1.10	1.23	1.79	2.30	2.44	2.64	3.25	2.30	2.44	2.64	3.25	ns
LVC MOS15, Slow, 12 mA	0.98	1.10	1.23	1.79	2.03	2.17	2.37	2.99	2.03	2.17	2.37	2.99	ns
LVC MOS15, Slow, 16 mA	0.98	1.10	1.23	1.79	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVC MOS15, Fast, 2 mA	0.98	1.10	1.23	1.79	3.29	3.43	3.63	4.24	3.29	3.43	3.63	4.24	ns
LVC MOS15, Fast, 4 mA	0.98	1.10	1.23	1.79	2.27	2.41	2.61	3.22	2.27	2.41	2.61	3.22	ns
LVC MOS15, Fast, 6 mA	0.98	1.10	1.23	1.79	1.78	1.92	2.12	2.74	1.78	1.92	2.12	2.74	ns
LVC MOS15, Fast, 8 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.69	1.73	1.87	2.07	2.69	ns
LVC MOS15, Fast, 12 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.64	1.73	1.87	2.07	2.64	ns
LVC MOS15, Fast, 16 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.64	1.73	1.87	2.07	2.64	ns
LVC MOS15_JEDEC, QUIETIO, 2 mA	1.03	1.15	1.28	1.49	5.49	5.63	5.83	6.37	5.49	5.63	5.83	6.37	ns
LVC MOS15_JEDEC, QUIETIO, 4 mA	1.03	1.15	1.28	1.49	4.61	4.75	4.95	5.51	4.61	4.75	4.95	5.51	ns
LVC MOS15_JEDEC, QUIETIO, 6 mA	1.03	1.15	1.28	1.49	4.07	4.21	4.41	4.97	4.07	4.21	4.41	4.97	ns
LVC MOS15_JEDEC, QUIETIO, 8 mA	1.03	1.15	1.28	1.49	3.92	4.06	4.26	4.81	3.92	4.06	4.26	4.81	ns
LVC MOS15_JEDEC, QUIETIO, 12 mA	1.03	1.15	1.28	1.49	3.54	3.68	3.88	4.51	3.54	3.68	3.88	4.51	ns
LVC MOS15_JEDEC, QUIETIO, 16 mA	1.03	1.15	1.28	1.49	3.33	3.47	3.67	4.31	3.33	3.47	3.67	4.31	ns
LVC MOS15_JEDEC, Slow, 2 mA	1.03	1.15	1.28	1.49	4.18	4.32	4.52	5.13	4.18	4.32	4.52	5.13	ns
LVC MOS15_JEDEC, Slow, 4 mA	1.03	1.15	1.28	1.49	3.42	3.56	3.76	4.35	3.42	3.56	3.76	4.35	ns
LVC MOS15_JEDEC, Slow, 6 mA	1.03	1.15	1.28	1.49	2.29	2.43	2.63	3.25	2.29	2.43	2.63	3.25	ns
LVC MOS15_JEDEC, Slow, 8 mA	1.03	1.15	1.28	1.49	2.30	2.44	2.64	3.26	2.30	2.44	2.64	3.26	ns
LVC MOS15_JEDEC, Slow, 12 mA	1.03	1.15	1.28	1.49	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVC MOS15_JEDEC, Slow, 16 mA	1.03	1.15	1.28	1.49	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVC MOS15_JEDEC, Fast, 2 mA	1.03	1.15	1.28	1.49	3.28	3.42	3.62	4.22	3.28	3.42	3.62	4.22	ns
LVC MOS15_JEDEC, Fast, 4 mA	1.03	1.15	1.28	1.49	2.27	2.41	2.61	3.23	2.27	2.41	2.61	3.23	ns
LVC MOS15_JEDEC, Fast, 6 mA	1.03	1.15	1.28	1.49	1.78	1.92	2.12	2.74	1.78	1.92	2.12	2.74	ns
LVC MOS15_JEDEC, Fast, 8 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.69	1.73	1.87	2.07	2.69	ns
LVC MOS15_JEDEC, Fast, 12 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.63	1.73	1.87	2.07	2.63	ns
LVC MOS15_JEDEC, Fast, 16 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.63	1.73	1.87	2.07	2.63	ns
LVC MOS12, QUIETIO, 2 mA	0.91	1.03	1.16	1.51	6.40	6.54	6.74	7.30	6.40	6.54	6.74	7.30	ns
LVC MOS12, QUIETIO, 4 mA	0.91	1.03	1.16	1.51	4.98	5.12	5.32	5.90	4.98	5.12	5.32	5.90	ns
LVC MOS12, QUIETIO, 6 mA	0.91	1.03	1.16	1.51	4.65	4.79	4.99	5.55	4.65	4.79	4.99	5.55	ns
LVC MOS12, QUIETIO, 8 mA	0.91	1.03	1.16	1.51	4.23	4.37	4.57	5.21	4.23	4.37	4.57	5.21	ns
LVC MOS12, QUIETIO, 12 mA	0.91	1.03	1.16	1.51	3.98	4.12	4.32	4.94	3.98	4.12	4.32	4.94	ns
LVC MOS12, Slow, 2 mA	0.91	1.03	1.16	1.51	4.98	5.12	5.32	5.91	4.98	5.12	5.32	5.91	ns
LVC MOS12, Slow, 4 mA	0.91	1.03	1.16	1.51	2.84	2.98	3.18	3.81	2.84	2.98	3.18	3.81	ns
LVC MOS12, Slow, 6 mA	0.91	1.03	1.16	1.51	2.77	2.91	3.11	3.72	2.77	2.91	3.11	3.72	ns
LVC MOS12, Slow, 8 mA	0.91	1.03	1.16	1.51	2.34	2.48	2.68	3.31	2.34	2.48	2.68	3.31	ns
LVC MOS12, Slow, 12 mA	0.91	1.03	1.16	1.51	2.08	2.22	2.42	3.06	2.08	2.22	2.42	3.06	ns

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices<sup>(1)</sup> (Cont'd)

I/O Standard	T <sub>IOPI</sub>		T <sub>IOOP</sub>		T <sub>IOTP</sub>		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
DIFF_SSTL3_I	1.26	1.44	1.95	2.15	1.95	2.15	ns
DIFF_SSTL3_II	1.26	1.44	1.94	2.14	1.94	2.14	ns
DIFF_SSTL2_I	1.09	1.27	1.94	2.14	1.94	2.14	ns
DIFF_SSTL2_II	1.09	1.27	1.90	2.10	1.90	2.10	ns
DIFF_SSTL18_I	1.04	1.22	1.86	2.06	1.86	2.06	ns
DIFF_SSTL18_II	1.05	1.23	1.82	2.02	1.82	2.02	ns
DIFF_SSTL15_II	1.01	1.19	1.81	2.01	1.81	2.01	ns
DIFF_MOBILE_DDR	1.04	1.22	1.89	2.09	1.89	2.09	ns
LVTTL, QUIETIO, 2 mA	1.42	1.60	5.64	5.84	5.64	5.84	ns
LVTTL, QUIETIO, 4 mA	1.42	1.60	4.46	4.66	4.46	4.66	ns
LVTTL, QUIETIO, 6 mA	1.42	1.60	3.92	4.12	3.92	4.12	ns
LVTTL, QUIETIO, 8 mA	1.42	1.60	3.37	3.57	3.37	3.57	ns
LVTTL, QUIETIO, 12 mA	1.42	1.60	3.42	3.62	3.42	3.62	ns
LVTTL, QUIETIO, 16 mA	1.42	1.60	3.09	3.29	3.09	3.29	ns
LVTTL, QUIETIO, 24 mA	1.42	1.60	2.83	3.03	2.83	3.03	ns
LVTTL, Slow, 2 mA	1.42	1.60	4.58	4.78	4.58	4.78	ns
LVTTL, Slow, 4 mA	1.42	1.60	3.38	3.58	3.38	3.58	ns
LVTTL, Slow, 6 mA	1.42	1.60	2.95	3.15	2.95	3.15	ns
LVTTL, Slow, 8 mA	1.42	1.60	2.73	2.93	2.73	2.93	ns
LVTTL, Slow, 12 mA	1.42	1.60	2.72	2.92	2.72	2.92	ns
LVTTL, Slow, 16 mA	1.42	1.60	2.53	2.73	2.53	2.73	ns
LVTTL, Slow, 24 mA	1.42	1.60	2.42	2.62	2.42	2.62	ns
LVTTL, Fast, 2 mA	1.42	1.60	4.04	4.24	4.04	4.24	ns
LVTTL, Fast, 4 mA	1.42	1.60	2.66	2.86	2.66	2.86	ns
LVTTL, Fast, 6 mA	1.42	1.60	2.58	2.78	2.58	2.78	ns
LVTTL, Fast, 8 mA	1.42	1.60	2.46	2.66	2.46	2.66	ns
LVTTL, Fast, 12 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns
LVTTL, Fast, 16 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns
LVTTL, Fast, 24 mA	1.42	1.60	1.97	2.17	1.97	2.17	ns
LVC MOS33, QUIETIO, 2 mA	1.41	1.59	5.65	5.85	5.65	5.85	ns
LVC MOS33, QUIETIO, 4 mA	1.41	1.59	4.20	4.40	4.20	4.40	ns
LVC MOS33, QUIETIO, 6 mA	1.41	1.59	3.65	3.85	3.65	3.85	ns
LVC MOS33, QUIETIO, 8 mA	1.41	1.59	3.51	3.71	3.51	3.71	ns
LVC MOS33, QUIETIO, 12 mA	1.41	1.59	3.09	3.29	3.09	3.29	ns
LVC MOS33, QUIETIO, 16 mA	1.41	1.59	2.91	3.11	2.91	3.11	ns
LVC MOS33, QUIETIO, 24 mA	1.41	1.59	2.73	2.93	2.73	2.93	ns
LVC MOS33, Slow, 2 mA	1.41	1.59	4.59	4.79	4.59	4.79	ns
LVC MOS33, Slow, 4 mA	1.41	1.59	3.14	3.34	3.14	3.34	ns

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices<sup>(1)</sup> (Cont'd)

I/O Standard	T <sub>IOPI</sub>		T <sub>IOOP</sub>		T <sub>IOTP</sub>		Units
	Speed Grade		Speed Grade		Speed Grade		
	-3	-2	-3	-2	-3	-2	
LVC MOS12, QUIETIO, 6 mA	0.98	1.16	4.79	4.99	4.79	4.99	ns
LVC MOS12, QUIETIO, 8 mA	0.98	1.16	4.43	4.63	4.43	4.63	ns
LVC MOS12, QUIETIO, 12 mA	0.98	1.16	4.18	4.38	4.18	4.38	ns
LVC MOS12, Slow, 2 mA	0.98	1.16	5.12	5.32	5.12	5.32	ns
LVC MOS12, Slow, 4 mA	0.98	1.16	3.00	3.20	3.00	3.20	ns
LVC MOS12, Slow, 6 mA	0.98	1.16	2.91	3.11	2.91	3.11	ns
LVC MOS12, Slow, 8 mA	0.98	1.16	2.51	2.71	2.51	2.71	ns
LVC MOS12, Slow, 12 mA	0.98	1.16	2.25	2.45	2.25	2.45	ns
LVC MOS12, Fast, 2 mA	0.98	1.16	3.60	3.80	3.60	3.80	ns
LVC MOS12, Fast, 4 mA	0.98	1.16	2.49	2.69	2.49	2.69	ns
LVC MOS12, Fast, 6 mA	0.98	1.16	1.94	2.14	1.94	2.14	ns
LVC MOS12, Fast, 8 mA	0.98	1.16	1.82	2.02	1.82	2.02	ns
LVC MOS12, Fast, 12 mA	0.98	1.16	1.80	2.00	1.80	2.00	ns
LVC MOS12_JEDEC, QUIETIO, 2 mA	1.57	1.75	6.53	6.73	6.53	6.73	ns
LVC MOS12_JEDEC, QUIETIO, 4 mA	1.57	1.75	5.12	5.32	5.12	5.32	ns
LVC MOS12_JEDEC, QUIETIO, 6 mA	1.57	1.75	4.81	5.01	4.81	5.01	ns
LVC MOS12_JEDEC, QUIETIO, 8 mA	1.57	1.75	4.44	4.64	4.44	4.64	ns
LVC MOS12_JEDEC, QUIETIO, 12 mA	1.57	1.75	4.20	4.40	4.20	4.40	ns
LVC MOS12_JEDEC, Slow, 2 mA	1.57	1.75	5.14	5.34	5.14	5.34	ns
LVC MOS12_JEDEC, Slow, 4 mA	1.57	1.75	2.99	3.19	2.99	3.19	ns
LVC MOS12_JEDEC, Slow, 6 mA	1.57	1.75	2.90	3.10	2.90	3.10	ns
LVC MOS12_JEDEC, Slow, 8 mA	1.57	1.75	2.50	2.70	2.50	2.70	ns
LVC MOS12_JEDEC, Slow, 12 mA	1.57	1.75	2.26	2.46	2.26	2.46	ns
LVC MOS12_JEDEC, Fast, 2 mA	1.57	1.75	3.60	3.80	3.60	3.80	ns
LVC MOS12_JEDEC, Fast, 4 mA	1.57	1.75	2.49	2.69	2.49	2.69	ns
LVC MOS12_JEDEC, Fast, 6 mA	1.57	1.75	1.94	2.14	1.94	2.14	ns
LVC MOS12_JEDEC, Fast, 8 mA	1.57	1.75	1.83	2.03	1.83	2.03	ns
LVC MOS12_JEDEC, Fast, 12 mA	1.57	1.75	1.80	2.00	1.80	2.00	ns

**Notes:**

1. The Spartan-6Q FPGA -1L values are listed in Table 28.

Table 30 summarizes the value of T<sub>IOTPHZ</sub>. T<sub>IOTPHZ</sub> is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). These delays are measured using LVC MOS25, Fast, 12 mA.

Table 30: IOB 3-state ON Output Switching Characteristics (T<sub>IOTPHZ</sub>)

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T <sub>IOTPHZ</sub>	T input to Pad high-impedance	1.39	1.59	1.59	1.91	ns

Table 32: Output Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	R <sub>REF</sub> (Ω)	C <sub>REF</sub> <sup>(1)</sup> (pF)	V <sub>MEAS</sub> (V)	V <sub>REF</sub> (V)
SSTL, Class II, 2.5V	SSTL2_II	25	0	V <sub>REF</sub>	1.25
SSTL, Class II, 1.5V	SSTL15_II	25	0	V <sub>REF</sub>	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	100	0	0 <sup>(3)</sup>	–
BLVDS (Bus LVDS), 2.5V	BLVDS_25	Note 4	0	0 <sup>(3)</sup>	–
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	100	0	0 <sup>(3)</sup>	–
RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RSDS_25, RSDS_33	100	0	0 <sup>(3)</sup>	–
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	Note 5	0	0 <sup>(3)</sup>	–
PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V)	PPDS_25, PPDS_33	100	0	0 <sup>(3)</sup>	–

**Notes:**

1. C<sub>REF</sub> is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. The value given is the differential output voltage.
4. See the *BLVDS Output Termination* section in [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.
5. See the *TMDS\_33 Termination* section in [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.

## Simultaneously Switching Outputs

Due to package electrical parasitics, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. [Table 33](#) and [Table 34](#) provide guidelines for the recommended maximum allowable number of SSOs. These guidelines describe the maximum number of user I/O pins of an output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise for that particular signal standard. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of GND and power bounce.

For each device/package combination, [Table 33](#) provides the number of equivalent V<sub>CCO</sub>/GND pairs per bank. For each output signal standard and drive strength, [Table 34](#) recommends the maximum number of SSOs, switching in the same direction, allowed per V<sub>CCO</sub>/GND pair within an I/O bank. The guidelines are categorized by package style, slew rate, and output drive current. The number of SSOs are also specified by I/O bank. Multiply the appropriate numbers from each table to calculate the maximum number of SSOs allowed within an I/O bank. The guidelines assume that all pins within a bank use the same I/O standard. Exceeding these SSO guidelines can result in increased power or GND bounce, degraded signal integrity, or increased system jitter. For a given I/O standard, if the SSO limit per pair in [Table 34](#) is greater than the maximum I/O per pair in [Table 33](#), then there is no SSO limit for the exclusive use of that I/O standard.

The recommended maximum SSO values assume that the FPGA is soldered on a printed circuit board and that the board uses sound design practices. Due to the additional inductance introduced by the socket, the SSO values do not apply for FPGAs mounted in sockets. The SSO values assume that the V<sub>CCAUX</sub> is powered at 3.3V. Setting V<sub>CCAUX</sub> to 2.5V provides better SSO characteristics. For more detail, see [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.



Table 34: SSO Limit per V<sub>CC0</sub>/GND Pair (Cont'd)

V <sub>CC0</sub>	I/O Standard	Drive	Slew	SSO Limit per V <sub>CC0</sub> /GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
2.5V	LVCMOS25	2	Fast	38	43	38	43
			Slow	46	52	46	48
			QuietIO	57	64	57	59
		4	Fast	21	24	21	23
			Slow	26	31	26	27
			QuietIO	33	32	33	30
		6	Fast	15	17	15	16
			Slow	19	22	19	19
			QuietIO	25	23	25	19
		8	Fast	12	15	12	14
			Slow	15	18	15	16
			QuietIO	21	19	21	16
		12	Fast	1	3	1	1
			Slow	2	7	2	4
			QuietIO	3	8	3	8
		16	Fast	1	3	1	1
			Slow	3	7	3	3
			QuietIO	4	9	4	8
		24	Fast	N/A	3	N/A	1
			Slow	N/A	5	N/A	2
QuietIO	N/A		8	N/A	6		
SSTL_2_I <sup>(3)</sup>				10	11	10	11
SSTL_2_II <sup>(3)</sup>				N/A	7	N/A	7
DIFF_SSTL_2_I <sup>(3)</sup>				30	33	30	33
DIFF_SSTL_2_II <sup>(3)</sup>				N/A	21	N/A	24

Table 34: SSO Limit per V<sub>CC0</sub>/GND Pair (Cont'd)

V <sub>CC0</sub>	I/O Standard	Drive	Slew	SSO Limit per V <sub>CC0</sub> /GND Pair					
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324			
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5		
3.3V	LVTTTL	2	Fast	53	65	53	62		
			Slow	70	80	70	73		
			QuietIO	79	89	79	91		
		4	Fast	23	30	23	27		
			Slow	34	41	34	37		
			QuietIO	44	49	44	46		
		6	Fast	16	21	16	20		
			Slow	21	28	21	25		
			QuietIO	34	39	34	34		
		8	Fast	12	16	12	15		
			Slow	16	22	16	19		
			QuietIO	27	28	27	24		
		12	Fast	1	3	1	1		
			Slow	2	5	2	4		
			QuietIO	2	10	2	8		
		16	Fast	1	3	1	1		
			Slow	1	7	1	2		
			QuietIO	3	11	3	8		
		24	Fast	1	2	1	1		
			Slow	2	5	2	2		
			QuietIO	8	9	8	8		
			PCI33_3			18	19	18	19
			PCI66_3			18	19	18	19
			SSTL_3_I			5	8	5	8
			SSTL_3_II			3	5	3	3
			DIFF_SSTL_3_I			15	24	15	24
			DIFF_SSTL_3_II			9	15	9	9
	SDIO			17	18	17	15		

## Block RAM Switching Characteristics

Table 43: Block RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
<b>Block RAM Clock to Out Delays</b>						
$T_{RCKO\_DO}$	Clock CLK to DOUT output (without output register) <sup>(1)</sup>	1.85	2.10	2.10	3.50	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register) <sup>(2)</sup>	1.60	1.75	1.75	2.30	ns, Max
<b>Setup and Hold Times Before/After Clock CLK</b>						
$T_{RCKC\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs for XC devices <sup>(3)</sup>	0.35/ 0.10	0.40/ 0.12	0.40/ 0.12	0.50/ 0.15	ns, Min
	ADDR inputs for XA and XQ devices <sup>(3)</sup>	0.35/ 0.17	N/A	0.40/ 0.17	0.50/ 0.15	ns, Min
$T_{RDCK\_DI}/T_{RCKD\_DI}$	DIN inputs <sup>(4)</sup>	0.30/ 0.10	0.30/ 0.10	0.30/ 0.10	0.40/ 0.15	ns, Min
$T_{RCKC\_EN}/T_{RCKC\_EN}$	Block RAM Enable (EN) input	0.22/ 0.05	0.25/ 0.06	0.25/ 0.06	0.44/ 0.10	ns, Min
$T_{RCKC\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.20/ 0.10	0.20/ 0.10	0.20/ 0.10	0.28/ 0.15	ns, Min
$T_{RCKC\_WE}/T_{RCKC\_WE}$	Write Enable (WE) input	0.25/ 0.10	0.33/ 0.10	0.33/ 0.10	0.28/ 0.15	ns, Min
<b>Maximum Frequency</b>						
$F_{MAX}$	Block RAM in all modes	320	280	280	150	MHz

### Notes:

- $T_{RCKO\_DO}$  includes  $T_{RCKO\_DOA}$  and  $T_{RCKO\_DOPA}$  as well as the B port equivalent timing parameters.
- $T_{RCKO\_DO\_REG}$  includes  $T_{RCKO\_DOA\_REG}$  and  $T_{RCKO\_DOPA\_REG}$  as well as the B port equivalent timing parameters.
- The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
- $T_{RDCK\_DI}$  includes both A and B inputs as well as the parity inputs of A and B.

## DSP48A1 Switching Characteristics

Table 44: DSP48A1 Switching Characteristics

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-3	-3N	-2	-1L	
<b>Setup and Hold Times of Data/Control Pins to the Input Register Clock</b>									
$T_{DSPDCK\_A\_A1REG}/$ $T_{DSPCKD\_A\_A1REG}$	A input to A1 register CLK	N/A	N/A	N/A	0.15/ 0.09	0.17/ 0.09	0.17/ 0.09	0.32/ 0.09	ns
$T_{DSPDCK\_D\_B1REG}/$ $T_{DSPCKD\_D\_B1REG}$	D input to B1 register CLK	Yes	N/A	N/A	1.90/ -0.07	1.95/ -0.07	1.95/ -0.07	2.82/ -0.07	ns
$T_{DSPDCK\_C\_CREG}/$ $T_{DSPCKD\_C\_CREG}$	C input to C register CLK for XC devices	N/A	N/A	N/A	0.11/ 0.15	0.13/ 0.15	0.13/ 0.15	0.24/ 0.09	ns
	C input to C register CLK for XA and XQ devices				0.11/ 0.19	N/A	0.13/ 0.23	0.24/ 0.09	
$T_{DSPDCK\_D\_DREG}/$ $T_{DSPCKD\_D\_DREG}$	D input to D register CLK for XC devices	N/A	N/A	N/A	0.09/ 0.15	0.10/ 0.15	0.10/ 0.15	0.19/ 0.12	ns
	D input to D register CLK for XA and XQ devices				0.09/ 0.23	N/A	0.10/ 0.27	0.19/ 0.12	
$T_{DSPDCK\_OPMODE\_B1REG}/$ $T_{DSPCKD\_OPMODE\_B1REG}$	OPMODE input to B1 register CLK	Yes	N/A	N/A	1.97/ 0.01	2.00/ 0.01	2.00/ 0.01	2.85/ 0.01	ns
$T_{DSPDCK\_OPMODE\_OPMODEREG}/$ $T_{DSPCKD\_OPMODE\_OPMODEREG}$	OPMODE input to OPMODE register CLK for XC devices	N/A	N/A	N/A	0.18/ 0.12	0.21/ 0.12	0.21/ 0.12	0.40/ 0.12	ns
	OPMODE input to OPMODE register CLK for XA and XQ devices				0.18/ 0.16	N/A	0.21/ 0.22	0.40/ 0.12	
<b>Setup and Hold Times of Data Pins to the Pipeline Register Clock</b>									
$T_{DSPDCK\_A\_MREG}/$ $T_{DSPCKD\_A\_MREG}$	A input to M register CLK	N/A	Yes	N/A	3.06/ -0.40	3.51/ -0.40	3.51/ -0.40	3.97/ -0.40	ns
$T_{DSPDCK\_B\_MREG}/$ $T_{DSPCKD\_B\_MREG}$	B input to M register CLK	Yes	Yes	N/A	3.96/ -0.68	4.58/ -0.68	4.58/ -0.68	7.00/ -0.68	ns
$T_{DSPDCK\_D\_MREG}/$ $T_{DSPCKD\_D\_MREG}$	D input to M register CLK	Yes	Yes	N/A	4.23/ -0.56	4.80/ -0.56	4.80/ -0.56	6.84/ -0.56	ns
$T_{DSPDCK\_OPMODE\_MREG}/$ $T_{DSPCKD\_OPMODE\_MREG}$	OPMODE to M register CLK	Yes	Yes	N/A	4.18/ -0.48	4.80/ -0.48	4.80/ -0.48	6.88/ -0.48	ns
		No	Yes	N/A	2.37/ -0.48	2.70/ -0.48	2.70/ -0.48	4.28/ -0.48	ns
<b>Setup and Hold Times of Data/Control Pins to the Output Register Clock</b>									
$T_{DSPDCK\_A\_PREG}/$ $T_{DSPCKD\_A\_PREG}$	A input to P register CLK	N/A	Yes	Yes	4.32/ -0.76	5.06/ -0.76	5.06/ -0.76	7.52/ -0.76	ns
$T_{DSPDCK\_B\_PREG}/$ $T_{DSPCKD\_B\_PREG}$	B input to P register CLK	Yes	Yes	Yes	5.87/ -0.59	6.87/ -0.59	6.87/ -0.59	10.55/ -0.59	ns
		No	Yes	Yes	4.14/ -0.93	4.68/ -0.93	4.68/ -0.93	8.12/ -0.93	ns
$T_{DSPDCK\_C\_PREG}/$ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK	N/A	N/A	Yes	2.20/ -0.23	2.25/ -0.23	2.25/ -0.23	3.27/ -0.23	ns
$T_{DSPDCK\_D\_PREG}/$ $T_{DSPCKD\_D\_PREG}$	D input to P register CLK	Yes	Yes	Yes	5.90/ -0.92	6.91/ -0.92	6.91/ -0.92	10.39/ -0.92	ns

Table 44: DSP48A1 Switching Characteristics (Cont'd)

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-3	-3N	-2	-1L	
T <sub>DSPDCK_OPMODE_PREG</sub> / T <sub>DSPCKD_OPMODE_PREG</sub>	OPMODE input to P register CLK	Yes	Yes	Yes	6.21/ -0.84	7.27/ -0.84	7.27/ -0.84	10.43/ -0.84	ns
		No	Yes	Yes	1.69/ -0.87	1.98/ -0.87	1.98/ -0.87	3.62/ -0.87	ns
		No	No	Yes	2.09/ -0.22	2.30/ -0.22	2.30/ -0.22	3.79/ -0.22	ns
<b>Clock to Out from Output Register Clock to Output Pin</b>									
T <sub>DSPCKO_P_PREG</sub>	CLK (PREG) to P output	N/A	N/A	N/A	1.20	1.34	1.34	1.90	ns
<b>Clock to Out from Pipeline Register Clock to Output Pins</b>									
T <sub>DSPCKO_P_MREG</sub>	CLK (MREG) to P output	N/A	N/A	Yes	3.38	3.95	3.95	5.83	ns
<b>Clock to Out from Input Register Clock to Output Pins</b>									
T <sub>DSPCKO_P_A1REG</sub>	CLK (A1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.65	ns
T <sub>DSPCKO_P_B1REG</sub>	CLK (B1REG) to P output	N/A	Yes	Yes	5.02	5.87	5.87	9.63	ns
T <sub>DSPCKO_P_CREG</sub>	CLK (CREG) to P output	N/A	N/A	Yes	3.12	3.64	3.64	5.24	ns
T <sub>DSPCKO_P_DREG</sub>	CLK (DREG) to P output	Yes	Yes	Yes	6.77	7.92	7.92	12.53	ns
<b>Combinatorial Delays from Input Pins to Output Pins</b>									
T <sub>DSPDO_A_P</sub>	A input to P output	N/A	No	Yes	2.85	3.33	3.33	4.73	ns
		N/A	Yes	No <sup>(2)</sup>	3.35	3.93	3.93	6.74	ns
		N/A	Yes	Yes	4.56	5.22	5.22	8.94	ns
T <sub>DSPDO_B_P</sub>	B input to P output	Yes	No	No <sup>(2)</sup>	3.22	3.76	3.76	5.55	ns
		Yes	Yes	No <sup>(2)</sup>	6.01	6.54	6.54	9.76	ns
		Yes	Yes	Yes	6.27	7.34	7.34	11.96	ns
T <sub>DSPDO_C_P</sub>	C input to P output	N/A	N/A	Yes	2.69	3.15	3.15	4.68	ns
T <sub>DSPDO_D_P</sub>	D input to P output	Yes	Yes	Yes	6.31	7.38	7.38	11.81	ns
T <sub>DSPDO_OPMODE_P</sub>	OPMODE input to P output	Yes	Yes	Yes	6.43	7.52	7.52	11.84	ns
		No	Yes	Yes	4.84	5.66	5.66	9.25	ns
		No	No	Yes	3.11	3.49	3.49	5.03	ns
<b>Maximum Frequency</b>									
F <sub>MAX</sub>	All registers used	Yes	Yes	Yes	390	333	333	213	MHz

**Notes:**

1. A Yes signifies that the component is in the path. A No signifies that the component is being bypassed. N/A signifies not applicable because no path exists.
2. Implemented in the post-adder by adding to zero.

Table 47: Configuration Switching Characteristics<sup>(1)</sup> (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
<b>BPI Master Flash Mode Programming Switching<sup>(4)</sup></b>						
T <sub>BPICCO</sub> <sup>(5)</sup>	A[25:0], FCS_B, FOE_B, FWE_B, LDC outputs valid after CCLK falling edge	15	15	15	20	ns, Max
T <sub>BPIICCK</sub>	Master BPI CCLK (output) delay	10/100	10/100	10/100	10/130	μs, Min/Max
T <sub>BPIDCC</sub> /T <sub>BPICCD</sub>	Setup/Hold on D[15:0] data input pins	5.0/1.0	5.0/1.0	5.0/1.0	6.0/2.0	ns, Min
<b>SPI Master Flash Mode Programming Switching<sup>(6)</sup></b>						
T <sub>SPIDCC</sub> /T <sub>SPIDCCD</sub>	DIN, MISO0, MISO1, MISO2, MISO3, Setup/Hold before/after the rising CCLK edge	5.0/1.0	5.0/1.0	5.0/1.0	7.0/1.0	ns, Min
T <sub>SPIICCK</sub>	Master SPI CCLK (output) delay	0.4/7.0	0.4/7.0	0.4/7.0	0.4/10.0	μs, Min/Max
T <sub>SPICCM</sub>	MOSI clock to out	13	13	13	19	ns, Max
T <sub>SPICCFC</sub>	CSO_B clock to out	16	16	16	26	ns, Max
<b>CCLK Output (Master Modes)</b>						
T <sub>MCCKL</sub>	Master CCLK clock duty cycle Low	40/60				%, Min/Max
T <sub>MCCKH</sub>	Master CCLK clock duty cycle High	40/60				%, Min/Max
F <sub>MCCK</sub>	Maximum frequency, serial mode (Master Serial/SPI) All devices	40	40	40	30	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T	40	40	40	25	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x8 mode, LX150, and LX150T	40	40	40	20	MHz, Max
	Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x16 mode	35	35	35	20	MHz, Max
F <sub>MCCKTOL</sub>	Frequency Tolerance, master mode	±50	±50	±50	±50	%
<b>CCLK Input (Slave Modes)</b>						
T <sub>SCCKL</sub>	Slave CCLK clock minimum Low time	5	5	5	8	ns, Min
T <sub>SCCKH</sub>	Slave CCLK clock minimum High time	5	5	5	8	ns, Min
<b>USERCCLK Input</b>						
T <sub>USERCCLKL</sub>	USERCCLK clock minimum Low time	12	12	12	16	ns, Min
T <sub>USERCCLKH</sub>	USERCCLK clock minimum High time	12	12	12	16	ns, Min
F <sub>USERCCLK</sub>	Maximum USERCCLK frequency	40	40	40	30	MHz, Max

**Notes:**

- Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
- To support longer delays in configuration, use the design solutions described in [UG380: Spartan-6 FPGA Configuration User Guide](#).
- [Table 6](#) specifies the power supply ramp time.
- BPI mode is not supported in:
  - LX4, LX25, or LX25T devices
  - LX9 devices in the TQG144 package
  - LX9 or LX16 devices in the CPG196 package.
- Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
- Defense-grade Spartan-6Q -2Q devices configure in single default SPI Master (x1) mode at T<sub>j</sub> = -55°C. During operation and when using all other configuration functions, the minimum operating temperature is -40°C.

Table 65: Global Clock Input to Output Delay With DCM in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in Source-Synchronous Mode.							
T <sub>ICKOFDCM_0</sub>	Global Clock and OUTFF <i>with</i> DCM	XC6SLX4	5.03	N/A	7.21	8.05	ns
		XC6SLX9	5.03	6.13	7.21	8.05	ns
		XC6SLX16	5.08	5.51	6.44	7.96	ns
		XC6SLX25	4.81	5.13	5.69	7.94	ns
		XC6SLX25T	4.81	5.13	5.69	N/A	ns
		XC6SLX45	5.26	5.69	6.63	7.92	ns
		XC6SLX45T	5.26	5.69	6.63	N/A	ns
		XC6SLX75	4.77	5.18	5.88	7.95	ns
		XC6SLX75T	4.77	5.18	5.88	N/A	ns
		XC6SLX100	4.72	5.11	5.76	8.59	ns
		XC6SLX100T	4.76	5.11	5.76	N/A	ns
		XC6SLX150	4.90	5.30	5.93	7.93	ns
		XC6SLX150T	4.90	5.30	5.93	N/A	ns
		XA6SLX4	5.35	N/A	7.21	N/A	ns
		XA6SLX9	5.35	N/A	7.21	N/A	ns
		XA6SLX16	5.42	N/A	6.44	N/A	ns
		XA6SLX25	5.13	N/A	5.69	N/A	ns
		XA6SLX25T	5.13	N/A	5.79	N/A	ns
		XA6SLX45	5.58	N/A	6.63	N/A	ns
		XA6SLX45T	5.58	N/A	6.63	N/A	ns
		XA6SLX75	5.09	N/A	5.87	N/A	ns
		XA6SLX75T	5.09	N/A	5.87	N/A	ns
		XA6SLX100	N/A	N/A	6.44	N/A	ns
		XQ6SLX75	N/A	N/A	5.87	7.95	ns
XQ6SLX75T	5.09	N/A	5.87	N/A	ns		
XQ6SLX150	N/A	N/A	6.06	7.93	ns		
XQ6SLX150T	5.50	N/A	6.06	N/A	ns		

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 73: Global Clock Setup and Hold With DCM in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
<b>Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.<sup>(1)</sup></b>							
T <sub>PSDCMO</sub> / T <sub>PHDCMO</sub>	No Delay Global Clock and IFF <sup>(2)</sup> with DCM in Source-Synchronous Mode	XC6SLX4	0.71/0.65	N/A	0.72/1.22	1.58/1.18	ns
		XC6SLX9	0.71/0.69	0.71/1.19	0.72/1.36	1.58/1.18	ns
		XC6SLX16	0.86/0.52	0.92/0.57	1.04/0.60	1.02/1.06	ns
		XC6SLX25	0.84/0.58	0.90/0.59	1.01/0.59	1.58/1.07	ns
		XC6SLX25T	0.84/0.58	0.90/0.59	1.01/0.59	N/A	ns
		XC6SLX45	0.85/0.70	0.90/0.76	0.98/0.79	1.34/1.34	ns
		XC6SLX45T	0.85/0.70	0.90/0.76	0.98/0.79	N/A	ns
		XC6SLX75	1.00/0.62	1.06/0.63	1.15/0.63	1.65/1.46	ns
		XC6SLX75T	1.00/0.71	1.06/0.72	1.15/0.72	N/A	ns
		XC6SLX100	0.81/0.68	0.81/0.69	0.94/0.69	1.42/2.07	ns
		XC6SLX100T	0.81/0.68	0.81/0.69	0.94/0.69	N/A	ns
		XC6SLX150	0.68/0.98	0.69/0.99	0.79/0.99	1.45/1.60	ns
		XC6SLX150T	0.68/0.98	0.69/0.99	0.79/0.99	N/A	ns
		XA6SLX4	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX9	0.81/0.74	N/A	0.72/1.36	N/A	ns
		XA6SLX16	1.01/0.56	N/A	1.04/0.60	N/A	ns
		XA6SLX25	0.94/0.76	N/A	1.06/0.77	N/A	ns
		XA6SLX25T	0.94/0.76	N/A	1.14/0.77	N/A	ns
		XA6SLX45	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX45T	0.86/0.74	N/A	0.98/0.78	N/A	ns
		XA6SLX75	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XA6SLX100	N/A	N/A	1.37/0.75	N/A	ns
		XQ6SLX75	N/A	N/A	1.15/0.72	1.65/1.46	ns
		XQ6SLX75T	1.02/0.71	N/A	1.15/0.72	N/A	ns
		XQ6SLX150	N/A	N/A	0.79/1.15	1.45/1.60	ns
XQ6SLX150T	0.73/1.15	N/A	0.79/1.15	N/A	ns		

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.



Table 75: Global Clock Setup and Hold With PLL in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
<b>Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.<sup>(1)</sup></b>							
T <sub>PSPLL0</sub> / T <sub>PHPLL0</sub>	No Delay Global Clock and IFF <sup>(2)</sup> with PLL in Source-Synchronous Mode	XC6SLX4	0.47/1.08	N/A	0.47/1.60	1.15/1.68	ns
		XC6SLX9	0.47/1.08	0.47/1.35	0.47/1.60	1.15/1.68	ns
		XC6SLX16	0.37/0.75	0.37/0.82	0.51/0.94	0.57/1.31	ns
		XC6SLX25	0.69/1.06	0.69/1.06	0.69/1.06	1.86/1.67	ns
		XC6SLX25T	0.69/1.06	0.69/1.06	0.69/1.06	N/A	ns
		XC6SLX45	0.57/1.05	0.65/1.10	0.65/1.18	1.02/1.65	ns
		XC6SLX45T	0.57/1.06	0.65/1.10	0.65/1.18	N/A	ns
		XC6SLX75	0.86/1.04	0.87/1.04	0.90/1.04	1.34/1.55	ns
		XC6SLX75T	0.86/1.04	0.87/1.04	0.90/1.04	N/A	ns
		XC6SLX100	0.53/1.13	0.54/1.13	0.55/1.13	0.89/2.39	ns
		XC6SLX100T	0.53/1.13	0.54/1.13	0.55/1.13	N/A	ns
		XC6SLX150	0.50/1.31	0.51/1.31	0.52/1.31	1.02/1.72	ns
		XC6SLX150T	0.50/1.31	0.51/1.31	0.52/1.31	N/A	ns
		XA6SLX4	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX9	0.71/0.93	N/A	0.62/1.47	N/A	ns
		XA6SLX16	0.92/0.69	N/A	0.63/0.82	N/A	ns
		XA6SLX25	0.99/0.94	N/A	0.96/0.94	N/A	ns
		XA6SLX25T	0.99/0.94	N/A	1.04/0.94	N/A	ns
		XA6SLX45	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX45T	0.63/1.02	N/A	0.72/1.05	N/A	ns
		XA6SLX75	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns
		XA6SLX100	N/A	N/A	1.25/0.96	N/A	ns
		XQ6SLX75	N/A	N/A	1.02/0.89	1.34/1.55	ns
XQ6SLX75T	0.88/0.89	N/A	1.02/0.89	N/A	ns		
XQ6SLX150	N/A	N/A	0.63/1.19	1.02/1.72	ns		
XQ6SLX150T	0.60/1.19	N/A	0.63/1.19	N/A	ns		

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 79: Package Skew (Cont'd)

Symbol	Description	Device	Package <sup>(2)</sup>	Value	Units
T <sub>PKGSKEW</sub>	Package Skew <sup>(1)</sup>	LX45	CSG324	70	ps
			CS(G)484	99	ps
			FG(G)484	109	ps
			FG(G)676	138	ps
		LX45T	CSG324	75	ps
			CS(G)484	100	ps
			FG(G)484	95	ps
		LX75	CS(G)484	101	ps
			FG(G)484	107	ps
		LX75T	FG(G)676	161	ps
			CS(G)484	107	ps
			FG(G)484	110	ps
		LX100	FG(G)676	134	ps
			CS(G)484	95	ps
			FG(G)484	155	ps
		LX100T	FG(G)676	144	ps
			CS(G)484	88	ps
			FG(G)484	111	ps
			FG(G)676	147	ps
		LX150	FG(G)900	134	ps
			CS(G)484	84	ps
			FG(G)484	103	ps
			FG(G)676	115	ps
		LX150T	FG(G)900	121	ps
CS(G)484	83		ps		
FG(G)484	88		ps		
FG(G)676	141		ps		
			FG(G)900	120	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from Pad to Ball.
2. Some of the devices are available in both Pb and Pb-free (additional G) packages as standard ordering options. See [DS160: Spartan-6 Family Overview](#) for more information.

Table 80: Sample Window

Symbol	Description	Device <sup>(1)</sup>	Speed Grade				Units
			-3	-3N	-2	-1L	
T <sub>SAMP</sub>	Sampling Error at Receiver Pins <sup>(2)</sup>	All	510	510	530	740	ps
T <sub>SAMP_BUFIO2</sub>	Sampling Error at Receiver Pins using BUFIO2 <sup>(3)</sup>	All	430	430	450	590	ps

Notes:

1. LXT devices are not available with a -1L speed grade.
2. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
  - CLK0 DCM jitter
  - DCM accuracy (phase offset)
  - DCM phase shift resolution
 These measurements do not include package or clock tree skew.
3. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO2 clock network and IODELAY2 to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 81: Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out Using BUFIO2 (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
<b>Pin-to-Pin Clock-to-Out Using BUFIO2</b>							
T <sub>ICKOFCS</sub>	OFF clock-to-out using BUFIO2 clock	XC6SLX4	5.51	N/A	6.95	8.45	ns
		XC6SLX9	5.51	5.89	6.95	8.45	ns
		XC6SLX16	5.31	5.70	6.67	8.21	ns
		XC6SLX25	5.53	6.00	7.02	8.72	ns
		XC6SLX25T	5.53	6.00	7.02	N/A	ns
		XC6SLX45	5.76	6.18	7.22	8.77	ns
		XC6SLX45T	5.76	6.18	7.22	N/A	ns
		XC6SLX75	5.94	6.46	7.57	9.72	ns
		XC6SLX75T	5.94	6.46	7.57	N/A	ns
		XC6SLX100	6.09	6.53	7.60	9.66	ns
		XC6SLX100T	6.09	6.53	7.60	N/A	ns
		XC6SLX150	6.29	6.69	7.81	9.94	ns
		XC6SLX150T	6.29	6.69	7.81	N/A	ns
		XA6SLX4	5.83	N/A	6.95	N/A	ns
		XA6SLX9	5.83	N/A	6.95	N/A	ns
		XA6SLX16	5.65	N/A	6.68	N/A	ns
		XA6SLX25	5.85	N/A	7.03	N/A	ns
		XA6SLX25T	5.85	N/A	7.03	N/A	ns
		XA6SLX45	6.07	N/A	7.25	N/A	ns
		XA6SLX45T	6.07	N/A	7.25	N/A	ns
		XA6SLX75	6.26	N/A	7.57	N/A	ns
		XA6SLX75T	6.26	N/A	7.57	N/A	ns
		XA6SLX100	N/A	N/A	7.48	N/A	ns
		XQ6SLX75	N/A	N/A	7.57	9.72	ns
		XQ6SLX75T	6.26	N/A	7.57	N/A	ns
		XQ6SLX150	N/A	N/A	7.81	9.94	ns
XQ6SLX150T	6.62	N/A	7.81	N/A	ns		

## Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
06/24/09	1.0	Initial Xilinx release.
08/26/09	1.1	Added $V_{FS}$ to <a href="#">Table 1</a> and <a href="#">Table 2</a> . Added $R_{FUSE}$ to <a href="#">Table 2</a> . Added XC6SLX75 and XC6SLX75T to $V_{BATT}$ and $I_{BATT}$ in <a href="#">Table 1</a> , <a href="#">Table 2</a> , and <a href="#">Table 4</a> . Corrected the quiescent supply current for the XC6SLX4 in <a href="#">Table 5</a> . Updated <a href="#">Table 11</a> . Removed $DV_{PPIN}$ from <a href="#">Figure 2</a> . Removed $F_{PCIECORE}$ from <a href="#">Table 24</a> and added values to $F_{PCIEUSER}$ . Added more networking applications to <a href="#">Table 25</a> . Updated values for $T_{SUSPENDLOW\_AWAKE}$ , $T_{SUSPEND\_ENABLE}$ , and $T_{SCP\_AWAKE}$ in <a href="#">Table 46</a> . Numerous changes to <a href="#">Table 47</a> , <a href="#">page 54</a> including the addition of new values to various specifications, revising the $T_{SMCKCSO}$ description, and changing the units of $T_{POR}$ . Also, removed <i>Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK</i> section from <a href="#">Table 47</a> and updated all the notes. In <a href="#">Table 52</a> , added to $F_{INMAX}$ , revised $F_{OUTMAX}$ , and removed PLL Maximum Output Frequency for BUFIO2. Revised values for DCM_DELAY_STEP in <a href="#">Table 54</a> . Updated CLKIN_FREQ_FX values in <a href="#">Table 55</a> .
01/04/10	1.2	Added -4 speed grade to entire document. Updated speed specification of -4, -3, -2 speed grades to version 1.03. Added -1L speed grade numbers per speed specification 1.00. Updated $T_{SOL}$ in <a href="#">Table 1</a> . Added -1L rows for LVCMOS12, LVCMOS15, and LVCMOS18 in <a href="#">Table 9</a> . Revised much of the detail in <a href="#">GTP Transceiver Specifications</a> in <a href="#">Table 12</a> through <a href="#">Table 23</a> . Added -2 data to <a href="#">Table 25</a> . Updated $F_{MAX}$ in <a href="#">Table 44</a> . Updated descriptions for $T_{DNACLKL}$ and $T_{DNACLKH}$ in <a href="#">Table 45</a> and revised values for all parameters. Removed $T_{INITADDR}$ from <a href="#">Table 47</a> and added new data. Updated values in <a href="#">Table 48</a> through <a href="#">Table 62</a> . Added <a href="#">Table 51</a> (BUFPLL) and <a href="#">Table 57</a> (DCM_CLKGEN). Removed $T_{LOCKMAX}$ note from <a href="#">Table 52</a> . Updated note 3 in <a href="#">Table 53</a> . In <a href="#">Table 79</a> : removed XC6SLX75CSG324 and XC6SLX75TCSG324; added XC6SLX75FG(G)484 and XC6SLX75FG(G)484.
02/22/10	1.3	Production release of XC6SLX16 -2 speed grade devices. The changes to <a href="#">Table 26</a> and <a href="#">Table 27</a> includes updating this data sheet to the data in ISE v11.5 software with speed specification v1.06. Updated maximum of $V_{IN}$ and $V_{TS}$ and note 2 in <a href="#">Table 1</a> . In <a href="#">Table 2</a> , changed $V_{IN}$ , added $I_{IN}$ and note 5, revised notes 1, 6, and 7, and added note 8 to $R_{FUSE}$ . In <a href="#">Table 4</a> , removed previous note 1 and added data to $I_{RPU}$ , $I_{RPD}$ , and $I_{BATT}$ , changed $C_{IN}$ , added $R_{DT}$ and $R_{IN\_TERM}$ , and added note 2 and 3. Updated $V_{CCO2}$ in <a href="#">Table 6</a> . Added <a href="#">Table 7</a> and <a href="#">Table 8</a> . Removed PCI66_3 from <a href="#">Table 9</a> . Updated PCI33_3 and I2C in <a href="#">Table 9</a> . Updated the description of <a href="#">Table 11</a> . Completely updated <a href="#">Table 25</a> . Updated <a href="#">Table 28</a> including adding values for PCI33_3. Updated $V_{REF}$ value for HSTL_III_18 in <a href="#">Table 31</a> . Updates missing $V_{REF}$ values in <a href="#">Table 32</a> . Added <a href="#">Simultaneously Switching Outputs</a> , <a href="#">page 36</a> . Removed $T_{GSRQ}$ and $T_{RPW}$ from <a href="#">Table 35</a> and <a href="#">Table 36</a> . Also removed $T_{DOQ}$ from <a href="#">Table 36</a> . Removed $T_{ISDO\_DO}$ and note 1 from <a href="#">Table 37</a> . Removed $T_{OSCK\_S}$ and combinatorial section from <a href="#">Table 38</a> . In <a href="#">Table 39</a> , removed $T_{IODDO\_T}$ and added new tap parameters and note 2. In <a href="#">Table 40</a> , <a href="#">Table 41</a> , and <a href="#">Table 42</a> , made typographical edits and removed notes. Removed clock CLK section in <a href="#">Table 41</a> . Removed clock CLK section and $T_{REG\_MUX}$ and $T_{REG\_M31}$ in <a href="#">Table 42</a> . Added block RAM $F_{MAX}$ values to <a href="#">Table 43</a> . Updated values and added note 2 to <a href="#">Table 45</a> . Added values to <a href="#">Table 46</a> and removed note 1. Numerous changes to <a href="#">Table 47</a> . Completely updated <a href="#">Table 57</a> . Revised data in <a href="#">Table 62</a> . Removed note 3 from <a href="#">Table 71</a> . Added values to <a href="#">Table 79</a> . Added data to <a href="#">Table 80</a> and <a href="#">Table 81</a> .
03/10/10	1.4	Production release of XC6SLX45 -2 speed grade devices, which includes changes to <a href="#">Table 26</a> and <a href="#">Table 27</a> updating this data sheet to the data in ISE v11.5 software with speed specification v1.07. Fixed $R_{IN\_TERM}$ description in <a href="#">Table 4</a> . Added PCI66_3 to <a href="#">Table 7</a> and replaced note 1. Corrected note 1 and the V, Max for TMDS_33 in <a href="#">Table 8</a> . In <a href="#">Table 10</a> , added note 1 to LVPECL_33 and TMDS_33. Also updated specifications for TMDS_33. Updated the <a href="#">GTP Transceiver Specifications</a> section including adding values to <a href="#">Table 16</a> , <a href="#">Table 17</a> , and <a href="#">Table 20</a> through <a href="#">Table 23</a> . Added PCI66_3 back into <a href="#">Table 9</a> , <a href="#">Table 28</a> , <a href="#">Table 31</a> , <a href="#">Table 32</a> , and <a href="#">Table 34</a> . Updated note 3 on <a href="#">Table 32</a> . In <a href="#">Table 34</a> , corrected some typographical errors and fixed SSO limits for bank1/3 in FG(G)484 package. Corrected $T_{OSCKC\_OCE}$ in <a href="#">Table 38</a> . In <a href="#">Table 57</a> , updated CLKFX_FREEZE_VAR and CLKFX_FREEZE_TEMP_SLOPE and added typical values to $T_{CENTER\_LOW\_SPREAD}$ and $T_{CENTER\_HIGH\_SPREAD}$ . Updated and added values to <a href="#">Table 63</a> through <a href="#">Table 78</a> , and <a href="#">Table 81</a> . In <a href="#">Table 79</a> , revised the XC6SLX16-CSG324 and the XC6SLX45-CSG484 and FG(G)484 values.

Date	Version	Description of Revisions
06/14/10	1.5	<p>In <a href="#">Table 2</a>, added note 5 and added temperature range to <math>V_{FS}</math> and <math>R_{FUSE}</math>. Removed speed grade delineation, revised <math>I_{RPD}</math> description, and updated note 2 in <a href="#">Table 4</a>. Added note 2 to <a href="#">Table 7</a>. Added DIFF_MOBILE_DDR to <a href="#">Table 8</a> and <a href="#">Table 10</a>. Added note 4 to <a href="#">Table 15</a>. Changed minimum <math>DV_{PPIN}</math> in <a href="#">Table 16</a>. Updated <math>F_{GTPDRPCLK}</math> in <a href="#">Table 19</a>. Increased maximum <math>T_{LLSKEW}</math> in <a href="#">Table 22</a>. Updated descriptions and added data to <a href="#">Table 23</a>. Removed note 1 and added new data to the Networking Applications section in <a href="#">Table 25</a>. Updated <a href="#">Table 26</a> and <a href="#">Table 27</a> to the data in ISE v12.1 software with speed specification v1.08. In <a href="#">Table 28</a>, added DIFF_MOBILE_DDR and updated -4 speed grade data. Updated the maximum I/O pairs per bank in <a href="#">Table 33</a>. Updated note 2 on <a href="#">Table 39</a>. Revised the <math>F_{MAX}</math> in <a href="#">Table 44</a>. In <a href="#">Table 47</a>, updated description for <math>T_{SMCKCSO}</math>, revised values for <math>T_{POR}</math> and added Min value, added <math>T_{BPIICCK}</math> and <math>T_{SPIICCK}</math>. Also in <a href="#">Table 47</a>, added device dependencies to <math>F_{SMCCK}</math> and <math>F_{RBCKK}</math>. Updated and added data to <a href="#">Table 63</a> through <a href="#">Table 78</a>, and <a href="#">Table 81</a>. In <a href="#">Table 79</a>, added data on the XC6SLX45-FG(G)676 and revised the XC6SLX45T and XC6SLX150T values.</p> <p>The following changes to this specification are addressed in the product change notice <a href="#">XCN10024</a>, <i>MCB Performance and JTAG Revision Code for Spartan-6 LX16 and LX45 FPGAs</i>. In <a href="#">Table 2</a>, revised the <math>V_{CCINT}</math> to add the memory controller block extended performance specifications. In <a href="#">Table 25</a>, changed the standard specifications and added extended performance specifications for the memory controller block and note 2. Added note 4 and updated values in <a href="#">Table 34</a>.</p>
06/24/10	1.6	<p>Production release of XC6SLX45T (-2 and -3 speed grades), XC6SLX16 and XC6SLX45 (-3 speed grade) devices which includes changes to <a href="#">Table 26</a> and <a href="#">Table 27</a> (ISE v12.1 software with speed specification v1.08).</p> <p>Added the -3N speed grade, which designates Spartan-6 devices that do not support MCB functionality. This includes changes to <a href="#">Table 2</a> (note 2), <a href="#">Table 25</a> (note 4), and <a href="#">Switching Characteristics</a> (<a href="#">Table 26</a>).</p> <p>Updated <a href="#">Simultaneously Switching Outputs</a> discussion. Added -3 speed grade values for <math>T_{TAP}</math> and <math>F_{MINCAL}</math> values in <a href="#">Table 39</a>. In <a href="#">Table 40</a>, updated <math>T_{RPW}</math> (-2 and -3 speed grade) values and <math>F_{TOG}</math> (-3 speed grade) values. In <a href="#">Table 48</a>, updated <math>T_{GIO}</math> (-2 and -3 speed grade) values. Updated -3 values in spread spectrum section of <a href="#">Table 57</a>.</p>
07/16/10	1.7	<p>Production release of specific devices listed in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v12.2 software with speed specification v1.11. Added note 4 advising designers of the patch which contains v1.11. Also updated the -1L speed specification to v1.04. Updated numerous -4 and -1L values. Added -4 <math>T_{TAP}</math> values and <math>F_{MINCAL}</math> to <a href="#">Table 39</a>. Revised <math>T_{CINCK}/T_{CKCIN}</math> in <a href="#">Table 40</a>. In <a href="#">Table 41</a>, revised <math>T_{SHCKO}</math>. In <a href="#">Table 42</a>, revised <math>T_{REG}</math>. Added new -1L values to <a href="#">Table 47</a>. Added and updated values in <a href="#">Table 79</a>.</p>
07/26/10	1.8	<p>Production release of XC6SLX25, XC6SLX25T, XC6SLX100 and XC6SLX100T in the specific speed grades listed in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v12.2 software with speed specification v1.11. Added note 7 to <a href="#">Table 2</a> and moved <math>V_{FS}</math> and <math>R_{FUSE}</math> to a new <a href="#">Table 3</a>. Added <math>I_{HS}</math> and note 4 to <a href="#">Table 4</a>. Added note 1 to <a href="#">Table 28</a>. Added and updated SSO limits per <math>V_{CC0}/GND</math> pairs in <a href="#">Table 34</a>. Added note 3 to <a href="#">Table 47</a>. In <a href="#">Table 54</a>, removed -1L specifications for CLKOUT_PER_JITT_DV1/2 and revised CLKIN_CLKFB_PHASE and CLKOUT_PHASE_DLL values. Updated note 3 in both <a href="#">Table 56</a> and <a href="#">Table 57</a>.</p>
08/23/10	1.9	<p>Updated values for <math>F_{GTPRANGE1}</math>, <math>F_{GTPRANGE2}</math>, and <math>F_{GPLLMIN}</math> in <a href="#">Table 18</a>. Revised -3 and -4 values in <a href="#">Table 21</a>. Removed the -1L speed grade readback support restriction and note 3 in <a href="#">Table 47</a>.</p>
11/05/10	1.10	<p>Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in <a href="#">Table 26</a> and <a href="#">Table 27</a> using ISE v12.3 software with speed specification v1.12 for the -2 speed grade available in the 12.3 <i>Speed Files Patch</i>. Added note 3 advising designers of the patch which contains v1.12.</p> <p>In <a href="#">Table 2</a>, added note 4. In <a href="#">Table 4</a>, added note 2. In <a href="#">Table 10</a>, added notes 2 and 3. In <a href="#">Table 44</a>, added note 2. In <a href="#">Table 47</a>, updated symbol for <math>T_{SMWCKK}/T_{SMCKKW}</math>, changed -1L values for <math>T_{USERCCLKH}</math> and <math>T_{USERCCLKL}</math>, and added and revised the modes for <math>F_{MCKK}</math> and <math>F_{SMCKK}</math>. In <a href="#">Table 53</a>, redefined and expanded description for CLKIN_FREQ_DLL and rewrote note 3. Updated title of <a href="#">Table 58</a>. Also in <a href="#">Table 78</a>, revised <math>T_{DCD\_CLK}</math> for XC6SLX150 and XC6SLX150T. Changed description of <math>T_{PSFD}/T_{PHFD}</math> in <a href="#">Table 71</a>.</p> <p>For the -1L speed grade, updated data sheet to ISE 12.3 software with speed specification v1.05 which revised the values in the following tables: <a href="#">Table 25</a>, <a href="#">Table 28</a>, <a href="#">Table 35</a>, <a href="#">Table 36</a>, <a href="#">Table 37</a>, <a href="#">Table 40</a> through <a href="#">Table 43</a>, <a href="#">Table 48</a> through <a href="#">Table 56</a>, <a href="#">Table 62</a> through <a href="#">Table 78</a>, <a href="#">Table 80</a>, and <a href="#">Table 81</a>. Updated <a href="#">Notice of Disclaimer</a>.</p>