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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 715 |
| Number of Logic Elements/Cells | 9152 |
| Total RAM Bits | 589824 |
| Number of I/O | 102 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc6slx9-l1tqg144c |

*Table 4:* **DC Characteristics Over Recommended Operating Conditions**

| Symbol | Description | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{DRINT}$ | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) | | 0.8 | – | – | V |
| $V_{DRAUX}$ | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) | | 2.0 | – | – | V |
| $I_{REF}$ | $V_{REF}$ leakage current per pin for commercial (C) and industrial (I) devices | | –10 | – | 10 | µA |
| | $V_{REF}$ leakage current per pin for expanded (Q) devices | | –15 | – | 15 | µA |
| $I_L$ | Input or output leakage current per pin (sample-tested) for commercial (C) and industrial (I) devices | | –10 | – | 10 | µA |
| | Input or output leakage current per pin (sample-tested) for expanded (Q) devices | | –15 | – | 15 | µA |
| $I_{HS}$ | Leakage current on pins during hot socketing with FPGA unpowered | All pins except PROGRAM_B, DONE, and JTAG pins when HSWAPEN = 1 | –20 | – | 20 | µA |
| | | PROGRAM_B, DONE, and JTAG pins, or other pins when HSWAPEN = 0 | $I_{HS} + I_{RPU}$ | | | µA |
| $C_{IN}$[1] | Die input capacitance at the pad | | – | – | 10 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V or $V_{CCAUX}$ = 3.3V | | 200 | – | 500 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V or $V_{CCAUX}$ = 2.5V | | 120 | – | 350 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | | 60 | – | 200 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | | 40 | – | 150 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | | 12 | – | 100 | µA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{IN}$ = $V_{CCO}$, $V_{CCAUX}$ = 3.3V | | 200 | – | 550 | µA |
| | Pad pull-down (when selected) @ $V_{IN}$ = $V_{CCO}$, $V_{CCAUX}$ = 2.5V | | 140 | – | 400 | µA |
| $I_{BATT}$[2] | Battery supply current | | – | – | 150 | nA |
| $R_{DT}$[3] | Resistance of optional input differential termination circuit, $V_{CCAUX}$ = 3.3V | | – | 100 | – | Ω |
| $R_{IN\_TERM}$[5] | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_25) for commercial (C) and industrial (I) devices | | 23 | 25 | 55 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_25) for expanded (Q) devices | | 20 | 25 | 55 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_50) for commercial (C) and industrial (I) devices | | 39 | 50 | 72 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_50) for expanded (Q) devices | | 32 | 50 | 74 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_75) for commercial (C) and industrial (I) devices | | 56 | 75 | 109 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$ (UNTUNED_SPLIT_75) for expanded (Q) devices | | 47 | 75 | 115 | Ω |
| $R_{OUT\_TERM}$ | Thevenin equivalent resistance of programmable output termination (UNTUNED_25) | | 11 | 25 | 52 | Ω |
| | Thevenin equivalent resistance of programmable output termination (UNTUNED_50) | | 21 | 50 | 96 | Ω |
| | Thevenin equivalent resistance of programmable output termination (UNTUNED_75) | | 29 | 75 | 145 | Ω |

**Notes:**

1. The $C_{IN}$ measurement represents the die capacitance at the pad, not including the package.
2. Maximum value specified for worst case process at 25°C. LX75, LX75T, LX100, LX100T, LX150, and LX150T only.
3. Refer to IBIS models for $R_{DT}$ variation and for values at $V_{CCAUX}$ = 2.5V. IBIS values for $R_{DT}$ are valid for all temperature ranges.
4. $V_{CCO2}$ is not required for data retention. The minimum $V_{CCO2}$ for power-on reset and configuration is 1.65V.
5. Termination resistance to a $V_{CCO}$/2 level.

*Table 10:* **Differential I/O Standard DC Input and Output Levels**

| I/O Standard | $V_{ID}$ | | $V_{ICM}$ | | $V_{OD}$ | | $V_{OCM}$ | | $V_{OH}$ | $V_{OL}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| | mV, Min | mV, Max | V, Min | V, Max | mV, Min | mV, Max | V, Min | V, Max | V, Min | V, Max |
| LVDS_33[2][3] | 100 | 600 | 0.3 | 2.35 | 247 | 454 | 1.125 | 1.375 | – | – |
| LVDS_25[2][3] | 100 | 600 | 0.3 | 2.35 | 247 | 454 | 1.125 | 1.375 | – | – |
| BLVDS_25[2][3] | 100 | – | 0.3 | 2.35 | 240 | 460 | Typical 50% $V_{CCO}$ | | – | – |
| MINI_LVDS_33 | 200 | 600 | 0.3 | 1.95 | 300 | 600 | 1.0 | 1.4 | – | – |
| MINI_LVDS_25 | 200 | 600 | 0.3 | 1.95 | 300 | 600 | 1.0 | 1.4 | – | – |
| LVPECL_33[2][3] | 100 | 1000 | 0.3 | 2.8[1] | Inputs only | | | | | |
| LVPECL_25[2][3] | 100 | 1000 | 0.3 | 1.95 | Inputs only | | | | | |
| RSDS_33[2][3] | 100 | – | 0.3 | 1.5 | 100 | 400 | 1.0 | 1.4 | – | – |
| RSDS_25[2][3] | 100 | – | 0.3 | 1.5 | 100 | 400 | 1.0 | 1.4 | – | – |
| TMDS_33 | 150 | 1200 | 2.7 | 3.23[1] | 400 | 800 | $V_{CCO}$ – 0.405 | $V_{CCO}$ – 0.190 | – | – |
| PPDS_33[2][3] | 100 | 400 | 0.2 | 2.3 | 100 | 400 | 0.5 | 1.4 | – | – |
| PPDS_25[2][3] | 100 | 400 | 0.2 | 2.3 | 100 | 400 | 0.5 | 1.4 | – | – |
| DISPLAY_PORT | 190 | 1260 | 0.3 | 2.35 | – | – | Typical 50% $V_{CCO}$ | | – | – |
| DIFF_MOBILE_DDR | 100 | – | 0.78 | 1.02 | – | – | – | – | 90% $V_{CCO}$ | 10% $V_{CCO}$ |
| DIFF_HSTL_I | 100 | – | 0.68 | 0.9 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_HSTL_II | 100 | – | 0.68 | 0.9 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_HSTL_III | 100 | – | 0.68 | 0.9 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_HSTL_I_18 | 100 | – | 0.8 | 1.1 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_HSTL_II_18 | 100 | – | 0.8 | 1.1 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_HSTL_III_18 | 100 | – | 0.8 | 1.1 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_SSTL3_I | 100 | – | 1.0 | 1.9 | – | – | – | – | $V_{TT}$ + 0.6 | $V_{TT}$ – 0.6 |
| DIFF_SSTL3_II | 100 | – | 1.0 | 1.9 | – | – | – | – | $V_{TT}$ + 0.8 | $V_{TT}$ – 0.8 |
| DIFF_SSTL2_I | 100 | – | 1.0 | 1.5 | – | – | – | – | $V_{TT}$ + 0.61 | $V_{TT}$ – 0.61 |
| DIFF_SSTL2_II | 100 | – | 1.0 | 1.5 | – | – | – | – | $V_{TT}$ + 0.81 | $V_{TT}$ – 0.81 |
| DIFF_SSTL18_I | 100 | – | 0.7 | 1.1 | – | – | – | – | $V_{TT}$ + 0.47 | $V_{TT}$ – 0.47 |
| DIFF_SSTL18_II | 100 | – | 0.7 | 1.1 | – | – | – | – | $V_{TT}$ + 0.6 | $V_{TT}$ – 0.6 |
| DIFF_SSTL15_II | 100 | – | 0.55 | 0.95 | – | – | – | – | $V_{TT}$ + 0.4 | $V_{TT}$ – 0.4 |

**Notes:**

1. LVPECL_33 and TMDS_33 maximum $V_{ICM}$ is the lower of V (maximum) or $V_{CCAUX}$ – ($V_{ID}$/2)
2. When $V_{CCAUX}$ = 3.3V, the DCD can be higher than 5% for $V_{ICM}$ < 0.7V when using these I/O standards: LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, LVPECL_33, RSDS_25, RSDS_33, PPDS_25, and PPDS_33.
3. The -1L devices require $V_{CCAUX}$ = 2.5V when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.

*Table 14:* **GTP Transceiver Current Supply (per Lane)**

| Symbol | Description | Typ[1] | Max | Units |
|---|---|---|---|---|
| $I_{MGTAVCC}$ | GTP transceiver internal analog supply current | 40.4 | Note 2 | mA |
| $I_{MGTAVTTTX}$ | GTP transmitter termination supply current | 27.4 | | mA |
| $I_{MGTAVTTRX}$ | GTP receiver termination supply current | 13.6 | | mA |
| $I_{MGTAVCCPLL}$ | GTP transmitter and receiver PLL supply current | 28.7 | | mA |
| $R_{MGTRREF}$ | Precision reference resistor for internal calibration termination | 50.0 ± 1% tolerance | | Ω |

**Notes:**
1. Typical values are specified at nominal voltage, 25°C, with a 2.5 Gb/s line rate, with a shared PLL use mode.
2. Values for currents of other transceiver configurations and conditions can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

*Table 15:* **GTP Transceiver Quiescent Supply Current (per Lane)[1][2][3][4]**

| Symbol | Description | Typ[5] | Max | Units |
|---|---|---|---|---|
| $I_{MGTAVCCQ}$ | Quiescent MGTAVCC supply current | 1.7 | Note 2 | mA |
| $I_{MGTAVTTTXQ}$ | Quiescent MGTAVTTTX supply current | 0.1 | | mA |
| $I_{MGTAVTTRXQ}$ | Quiescent MGTAVTTRX supply current | 1.2 | | mA |
| $I_{MGTAVCCPLLQ}$ | Quiescent MGTAVCCPLL supply current | 1.0 | | mA |

**Notes:**
1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
3. GTP transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTP transceivers.
4. Does not include power-up MGTAVTTRCAL supply current during device configuration.
5. Typical values are specified at nominal voltage, 25°C.

# Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.20 for -3, -3N, and -2; and v1.08 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

### Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

The -1L speed grade refers to the lower-power Spartan-6 devices. The -3N speed grade refers to the Spartan-6 devices that do not support MCB functionality.

Table 26 correlates the current status of each Spartan-6 device on a per speed grade basis.

*Table 26:* **Spartan-6 Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC6SLX4[1] | | | -3, -2, -1L |
| XC6SLX9 | | | -3, -3N, -2, -1L |
| XC6SLX16 | | | -3, -3N, -2, -1L |
| XC6SLX25 | | | -3, -3N, -2, -1L |
| XC6SLX25T | | | -3, -3N, -2 |
| XC6SLX45 | | | -3, -3N, -2, -1L |
| XC6SLX45T | | | -3, -3N, -2 |
| XC6SLX75 | | | -3, -3N, -2, -1L |
| XC6SLX75T | | | -3, -3N, -2 |
| XC6SLX100 | | | -3, -3N, -2, -1L |
| XC6SLX100T | | | -3, -3N, -2 |
| XC6SLX150 | | | -3, -3N, -2, -1L |
| XC6SLX150T | | | -3, -3N, -2 |
| XA6SLX4 | | | -3, -2 |
| XA6SLX9 | | | -3, -2 |
| XA6SLX16 | | | -3, -2 |
| XA6SLX25 | | | -3, -2 |
| XA6SLX25T | | | -3, -2 |
| XA6SLX45 | | | -3, -2 |
| XA6SLX45T | | | -3, -2 |
| XA6SLX75 | | | -3, -2 |
| XA6SLX75T | | | -3, -2 |
| XA6SLX100 | | | -2 |
| XQ6SLX75 | | | -2, -1L |
| XQ6SLX75T | | | -3, -2 |
| XQ6SLX150 | | | -2, -1L |
| XQ6SLX150T | | | -3, -2 |

**Notes:**

1. The XC6SLX4 is not available in the -3N speed grade.

## Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-6 devices.

*Table 29:* **IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices[1] *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | $T_{IOOP}$ | | $T_{IOTP}$ | | Units |
|---|---|---|---|---|---|---|---|
| | Speed Grade | | Speed Grade | | Speed Grade | | |
| | -3 | -2 | -3 | -2 | -3 | -2 | |
| LVCMOS15, QUIETIO, 2 mA | 1.05 | 1.23 | 5.63 | 5.83 | 5.63 | 5.83 | ns |
| LVCMOS15, QUIETIO, 4 mA | 1.05 | 1.23 | 4.75 | 4.95 | 4.75 | 4.95 | ns |
| LVCMOS15, QUIETIO, 6 mA | 1.05 | 1.23 | 4.21 | 4.41 | 4.21 | 4.41 | ns |
| LVCMOS15, QUIETIO, 8 mA | 1.05 | 1.23 | 4.05 | 4.25 | 4.05 | 4.25 | ns |
| LVCMOS15, QUIETIO, 12 mA | 1.05 | 1.23 | 3.74 | 3.94 | 3.74 | 3.94 | ns |
| LVCMOS15, QUIETIO, 16 mA | 1.05 | 1.23 | 3.52 | 3.72 | 3.52 | 3.72 | ns |
| LVCMOS15, Slow, 2 mA | 1.05 | 1.23 | 4.32 | 4.52 | 4.32 | 4.52 | ns |
| LVCMOS15, Slow, 4 mA | 1.05 | 1.23 | 3.58 | 3.78 | 3.58 | 3.78 | ns |
| LVCMOS15, Slow, 6 mA | 1.05 | 1.23 | 2.45 | 2.65 | 2.45 | 2.65 | ns |
| LVCMOS15, Slow, 8 mA | 1.05 | 1.23 | 2.46 | 2.66 | 2.46 | 2.66 | ns |
| LVCMOS15, Slow, 12 mA | 1.05 | 1.23 | 2.17 | 2.37 | 2.17 | 2.37 | ns |
| LVCMOS15, Slow, 16 mA | 1.05 | 1.23 | 2.15 | 2.35 | 2.15 | 2.35 | ns |
| LVCMOS15, Fast, 2 mA | 1.05 | 1.23 | 3.43 | 3.63 | 3.43 | 3.63 | ns |
| LVCMOS15, Fast, 4 mA | 1.05 | 1.23 | 2.42 | 2.62 | 2.42 | 2.62 | ns |
| LVCMOS15, Fast, 6 mA | 1.05 | 1.23 | 1.92 | 2.12 | 1.92 | 2.12 | ns |
| LVCMOS15, Fast, 8 mA | 1.05 | 1.23 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVCMOS15, Fast, 12 mA | 1.05 | 1.23 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVCMOS15, Fast, 16 mA | 1.05 | 1.23 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVCMOS15_JEDEC, QUIETIO, 2 mA | 1.10 | 1.28 | 5.64 | 5.84 | 5.64 | 5.84 | ns |
| LVCMOS15_JEDEC, QUIETIO, 4 mA | 1.10 | 1.28 | 4.75 | 4.95 | 4.75 | 4.95 | ns |
| LVCMOS15_JEDEC, QUIETIO, 6 mA | 1.10 | 1.28 | 4.21 | 4.41 | 4.21 | 4.41 | ns |
| LVCMOS15_JEDEC, QUIETIO, 8 mA | 1.10 | 1.28 | 4.06 | 4.26 | 4.06 | 4.26 | ns |
| LVCMOS15_JEDEC, QUIETIO, 12 mA | 1.10 | 1.28 | 3.75 | 3.95 | 3.75 | 3.95 | ns |
| LVCMOS15_JEDEC, QUIETIO, 16 mA | 1.10 | 1.28 | 3.53 | 3.73 | 3.53 | 3.73 | ns |
| LVCMOS15_JEDEC, Slow, 2 mA | 1.10 | 1.28 | 4.32 | 4.52 | 4.32 | 4.52 | ns |
| LVCMOS15_JEDEC, Slow, 4 mA | 1.10 | 1.28 | 3.56 | 3.76 | 3.56 | 3.76 | ns |
| LVCMOS15_JEDEC, Slow, 6 mA | 1.10 | 1.28 | 2.44 | 2.64 | 2.44 | 2.64 | ns |
| LVCMOS15_JEDEC, Slow, 8 mA | 1.10 | 1.28 | 2.47 | 2.67 | 2.47 | 2.67 | ns |
| LVCMOS15_JEDEC, Slow, 12 mA | 1.10 | 1.28 | 2.15 | 2.35 | 2.15 | 2.35 | ns |
| LVCMOS15_JEDEC, Slow, 16 mA | 1.10 | 1.28 | 2.15 | 2.35 | 2.15 | 2.35 | ns |
| LVCMOS15_JEDEC, Fast, 2 mA | 1.10 | 1.28 | 3.43 | 3.63 | 3.43 | 3.63 | ns |
| LVCMOS15_JEDEC, Fast, 4 mA | 1.10 | 1.28 | 2.42 | 2.62 | 2.42 | 2.62 | ns |
| LVCMOS15_JEDEC, Fast, 6 mA | 1.10 | 1.28 | 1.92 | 2.12 | 1.92 | 2.12 | ns |
| LVCMOS15_JEDEC, Fast, 8 mA | 1.10 | 1.28 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVCMOS15_JEDEC, Fast, 12 mA | 1.10 | 1.28 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVCMOS15_JEDEC, Fast, 16 mA | 1.10 | 1.28 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVCMOS12, QUIETIO, 2 mA | 0.98 | 1.16 | 6.54 | 6.74 | 6.54 | 6.74 | ns |
| LVCMOS12, QUIETIO, 4 mA | 0.98 | 1.16 | 5.12 | 5.32 | 5.12 | 5.32 | ns |

*Table 33:* **Spartan-6 FPGA $V_{CCO}$/GND Pairs per Bank**

| Package | Devices | Description | Bank 0 | Bank 1 | Bank 2 | Bank 3 | Bank 4 | Bank 5 |
|---|---|---|---|---|---|---|---|---|
| TQG144 | LX | $V_{CCO}$/GND Pairs | 3 | 3 | 2 | 3 | N/A | N/A |
| | | Maximum I/O per Pair | 8 | 8 | 13 | 8 | N/A | N/A |
| CPG196 | LX | VCCO/GND Pairs | 4 | 6 | 4 | 6 | N/A | N/A |
| | | Maximum I/O per Pair | 6 | 4 | 7 | 4 | N/A | N/A |
| CSG225 | LX | $V_{CCO}$/GND Pairs | 4 | 4 | 4 | 4 | N/A | N/A |
| | | Maximum I/O per Pair | 10 | 10 | 9 | 10 | N/A | N/A |
| FT(G)256 | LX | $V_{CCO}$/GND Pairs | 5 | 6 | 4 | 5 | N/A | N/A |
| | | Maximum I/O per Pair | 8 | 9 | 9 | 10 | N/A | N/A |
| CSG324 | LX | $V_{CCO}$/GND Pairs | 6 | 6 | 6 | 6 | N/A | N/A |
| | | Maximum I/O per Pair | 10 | 9 | 10 | 9 | N/A | N/A |
| | LXT | $V_{CCO}$/GND Pairs | 4 | 6 | 6 | 6 | N/A | N/A |
| | | Maximum I/O per Pair | 4 | 9 | 10 | 9 | N/A | N/A |
| CS(G)484 | LX | $V_{CCO}$/GND Pairs | 8 | 13 | 8 | 13 | N/A | N/A |
| | | Maximum I/O per Pair | 7 | 8 | 7 | 8 | N/A | N/A |
| | LXT | $V_{CCO}$/GND Pairs | 7 | 12 | 8 | 13 | N/A | N/A |
| | | Maximum I/O per Pair | 5 | 8 | 6 | 8 | N/A | N/A |
| FG(G)484 | LX | $V_{CCO}$/GND Pairs | 10 | 10 | 11 | 11 | N/A | N/A |
| | | Maximum I/O per Pair | 6 | 8 | 9 | 8 | N/A | N/A |
| | LXT | $V_{CCO}$/GND Pairs | 6 | 10 | 11 | 10 | N/A | N/A |
| | | Maximum I/O per Pair | 7 | 8 | 7 | 8 | N/A | N/A |
| FG(G)676 | LX45 | $V_{CCO}$/GND Pairs | 12 | 15 | 10 | 16 | N/A | N/A |
| | | Maximum I/O per Pair | 3 | 7 | 8 | 7 | N/A | N/A |
| | LX75, LX100, LX150 | $V_{CCO}$/GND Pairs | 12 | 9 | 10 | 10 | 6 | 6 |
| | | Maximum I/O per Pair | 9 | 10 | 9 | 9 | 8 | 9 |
| | LXT | $V_{CCO}$/GND Pairs | 10 | 8 | 10 | 8 | 7 | 7 |
| | | Maximum I/O per Pair | 8 | 7 | 8 | 8 | 7 | 7 |
| FG(G)900 | LX | $V_{CCO}$/GND Pairs | 17 | 14 | 17 | 14 | 7 | 8 |
| | | Maximum I/O per Pair | 7 | 6 | 7 | 8 | 7 | 6 |
| | LXT | $V_{CCO}$/GND Pairs | 15 | 14 | 13 | 14 | 7 | 8 |
| | | Maximum I/O per Pair | 7 | 6 | 8 | 8 | 7 | 6 |

## Input Serializer/Deserializer Switching Characteristics

*Table 37:* **ISERDES2 Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| **Setup/Hold for Control Lines** | | | | | | |
| $T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$ | BITSLIP pin Setup/Hold with respect to CLKDIV | 0.16/ –0.09 | 0.20/ –0.09 | 0.31/ –0.09 | 0.34/ –0.14 | ns |
| $T_{ISCCK\_CE}$ / $T_{ISCKC\_CE}$ | CE pin Setup/Hold with respect to CLK | 0.71/ –0.47 | 0.71/ –0.42 | 0.97/ –0.42 | 1.39/ –0.71 | ns |
| **Setup/Hold for Data Lines** | | | | | | |
| $T_{ISDCK\_D}$ /$T_{ISCKD\_D}$ | D pin Setup/Hold with respect to CLK | 0.24/ –0.15 | 0.25/ –0.05 | 0.29/ –0.05 | 0.09/ –0.05 | ns |
| $T_{ISDCK\_DDLY}$ /$T_{ISCKD\_DDLY}$ | DDLY pin Setup/Hold with respect to CLK (using IODELAY2) | –0.25/ 0.30 | –0.25/ 0.42 | –0.25/ 0.56 | –0.54/ 0.67 | ns |
| $T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode | –0.03/ 0.04 | –0.03/ 0.16 | –0.03/ 0.18 | –0.05/ 0.12 | ns |
| $T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY2) | –0.40/ 0.48 | –0.40/ 0.53 | –0.40/ 0.71 | –0.71/ 0.86 | ns |
| **Sequential Delays** | | | | | | |
| $T_{ISCKO\_Q}$ | CLKDIV to out at Q pin | 1.30 | 1.44 | 2.02 | 2.22 | ns |
| $F_{CLKDIV}$ | CLKDIV maximum frequency | 270 | 262.5 | 250 | 125 | MHz |

## Output Serializer/Deserializer Switching Characteristics

*Table 38:* **OSERDES2 Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| **Setup/Hold** | | | | | | |
| $T_{OSDCK\_D}$/$T_{OSCKD\_D}$ | D input Setup/Hold with respect to CLKDIV | –0.03/ 1.02 | –0.03/ 1.17 | –0.03/ 1.27 | –0.02/ 0.23 | ns |
| $T_{OSDCK\_T}$/$T_{OSCKD\_T}$(1) | T input Setup/Hold with respect to CLK | –0.05/ 1.03 | –0.05/ 1.13 | –0.05/ 1.23 | –0.05/ 0.24 | ns |
| $T_{OSCCK\_OCE}$/$T_{OSCKC\_OCE}$ | OCE input Setup/Hold with respect to CLK | 0.12/ –0.03 | 0.15/ –0.03 | 0.24/ –0.03 | 0.28/ –0.17 | ns |
| $T_{OSCCK\_TCE}$/$T_{OSCKC\_TCE}$ | TCE input Setup/Hold with respect to CLK | 0.14/ –0.08 | 0.17/ –0.08 | 0.27/ –0.08 | 0.31/ –0.16 | ns |
| **Sequential Delays** | | | | | | |
| $T_{OSCKO\_OQ}$ | Clock to out from CLK to OQ | 0.94 | 1.11 | 1.51 | 1.89 | ns |
| $T_{OSCKO\_TQ}$ | Clock to out from CLK to TQ | 0.94 | 1.11 | 1.51 | 1.91 | ns |
| $F_{CLKDIV}$ | CLKDIV maximum frequency | 270 | 262.5 | 250 | 125 | MHz |

**Notes:**
1. $T_{OSDCK\_T2}$/$T_{OSCKD\_T2}$ (T input setup/hold with respect to CLKDIV) are reported as $T_{OSDCK\_T}$/$T_{OSCKD\_T}$ in TRACE report.

## CLB Switching Characteristics (SLICEM Only)

*Table 40:* **CLB Switching Characteristics (SLICEM Only)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| **Combinatorial Delays** | | | | | | |
| $T_{ILO}$ | An – Dn LUT inputs to A to D outputs | 0.21 | 0.26 | 0.26 | 0.46 | ns, Max |
| | An – Dn LUT inputs through F7AMUX/F7BMUX to AMUX/CMUX output | 0.37 | 0.43 | 0.43 | 0.77 | ns, Max |
| $T_{OPAB}$ | An – Dn LUT inputs through F7AMUX or F7BMUX and F8MUX to BMUX output | 0.37 | 0.46 | 0.46 | 0.84 | ns, Max |
| $T_{ITO}$ | An – Dn LUT inputs through latch to AQ – DQ outputs | 0.82 | 0.95 | 0.95 | 1.64 | ns, Max |
| $T_{TITO\_LOGIC}$ | An – Dn LUT inputs to AQ – DQ outputs (latch as logic) | 0.82 | 0.95 | 0.95 | 1.64 | ns, Max |
| $T_{OPCYA}$ | An LUT inputs to COUT output | 0.38 | 0.48 | 0.48 | 0.69 | ns, Max |
| $T_{OPCYB}$ | Bn LUT inputs to COUT output | 0.38 | 0.49 | 0.49 | 0.71 | ns, Max |
| $T_{OPCYC}$ | Cn LUT inputs to COUT output | 0.28 | 0.33 | 0.33 | 0.55 | ns, Max |
| $T_{OPCYD}$ | Dn LUT inputs to COUT output | 0.28 | 0.35 | 0.35 | 0.52 | ns, Max |
| $T_{AXCY}$ | AX input to COUT output | 0.21 | 0.26 | 0.26 | 0.36 | ns, Max |
| $T_{BXCY}$ | BX input to COUT output | 0.13 | 0.16 | 0.16 | 0.18 | ns, Max |
| $T_{CXCY}$ | CX input to COUT output | 0.10 | 0.12 | 0.12 | 0.09 | ns, Max |
| $T_{DXCY}$ | DX input to COUT output | 0.09 | 0.11 | 0.11 | 0.09 | ns, Max |
| $T_{BYP}$ | CIN input to COUT output | 0.08 | 0.10 | 0.10 | 0.06 | ns, Max |
| $T_{CINA}$ | CIN input to AMUX output | 0.21 | 0.22 | 0.22 | 0.47 | ns, Max |
| $T_{CINB}$ | CIN input to BMUX output | 0.30 | 0.31 | 0.31 | 0.57 | ns, Max |
| $T_{CINC}$ | CIN input to CMUX output | 0.29 | 0.31 | 0.31 | 0.58 | ns, Max |
| $T_{CIND}$ | CIN input to DMUX output | 0.31 | 0.32 | 0.32 | 0.68 | ns, Max |
| **Sequential Delays** | | | | | | |
| $T_{CKO}$ | Clock to AQ – DQ outputs | 0.45 | 0.53 | 0.53 | 0.74 | ns, Max |
| **Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK** | | | | | | |
| $T_{DICK}/T_{CKDI}$ | AX – DX input to CLK on A – D flip-flops | 0.42/ 0.28 | 0.47/ 0.39 | 0.47/ 0.39 | 0.90/ 0.56 | ns, Min |
| $T_{CECK}/T_{CKCE}$ | CE input to CLK on A – D flip-flops | 0.31/ –0.07 | 0.37/ –0.07 | 0.37/ –0.07 | 0.59/ –0.27 | ns, Min |
| $T_{SRCK}/T_{CKSR}$ | SR input to CLK on A – D flip-flops for XC devices | 0.41/ 0.02 | 0.42/ 0.02 | 0.42/ 0.02 | 0.68/ –0.29 | ns, Min |
| | SR input to CLK on A – D flip-flops for XA and XQ devices | 0.41/ 0.02 | N/A | 0.44/ 0.02 | 0.68/ –0.29 | ns, Min |
| $T_{CINCK}/T_{CKCIN}$ | CIN input to CLK on A – D flip-flops | 0.31/ –0.17 | 0.31/ –0.13 | 0.31/ –0.13 | 0.81/ –0.42 | ns, Min |
| **Set/Reset** | | | | | | |
| $T_{RPW}$ | SR input minimum pulse width | 0.41 | 0.48 | 0.48 | 1.37 | ns, Min |
| $T_{RQ}$ | Delay from SR input to AQ – DQ flip-flops | 0.60 | 0.70 | 0.70 | 0.88 | ns, Max |
| $T_{CEO}$ | Delay from CE input to AQ – DQ flip-flops | 0.60 | 0.65 | 0.65 | 0.90 | ns, Max |
| $F_{TOG}$ | Toggle frequency (for export control) | 862 | 806 | 667 | 500 | MHz |

## DSP48A1 Switching Characteristics

*Table 44:* **DSP48A1 Switching Characteristics**

| Symbol | Description | Pre-adder | Multiplier | Post-adder | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | -3 | -3N | -2 | -1L | |
| **Setup and Hold Times of Data/Control Pins to the Input Register Clock** | | | | | | | | | |
| $T_{DSPDCK\_A\_A1REG}$/ $T_{DSPCKD\_A\_A1REG}$ | A input to A1 register CLK | N/A | N/A | N/A | 0.15/ 0.09 | 0.17/ 0.09 | 0.17/ 0.09 | 0.32/ 0.09 | ns |
| $T_{DSPDCK\_D\_B1REG}$/ $T_{DSPCKD\_D\_B1REG}$ | D input to B1 register CLK | Yes | N/A | N/A | 1.90/ –0.07 | 1.95/ –0.07 | 1.95/ –0.07 | 2.82/ –0.07 | ns |
| $T_{DSPDCK\_C\_CREG}$/ $T_{DSPCKD\_C\_CREG}$ | C input to C register CLK for XC devices | N/A | N/A | N/A | 0.11/ 0.15 | 0.13/ 0.15 | 0.13/ 0.15 | 0.24/ 0.09 | ns |
| | C input to C register CLK for XA and XQ devices | | | | 0.11/ 0.19 | N/A | 0.13/ 0.23 | 0.24/ 0.09 | |
| $T_{DSPDCK\_D\_DREG}$/ $T_{DSPCKD\_D\_DREG}$ | D input to D register CLK for XC devices | N/A | N/A | N/A | 0.09/ 0.15 | 0.10/ 0.15 | 0.10/ 0.15 | 0.19/ 0.12 | ns |
| | D input to D register CLK for XA and XQ devices | | | | 0.09/ 0.23 | N/A | 0.10/ 0.27 | 0.19/ 0.12 | |
| $T_{DSPDCK\_OPMODE\_B1REG}$/ $T_{DSPCKD\_OPMODE\_B1REG}$ | OPMODE input to B1 register CLK | Yes | N/A | N/A | 1.97/ 0.01 | 2.00/ 0.01 | 2.00/ 0.01 | 2.85/ 0.01 | ns |
| $T_{DSPDCK\_OPMODE\_OPMODEREG}$/ $T_{DSPCKD\_OPMODE\_OPMODEREG}$ | OPMODE input to OPMODE register CLK for XC devices | N/A | N/A | N/A | 0.18/ 0.12 | 0.21/ 0.12 | 0.21/ 0.12 | 0.40/ 0.12 | ns |
| | OPMODE input to OPMODE register CLK for XA and XQ devices | | | | 0.18/ 0.16 | N/A | 0.21/ 0.22 | 0.40/ 0.12 | |
| **Setup and Hold Times of Data Pins to the Pipeline Register Clock** | | | | | | | | | |
| $T_{DSPDCK\_A\_MREG}$/ $T_{DSPCKD\_A\_MREG}$ | A input to M register CLK | N/A | Yes | N/A | 3.06/ –0.40 | 3.51/ –0.40 | 3.51/ –0.40 | 3.97/ –0.40 | ns |
| $T_{DSPDCK\_B\_MREG}$/ $T_{DSPCKD\_B\_MREG}$ | B input to M register CLK | Yes | Yes | N/A | 3.96/ –0.68 | 4.58/ –0.68 | 4.58/ –0.68 | 7.00/ –0.68 | ns |
| $T_{DSPDCK\_D\_MREG}$/ $T_{DSPCKD\_D\_MREG}$ | D input to M register CLK | Yes | Yes | N/A | 4.23/ –0.56 | 4.80/ –0.56 | 4.80/ –0.56 | 6.84/ –0.56 | ns |
| $T_{DSPDCK\_OPMODE\_MREG}$/ $T_{DSPCKD\_OPMODE\_MREG}$ | OPMODE to M register CLK | Yes | Yes | N/A | 4.18/ –0.48 | 4.80/ –0.48 | 4.80/ –0.48 | 6.88/ –0.48 | ns |
| | | No | Yes | N/A | 2.37/ –0.48 | 2.70/ –0.48 | 2.70/ –0.48 | 4.28/ –0.48 | ns |
| **Setup and Hold Times of Data/Control Pins to the Output Register Clock** | | | | | | | | | |
| $T_{DSPDCK\_A\_PREG}$/ $T_{DSPCKD\_A\_PREG}$ | A input to P register CLK | N/A | Yes | Yes | 4.32/ –0.76 | 5.06/ –0.76 | 5.06/ –0.76 | 7.52/ –0.76 | ns |
| $T_{DSPDCK\_B\_PREG}$/ $T_{DSPCKD\_B\_PREG}$ | B input to P register CLK | Yes | Yes | Yes | 5.87/ –0.59 | 6.87/ –0.59 | 6.87/ –0.59 | 10.55/ –0.59 | ns |
| | | No | Yes | Yes | 4.14/ –0.93 | 4.68/ –0.93 | 4.68/ –0.93 | 8.12/ –0.93 | ns |
| $T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$ | C input to P register CLK | N/A | N/A | Yes | 2.20/ –0.23 | 2.25/ –0.23 | 2.25/ –0.23 | 3.27/ –0.23 | ns |
| $T_{DSPDCK\_D\_PREG}$/ $T_{DSPCKD\_D\_PREG}$ | D input to P register CLK | Yes | Yes | Yes | 5.90/ –0.92 | 6.91/ –0.92 | 6.91/ –0.92 | 10.39/ –0.92 | ns |

## Configuration Switching Characteristics

*Table 47:* **Configuration Switching Characteristics(1)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| **Power-up Timing Characteristics** | | | | | | |
| $T_{PL}$(2) | PROGRAM_B Latency | 4 | 4 | 4 | 5 | ms, Max |
| $T_{POR}$(2) | Power-on reset (50 ms ramp time)(3) | 5/30 | 5/34 | 5/40 | 5/40 | ms, Min/Max |
| | Power-on reset (10 ms ramp time) | 5/25 | 5/29 | 5/35 | 5/40 | ms, Min/Max |
| $T_{PROGRAM}$ | PROGRAM_B Pulse Width | 500 | 500 | 500 | 500 | ns, Min |
| **Slave Serial Mode Programming Switching** | | | | | | |
| $T_{DCCK}/T_{CCKD}$ | DIN Setup/Hold, slave mode | 6.0/1.0 | 6.0/1.0 | 6.0/1.0 | 8.0/2.0 | ns, Min |
| $T_{CCO}$ | CCLK to DOUT | 12 | 12 | 12 | 17 | ns, Max |
| $F_{SCCK}$ | Slave mode external CCLK | 80 | 80 | 80 | 50 | MHz, Max |
| **Slave SelectMAP Mode Programming Switching** | | | | | | |
| $T_{SMDCCK}/T_{SMCCKD}$ | SelectMAP Data Setup/Hold | 6.0/1.0 | 6.0/1.0 | 6.0/1.0 | 8.0/2.0 | ns, Min |
| $T_{SMCSCCK}/T_{SMCCKCS}$ | CSI_B Setup/Hold | 7.0/0.0 | 7.0/0.0 | 7.0/0.0 | 9.0/2.0 | ns, Min |
| $T_{SMWCCK}/T_{SMCCKW}$ | RDWR_B Setup/Hold | 17.0/1.0 | 17.0/1.0 | 17.0/1.0 | 27.0/2.0 | ns, Min |
| $T_{SMCKCSO}$ | CSO_B clock to out | 16 | 16 | 16 | 26 | ns, Max |
| $T_{SMCO}$ | CCLK to DATA out in readback | 13 | 13 | 13 | 25 | ns, Max |
| $T_{SMCKBY}$ | CCLK to BUSY out in readback | 12 | 12 | 12 | 17 | ns, Max |
| $F_{SMCCK}$ | Maximum CCLK frequency (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only) | 50 | 50 | 50 | 25 | MHz, Max |
| | Maximum CCLK frequency (LX100 and LX100T in x8 mode, LX150, and LX150T only) | 40 | 40 | 40 | 20 | MHz, Max |
| | Maximum CCLK frequency (LX100 and LX100T in x16 mode only) | 35 | 35 | 35 | 20 | MHz, Max |
| $F_{RBCCK}$ | Maximum Readback CCLK frequency, including block RAM (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only) | 20 | 20 | 20 | 4 | MHz, Max |
| | Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only) | 50 | 50 | 50 | 30 | MHz, Max |
| | Maximum Readback CCLK frequency, including block RAM (LX100, LX100T, LX150, and LX150T only) | 12 | 12 | 12 | 4 | MHz, Max |
| | Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX100, LX100T, LX150, and LX150T only) | 35 | 35 | 35 | 20 | MHz, Max |
| **Boundary-Scan Port Timing Specifications** | | | | | | |
| $T_{TAPTCK}$ | TMS and TDI Setup time before TCK | 10 | 10 | 10 | 17 | ns, Min |
| $T_{TCKTAP}$ | TMS and TDI Hold time after TCK | 5.5 | 5.5 | 5.5 | 5.5 | ns, Min |
| $T_{TCKTDO}$ | TCK falling edge to TDO output valid | 6.5 | 6.5 | 6.5 | 8 | ns, Max |
| $T_{TCKH}$ | TCK clock minimum High time | 12 | 12 | 12 | 21 | ns, Min |
| $T_{TCKL}$ | TCK clock minimum Low time | 12 | 12 | 12 | 21 | ns, Min |
| $F_{TCK}$ | Maximum configuration TCK clock frequency | 33 | 33 | 33 | 18 | MHz, Max |
| $F_{TCKB}$ | Maximum boundary-scan TCK clock frequency | 33 | 33 | 33 | 18 | MHz, Max |
| $F_{TCKAES}$ | Maximum AES key TCK clock frequency | 2 | 2 | 2 | 2 | MHz, Max |

*Table 52:* **PLL Specification *(Cont'd)***

| Symbol | Description | Device[1] | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| $F_{INMIN}$ | Minimum Input Clock Frequency | LX devices | 19 | 19 | 19 | 19 | MHz |
| | | LXT devices | 19 | 19 | 19 | N/A | MHz |
| $F_{INJITTER}$ | Maximum Input Clock Period Jitter: 19–200 MHz | All | 1 ns Maximum | | | | |
| | Maximum Input Clock Period Jitter: > 200 MHz | All | <20% of clock input period Maximum | | | | |
| $F_{INDUTY}$ | Allowable Input Duty Cycle: 19—199 MHz | All | 25/75 | | | | % |
| | Allowable Input Duty Cycle: 200—299 MHz | All | 35/65 | | | | % |
| | Allowable Input Duty Cycle: > 300 MHz | All | 45/55 | | | | % |
| $F_{VCOMIN}$ | Minimum PLL VCO Frequency | LX devices | 400 | 400 | 400 | 400 | MHz |
| | | LXT devices | 400 | 400 | 400 | N/A | MHz |
| $F_{VCOMAX}$ | Maximum PLL VCO Frequency | LX devices | 1080 | 1050 | 1000 | 1000 | MHz |
| | | LXT devices | 1080 | 1050 | 1000 | N/A | MHz |
| $F_{BANDWIDTH}$ | Low PLL Bandwidth at Typical[3] | All | 1 | 1 | 1 | 1 | MHz |
| | High PLL Bandwidth at Typical[3] | All | 4 | 4 | 4 | 4 | MHz |
| $T_{STAPHAOFFSET}$ | Static Phase Offset of the PLL Outputs | All | 0.12 | 0.12 | 0.12 | 0.15 | ns |
| $T_{OUTJITTER}$ | PLL Output Jitter[3] | All | Note 2 | | | | |
| $T_{OUTDUTY}$ | PLL Output Clock Duty Cycle Precision[4] | All | 0.15 | 0.15 | 0.20 | 0.25 | ns |
| $T_{LOCKMAX}$ | PLL Maximum Lock Time | All | 100 | 100 | 100 | 100 | µs |
| $F_{OUTMAX}$ | PLL Maximum Output Frequency for BUFGMUX | LX devices | 400 | 400 | 375 | 250 | MHz |
| | | LXT devices | 400 | 400 | 375 | N/A | MHz |
| | PLL Maximum Output Frequency for BUFPLL | LX devices | 1080 | 1050 | 950 | 500 | MHz |
| | | LXT devices | 1080 | 1050 | 950 | N/A | MHz |
| $F_{OUTMIN}$ | PLL Minimum Output Frequency[5] | All | 3.125 | 3.125 | 3.125 | 3.125 | MHz |
| $T_{EXTFDVAR}$ | External Clock Feedback Variation: 19–200 MHz | All | 1 ns Maximum | | | | |
| | External Clock Feedback Variation: > 200 MHz | All | < 20% of clock input period Maximum | | | | |
| $RST_{MINPULSE}$ | Minimum Reset Pulse Width | All | 5 | 5 | 5 | 5 | ns |
| $F_{PFDMAX}$[5] | Maximum Frequency at the Phase Frequency Detector | LX devices | 500 | 500 | 400 | 300 | MHz |
| | | LXT devices | 500 | 500 | 400 | N/A | MHz |
| $F_{PFDMIN}$ | Minimum Frequency at the Phase Frequency Detector | LX devices | 19 | 19 | 19 | 19 | MHz |
| | | LXT devices | 19 | 19 | 19 | N/A | MHz |
| $T_{FBDELAY}$ | Maximum Delay in the Feedback Path | All | 3 ns Max or one CLKIN cycle | | | | |

**Notes:**

1. LXT devices are not available with a -1L speed grade.
2. Values for this parameter are available in the Clocking Wizard.
3. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When using CLK_FEEDBACK = CLKOUT0 with BUFIO2 feedback, the feedback frequency will be higher than the phase frequency detector frequency. $F_{PFDMAX} = F_{CLKFB}$ / CLKFBOUT_MULT

*Table 57:* **Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)[1] *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| **Spread Spectrum** | | | | | | | | | | |
| $F_{CLKIN\_FIXED\_SPREAD\_SPECTRUM}$ | Frequency of the CLKIN input for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD/ CENTER_HIGH_SPREAD) | 30 | 200 | 30 | 200 | 30 | 200 | 30 | 200 | MHz |
| $T_{CENTER\_LOW\_SPREAD}$[6] | Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD) | Typical = $\frac{100}{CLKFX\_DIVIDE}$ Maximum = 250 | | | | | | | | ps |
| $T_{CENTER\_HIGH\_SPREAD}$[6] | Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM= CENTER_HIGH_SPREAD) | Typical = $\frac{240}{CLKFX\_DIVIDE}$ Maximum = 400 | | | | | | | | ps |
| $F_{MOD\_FIXED\_SPREAD\_SPECTRUM}$[6] | Average modulation frequency when using fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD / CENTER_HIGH_SPREAD) | Typical = $F_{IN}/1024$ | | | | | | | | MHz |

**Notes:**
1. The values in this table are based on the operating conditions described in Table 2 and Table 55.
2. For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
3. Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
5. Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.
6. When using CENTER_LOW_SPREAD, CENTER_HIGH_SPREAD, the valid values for CLKFX_MULTIPLY are limited to 2 through 32, and the valid values for CLKFX_DIVIDE are limited to 1 through 4.

*Table 58:* **Recommended Operating Conditions for the Phase-Shift Clock in Variable Phase Mode (DCM_SP) or Dynamic Frequency Synthesis (DCM_CLKGEN)**

| Symbol | Description | Speed Grade | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| **Operating Frequency Ranges** | | | | | | | | | | |
| PSCLK_FREQ | Frequency for the PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) input. | 1 | 167 | 1 | 167 | 1 | 167 | 1 | 100 | MHz |
| **Input Pulse Requirements** | | | | | | | | | | |
| PSCLK_PULSE | PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) pulse width as a percentage of the clock period. | 40 | 60 | 40 | 60 | 40 | 60 | 40 | 60 | % |

*Table 59:* **Switching Characteristics for the Phase-Shift Clock in Variable Phase Mode(1)**

| Symbol | Description | Amount of Phase Shift | Units |
|---|---|---|---|
| **Phase Shifting Range** | | | |
| MAX_STEPS(2) | When CLKIN < 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period. | ±(INTEGER(10 x (TCLKIN – 3 ns))) | steps |
| | When CLKIN ≥ 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period. | ±(INTEGER(15 x (TCLKIN – 3 ns))) | steps |
| FINE_SHIFT_RANGE_MIN | Minimum guaranteed delay for variable phase shifting. | ±(MAX_STEPS x DCM_DELAY_STEP_MIN) | ps |
| FINE_SHIFT_RANGE_MAX | Maximum guaranteed delay for variable phase shifting | ±(MAX_STEPS x DCM_DELAY_STEP_MAX) | ps |

**Notes:**
1. The values in this table are based on the operating conditions described in Table 53 and Table 58.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM has no initial fixed-phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the end of Table 54.

*Table 60:* **Miscellaneous DCM Timing Parameters(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| DCM_RST_PW_MIN | Minimum duration of a RST pulse width | 3 | – | CLKIN cycles |

**Notes:**
1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFXDV, CLKFX180) are unaffected.

*Table 61:* **Frequency Synthesis**

| Attribute | Min | Max |
|---|---|---|
| CLKFX_MULTIPLY (DCM_SP) | 2 | 32 |
| CLKFX_DIVIDE (DCM_SP) | 1 | 32 |
| CLKDV_DIVIDE (DCM_SP) | 1.5 | 16 |
| CLKFX_MULTIPLY (DCM_CLKGEN) | 2 | 256 |
| CLKFX_DIVIDE (DCM_CLKGEN) | 1 | 256 |
| CLKFXDV_DIVIDE (DCM_CLKGEN) | 2 | 32 |

*Table 62:* **DCM Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -3N | -2 | -1L | |
| $T_{DMCCK\_PSEN}$/ $T_{DMCKC\_PSEN}$ | PSEN Setup/Hold | 1.50/ 0.00 | 1.50/ 0.00 | 1.50/ 0.00 | 1.50/ 0.00 | ns |
| $T_{DMCCK\_PSINCDEC}$/ $T_{DMCKC\_PSINCDEC}$ | PSINCDEC Setup/Hold | 1.50/ 0.00 | 1.50/ 0.00 | 1.50/ 0.00 | 1.50/ 0.00 | ns |
| $T_{DMCKO\_PSDONE}$ | Clock to out of PSDONE | 1.50 | 1.50 | 1.50 | 1.50 | ns |

## Spartan-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 63 through Table 69. Values are expressed in nanoseconds unless otherwise noted.

*Table 63:* **Global Clock Input to Output Delay Without DCM or PLL**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* DCM or PLL | | | | | | | |
| $T_{ICKOF}$ | Global Clock and OUTFF *without* DCM or PLL | XC6SLX4 | 6.12 | N/A | 7.68 | 9.41 | ns |
| | | XC6SLX9 | 6.12 | 6.51 | 7.68 | 9.41 | ns |
| | | XC6SLX16 | 5.98 | 6.42 | 7.48 | 9.10 | ns |
| | | XC6SLX25 | 6.20 | 6.69 | 7.84 | 9.44 | ns |
| | | XC6SLX25T | 6.20 | 6.69 | 7.84 | N/A | ns |
| | | XC6SLX45 | 6.37 | 6.88 | 8.10 | 9.61 | ns |
| | | XC6SLX45T | 6.37 | 6.88 | 8.10 | N/A | ns |
| | | XC6SLX75 | 6.39 | 6.99 | 8.16 | 10.18 | ns |
| | | XC6SLX75T | 6.39 | 6.99 | 8.16 | N/A | ns |
| | | XC6SLX100 | 6.59 | 7.18 | 8.41 | 10.31 | ns |
| | | XC6SLX100T | 6.59 | 7.18 | 8.41 | N/A | ns |
| | | XC6SLX150 | 6.98 | 7.68 | 8.80 | 10.62 | ns |
| | | XC6SLX150T | 6.98 | 7.68 | 8.80 | N/A | ns |
| | | XA6SLX4 | 6.44 | N/A | 7.68 | N/A | ns |
| | | XA6SLX9 | 6.44 | N/A | 7.68 | N/A | ns |
| | | XA6SLX16 | 6.30 | N/A | 7.48 | N/A | ns |
| | | XA6SLX25 | 6.52 | N/A | 7.84 | N/A | ns |
| | | XA6SLX25T | 6.52 | N/A | 7.84 | N/A | ns |
| | | XA6SLX45 | 6.69 | N/A | 8.12 | N/A | ns |
| | | XA6SLX45T | 6.69 | N/A | 8.12 | N/A | ns |
| | | XA6SLX75 | 6.89 | N/A | 8.16 | N/A | ns |
| | | XA6SLX75T | 6.89 | N/A | 8.16 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 8.36 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 8.16 | 10.18 | ns |
| | | XQ6SLX75T | 6.89 | N/A | 8.16 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | 8.80 | 10.62 | ns |
| | | XQ6SLX150T | 7.61 | N/A | 8.80 | N/A | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

*Table 72:* **Global Clock Setup and Hold With DCM in System-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)** | | | | | | | |
| $T_{PSDCM}$/ $T_{PHDCM}$ | No Delay Global Clock and IFF(2) with DCM in System-Synchronous Mode | XC6SLX4 | 1.54/0.06 | N/A | 1.75/0.12 | 2.84/0.27 | ns |
| | | XC6SLX9 | 1.54/0.06 | 1.63/0.12 | 1.75/0.12 | 2.84/0.27 | ns |
| | | XC6SLX16 | 1.72/–0.18 | 1.87/–0.17 | 2.13/–0.17 | 2.31/0.26 | ns |
| | | XC6SLX25 | 1.70/–0.03 | 1.78/–0.02 | 2.00/–0.02 | 2.88/0.20 | ns |
| | | XC6SLX25T | 1.70/0.07 | 1.78/0.08 | 2.00/0.08 | N/A | ns |
| | | XC6SLX45 | 1.74/–0.03 | 1.84/–0.02 | 2.02/–0.02 | 2.64/0.52 | ns |
| | | XC6SLX45T | 1.74/–0.01 | 1.84/0.00 | 2.02/0.00 | N/A | ns |
| | | XC6SLX75 | 1.86/0.11 | 1.98/0.12 | 2.20/0.12 | 2.96/0.58 | ns |
| | | XC6SLX75T | 1.86/0.11 | 1.98/0.12 | 2.20/0.12 | N/A | ns |
| | | XC6SLX100 | 1.64/0.07 | 1.72/0.08 | 1.97/0.08 | 2.70/0.99 | ns |
| | | XC6SLX100T | 1.64/0.09 | 1.72/0.10 | 1.97/0.10 | N/A | ns |
| | | XC6SLX150 | 1.53/0.39 | 1.62/0.40 | 1.82/0.40 | 2.75/1.00 | ns |
| | | XC6SLX150T | 1.53/0.39 | 1.62/0.40 | 1.82/0.40 | N/A | ns |
| | | XA6SLX4 | 1.65/0.16 | N/A | 1.75/0.26 | N/A | ns |
| | | XA6SLX9 | 1.65/0.16 | N/A | 1.75/0.26 | N/A | ns |
| | | XA6SLX16 | 1.88/0.02 | N/A | 2.13/0.03 | N/A | ns |
| | | XA6SLX25 | 1.80/0.16 | N/A | 2.05/0.17 | N/A | ns |
| | | XA6SLX25T | 1.80/0.16 | N/A | 2.13/0.17 | N/A | ns |
| | | XA6SLX45 | 1.75/0.12 | N/A | 2.02/0.13 | N/A | ns |
| | | XA6SLX45T | 1.75/0.12 | N/A | 2.02/0.13 | N/A | ns |
| | | XA6SLX75 | 1.87/0.11 | N/A | 2.20/0.12 | N/A | ns |
| | | XA6SLX75T | 1.87/0.11 | N/A | 2.20/0.12 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 2.46/0.24 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 2.20/0.12 | 2.96/0.58 | ns |
| | | XQ6SLX75T | 1.87/0.11 | N/A | 2.20/0.12 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | 1.82/0.56 | 2.75/1.00 | ns |
| | | XQ6SLX150T | 1.65/0.55 | N/A | 1.82/0.56 | N/A | ns |

**Notes:**
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 73:* **Global Clock Setup and Hold With DCM in Source-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)** | | | | | | | |
| $T_{PSDCM0}$/ $T_{PHDCM0}$ | No Delay Global Clock and IFF(2) with DCM in Source-Synchronous Mode | XC6SLX4 | 0.71/0.65 | N/A | 0.72/1.22 | 1.58/1.18 | ns |
| | | XC6SLX9 | 0.71/0.69 | 0.71/1.19 | 0.72/1.36 | 1.58/1.18 | ns |
| | | XC6SLX16 | 0.86/0.52 | 0.92/0.57 | 1.04/0.60 | 1.02/1.06 | ns |
| | | XC6SLX25 | 0.84/0.58 | 0.90/0.59 | 1.01/0.59 | 1.58/1.07 | ns |
| | | XC6SLX25T | 0.84/0.58 | 0.90/0.59 | 1.01/0.59 | N/A | ns |
| | | XC6SLX45 | 0.85/0.70 | 0.90/0.76 | 0.98/0.79 | 1.34/1.34 | ns |
| | | XC6SLX45T | 0.85/0.70 | 0.90/0.76 | 0.98/0.79 | N/A | ns |
| | | XC6SLX75 | 1.00/0.62 | 1.06/0.63 | 1.15/0.63 | 1.65/1.46 | ns |
| | | XC6SLX75T | 1.00/0.71 | 1.06/0.72 | 1.15/0.72 | N/A | ns |
| | | XC6SLX100 | 0.81/0.68 | 0.81/0.69 | 0.94/0.69 | 1.42/2.07 | ns |
| | | XC6SLX100T | 0.81/0.68 | 0.81/0.69 | 0.94/0.69 | N/A | ns |
| | | XC6SLX150 | 0.68/0.98 | 0.69/0.99 | 0.79/0.99 | 1.45/1.60 | ns |
| | | XC6SLX150T | 0.68/0.98 | 0.69/0.99 | 0.79/0.99 | N/A | ns |
| | | XA6SLX4 | 0.81/0.74 | N/A | 0.72/1.36 | N/A | ns |
| | | XA6SLX9 | 0.81/0.74 | N/A | 0.72/1.36 | N/A | ns |
| | | XA6SLX16 | 1.01/0.56 | N/A | 1.04/0.60 | N/A | ns |
| | | XA6SLX25 | 0.94/0.76 | N/A | 1.06/0.77 | N/A | ns |
| | | XA6SLX25T | 0.94/0.76 | N/A | 1.14/0.77 | N/A | ns |
| | | XA6SLX45 | 0.86/0.74 | N/A | 0.98/0.78 | N/A | ns |
| | | XA6SLX45T | 0.86/0.74 | N/A | 0.98/0.78 | N/A | ns |
| | | XA6SLX75 | 1.02/0.71 | N/A | 1.15/0.72 | N/A | ns |
| | | XA6SLX75T | 1.02/0.71 | N/A | 1.15/0.72 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 1.37/0.75 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 1.15/0.72 | 1.65/1.46 | ns |
| | | XQ6SLX75T | 1.02/0.71 | N/A | 1.15/0.72 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | 0.79/1.15 | 1.45/1.60 | ns |
| | | XQ6SLX150T | 0.73/1.15 | N/A | 0.79/1.15 | N/A | ns |

**Notes:**
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 75:* **Global Clock Setup and Hold With PLL in Source-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)** | | | | | | | |
| $T_{PSPLL0}$/ $T_{PHPLL0}$ | No Delay Global Clock and IFF(2) with PLL in Source-Synchronous Mode | XC6SLX4 | 0.47/1.08 | N/A | 0.47/1.60 | 1.15/1.68 | ns |
| | | XC6SLX9 | 0.47/1.08 | 0.47/1.35 | 0.47/1.60 | 1.15/1.68 | ns |
| | | XC6SLX16 | 0.37/0.75 | 0.37/0.82 | 0.51/0.94 | 0.57/1.31 | ns |
| | | XC6SLX25 | 0.69/1.06 | 0.69/1.06 | 0.69/1.06 | 1.86/1.67 | ns |
| | | XC6SLX25T | 0.69/1.06 | 0.69/1.06 | 0.69/1.06 | N/A | ns |
| | | XC6SLX45 | 0.57/1.05 | 0.65/1.10 | 0.65/1.18 | 1.02/1.65 | ns |
| | | XC6SLX45T | 0.57/1.06 | 0.65/1.10 | 0.65/1.18 | N/A | ns |
| | | XC6SLX75 | 0.86/1.04 | 0.87/1.04 | 0.90/1.04 | 1.34/1.55 | ns |
| | | XC6SLX75T | 0.86/1.04 | 0.87/1.04 | 0.90/1.04 | N/A | ns |
| | | XC6SLX100 | 0.53/1.13 | 0.54/1.13 | 0.55/1.13 | 0.89/2.39 | ns |
| | | XC6SLX100T | 0.53/1.13 | 0.54/1.13 | 0.55/1.13 | N/A | ns |
| | | XC6SLX150 | 0.50/1.31 | 0.51/1.31 | 0.52/1.31 | 1.02/1.72 | ns |
| | | XC6SLX150T | 0.50/1.31 | 0.51/1.31 | 0.52/1.31 | N/A | ns |
| | | XA6SLX4 | 0.71/0.93 | N/A | 0.62/1.47 | N/A | ns |
| | | XA6SLX9 | 0.71/0.93 | N/A | 0.62/1.47 | N/A | ns |
| | | XA6SLX16 | 0.92/0.69 | N/A | 0.63/0.82 | N/A | ns |
| | | XA6SLX25 | 0.99/0.94 | N/A | 0.96/0.94 | N/A | ns |
| | | XA6SLX25T | 0.99/0.94 | N/A | 1.04/0.94 | N/A | ns |
| | | XA6SLX45 | 0.63/1.02 | N/A | 0.72/1.05 | N/A | ns |
| | | XA6SLX45T | 0.63/1.02 | N/A | 0.72/1.05 | N/A | ns |
| | | XA6SLX75 | 0.88/0.89 | N/A | 1.02/0.89 | N/A | ns |
| | | XA6SLX75T | 0.88/0.89 | N/A | 1.02/0.89 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 1.25/0.96 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 1.02/0.89 | 1.34/1.55 | ns |
| | | XQ6SLX75T | 0.88/0.89 | N/A | 1.02/0.89 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | 0.63/1.19 | 1.02/1.72 | ns |
| | | XQ6SLX150T | 0.60/1.19 | N/A | 0.63/1.19 | N/A | ns |

**Notes:**
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 77:* **Global Clock Setup and Hold With DCM and PLL in Source-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -3N | -2 | -1L | |
| Example Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin,(1) Using DCM, PLL, and Global Clock Buffer for the LVCMOS25 standard. | | | | | | | |
| $T_{PSDCMPLL\_0}$/ $T_{PHDCMPLL\_0}$ | No Delay Global Clock and IFF(2) with DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode. | XC6SLX4 | 0.43/1.07 | N/A | 0.43/1.43 | 1.10/1.67 | ns |
| | | XC6SLX9 | 0.43/1.03 | 0.45/1.14 | 0.45/1.43 | 1.10/1.67 | ns |
| | | XC6SLX16 | 0.74/0.93 | 0.74/1.12 | 0.74/1.21 | 0.77/1.35 | ns |
| | | XC6SLX25 | 0.67/1.02 | 0.76/1.11 | 0.84/1.18 | 1.23/1.46 | ns |
| | | XC6SLX25T | 0.67/1.02 | 0.76/1.11 | 0.84/1.18 | N/A | ns |
| | | XC6SLX45 | 0.65/0.99 | 0.65/1.04 | 0.71/1.12 | 1.18/1.58 | ns |
| | | XC6SLX45T | 0.65/1.00 | 0.65/1.04 | 0.71/1.12 | N/A | ns |
| | | XC6SLX75 | 0.86/1.01 | 0.88/1.06 | 0.94/1.14 | 1.29/1.67 | ns |
| | | XC6SLX75T | 0.86/1.01 | 0.88/1.06 | 0.94/1.14 | N/A | ns |
| | | XC6SLX100 | 0.50/1.10 | 0.56/1.10 | 0.61/1.17 | 0.84/2.24 | ns |
| | | XC6SLX100T | 0.50/1.10 | 0.56/1.10 | 0.61/1.17 | N/A | ns |
| | | XC6SLX150 | 0.45/1.28 | 0.47/1.28 | 0.52/1.28 | 1.27/1.56 | ns |
| | | XC6SLX150T | 0.45/1.28 | 0.47/1.28 | 0.52/1.28 | N/A | ns |
| | | XA6SLX4 | 0.74/1.00 | N/A | 0.74/1.43 | N/A | ns |
| | | XA6SLX9 | 0.74/1.00 | N/A | 0.74/1.43 | N/A | ns |
| | | XA6SLX16 | 1.81/1.15 | N/A | 1.81/1.03 | N/A | ns |
| | | XA6SLX25 | 0.89/1.01 | N/A | 0.96/1.05 | N/A | ns |
| | | XA6SLX25T | 0.89/1.01 | N/A | 1.04/1.15 | N/A | ns |
| | | XA6SLX45 | 0.69/0.95 | N/A | 0.83/0.96 | N/A | ns |
| | | XA6SLX45T | 0.69/0.95 | N/A | 0.83/0.96 | N/A | ns |
| | | XA6SLX75 | 0.88/0.94 | N/A | 1.06/0.96 | N/A | ns |
| | | XA6SLX75T | 0.88/0.94 | N/A | 1.06/0.96 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 1.55/1.33 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 1.06/0.96 | 1.29/1.67 | ns |
| | | XQ6SLX75T | 0.88/0.94 | N/A | 1.06/0.96 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | 0.64/1.30 | 1.27/1.56 | ns |
| | | XQ6SLX150T | 0.58/1.30 | N/A | 0.64/1.30 | N/A | ns |

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG. Package skew is not included in these measurements.
2. IFF = Input Flip-Flop

| Date | Version | Description of Revisions |
|---|---|---|
| 01/10/11 | 1.11 | Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.4 software with speed specification v1.15 for the -4, -3, -3N, and -2 speed grades. Added note 3 to Table 27. Also updated the -1L speed grade requirements to ISE v12.4 software with speed specification v1.06. Revised -3N definition throughout the document.<br>Added note 4 to Table 2 and updated note 5. Added information on $V_{CCINT}$ to note 1 in Table 5. Updated Networking Applications -3 values in Table 25 to match improvements made in ISE v12.4. In Table 28, added note 1 and revised the $T_{IOTP}$ values for LVDS_33, LVDS_25, MINI_LVDS_33, MINI_LVDS_25, RSDS_33, RSDS_25, TMDS_33. PPDS_33, and PPDS_25. Added note 3 to Table 55. |
| 02/11/11 | 1.12 | As described in XCN11008: *Product Discontinuation Notice For Spartan-6 LXT -4 Devices*, the -4 speed specifications have been discontinued. As outlined in page 2 of the XCN, designers currently using -4 speed specifications should rerun timing analysis using the new -3 speed specifications before moving to a replacement device.<br>Updated the networking applications section of Table 25. Updated -2 speed specifications throughout document and added note 3 to Table 27 advising designers to use the -2 speed specification update (v1.17) with the ISE 12.4 software patch. Added $F_{CLKDIV}$ to Table 37 and Table 38. Updated note 2 in Table 39. Updated units for $T_{SMCKCSO}$ and $T_{BPICCO}$ in Table 47. Updated -1L in Table 71. Removed Note 2: *Package delay information is available for these device/package combinations. This information can be used to deskew the package* from Table 79. |
| 03/31/11 | 2.0 | Production release of XC6SLX45 in the -1L speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06.<br>In Table 39, removed values in the -1L column and added note 3 as IODELAY2 only supports Tap0 for lower-power devices. Updated copyright page 1 and Notice of Disclaimer. |
| 05/20/11 | 2.1 | Production release of XC6SLX100 and XC6SLX150 in the specific speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. Updated Table 27 and Note 7 with changes per XCN11012: *Speed File Change for -3N Devices*. Revised Switching Characteristics section for speed specifications: v1.18 for -3, -3N, and -2; including improvements in Table 73 through Table 77 and Table 81.<br>Removed *Memory Controller Block* from the performance heading in Table 2 and revised Note 2. In Table 4, added Note 1 to $C_{IN}$ and updated the description of $R_{IN\_TERM}$. Updated Note 1 in Table 5. Updated Note 1 of Table 7. In Table 25, added and removed -1L specifications, increased the standard performance DDR3 specifications, removed the extended performance DDR3 row and updated Note 3 and Note 4. Clarified the introductory information for Table 28 and Table 30.<br>In Table 32: Revised $V_{MEAS}$ value for LVCMOS12; revised $V_{REF}$ for LVDS_25, LVDS_33, BLVDS_25,MINI_LVDS_25, MINI_LVDS_33, RSDS_25, and RSDS_33; revised $R_{REF}$ for BLVDS_25 and TMDS_33; and added Note 4 and Note 5. Updated Note 2 and Note 3 in Table 39.<br>In Table 47, revised the values and description of $T_{POR}$ including adding Note 3. Also in Table 47, augmented the description and added specifications for $F_{RBCCK}$ and removed XC6SLX4 from $F_{MCCK}$ (maximum frequency, parallel mode (Master SelectMAP/BPI). Added BUFGMUX to Table 48 title. Added Table 50.<br>In Table 52, revised specifications for $T_{EXTFDVAR}$ and $F_{INJITTER}$. In Table 54 removed the 5 MHz < CLKIN_FREQ_DLL parameter in the LOCK_DLL description. In both Table 56 and Table 57, removed the 5 MHz < $F_{CLKIN}$ parameter in the LOCK_FX description. In Table 58, updated description for PSCLK_FREQ and PSCLK_PULSE.<br>Revised title and symbol of Table 70, added new speed specifications for -1L, and added Note 2. Added Table 71. |
| 07/11/11 | 2.2 | Added the Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices to all appropriate tables while sometimes removing the XC6S nomenclature. Added expanded temperature range (Q) to all appropriate tables. Updated $T_{SOL}$ packages in Table 1. Added $R_{OUT\_TERM}$ to Table 4. Updated Note 2 on Table 13.<br>Production release of the XC6SLX4, XC6SLX9, XC6SLX16, XC6SLX25, XC6SLX75, XQ6SLX75, and XQ6SLX150 in Table 26 and Table 27 using ISE v13.2 software with -1L speed specification v1.07.<br>Production release of the XA6SLX16, XA6SLX25T, XA6SLX45, XA6SLX45T, XQ6SLX75, XQ6SLX75T, XQ6SLX150, and XQ6SLX150T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19.<br>Added Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices(1). Updated CS(G)484 from CSG484 throughout data sheet. Clarified Note 3 in Table 39. |
| 08/08/11 | 2.3 | Production release of the XA6SLX25, XA6SLX75, and XA6SLX75T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. |

| Date | Version | Description of Revisions |
|---|---|---|
| 09/14/11 | 2.4 | Production release of the XA6SLX4 and XA6SLX9 devices in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added production released version of the XA6SLX100 to Table 26 and Table 27 using ISE v13.3 software with -2 speed specification v1.20.<br><br>Updated $R_{OUT\_TERM}$ description in Table 4. Fixed the LVPECL $V_H$ error in Table 31. Updated introduction in Simultaneously Switching Outputs. Added the XA6SLX100 to Table 63 through Table 78, and Table 81. Added Note 4 to Table 78 because the $T_{CKSKEW}$ for the XC6SLX100 is not the same as the $T_{CKSKEW}$ for the XA6SLX100.<br><br>Revised the revision history for version 1.6 dated 06/24/10. Removed the parenthetical statement about the -3N speed grade: (specifications are identical to the -3 speed grade). |
| 10/17/11 | 3.0 | Changed the data sheet from Preliminary Product Specification to Product Specification.<br>Updated the Switching Characteristics, page 19 speed specification version ISE v13.3 software to -2 and -3 speed specification v1.20 and -1L speed specification of v1.08. Also updated Note 1 in Table 27.<br>In Table 43, *Block RAM Switching Characteristics*, the $F_{MAX}$ value for the -2 speed grade has been changed from 260 MHz to 280 MHz.<br>In Table 54, *Switching Characteristics for the DLL*, a Note 6 was added and linked to CLKIN_CLKFB_PHASE. |