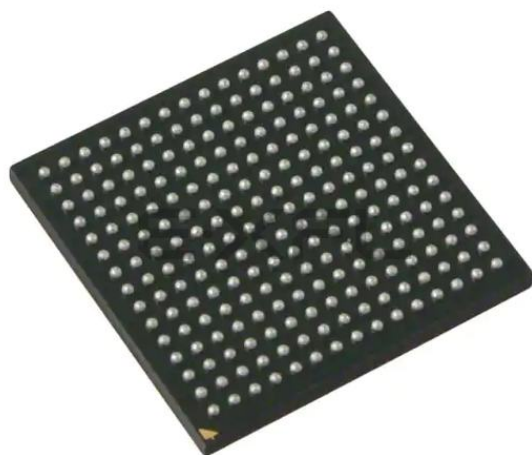




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	715
Number of Logic Elements/Cells	9152
Total RAM Bits	589824
Number of I/O	160
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	225-LFBGA, CSPBGA
Supplier Device Package	225-CSPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx9-n3csg225i

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description					Units
V_{IN} and V_{TS} ⁽³⁾	I/O input voltage or voltage applied to 3-state output, relative to GND ⁽⁴⁾	All user and dedicated I/Os	Commercial	DC	–0.60 to 4.10	V
				20% overshoot duration	–0.75 to 4.25	V
				8% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
			Industrial	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
			Expanded (Q)	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
		Restricted to maximum of 100 user I/Os	Commercial	20% overshoot duration	–0.75 to 4.35	V
				15% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
				10% overshoot duration	–0.75 to 4.45	V
			Industrial	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
			Expanded (Q)	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration ⁽⁵⁾	–0.75 to 4.40	V
T_{STG}	Storage temperature (ambient)				–65 to 150	°C
T_{SOL}	Maximum soldering temperature ⁽⁶⁾ (TQG144, CPG196, CSG225, CSG324, CSG484, and FTG256)				+260	°C
	Maximum soldering temperature ⁽⁶⁾ (Pb-free packages: FGG484, FGG676, and FGG900)				+250	°C
	Maximum soldering temperature ⁽⁶⁾ (Pb packages: CS484, FT256, FG484, FG676, and FG900)				+220	°C
T_j	Maximum junction temperature ⁽⁶⁾				+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- When programming eFUSE, $V_{FS} \leq V_{CCAUX}$. Requires up to 40 mA current. For read mode, V_{FS} can be between GND and 3.45 V.
- I/O absolute maximum limit applied to DC and AC signals. Overshoot duration is the percentage of a data period that the I/O is stressed beyond 3.45V.
- For I/O operation, refer to [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.
- Maximum percent overshoot duration to meet 4.40V maximum.
- For soldering guidelines and thermal considerations, see [UG385](#): *Spartan-6 FPGA Packaging and Pinout Specification*.

Table 5: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	LX4	2.5	2.5	2.5	2.5	mA
		LX9	2.5	2.5	2.5	2.5	mA
		LX16	3.0	3.0	3.0	3.0	mA
		LX25	4.0	4.0	4.0	4.0	mA
		LX25T	4.0	4.0	4.0	N/A	mA
		LX45	5.0	5.0	5.0	5.0	mA
		LX45T	5.0	5.0	5.0	N/A	mA
		LX75	7.0	7.0	7.0	7.0	mA
		LX75T	7.0	7.0	7.0	N/A	mA
		LX100	9.0	9.0	9.0	9.0	mA
		LX100T	9.0	9.0	9.0	N/A	mA
		LX150	12.0	12.0	12.0	12.0	mA
		LX150T	12.0	12.0	12.0	N/A	mA

Notes:

- Typical values are specified at nominal voltage, 25°C junction temperatures (T_j). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 25°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. Nominal V_{CCINT} is 1.20V; use the XPE tool to calculate 1.23V values for the nominal V_{CCINT} of the extended performance range.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- If differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 6: Power Supply Ramp Time

Symbol	Description	Speed Grade	Ramp Time	Units
V _{CCINTR}	Internal supply voltage ramp time	-3, -3N, -2	0.20 to 50.0	ms
		-1L	0.20 to 40.0	ms
V _{CCO2} ⁽¹⁾	Output drivers bank 2 supply voltage ramp time	All	0.20 to 50.0	ms
V _{CCAUXR}	Auxiliary supply voltage ramp time	All	0.20 to 50.0	ms

Notes:

- The minimum V_{CCO2} for power-on reset and configuration is 1.65V.
- Spartan-6 FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply. Use the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools to estimate current drain on these supplies. Spartan-6 devices do not have a required power-on sequence.

Table 8: Recommended Operating Conditions for User I/Os Using Differential Signal Standards

I/O Standard	V _{CCO} for Drivers		
	V, Min	V, Nom	V, Max
LVDS_33	3.0	3.3	3.45
LVDS_25	2.25	2.5	2.75
BLVDS_25	2.25	2.5	2.75
MINI_LVDS_33	3.0	3.3	3.45
MINI_LVDS_25	2.25	2.5	2.75
LVPECL_33 ⁽¹⁾	N/A—Inputs Only		
LVPECL_25	N/A—Inputs Only		
RSDS_33	3.0	3.3	3.45
RSDS_25	2.25	2.5	2.75
TMDS_33 ⁽¹⁾	3.14	3.3	3.45
PPDS_33	3.0	3.3	3.45
PPDS_25	2.25	2.5	2.75
DISPLAY_PORT	2.3	2.5	2.7
DIFF_MOBILE_DDR	1.7	1.8	1.9
DIFF_HSTL_I	1.4	1.5	1.6
DIFF_HSTL_II	1.4	1.5	1.6
DIFF_HSTL_III	1.4	1.5	1.6
DIFF_HSTL_I_18	1.7	1.8	1.9
DIFF_HSTL_II_18	1.7	1.8	1.9
DIFF_HSTL_III_18	1.7	1.8	1.9
DIFF_SSTL3_I	3.0	3.3	3.45
DIFF_SSTL3_II	3.0	3.3	3.45
DIFF_SSTL2_I	2.3	2.5	2.7
DIFF_SSTL2_II	2.3	2.5	2.7
DIFF_SSTL18_I	1.7	1.8	1.9
DIFF_SSTL18_II	1.7	1.8	1.9
DIFF_SSTL15_II	1.425	1.5	1.575

Notes:

1. LVPECL_33 and TMDS_33 inputs require V_{CCAUX} = 3.3V nominal.

In Table 9 and Table 10, values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: Single-Ended I/O Standard DC Input and Output Levels

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTTL	−0.5	0.8	2.0	4.1	0.4	2.4	Note 2	Note 2
LVC MOS33	−0.5	0.8	2.0	4.1	0.4	$V_{CCO} - 0.4$	Note 2	Note 2
LVC MOS25	−0.5	0.7	1.7	4.1	0.4	$V_{CCO} - 0.4$	Note 2	Note 2
LVC MOS18	−0.5	0.38	0.8	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS18 (−1L)	−0.5	0.33	0.71	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS18_JEDEC	−0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.45	$V_{CCO} - 0.45$	Note 2	Note 2
LVC MOS15	−0.5	0.38	0.8	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVC MOS15 (−1L)	−0.5	0.33	0.71	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVC MOS15_JEDEC	−0.5	35% V_{CCO}	65% V_{CCO}	4.1	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVC MOS12	−0.5	0.38	0.8	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
LVC MOS12 (−1L)	−0.5	0.33	0.71	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
LVC MOS12_JEDEC	−0.5	35% V_{CCO}	65% V_{CCO}	4.1	0.4	$V_{CCO} - 0.4$	Note 4	Note 4
PCI33_3	−0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	1.5	−0.5
PCI66_3	−0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	1.5	−0.5
I2C	−0.5	25% V_{CCO}	70% V_{CCO}	4.1	20% V_{CCO}	—	3	—
SMBUS	−0.5	0.8	2.1	4.1	0.4	—	4	—
SDIO	−0.5	12.5% V_{CCO}	75% V_{CCO}	4.1	12.5% V_{CCO}	75% V_{CCO}	0.1	−0.1
MOBILE_DDR	−0.5	20% V_{CCO}	80% V_{CCO}	4.1	10% V_{CCO}	90% V_{CCO}	0.1	−0.1
HSTL_I	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	8	−8
HSTL_II	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	16	−16
HSTL_III	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	24	−8
HSTL_I_18	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	11	−11
HSTL_II_18	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	22	−22
HSTL_III_18	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	0.4	$V_{CCO} - 0.4$	30	−11
SSTL3_I	−0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	4.1	$V_{TT} - 0.6$	$V_{TT} + 0.6$	8	−8
SSTL3_II	−0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	4.1	$V_{TT} - 0.8$	$V_{TT} + 0.8$	16	−16
SSTL2_I	−0.5	$V_{REF} - 0.15$	$V_{REF} + 0.15$	4.1	$V_{TT} - 0.61$	$V_{TT} + 0.61$	8.1	−8.1
SSTL2_II	−0.5	$V_{REF} - 0.15$	$V_{REF} + 0.15$	4.1	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	−16.2
SSTL18_I	−0.5	$V_{REF} - 0.125$	$V_{REF} + 0.125$	4.1	$V_{TT} - 0.47$	$V_{TT} + 0.47$	6.7	−6.7
SSTL18_II	−0.5	$V_{REF} - 0.125$	$V_{REF} + 0.125$	4.1	$V_{TT} - 0.60$	$V_{TT} + 0.60$	13.4	−13.4
SSTL15_II	−0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	4.1	$V_{TT} - 0.4$	$V_{TT} + 0.4$	13.4	−13.4

Notes:

1. Tested according to relevant specifications.
2. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
3. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
4. Using drive strengths of 2, 4, 6, 8, or 12 mA.
5. For more information, refer to [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 17: GTP Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	200	800	2000	mV
R_{IN}	Differential input resistance	80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult [UG386](#): *Spartan-6 FPGA GTP Transceivers User Guide* for further information.

Table 18: GTP Transceiver Performance

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
F_{GTPMAX}	Maximum GTP transceiver data rate	3.2	3.2	2.7	N/A	Gb/s
$F_{GTPRANGE1}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 1	1.88 to 3.2	1.88 to 3.2	1.88 to 2.7	N/A	Gb/s
$F_{GTPRANGE2}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 2	0.94 to 1.62	0.94 to 1.62	0.94 to 1.62	N/A	Gb/s
$F_{GTPRANGE3}$	GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 4	0.6 to 0.81	0.6 to 0.81	0.6 to 0.81	N/A	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	1.62	1.62	1.62	N/A	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	0.94	0.94	0.94	N/A	GHz

Table 19: GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
$F_{GTPDRCLK}$	GTP transceiver DCLK (DRP clock) maximum frequency	125	125	100	N/A	MHz

Table 20: GTP Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All LXT Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	160	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	μ s

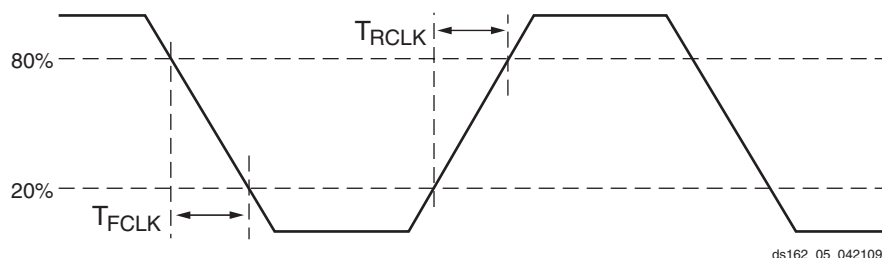


Figure 3: Reference Clock Timing Parameters

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
PPDS_33	1.17	1.29	1.42	1.68	1.57	1.71	1.91	2.43	3000	3000	3000	3000	ns
PPDS_25	1.01	1.13	1.26	1.56	1.68	1.82	2.02	2.47	3000	3000	3000	3000	ns
PCI33_3	1.07	1.19	1.32	1.57 ⁽²⁾	3.51	3.65	3.85	4.38 ⁽²⁾	3.51	3.65	3.85	4.38 ⁽¹⁾	ns
PCI66_3	1.07	1.19	1.32	1.57 ⁽²⁾	3.53	3.67	3.87	4.39 ⁽²⁾	3.53	3.67	3.87	4.39 ⁽¹⁾	ns
DISPLAY_PORT	1.02	1.14	1.27	1.56	3.15	3.29	3.49	4.08	3.15	3.29	3.49	4.08	ns
I2C	1.33	1.45	1.58	1.82	11.56	11.70	11.90	12.52	11.56	11.70	11.90	12.52	ns
SMBUS	1.33	1.45	1.58	1.82	11.56	11.70	11.90	12.52	11.56	11.70	11.90	12.52	ns
SDIO	1.36	1.48	1.61	1.84	2.64	2.78	2.98	3.60	2.64	2.78	2.98	3.60	ns
MOBILE_DDR	0.94	1.06	1.19	1.43	2.35	2.49	2.69	3.31	2.35	2.49	2.69	3.31	ns
HSTL_I	0.90	1.02	1.15	1.39	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
HSTL_II	0.91	1.03	1.16	1.40	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
HSTL_III	0.95	1.07	1.20	1.44	1.67	1.81	2.01	2.61	1.67	1.81	2.01	2.61	ns
HSTL_I_18	0.94	1.06	1.19	1.43	1.77	1.91	2.11	2.73	1.77	1.91	2.11	2.73	ns
HSTL_II_18	0.94	1.06	1.19	1.43	1.85	1.99	2.19	2.81	1.85	1.99	2.19	2.81	ns
HSTL_III_18	0.99	1.11	1.24	1.47	1.79	1.93	2.13	2.72	1.79	1.93	2.13	2.72	ns
SSTL3_I	1.58	1.70	1.83	2.16	1.83	1.97	2.17	2.72	1.83	1.97	2.17	2.72	ns
SSTL3_II	1.58	1.70	1.83	2.16	2.01	2.15	2.35	2.94	2.01	2.15	2.35	2.94	ns
SSTL2_I	1.30	1.42	1.55	1.87	1.77	1.91	2.11	2.69	1.77	1.91	2.11	2.69	ns
SSTL2_II	1.30	1.42	1.55	1.88	1.86	2.00	2.20	2.82	1.86	2.00	2.20	2.82	ns
SSTL18_I	0.92	1.04	1.17	1.41	1.63	1.77	1.97	2.59	1.63	1.77	1.97	2.59	ns
SSTL18_II	0.92	1.04	1.17	1.41	1.66	1.80	2.00	2.62	1.66	1.80	2.00	2.62	ns
SSTL15_II	0.92	1.04	1.17	1.41	1.67	1.81	2.01	2.63	1.67	1.81	2.01	2.63	ns
DIFF_HSTL_I	0.94	1.06	1.19	1.46	1.77	1.91	2.11	2.62	1.77	1.91	2.11	2.62	ns
DIFF_HSTL_II	0.93	1.05	1.18	1.45	1.72	1.86	2.06	2.54	1.72	1.86	2.06	2.54	ns
DIFF_HSTL_III	0.93	1.05	1.18	1.46	1.69	1.83	2.03	2.53	1.69	1.83	2.03	2.53	ns
DIFF_HSTL_I_18	0.97	1.09	1.22	1.50	1.79	1.93	2.13	2.63	1.79	1.93	2.13	2.63	ns
DIFF_HSTL_II_18	0.97	1.09	1.22	1.49	1.69	1.83	2.03	2.51	1.69	1.83	2.03	2.51	ns
DIFF_HSTL_III_18	0.97	1.09	1.22	1.50	1.69	1.83	2.03	2.53	1.69	1.83	2.03	2.53	ns
DIFF_SSTL3_I	1.18	1.30	1.43	1.68	1.81	1.95	2.15	2.64	1.81	1.95	2.15	2.64	ns
DIFF_SSTL3_II	1.19	1.31	1.44	1.68	1.80	1.94	2.14	2.63	1.80	1.94	2.14	2.63	ns
DIFF_SSTL2_I	1.02	1.14	1.27	1.57	1.80	1.94	2.14	2.62	1.80	1.94	2.14	2.62	ns
DIFF_SSTL2_II	1.02	1.14	1.27	1.57	1.76	1.90	2.10	2.57	1.76	1.90	2.10	2.57	ns
DIFF_SSTL18_I	0.97	1.09	1.22	1.51	1.72	1.86	2.06	2.56	1.72	1.86	2.06	2.56	ns
DIFF_SSTL18_II	0.98	1.10	1.23	1.50	1.68	1.82	2.02	2.52	1.68	1.82	2.02	2.52	ns
DIFF_SSTL15_II	0.94	1.06	1.19	1.46	1.67	1.81	2.01	2.50	1.67	1.81	2.01	2.50	ns
DIFF_MOBILE_DDR	0.97	1.09	1.22	1.51	1.75	1.89	2.09	2.57	1.75	1.89	2.09	2.57	ns

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVC MOS33, Fast, 8 mA	1.34	1.46	1.59	1.82	2.07	2.21	2.41	3.03	2.07	2.21	2.41	3.03	ns
LVC MOS33, Fast, 12 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns
LVC MOS33, Fast, 16 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns
LVC MOS33, Fast, 24 mA	1.34	1.46	1.59	1.82	1.65	1.79	1.99	2.62	1.65	1.79	1.99	2.62	ns
LVC MOS25, QUIETIO, 2 mA	0.82	0.94	1.07	1.31	4.81	4.95	5.15	5.79	4.81	4.95	5.15	5.79	ns
LVC MOS25, QUIETIO, 4 mA	0.82	0.94	1.07	1.31	3.70	3.84	4.04	4.66	3.70	3.84	4.04	4.66	ns
LVC MOS25, QUIETIO, 6 mA	0.82	0.94	1.07	1.31	3.46	3.60	3.80	4.38	3.46	3.60	3.80	4.38	ns
LVC MOS25, QUIETIO, 8 mA	0.82	0.94	1.07	1.31	3.20	3.34	3.54	4.12	3.20	3.34	3.54	4.12	ns
LVC MOS25, QUIETIO, 12 mA	0.82	0.94	1.07	1.31	2.83	2.97	3.17	3.75	2.83	2.97	3.17	3.75	ns
LVC MOS25, QUIETIO, 16 mA	0.82	0.94	1.07	1.31	2.64	2.78	2.98	3.64	2.64	2.78	2.98	3.64	ns
LVC MOS25, QUIETIO, 24 mA	0.82	0.94	1.07	1.31	2.45	2.59	2.79	3.42	2.45	2.59	2.79	3.42	ns
LVC MOS25, Slow, 2 mA	0.82	0.94	1.07	1.31	3.78	3.92	4.12	4.76	3.78	3.92	4.12	4.76	ns
LVC MOS25, Slow, 4 mA	0.82	0.94	1.07	1.31	2.79	2.93	3.13	3.73	2.79	2.93	3.13	3.73	ns
LVC MOS25, Slow, 6 mA	0.82	0.94	1.07	1.31	2.73	2.87	3.07	3.66	2.73	2.87	3.07	3.66	ns
LVC MOS25, Slow, 8 mA	0.82	0.94	1.07	1.31	2.48	2.62	2.82	3.42	2.48	2.62	2.82	3.42	ns
LVC MOS25, Slow, 12 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.95	2.01	2.15	2.35	2.95	ns
LVC MOS25, Slow, 16 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.95	2.01	2.15	2.35	2.95	ns
LVC MOS25, Slow, 24 mA	0.82	0.94	1.07	1.31	2.01	2.15	2.35	2.94	2.01	2.15	2.35	2.94	ns
LVC MOS25, Fast, 2 mA	0.82	0.94	1.07	1.31	3.35	3.49	3.69	4.31	3.35	3.49	3.69	4.31	ns
LVC MOS25, Fast, 4 mA	0.82	0.94	1.07	1.31	2.25	2.39	2.59	3.22	2.25	2.39	2.59	3.22	ns
LVC MOS25, Fast, 6 mA	0.82	0.94	1.07	1.31	2.09	2.23	2.43	3.05	2.09	2.23	2.43	3.05	ns
LVC MOS25, Fast, 8 mA	0.82	0.94	1.07	1.31	2.02	2.16	2.36	2.98	2.02	2.16	2.36	2.98	ns
LVC MOS25, Fast, 12 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns
LVC MOS25, Fast, 16 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns
LVC MOS25, Fast, 24 mA	0.82	0.94	1.07	1.31	1.56	1.70	1.90	2.52	1.56	1.70	1.90	2.52	ns
LVC MOS18, QUIETIO, 2 mA	1.18	1.30	1.43	2.04	5.92	6.06	6.26	6.80	5.92	6.06	6.26	6.80	ns
LVC MOS18, QUIETIO, 4 mA	1.18	1.30	1.43	2.04	4.74	4.88	5.08	5.63	4.74	4.88	5.08	5.63	ns
LVC MOS18, QUIETIO, 6 mA	1.18	1.30	1.43	2.04	4.05	4.19	4.39	4.96	4.05	4.19	4.39	4.96	ns
LVC MOS18, QUIETIO, 8 mA	1.18	1.30	1.43	2.04	3.71	3.85	4.05	4.63	3.71	3.85	4.05	4.63	ns
LVC MOS18, QUIETIO, 12 mA	1.18	1.30	1.43	2.04	3.35	3.49	3.69	4.27	3.35	3.49	3.69	4.27	ns
LVC MOS18, QUIETIO, 16 mA	1.18	1.30	1.43	2.04	3.20	3.34	3.54	4.14	3.20	3.34	3.54	4.14	ns
LVC MOS18, QUIETIO, 24 mA	1.18	1.30	1.43	2.04	2.96	3.10	3.30	3.98	2.96	3.10	3.30	3.98	ns
LVC MOS18, Slow, 2 mA	1.18	1.30	1.43	2.04	4.62	4.76	4.96	5.54	4.62	4.76	4.96	5.54	ns
LVC MOS18, Slow, 4 mA	1.18	1.30	1.43	2.04	3.69	3.83	4.03	4.60	3.69	3.83	4.03	4.60	ns
LVC MOS18, Slow, 6 mA	1.18	1.30	1.43	2.04	3.00	3.14	3.34	3.94	3.00	3.14	3.34	3.94	ns
LVC MOS18, Slow, 8 mA	1.18	1.30	1.43	2.04	2.19	2.33	2.53	3.17	2.19	2.33	2.53	3.17	ns
LVC MOS18, Slow, 12 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVC MOS18, Slow, 16 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	-3	-3N	-2	-1L ⁽¹⁾	
LVC MOS15, Slow, 8 mA	0.98	1.10	1.23	1.79	2.30	2.44	2.64	3.25	2.30	2.44	2.64	3.25	ns
LVC MOS15, Slow, 12 mA	0.98	1.10	1.23	1.79	2.03	2.17	2.37	2.99	2.03	2.17	2.37	2.99	ns
LVC MOS15, Slow, 16 mA	0.98	1.10	1.23	1.79	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVC MOS15, Fast, 2 mA	0.98	1.10	1.23	1.79	3.29	3.43	3.63	4.24	3.29	3.43	3.63	4.24	ns
LVC MOS15, Fast, 4 mA	0.98	1.10	1.23	1.79	2.27	2.41	2.61	3.22	2.27	2.41	2.61	3.22	ns
LVC MOS15, Fast, 6 mA	0.98	1.10	1.23	1.79	1.78	1.92	2.12	2.74	1.78	1.92	2.12	2.74	ns
LVC MOS15, Fast, 8 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.69	1.73	1.87	2.07	2.69	ns
LVC MOS15, Fast, 12 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.64	1.73	1.87	2.07	2.64	ns
LVC MOS15, Fast, 16 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.64	1.73	1.87	2.07	2.64	ns
LVC MOS15_JEDEC, QUIETIO, 2 mA	1.03	1.15	1.28	1.49	5.49	5.63	5.83	6.37	5.49	5.63	5.83	6.37	ns
LVC MOS15_JEDEC, QUIETIO, 4 mA	1.03	1.15	1.28	1.49	4.61	4.75	4.95	5.51	4.61	4.75	4.95	5.51	ns
LVC MOS15_JEDEC, QUIETIO, 6 mA	1.03	1.15	1.28	1.49	4.07	4.21	4.41	4.97	4.07	4.21	4.41	4.97	ns
LVC MOS15_JEDEC, QUIETIO, 8 mA	1.03	1.15	1.28	1.49	3.92	4.06	4.26	4.81	3.92	4.06	4.26	4.81	ns
LVC MOS15_JEDEC, QUIETIO, 12 mA	1.03	1.15	1.28	1.49	3.54	3.68	3.88	4.51	3.54	3.68	3.88	4.51	ns
LVC MOS15_JEDEC, QUIETIO, 16 mA	1.03	1.15	1.28	1.49	3.33	3.47	3.67	4.31	3.33	3.47	3.67	4.31	ns
LVC MOS15_JEDEC, Slow, 2 mA	1.03	1.15	1.28	1.49	4.18	4.32	4.52	5.13	4.18	4.32	4.52	5.13	ns
LVC MOS15_JEDEC, Slow, 4 mA	1.03	1.15	1.28	1.49	3.42	3.56	3.76	4.35	3.42	3.56	3.76	4.35	ns
LVC MOS15_JEDEC, Slow, 6 mA	1.03	1.15	1.28	1.49	2.29	2.43	2.63	3.25	2.29	2.43	2.63	3.25	ns
LVC MOS15_JEDEC, Slow, 8 mA	1.03	1.15	1.28	1.49	2.30	2.44	2.64	3.26	2.30	2.44	2.64	3.26	ns
LVC MOS15_JEDEC, Slow, 12 mA	1.03	1.15	1.28	1.49	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVC MOS15_JEDEC, Slow, 16 mA	1.03	1.15	1.28	1.49	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVC MOS15_JEDEC, Fast, 2 mA	1.03	1.15	1.28	1.49	3.28	3.42	3.62	4.22	3.28	3.42	3.62	4.22	ns
LVC MOS15_JEDEC, Fast, 4 mA	1.03	1.15	1.28	1.49	2.27	2.41	2.61	3.23	2.27	2.41	2.61	3.23	ns
LVC MOS15_JEDEC, Fast, 6 mA	1.03	1.15	1.28	1.49	1.78	1.92	2.12	2.74	1.78	1.92	2.12	2.74	ns
LVC MOS15_JEDEC, Fast, 8 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.69	1.73	1.87	2.07	2.69	ns
LVC MOS15_JEDEC, Fast, 12 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.63	1.73	1.87	2.07	2.63	ns
LVC MOS15_JEDEC, Fast, 16 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.63	1.73	1.87	2.07	2.63	ns
LVC MOS12, QUIETIO, 2 mA	0.91	1.03	1.16	1.51	6.40	6.54	6.74	7.30	6.40	6.54	6.74	7.30	ns
LVC MOS12, QUIETIO, 4 mA	0.91	1.03	1.16	1.51	4.98	5.12	5.32	5.90	4.98	5.12	5.32	5.90	ns
LVC MOS12, QUIETIO, 6 mA	0.91	1.03	1.16	1.51	4.65	4.79	4.99	5.55	4.65	4.79	4.99	5.55	ns
LVC MOS12, QUIETIO, 8 mA	0.91	1.03	1.16	1.51	4.23	4.37	4.57	5.21	4.23	4.37	4.57	5.21	ns
LVC MOS12, QUIETIO, 12 mA	0.91	1.03	1.16	1.51	3.98	4.12	4.32	4.94	3.98	4.12	4.32	4.94	ns
LVC MOS12, Slow, 2 mA	0.91	1.03	1.16	1.51	4.98	5.12	5.32	5.91	4.98	5.12	5.32	5.91	ns
LVC MOS12, Slow, 4 mA	0.91	1.03	1.16	1.51	2.84	2.98	3.18	3.81	2.84	2.98	3.18	3.81	ns
LVC MOS12, Slow, 6 mA	0.91	1.03	1.16	1.51	2.77	2.91	3.11	3.72	2.77	2.91	3.11	3.72	ns
LVC MOS12, Slow, 8 mA	0.91	1.03	1.16	1.51	2.34	2.48	2.68	3.31	2.34	2.48	2.68	3.31	ns
LVC MOS12, Slow, 12 mA	0.91	1.03	1.16	1.51	2.08	2.22	2.42	3.06	2.08	2.22	2.42	3.06	ns

I/O Standard Measurement Methodology

Input Delay Measurements

Table 31 shows the test setup parameters used for measuring input delay.

Table 31: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)}$	$V_H^{(1)}$	$V_{MEAS}^{(3)(4)}$	$V_{REF}^{(2)(4)}$
LVTTTL (Low-Voltage Transistor-Transistor Logic)	LVTTTL	0	3.0	1.4	—
LVC MOS (Low-Voltage CMOS), 3.3V	LVC MOS33	0	3.3	1.65	—
LVC MOS, 2.5V	LVC MOS25	0	2.5	1.25	—
LVC MOS, 1.8V	LVC MOS18	0	1.8	0.9	—
LVC MOS, 1.5V	LVC MOS15	0	1.5	0.75	—
LVC MOS, 1.2V	LVC MOS12	0	1.2	0.6	—
PCI (Peripheral Component Interface), 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3	Per PCI Specification			—
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III	HSTL_III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	1.1
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
SSTL, Class II, 1.5V	SSTL15_II	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	$1.25 - 0.125$	$1.25 + 0.125$	0 ⁽⁵⁾	—
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V & 3.3V	LVPECL_25, LVPECL_33	$1.2 - 0.3$	$1.2 + 0.3$	0 ⁽⁵⁾	—
BLVDS (Bus LVDS), 2.5V	BLVDS_25	$1.3 - 0.125$	$1.3 + 0.125$	0 ⁽⁵⁾	—
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	$1.2 - 0.125$	$1.2 + 0.125$	0 ⁽⁵⁾	—
RS DS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RS DS_25, RS DS_33	$1.2 - 0.1$	$1.2 + 0.1$	0 ⁽⁵⁾	—
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	$3.0 - 0.1$	$3.0 + 0.1$	0 ⁽⁵⁾	—
PPDS (Point-to-Point Differential Signaling), 2.5V & 3.3V	PPDS_25, PPDS_33	$1.25 - 0.1$	$1.25 + 0.1$	0 ⁽⁵⁾	—

Notes:

1. Input waveform switches between V_L and V_H .
2. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 4.
5. The value given is the differential input voltage.

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

V _{CCO}	I/O Standard	Drive	Slew	SSO Limit per V _{CCO} /GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
1.5V	LVCMOS15, LVCMOS15_JEDEC	2	Fast	33	40	33	41
			Slow	57	62	57	56
			QuietIO	70	67	70	66
		4	Fast	19	21	19	21
			Slow	30	30	30	24
			QuietIO	38	33	38	30
		6	Fast	14	16	14	16
			Slow	18	19	18	17
			QuietIO	27	24	27	21
		8	Fast	11	13	11	12
			Slow	16	16	16	14
			QuietIO	23	20	23	17
		12	Fast	N/A	5	N/A	4
			Slow	N/A	8	N/A	5
			QuietIO	N/A	10	N/A	9
		16	Fast	N/A	5	N/A	4
			Slow	N/A	8	N/A	8
			QuietIO	N/A	10	N/A	9
	HSTL_I			9	10	9	10
	HSTL_II			N/A	5	N/A	6
	HSTL_III			7	9	7	9
	DIFF_HSTL_I			27	30	27	30
	DIFF_HSTL_II			N/A	15	N/A	18
	DIFF_HSTL_III			21	27	21	27
	SSTL_15_II ⁽³⁾			N/A	5	N/A	4
	DIFF_SSTL_15_II ⁽³⁾			N/A	15	N/A	12

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

V _{CCO}	I/O Standard	Drive	Slew	SSO Limit per V _{CCO} /GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
3.3V	LVCMOS33	2	Fast	42	46	42	44
			Slow	50	55	50	49
			QuietIO	60	68	60	60
		4	Fast	21	27	21	25
			Slow	32	37	32	32
			QuietIO	39	42	39	37
		6	Fast	14	19	14	17
			Slow	19	25	19	22
			QuietIO	29	30	29	25
		8	Fast	11	15	11	14
			Slow	15	20	15	18
			QuietIO	25	24	25	20
		12	Fast	1	3	1	1
			Slow	2	5	2	2
			QuietIO	4	9	4	7
		16	Fast	1	2	1	1
			Slow	1	5	1	1
			QuietIO	3	10	3	8
		24	Fast	1	2	1	1
			Slow	2	5	2	1
			QuietIO	7	9	7	7

Input/Output Logic Switching Characteristics

Table 35: ILOGIC2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T _{ICE0CK} /T _{ICKCE0}	CE0 pin Setup/Hold with respect to CLK	0.56/ −0.30	0.56/ −0.25	0.79/ −0.22	1.21/ −0.52	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.74/ −0.23	0.74/ −0.22	0.98/ −0.20	1.31/ −0.45	ns
T _{IDOCK} /T _{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	1.19/ −0.83	1.36/ −0.83	1.73/ −0.83	2.18/ −1.77	ns
T _{IDOCKD} /T _{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	0.31/ 0.00	0.47/ 0.00	0.54/ 0.00	0.63/ −0.39	ns
Combinatorial						
T _{IDI}	D pin to O pin propagation delay, no Delay	0.95	1.28	1.53	2.25	ns
T _{IDID}	DDLY pin to O pin propagation delay (using IODELAY2)	0.23	0.39	0.44	0.74	ns
Sequential Delays						
T _{IDLO}	D pin to Q pin using flip-flop as a latch without Delay	1.56	1.86	2.39	3.49	ns
T _{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY2)	0.68	0.97	1.20	1.94	ns
T _{ICKQ}	CLK to Q outputs for XC devices	1.03	1.24	1.43	2.11	ns
	CLK to Q outputs for XA and XQ devices	1.38	N/A	1.78	2.11	ns
T _{RQ_ILOGIC2}	SR pin to Q outputs	1.81	1.81	2.50	3.05	ns

Table 36: OLOGIC2 Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T _{ODCK} /T _{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.81/ −0.05	0.86/ −0.05	1.18/ 0.00	1.73/ −0.27	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.75/ −0.10	0.75/ −0.10	1.01/ −0.05	1.66/ −0.23	ns
T _{OSRCK} /T _{OCKSR}	SR pin Setup/Hold with respect to CLK	0.70/ −0.28	0.79/ −0.28	1.03/ −0.23	1.39/ −0.47	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.24/ −0.08	0.56/ −0.06	0.83/ −0.01	0.99/ −0.19	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.58/ −0.06	0.72/ −0.06	1.18/ −0.01	1.51/ −0.13	ns
Sequential Delays						
T _{OCKQ}	CLK to OQ/TQ out for XC devices	0.48	0.51	0.74	0.74	ns
	CLK to OQ/TQ out for XA and XQ devices	0.85	N/A	1.16	0.74	ns
T _{RQ_OLOGIC2}	SR pin to OQ/TQ out	1.81	1.81	2.50	3.05	ns

Block RAM Switching Characteristics

Table 43: Block RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Block RAM Clock to Out Delays						
T _{RCKO_DO}	Clock CLK to DOUT output (without output register) ⁽¹⁾	1.85	2.10	2.10	3.50	ns, Max
T _{RCKO_DO_REG}	Clock CLK to DOUT output (with output register) ⁽²⁾	1.60	1.75	1.75	2.30	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{RCCK_ADDR} /T _{RCKC_ADDR}	ADDR inputs for XC devices ⁽³⁾	0.35/ 0.10	0.40/ 0.12	0.40/ 0.12	0.50/ 0.15	ns, Min
	ADDR inputs for XA and XQ devices ⁽³⁾	0.35/ 0.17	N/A	0.40/ 0.17	0.50/ 0.15	ns, Min
T _{RDCK_DI} /T _{RCKD_DI}	DIN inputs ⁽⁴⁾	0.30/ 0.10	0.30/ 0.10	0.30/ 0.10	0.40/ 0.15	ns, Min
T _{RCCK_EN} /T _{RCKC_EN}	Block RAM Enable (EN) input	0.22/ 0.05	0.25/ 0.06	0.25/ 0.06	0.44/ 0.10	ns, Min
T _{RCCK_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.20/ 0.10	0.20/ 0.10	0.20/ 0.10	0.28/ 0.15	ns, Min
T _{RCCK_WE} /T _{RCKC_WE}	Write Enable (WE) input	0.25/ 0.10	0.33/ 0.10	0.33/ 0.10	0.28/ 0.15	ns, Min
Maximum Frequency						
F _{MAX}	Block RAM in all modes	320	280	280	150	MHz

Notes:

1. T_{RCKO_DO} includes T_{RCKO_DOA} and T_{RCKO_DOPA} as well as the B port equivalent timing parameters.
2. $T_{RCKO_DO_REG}$ includes $T_{RCKO_DOA_REG}$ and $T_{RCKO_DOPA_REG}$ as well as the B port equivalent timing parameters.
3. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
4. T_{RDCK_DI} includes both A and B inputs as well as the parity inputs of A and B.

Table 45: Device DNA Interface Port Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T _{DNASSU}	Setup time on SHIFT before the rising edge of CLK	7				ns, Min
T _{DNASH}	Hold time on SHIFT after the rising edge of CLK	1				ns, Min
T _{DNADSU}	Setup time on DIN before the rising edge of CLK	7				ns, Min
T _{DNADH}	Hold time on DIN after the rising edge of CLK	1				ns, Min
T _{DNARSU}	Setup time on READ before the rising edge of CLK	7				ns, Min
		1,000				ns, Max
T _{DNARH}	Hold time on READ after the rising edge of CLK	1				ns, Min
T _{DNADCKO}	Clock-to-output delay on DOUT after rising edge of CLK	0.5				ns, Min
		6				ns, Max
T _{DNACKF} ⁽²⁾	CLK frequency	2				MHz, Max
T _{DNACKL}	CLK Low time	50				ns, Min
T _{DNACKH}	CLK High time	50				ns, Min

Notes:

1. The minimum READ pulse width is 8 ns, the maximum READ pulse width is 1 μ s.
2. Also applies to TCK when reading DNA through the boundary-scan port.

Table 46: Suspend Mode Switching Characteristics

Symbol	Description	Min	Max	Units
Entering Suspend Mode				
T _{SUSPENDHIGH_AWAKE}	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter	2.5	14	ns
T _{SUSPENDFILTER}	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled	31	430	ns
T _{SUSPEND_GWE}	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior (without glitch filter)	–	15	ns
T _{SUSPEND_GTS}	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements (without glitch filter)	–	15	ns
T _{SUSPEND_DISABLE}	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled (without glitch filter)	–	1500	ns
Exiting Suspend Mode				
T _{SUSPENDLOW_AWAKE}	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM or PLL lock time.	7	75	μ s
T _{SUSPEND_ENABLE}	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	7	41	μ s
T _{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using sw_clk:InternalClock and sw_gwe_cycle:1 .	–	80	ns
T _{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using sw_clk:InternalClock and sw_gwe_cycle:512 .	–	20.5	μ s
T _{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using sw_clk:InternalClock and sw_gts_cycle:1 .	–	80	ns
T _{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using sw_clk:InternalClock and sw_gts_cycle:512 .	–	20.5	μ s
T _{SCP_AWAKE}	Rising edge of SCP pins to rising edge of AWAKE pin	7	75	μ s

Clock Buffers and Networks

Table 48: Global Clock Switching Characteristics (BUFGMUX)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{GSI}	S pin Setup to I0/I1 inputs	LX devices	0.25	0.31	0.48	0.48	ns
		LXT devices	0.25	0.31	0.48	N/A	ns
T _{GIO}	BUFGMUX delay from I0/I1 to O	LX devices	0.21	0.21	0.21	0.21	ns
		LXT devices	0.21	0.21	0.21	N/A	ns
Maximum Frequency							
F _{MAX}	Global clock tree (BUFGMUX)	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 49: Input/Output Clock Switching Characteristics (BUFIO2)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T _{BUFCO_O}	Clock to out delay from I to O	LX devices	0.67	0.82	1.09	1.50	ns
		LXT devices	0.67	0.82	1.09	N/A	ns
Maximum Frequency							
F _{MAX}	I/O clock tree (BUFIO2)	LX devices	540	525	500	300	MHz
		LXT devices	540	525	500	N/A	MHz

Table 50: Input/Output Clock Switching Characteristics (BUFIO2FB)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
Maximum Frequency							
F _{MAX}	I/O clock tree (BUFIO2FB)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

Table 51: Input/Output Clock Switching Characteristics (BUFPLL)

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
Maximum Frequency							
F _{MAX}	BUFPLL clock tree (BUFPLL)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

PLL Switching Characteristics

Table 52: PLL Specification

Symbol	Description	Device ⁽¹⁾	Speed Grade				Units
			-3	-3N	-2	-1L	
F_{INMAX}	Maximum Input Clock Frequency from I/O Clock	LX devices	540	525	450	300	MHz
		LXT devices	540	525	450	N/A	MHz
	Maximum Input Clock Frequency from Global Clock	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

DCM Switching Characteristics

Table 53: Operating Frequency Ranges and Conditions for the Delay-Locked Loop (DLL)⁽¹⁾

Symbol	Description	Speed Grade								Units	
		-3		-3N		-2		-1L			
		Min	Max	Min	Max	Min	Max	Min	Max		
Input Frequency Ranges											
CLKIN_FREQ_DLL	Frequency of the CLKIN clock input when the CLKDV output is not used.	5 ⁽²⁾	280 ⁽³⁾	5 ⁽²⁾	280 ⁽³⁾	5 ⁽²⁾	250 ⁽³⁾	5 ⁽²⁾	175 ⁽³⁾	MHz	
	Frequency of the CLKIN clock input when using the CLKDV output.	5 ⁽²⁾	280 ⁽³⁾	5 ⁽²⁾	280 ⁽³⁾	5 ⁽²⁾	250 ⁽³⁾	5 ⁽²⁾	133 ⁽³⁾	MHz	
Input Pulse Requirements											
CLKIN_PULSE	CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL < 150 MHz	40	60	40	60	40	60	40	60	%	
	CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL > 150 MHz	45	55	45	55	45	55	45	55	%	
Input Clock Jitter Tolerance and Delay Path Variation ⁽⁴⁾											
CLKIN_CYC_JITT_DLL_LF	Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL < 150 MHz	–	±300	–	±300	–	±300	–	±300	ps	
CLKIN_CYC_JITT_DLL_HF	Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL > 150 MHz.	–	±150	–	±150	–	±150	–	±150	ps	
CLKIN_PER_JITT_DLL	Period jitter at the CLKIN input.	–	±1	–	±1	–	±1	–	±1	ns	
CLKFB_DELAY_VAR_EXT	Allowable variation of the off-chip feedback delay from the DCM output to the CLKFB input.	–	±1	–	±1	–	±1	–	±1	ns	

Notes:

- DLL specifications apply when using any of the DLL outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV.
- When operating independently of the DLL, the DFS supports lower CLKIN_FREQ_DLL frequencies. See Table 55.
- The CLKIN_DIVIDE_BY_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the F_{MAX} (see Table 48 and Table 49 for BUFG and BUFGIO2 limits). When used with CLK_FEEDBACK=2X, the input clock frequency matches the frequency for CLK2X, and is limited to CLKOUT_FREQ_2X.
- CLKIN_FREQ_DLL input jitter beyond these limits can cause the DCM to lose LOCK, indicated by the LOCKED output deasserting. The user must then reset the DCM.
- When using both DCMs in a CMT, both DCMs must be LOCKED.

Table 57: Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)⁽¹⁾ (Cont'd)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Spread Spectrum										
F _{CLKIN_FIXED_SPREAD_SPECTRUM}	Frequency of the CLKIN input for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD/ CENTER_HIGH_SPREAD)	30	200	30	200	30	200	30	200	MHz
T _{CENTER_LOW_SPREAD} ⁽⁶⁾	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD)	Typical = $\frac{100}{\text{CLKFX_DIVIDE}}$ Maximum = 250								ps
T _{CENTER_HIGH_SPREAD} ⁽⁶⁾	Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM= CENTER_HIGH_SPREAD)	Typical = $\frac{240}{\text{CLKFX_DIVIDE}}$ Maximum = 400								ps
F _{MOD_FIXED_SPREAD_SPECTRUM} ⁽⁶⁾	Average modulation frequency when using fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD / CENTER_HIGH_SPREAD)	Typical = F _{IN} /1024								MHz

Notes:

- The values in this table are based on the operating conditions described in Table 2 and Table 55.
- For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
- Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
- The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
- Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of $\pm(1\% \text{ of CLKFX period} + 200 \text{ ps})$. Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is $\pm(100 \text{ ps} + 200 \text{ ps}) = \pm 300 \text{ ps}$.
- When using CENTER_LOW_SPREAD, CENTER_HIGH_SPREAD, the valid values for CLKFX_MULTIPLY are limited to 2 through 32, and the valid values for CLKFX_DIVIDE are limited to 1 through 4.

Table 58: Recommended Operating Conditions for the Phase-Shift Clock in Variable Phase Mode (DCM_SP) or Dynamic Frequency Synthesis (DCM_CLKGEN)

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Operating Frequency Ranges										
PSCLK_FREQ	Frequency for the PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) input.	1	167	1	167	1	167	1	100	MHz
Input Pulse Requirements										
PSCLK_PULSE	PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) pulse width as a percentage of the clock period.	40	60	40	60	40	60	40	60	%

Table 64: Global Clock Input to Output Delay With DCM in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in System-Synchronous Mode.							
T _{ICKOFDCM}	Global Clock and OUTFF <i>with</i> DCM	XC6SLX4	4.23	N/A	6.11	6.60	ns
		XC6SLX9	4.23	5.17	6.11	6.60	ns
		XC6SLX16	4.28	4.57	5.34	6.36	ns
		XC6SLX25	3.95	4.18	4.59	6.91	ns
		XC6SLX25T	3.95	4.18	4.59	N/A	ns
		XC6SLX45	4.37	4.70	5.50	6.85	ns
		XC6SLX45T	4.37	4.70	5.50	N/A	ns
		XC6SLX75	3.90	4.23	4.77	6.31	ns
		XC6SLX75T	3.90	4.23	4.77	N/A	ns
		XC6SLX100	3.86	4.16	4.66	7.25	ns
		XC6SLX100T	3.90	4.16	4.66	N/A	ns
		XC6SLX150	4.03	4.33	4.83	6.63	ns
		XC6SLX150T	4.03	4.33	4.83	N/A	ns
		XA6SLX4	4.55	N/A	6.11	N/A	ns
		XA6SLX9	4.55	N/A	6.11	N/A	ns
		XA6SLX16	4.62	N/A	5.33	N/A	ns
		XA6SLX25	4.27	N/A	4.59	N/A	ns
		XA6SLX25T	4.27	N/A	4.69	N/A	ns
		XA6SLX45	4.69	N/A	5.50	N/A	ns
		XA6SLX45T	4.69	N/A	5.50	N/A	ns
		XA6SLX75	4.22	N/A	4.77	N/A	ns
		XA6SLX75T	4.22	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.34	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	6.31	ns
		XQ6SLX75T	4.22	N/A	4.77	N/A	ns
		XQ6SLX150	N/A	N/A	4.96	6.63	ns
		XQ6SLX150T	4.62	N/A	4.96	N/A	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
- DCM output jitter is already included in the timing calculation.

Table 66: Global Clock Input to Output Delay With PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> PLL in System-Synchronous Mode.							
T _{ICKOFFPLL}	Global Clock and OUTFF <i>with</i> PLL	XC6SLX4	4.57	N/A	6.25	7.34	ns
		XC6SLX9	4.57	5.25	6.25	7.34	ns
		XC6SLX16	4.41	4.64	5.39	6.92	ns
		XC6SLX25	4.03	4.32	4.91	7.64	ns
		XC6SLX25T	4.03	4.32	4.91	N/A	ns
		XC6SLX45	4.63	4.96	5.75	7.36	ns
		XC6SLX45T	4.63	4.96	5.75	N/A	ns
		XC6SLX75	4.01	4.30	4.88	7.15	ns
		XC6SLX75T	4.01	4.30	4.88	N/A	ns
		XC6SLX100	4.02	4.33	4.90	7.37	ns
		XC6SLX100T	4.06	4.33	4.90	N/A	ns
		XC6SLX150	3.65	3.98	4.58	6.94	ns
		XC6SLX150T	3.65	3.98	4.58	N/A	ns
		XA6SLX4	4.88	N/A	6.13	N/A	ns
		XA6SLX9	4.88	N/A	6.13	N/A	ns
		XA6SLX16	4.74	N/A	5.27	N/A	ns
		XA6SLX25	4.43	N/A	4.78	N/A	ns
		XA6SLX25T	4.43	N/A	4.88	N/A	ns
		XA6SLX45	4.94	N/A	5.62	N/A	ns
		XA6SLX45T	4.94	N/A	5.62	N/A	ns
		XA6SLX75	4.32	N/A	4.77	N/A	ns
		XA6SLX75T	4.32	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.41	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	7.15	ns
		XQ6SLX75T	4.32	N/A	4.77	N/A	ns
		XQ6SLX150	N/A	N/A	4.60	6.94	ns
		XQ6SLX150T	4.35	N/A	4.60	N/A	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
- PLL output jitter is included in the timing calculation.

Table 74: Global Clock Setup and Hold With PLL in System-Synchronous Mode

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.(1)							
T _{PSPLL} / T _{PHPLL}	No Delay Global Clock and IFF(2) with PLL in System-Synchronous Mode	XC6SLX4	1.37/0.25	N/A	1.52/0.41	2.07/0.69	ns
		XC6SLX9	1.37/0.21	1.48/0.21	1.52/0.26	2.07/0.69	ns
		XC6SLX16	1.33/−0.03	1.53/−0.02	1.60/−0.02	1.57/0.48	ns
		XC6SLX25	1.65/0.28	1.71/0.28	1.91/0.28	2.44/0.76	ns
		XC6SLX25T	1.65/0.28	1.71/0.28	1.91/0.28	N/A	ns
		XC6SLX45	1.55/0.18	1.64/0.18	1.75/0.18	2.02/0.90	ns
		XC6SLX45T	1.55/0.18	1.64/0.18	1.75/0.18	N/A	ns
		XC6SLX75	1.77/0.21	1.89/0.21	2.13/0.21	2.46/0.53	ns
		XC6SLX75T	1.77/0.21	1.89/0.21	2.13/0.21	N/A	ns
		XC6SLX100	1.44/0.32	1.52/0.32	1.70/0.32	1.78/0.86	ns
		XC6SLX100T	1.44/0.32	1.52/0.32	1.70/0.32	N/A	ns
		XC6SLX150	1.39/0.49	1.48/0.49	1.67/0.49	1.94/0.94	ns
		XC6SLX150T	1.39/0.49	1.48/0.49	1.67/0.49	N/A	ns
		XA6SLX4	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX9	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX16	1.89/−0.08	N/A	1.72/−0.08	N/A	ns
		XA6SLX25	1.85/0.16	N/A	2.08/0.16	N/A	ns
		XA6SLX25T	1.85/0.16	N/A	2.17/0.16	N/A	ns
		XA6SLX45	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX45T	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX75	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX100	N/A	N/A	2.34/0.14	N/A	ns
		XQ6SLX75	N/A	N/A	2.25/0.06	2.46/0.53	ns
		XQ6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XQ6SLX150	N/A	N/A	1.79/0.37	1.94/0.94	ns
		XQ6SLX150T	1.43/0.37	N/A	1.79/0.37	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.