AMD Xilinx - XC6SLX9-N3CSG324C Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	715
Number of Logic Elements/Cells	9152
Total RAM Bits	589824
Number of I/O	200
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-LFBGA, CSPBGA
Supplier Device Package	324-CSPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6slx9-n3csg324c

Table 1: **Absolute Maximum Ratings(1)** ***(Cont'd)***

Symbol	Description					Units
V_{IN} and V_{TS}(3)	I/O input voltage or voltage applied to 3-state output, relative to GND(4)	All user and dedicated I/Os	Commercial	DC	–0.60 to 4.10	V
				20% overshoot duration	–0.75 to 4.25	V
				8% overshoot duration(5)	–0.75 to 4.40	V
			Industrial	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration(5)	–0.75 to 4.40	V
			Expanded (Q)	DC	–0.60 to 3.95	V
				20% overshoot duration	–0.75 to 4.15	V
				4% overshoot duration(5)	–0.75 to 4.40	V
		Restricted to maximum of 100 user I/Os	Commercial	20% overshoot duration	–0.75 to 4.35	V
				15% overshoot duration(5)	–0.75 to 4.40	V
				10% overshoot duration	–0.75 to 4.45	V
			Industrial	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration(5)	–0.75 to 4.40	V
			Expanded (Q)	20% overshoot duration	–0.75 to 4.25	V
				10% overshoot duration	–0.75 to 4.35	V
				8% overshoot duration(5)	–0.75 to 4.40	V
T_{STG}	Storage temperature (ambient)				–65 to 150	°C
T_{SOL}	Maximum soldering temperature(6) (TQG144, CPG196, CSG225, CSG324, CSG484, and FTG256)				+260	°C
	Maximum soldering temperature(6) (Pb-free packages: FGG484, FGG676, and FGG900)				+250	°C
	Maximum soldering temperature(6) (Pb packages: CS484, FT256, FG484, FG676, and FG900)				+220	°C
T_j	Maximum junction temperature(6)				+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When programming eFUSE, $V_{FS} \leq V_{CCAUX}$. Requires up to 40 mA current. For read mode, V_{FS} can be between GND and 3.45 V.
3. I/O absolute maximum limit applied to DC and AC signals. Overshoot duration is the percentage of a data period that the I/O is stressed beyond 3.45V.
4. For I/O operation, refer to UG381: *Spartan-6 FPGA SelectIO Resources User Guide*.
5. Maximum percent overshoot duration to meet 4.40V maximum.
6. For soldering guidelines and thermal considerations, see UG385: *Spartan-6 FPGA Packaging and Pinout Specification*.

Table 3: **eFUSE Programming Conditions**(1)

Symbol	Description	Min	Typ	Max	Units
V_{FS}(2)	External voltage supply	3.2	3.3	3.4	V
I_{FS}	V_{FS} supply current	–	–	40	mA
V_{CCAUX}	Auxiliary supply voltage relative to GND	3.2	3.3	3.45	V
R_{FUSE}(3)	External resistor from R_{FUSE} pin to GND	1129	1140	1151	Ω
V_{CCINT}	Internal supply voltage relative to GND	1.14	1.2	1.26	V
t_j	Temperature range	15	–	85	°C

Notes:

1. These specifications apply during programming of the eFUSE AES key. Programming is only supported through JTAG.The AES key is only supported in the following devices: LX75, LX75T, LX100, LX100T, LX150, and LX150T.
2. When programming eFUSE, V_{FS} must be less than or equal to V_{CCAUX}. When not programming or when eFUSE is not used, Xilinx recommends connecting V_{FS} to GND. However, V_{FS} can be between GND and 3.45 V.
3. An R_{FUSE} resistor is required when programming the eFUSE AES key. When not programming or when eFUSE is not used, Xilinx recommends connecting the R_{FUSE} pin to V_{CCAUX} or GND. However, R_{FUSE} can be unconnected.

Table 4: **DC Characteristics Over Recommended Operating Conditions**

<table>
<tr><th>Symbol</th><th colspan="2">Description</th><th>Min</th><th>Typ</th><th>Max</th><th>Units</th></tr>
<tr><td>V_{DRINT}</td><td colspan="2">Data retention V_{CCINT} voltage (below which configuration data might be lost)</td><td>0.8</td><td>–</td><td>–</td><td>V</td></tr>
<tr><td>V_{DRAUX}</td><td colspan="2">Data retention V_{CCAUX} voltage (below which configuration data might be lost)</td><td>2.0</td><td>–</td><td>–</td><td>V</td></tr>
<tr><td rowspan="2">I_{REF}</td><td colspan="2">V_{REF} leakage current per pin for commercial (C) and industrial (I) devices</td><td>–10</td><td>–</td><td>10</td><td>µA</td></tr>
<tr><td colspan="2">V_{REF} leakage current per pin for expanded (Q) devices</td><td>–15</td><td>–</td><td>15</td><td>µA</td></tr>
<tr><td rowspan="2">I_L</td><td colspan="2">Input or output leakage current per pin (sample-tested) for commercial (C) and industrial (I) devices</td><td>–10</td><td>–</td><td>10</td><td>µA</td></tr>
<tr><td colspan="2">Input or output leakage current per pin (sample-tested) for expanded (Q) devices</td><td>–15</td><td>–</td><td>15</td><td>µA</td></tr>
<tr><td rowspan="2">I_{HS}</td><td rowspan="2">Leakage current on pins during hot socketing with FPGA unpowered</td><td>All pins except PROGRAM_B, DONE, and JTAG pins when HSWAPEN = 1</td><td>–20</td><td>–</td><td>20</td><td>µA</td></tr>
<tr><td>PROGRAM_B, DONE, and JTAG pins, or other pins when HSWAPEN = 0</td><td colspan="3">$I_{HS} + I_{RPU}$</td><td>µA</td></tr>
<tr><td>C_{IN}[1]</td><td colspan="2">Die input capacitance at the pad</td><td>–</td><td>–</td><td>10</td><td>pF</td></tr>
<tr><td rowspan="5">I_{RPU}</td><td colspan="2">Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V or V_{CCAUX} = 3.3V</td><td>200</td><td>–</td><td>500</td><td>µA</td></tr>
<tr><td colspan="2">Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V or V_{CCAUX} = 2.5V</td><td>120</td><td>–</td><td>350</td><td>µA</td></tr>
<tr><td colspan="2">Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V</td><td>60</td><td>–</td><td>200</td><td>µA</td></tr>
<tr><td colspan="2">Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V</td><td>40</td><td>–</td><td>150</td><td>µA</td></tr>
<tr><td colspan="2">Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V</td><td>12</td><td>–</td><td>100</td><td>µA</td></tr>
<tr><td rowspan="2">I_{RPD}</td><td colspan="2">Pad pull-down (when selected) @ V_{IN} = V_{CCO}, V_{CCAUX} = 3.3V</td><td>200</td><td>–</td><td>550</td><td>µA</td></tr>
<tr><td colspan="2">Pad pull-down (when selected) @ V_{IN} = V_{CCO}, V_{CCAUX} = 2.5V</td><td>140</td><td>–</td><td>400</td><td>µA</td></tr>
<tr><td>I_{BATT}[2]</td><td colspan="2">Battery supply current</td><td>–</td><td>–</td><td>150</td><td>nA</td></tr>
<tr><td>R_{DT}[3]</td><td colspan="2">Resistance of optional input differential termination circuit, V_{CCAUX} = 3.3V</td><td>–</td><td>100</td><td>–</td><td>Ω</td></tr>
<tr><td rowspan="6">R_{IN_TERM}[5]</td><td colspan="2">Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for commercial (C) and industrial (I) devices</td><td>23</td><td>25</td><td>55</td><td>Ω</td></tr>
<tr><td colspan="2">Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for expanded (Q) devices</td><td>20</td><td>25</td><td>55</td><td>Ω</td></tr>
<tr><td colspan="2">Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for commercial (C) and industrial (I) devices</td><td>39</td><td>50</td><td>72</td><td>Ω</td></tr>
<tr><td colspan="2">Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for expanded (Q) devices</td><td>32</td><td>50</td><td>74</td><td>Ω</td></tr>
<tr><td colspan="2">Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for commercial (C) and industrial (I) devices</td><td>56</td><td>75</td><td>109</td><td>Ω</td></tr>
<tr><td colspan="2">Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for expanded (Q) devices</td><td>47</td><td>75</td><td>115</td><td>Ω</td></tr>
<tr><td rowspan="3">R_{OUT_TERM}</td><td colspan="2">Thevenin equivalent resistance of programmable output termination (UNTUNED_25)</td><td>11</td><td>25</td><td>52</td><td>Ω</td></tr>
<tr><td colspan="2">Thevenin equivalent resistance of programmable output termination (UNTUNED_50)</td><td>21</td><td>50</td><td>96</td><td>Ω</td></tr>
<tr><td colspan="2">Thevenin equivalent resistance of programmable output termination (UNTUNED_75)</td><td>29</td><td>75</td><td>145</td><td>Ω</td></tr>
</table>

Notes:

1. The C_{IN} measurement represents the die capacitance at the pad, not including the package.
2. Maximum value specified for worst case process at 25°C. LX75, LX75T, LX100, LX100T, LX150, and LX150T only.
3. Refer to IBIS models for R_{DT} variation and for values at V_{CCAUX} = 2.5V. IBIS values for R_{DT} are valid for all temperature ranges.
4. V_{CCO2} is not required for data retention. The minimum V_{CCO2} for power-on reset and configuration is 1.65V.
5. Termination resistance to a V_{CCO}/2 level.

Table 21: **GTP Transceiver User Clock Switching Characteristics[(1)]**

Symbol	Description	Conditions	Speed Grade				Units
			-3	-3N	-2	-1L	
F_{TXOUT}	TXOUTCLK maximum frequency		320	320	270	N/A	MHz
F_{RXREC}	RXRECCLK maximum frequency		320	320	270	N/A	MHz
T_{RX}	RXUSRCLK maximum frequency		320	320	270	N/A	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz
T_{TX}	TXUSRCLK maximum frequency		320	320	270	N/A	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	156.25	156.25	125	N/A	MHz
		2 byte interface	160	160	125	N/A	MHz
		4 byte interface	80	80	67.5	N/A	MHz

Notes:

1. Clocking must be implemented as described in UG386: *Spartan-6 FPGA GTP Transceivers User Guide*.

Table 22: **GTP Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
T_{RTX}	TX Rise time	20%–80%	–	140	–	ps
T_{FTX}	TX Fall time	80%–20%	–	120	–	ps
T_{LLSKEW}	TX lane-to-lane skew[(1)]		–	–	400	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	20	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	50	ns
$T_{J3.125}$	Total Jitter[(2)]	3.125 Gb/s	–	–	0.35	UI
$D_{J3.125}$	Deterministic Jitter[(2)]		–	–	0.15	UI
$T_{J2.5}$	Total Jitter[(2)]	2.5 Gb/s	–	–	0.33	UI
$D_{J2.5}$	Deterministic Jitter[(2)]		–	–	0.15	UI
$T_{J1.62}$	Total Jitter[(2)]	1.62 Gb/s	–	–	0.20	UI
$D_{J1.62}$	Deterministic Jitter[(2)]		–	–	0.10	UI
$T_{J1.25}$	Total Jitter[(2)]	1.25 Gb/s	–	–	0.20	UI
$D_{J1.25}$	Deterministic Jitter[(2)]		–	–	0.10	UI
T_{J614}	Total Jitter[(2)]	614 Mb/s	–	–	0.10	UI
D_{J614}	Deterministic Jitter[(2)]		–	–	0.05	UI

Notes:

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP transceiver sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.

Table 27: **Spartan-6 Device Production Software and Speed Specification Release[1] *(Cont'd)***

Device	Speed Grade Designations[2]			
	-3[3]	-3N	-2[4]	-1L
XQ6SLX75	N/A	N/A	ISE 13.2 v1.19	ISE 13.2 v1.07
XQ6SLX75T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A
XQ6SLX150	N/A	N/A	ISE 13.2 v1.19	ISE 13.2 v1.07
XQ6SLX150T	ISE 13.2 v1.19	N/A	ISE 13.2 v1.19	N/A

Notes:

1. ISE 13.3 software with v1.20 for -3, -3N, and -2; and v1.08 for -1L speed specification reflects the changes outlined in XCN11028: *Spartan-6 FPGA Speed File Changes*.
2. As marked with an N/A, LXT devices and all XA devices are not available with a -1L speed grade; LX4 devices and all XA and XQ devices are not available with a -3N speed grade.
3. Improved -3 specifications reflected in this data sheet require ISE 12.4 software with v1.15 speed specification.
4. Improved -2 specifications reflected in this data sheet require ISE 12.4 software and the *12.4 Speed Files Patch* which contains the v1.17 speed specification available on the Xilinx Download Center.
5. ISE 12.3 software with v1.12 speed specification is available using ISE 12.3 software and the *12.3 Speed Files Patch* available on the Xilinx Download Center.
6. ISE 12.2 software with v1.11 speed specification is available using ISE 12.2 software and the *12.2 Speed Files Patch* available on the Xilinx Download Center.
7. ISE 13.1 software with v1.18 speed specification is available using ISE 13.1 software and the *13.1 Update* available on the Xilinx Download Center. See XCN11012: *Speed File Change for -3N Devices*.

IOB Pad Input/Output/3-State Switching Characteristics

Table 28 (for commercial (XC) Spartan-6 devices) and Table 29 (for Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices) summarizes the values of standard-specific data input delays, output delays terminating at pads (based on standard), and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

See the TRACE report for further information on delays when using an I/O standard with UNTUNED termination on inputs or outputs.

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	-3	-3N	-2	-1L[1]	
LVDS_33	1.17	1.29	1.42	1.68	1.55	1.69	1.89	2.42	3000	3000	3000	3000	ns
LVDS_25	1.01	1.13	1.26	1.57	1.65	1.79	1.99	2.47	3000	3000	3000	3000	ns
BLVDS_25	1.02	1.14	1.27	1.57	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
MINI_LVDS_33	1.17	1.29	1.42	1.68	1.57	1.71	1.91	2.41	3000	3000	3000	3000	ns
MINI_LVDS_25	1.01	1.13	1.26	1.57	1.65	1.79	1.99	2.47	3000	3000	3000	3000	ns
LVPECL_33	1.18	1.30	1.43	1.68	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL_25	1.02	1.14	1.27	1.57	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
RSDS_33 (point to point)	1.17	1.29	1.42	1.68	1.57	1.71	1.91	2.42	3000	3000	3000	3000	ns
RSDS_25 (point to point)	1.01	1.13	1.26	1.56	1.65	1.79	1.99	2.47	3000	3000	3000	3000	ns
TMDS_33	1.21	1.33	1.46	1.71	1.54	1.68	1.88	2.50	3000	3000	3000	3000	ns

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L(1)	-3	-3N	-2	-1L(1)	-3	-3N	-2	-1L(1)	
LVCMOS18, Slow, 24 mA	1.18	1.30	1.43	2.04	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18, Fast, 2 mA	1.18	1.30	1.43	2.04	3.59	3.73	3.93	4.53	3.59	3.73	3.93	4.53	ns
LVCMOS18, Fast, 4 mA	1.18	1.30	1.43	2.04	2.39	2.53	2.73	3.35	2.39	2.53	2.73	3.35	ns
LVCMOS18, Fast, 6 mA	1.18	1.30	1.43	2.04	1.88	2.02	2.22	2.84	1.88	2.02	2.22	2.84	ns
LVCMOS18, Fast, 8 mA	1.18	1.30	1.43	2.04	1.81	1.95	2.15	2.77	1.81	1.95	2.15	2.77	ns
LVCMOS18, Fast, 12 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVCMOS18, Fast, 16 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVCMOS18, Fast, 24 mA	1.18	1.30	1.43	2.04	1.71	1.85	2.05	2.67	1.71	1.85	2.05	2.67	ns
LVCMOS18_JEDEC, QUIETIO, 2 mA	0.94	1.06	1.19	1.41	5.91	6.05	6.25	6.79	5.91	6.05	6.25	6.79	ns
LVCMOS18_JEDEC, QUIETIO, 4 mA	0.94	1.06	1.19	1.41	4.75	4.89	5.09	5.64	4.75	4.89	5.09	5.64	ns
LVCMOS18_JEDEC, QUIETIO, 6 mA	0.94	1.06	1.19	1.41	4.04	4.18	4.38	4.96	4.04	4.18	4.38	4.96	ns
LVCMOS18_JEDEC, QUIETIO, 8 mA	0.94	1.06	1.19	1.41	3.71	3.85	4.05	4.62	3.71	3.85	4.05	4.62	ns
LVCMOS18_JEDEC, QUIETIO, 12 mA	0.94	1.06	1.19	1.41	3.35	3.49	3.69	4.28	3.35	3.49	3.69	4.28	ns
LVCMOS18_JEDEC, QUIETIO, 16 mA	0.94	1.06	1.19	1.41	3.20	3.34	3.54	4.13	3.20	3.34	3.54	4.13	ns
LVCMOS18_JEDEC, QUIETIO, 24 mA	0.94	1.06	1.19	1.41	2.96	3.10	3.30	3.98	2.96	3.10	3.30	3.98	ns
LVCMOS18_JEDEC, Slow, 2 mA	0.94	1.06	1.19	1.41	4.59	4.73	4.93	5.54	4.59	4.73	4.93	5.54	ns
LVCMOS18_JEDEC, Slow, 4 mA	0.94	1.06	1.19	1.41	3.69	3.83	4.03	4.60	3.69	3.83	4.03	4.60	ns
LVCMOS18_JEDEC, Slow, 6 mA	0.94	1.06	1.19	1.41	3.00	3.14	3.34	3.94	3.00	3.14	3.34	3.94	ns
LVCMOS18_JEDEC, Slow, 8 mA	0.94	1.06	1.19	1.41	2.19	2.33	2.53	3.18	2.19	2.33	2.53	3.18	ns
LVCMOS18_JEDEC, Slow, 12 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18_JEDEC, Slow, 16 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18_JEDEC, Slow, 24 mA	0.94	1.06	1.19	1.41	1.99	2.13	2.33	2.95	1.99	2.13	2.33	2.95	ns
LVCMOS18_JEDEC, Fast, 2 mA	0.94	1.06	1.19	1.41	3.57	3.71	3.91	4.52	3.57	3.71	3.91	4.52	ns
LVCMOS18_JEDEC, Fast, 4 mA	0.94	1.06	1.19	1.41	2.39	2.53	2.73	3.35	2.39	2.53	2.73	3.35	ns
LVCMOS18_JEDEC, Fast, 6 mA	0.94	1.06	1.19	1.41	1.88	2.02	2.22	2.84	1.88	2.02	2.22	2.84	ns
LVCMOS18_JEDEC, Fast, 8 mA	0.94	1.06	1.19	1.41	1.80	1.94	2.14	2.76	1.80	1.94	2.14	2.76	ns
LVCMOS18_JEDEC, Fast, 12 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVCMOS18_JEDEC, Fast, 16 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVCMOS18_JEDEC, Fast, 24 mA	0.94	1.06	1.19	1.41	1.72	1.86	2.06	2.68	1.72	1.86	2.06	2.68	ns
LVCMOS15, QUIETIO, 2 mA	0.98	1.10	1.23	1.79	5.47	5.61	5.81	6.38	5.47	5.61	5.81	6.38	ns
LVCMOS15, QUIETIO, 4 mA	0.98	1.10	1.23	1.79	4.61	4.75	4.95	5.51	4.61	4.75	4.95	5.51	ns
LVCMOS15, QUIETIO, 6 mA	0.98	1.10	1.23	1.79	4.07	4.21	4.41	4.97	4.07	4.21	4.41	4.97	ns
LVCMOS15, QUIETIO, 8 mA	0.98	1.10	1.23	1.79	3.91	4.05	4.25	4.81	3.91	4.05	4.25	4.81	ns
LVCMOS15, QUIETIO, 12 mA	0.98	1.10	1.23	1.79	3.53	3.67	3.87	4.51	3.53	3.67	3.87	4.51	ns
LVCMOS15, QUIETIO, 16 mA	0.98	1.10	1.23	1.79	3.32	3.46	3.66	4.31	3.32	3.46	3.66	4.31	ns
LVCMOS15, Slow, 2 mA	0.98	1.10	1.23	1.79	4.18	4.32	4.52	5.11	4.18	4.32	4.52	5.11	ns
LVCMOS15, Slow, 4 mA	0.98	1.10	1.23	1.79	3.42	3.56	3.76	4.34	3.42	3.56	3.76	4.34	ns
LVCMOS15, Slow, 6 mA	0.98	1.10	1.23	1.79	2.29	2.43	2.63	3.24	2.29	2.43	2.63	3.24	ns

Table 28: **IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-3N	-2	-1L(1)	-3	-3N	-2	-1L(1)	-3	-3N	-2	-1L(1)	
LVCMOS15, Slow, 8 mA	0.98	1.10	1.23	1.79	2.30	2.44	2.64	3.25	2.30	2.44	2.64	3.25	ns
LVCMOS15, Slow, 12 mA	0.98	1.10	1.23	1.79	2.03	2.17	2.37	2.99	2.03	2.17	2.37	2.99	ns
LVCMOS15, Slow, 16 mA	0.98	1.10	1.23	1.79	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVCMOS15, Fast, 2 mA	0.98	1.10	1.23	1.79	3.29	3.43	3.63	4.24	3.29	3.43	3.63	4.24	ns
LVCMOS15, Fast, 4 mA	0.98	1.10	1.23	1.79	2.27	2.41	2.61	3.22	2.27	2.41	2.61	3.22	ns
LVCMOS15, Fast, 6 mA	0.98	1.10	1.23	1.79	1.78	1.92	2.12	2.74	1.78	1.92	2.12	2.74	ns
LVCMOS15, Fast, 8 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.69	1.73	1.87	2.07	2.69	ns
LVCMOS15, Fast, 12 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.64	1.73	1.87	2.07	2.64	ns
LVCMOS15, Fast, 16 mA	0.98	1.10	1.23	1.79	1.73	1.87	2.07	2.64	1.73	1.87	2.07	2.64	ns
LVCMOS15_JEDEC, QUIETIO, 2 mA	1.03	1.15	1.28	1.49	5.49	5.63	5.83	6.37	5.49	5.63	5.83	6.37	ns
LVCMOS15_JEDEC, QUIETIO, 4 mA	1.03	1.15	1.28	1.49	4.61	4.75	4.95	5.51	4.61	4.75	4.95	5.51	ns
LVCMOS15_JEDEC, QUIETIO, 6 mA	1.03	1.15	1.28	1.49	4.07	4.21	4.41	4.97	4.07	4.21	4.41	4.97	ns
LVCMOS15_JEDEC, QUIETIO, 8 mA	1.03	1.15	1.28	1.49	3.92	4.06	4.26	4.81	3.92	4.06	4.26	4.81	ns
LVCMOS15_JEDEC, QUIETIO, 12 mA	1.03	1.15	1.28	1.49	3.54	3.68	3.88	4.51	3.54	3.68	3.88	4.51	ns
LVCMOS15_JEDEC, QUIETIO, 16 mA	1.03	1.15	1.28	1.49	3.33	3.47	3.67	4.31	3.33	3.47	3.67	4.31	ns
LVCMOS15_JEDEC, Slow, 2 mA	1.03	1.15	1.28	1.49	4.18	4.32	4.52	5.13	4.18	4.32	4.52	5.13	ns
LVCMOS15_JEDEC, Slow, 4 mA	1.03	1.15	1.28	1.49	3.42	3.56	3.76	4.35	3.42	3.56	3.76	4.35	ns
LVCMOS15_JEDEC, Slow, 6 mA	1.03	1.15	1.28	1.49	2.29	2.43	2.63	3.25	2.29	2.43	2.63	3.25	ns
LVCMOS15_JEDEC, Slow, 8 mA	1.03	1.15	1.28	1.49	2.30	2.44	2.64	3.26	2.30	2.44	2.64	3.26	ns
LVCMOS15_JEDEC, Slow, 12 mA	1.03	1.15	1.28	1.49	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVCMOS15_JEDEC, Slow, 16 mA	1.03	1.15	1.28	1.49	2.01	2.15	2.35	2.97	2.01	2.15	2.35	2.97	ns
LVCMOS15_JEDEC, Fast, 2 mA	1.03	1.15	1.28	1.49	3.28	3.42	3.62	4.22	3.28	3.42	3.62	4.22	ns
LVCMOS15_JEDEC, Fast, 4 mA	1.03	1.15	1.28	1.49	2.27	2.41	2.61	3.23	2.27	2.41	2.61	3.23	ns
LVCMOS15_JEDEC, Fast, 6 mA	1.03	1.15	1.28	1.49	1.78	1.92	2.12	2.74	1.78	1.92	2.12	2.74	ns
LVCMOS15_JEDEC, Fast, 8 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.69	1.73	1.87	2.07	2.69	ns
LVCMOS15_JEDEC, Fast, 12 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.63	1.73	1.87	2.07	2.63	ns
LVCMOS15_JEDEC, Fast, 16 mA	1.03	1.15	1.28	1.49	1.73	1.87	2.07	2.63	1.73	1.87	2.07	2.63	ns
LVCMOS12, QUIETIO, 2 mA	0.91	1.03	1.16	1.51	6.40	6.54	6.74	7.30	6.40	6.54	6.74	7.30	ns
LVCMOS12, QUIETIO, 4 mA	0.91	1.03	1.16	1.51	4.98	5.12	5.32	5.90	4.98	5.12	5.32	5.90	ns
LVCMOS12, QUIETIO, 6 mA	0.91	1.03	1.16	1.51	4.65	4.79	4.99	5.55	4.65	4.79	4.99	5.55	ns
LVCMOS12, QUIETIO, 8 mA	0.91	1.03	1.16	1.51	4.23	4.37	4.57	5.21	4.23	4.37	4.57	5.21	ns
LVCMOS12, QUIETIO, 12 mA	0.91	1.03	1.16	1.51	3.98	4.12	4.32	4.94	3.98	4.12	4.32	4.94	ns
LVCMOS12, Slow, 2 mA	0.91	1.03	1.16	1.51	4.98	5.12	5.32	5.91	4.98	5.12	5.32	5.91	ns
LVCMOS12, Slow, 4 mA	0.91	1.03	1.16	1.51	2.84	2.98	3.18	3.81	2.84	2.98	3.18	3.81	ns
LVCMOS12, Slow, 6 mA	0.91	1.03	1.16	1.51	2.77	2.91	3.11	3.72	2.77	2.91	3.11	3.72	ns
LVCMOS12, Slow, 8 mA	0.91	1.03	1.16	1.51	2.34	2.48	2.68	3.31	2.34	2.48	2.68	3.31	ns
LVCMOS12, Slow, 12 mA	0.91	1.03	1.16	1.51	2.08	2.22	2.42	3.06	2.08	2.22	2.42	3.06	ns

I/O Standard Measurement Methodology

Input Delay Measurements

Table 31 shows the test setup parameters used for measuring input delay.

Table 31: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L[(1)]	V_H[(1)]	V_{MEAS}[(3)(4)]	V_{REF}[(2)(4)]
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	0	3.0	1.4	–
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	0	3.3	1.65	–
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
LVCMOS, 1.2V	LVCMOS12	0	1.2	0.6	–
PCI (Peripheral Component Interface), 33 MHz and 66 MHz, 3.3V	PCI33_3, PCI66_3	Per PCI Specification			–
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III	HSTL_III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	1.1
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
SSTL, Class II, 1.5V	SSTL15_II	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.75
LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V	LVDS_25, LVDS_33	1.25 – 0.125	1.25 + 0.125	0[(5)]	–
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V & 3.3V	LVPECL_25, LVPECL_33	1.2 – 0.3	1.2 + 0.3	0[(5)]	–
BLVDS (Bus LVDS), 2.5V	BLVDS_25	1.3 – 0.125	1.3 + 0.125	0[(5)]	–
Mini-LVDS, 2.5V & 3.3V	MINI_LVDS_25, MINI_LVDS_33	1.2 – 0.125	1.2 + 0.125	0[(5)]	–
RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V	RSDS_25, RSDS_33	1.2 – 0.1	1.2 + 0.1	0[(5)]	–
TMDS (Transition Minimized Differential Signaling), 3.3V	TMDS_33	3.0 – 0.1	3.0 + 0.1	0[(5)]	–
PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V	PPDS_25, PPDS_33	1.25 – 0.1	1.25 + 0.1	0[(5)]	–

Notes:

1. Input waveform switches between V_L and V_H.
2. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 4.
5. The value given is the differential input voltage.

Table 34: **SSO Limit per V_{CCO}/GND Pair *(Cont'd)***

V_{CCO}	I/O Standard	Drive	Slew	SSO Limit per V_{CCO}/GND Pair			
				All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324		All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324	
				Bank 0/2	Bank 1/3	Bank 0/2	Bank 1/3/4/5
Various	LVDS_33			16	N/A	16	N/A
	LVDS_25			20	N/A	20	N/A
	BLVDS_25			20	48	20	20
	MINI_LVDS_33			13	N/A	13	N/A
	MINI_LVDS_25			18	N/A	18	N/A
	RSDS_33			12	N/A	12	N/A
	RSDS_25			15	N/A	15	N/A
	TMDS_33			83	N/A	83	N/A
	PPDS_33			12	N/A	12	N/A
	PPDS_25			16	N/A	16	N/A
	DISPLAY_PORT			42	40	42	30
	I2C			47	55	47	42
	SMBUS			44	52	44	40

Notes:

1. SSO limits greater than the number of I/O per V_{CCO}/GND pair (Table 33) indicate No Limit for the given I/O standard. They are provided in this table to calculate limits when using multiple I/O standards in a bank.
2. Not available (N/A) indicates that the I/O standard is not available in the given bank.
3. When used with the MCB, these signals are exempt from SSO analysis due to the known activity of the MCB switching patterns. SSO performance is validated for all MCB instances. MCB outputs can, in some cases, exceed the SSO limits.

Input Serializer/Deserializer Switching Characteristics

Table 37: **ISERDES2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold for Control Lines						
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.16/ –0.09	0.20/ –0.09	0.31/ –0.09	0.34/ –0.14	ns
T_{ISCCK_CE} / T_{ISCKC_CE}	CE pin Setup/Hold with respect to CLK	0.71/ –0.47	0.71/ –0.42	0.97/ –0.42	1.39/ –0.71	ns
Setup/Hold for Data Lines						
T_{ISDCK_D} /T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.24/ –0.15	0.25/ –0.05	0.29/ –0.05	0.09/ –0.05	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY2)	–0.25/ 0.30	–0.25/ 0.42	–0.25/ 0.56	–0.54/ 0.67	ns
$T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	–0.03/ 0.04	–0.03/ 0.16	–0.03/ 0.18	–0.05/ 0.12	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY2)	–0.40/ 0.48	–0.40/ 0.53	–0.40/ 0.71	–0.71/ 0.86	ns
Sequential Delays						
T_{ISCKO_Q}	CLKDIV to out at Q pin	1.30	1.44	2.02	2.22	ns
F_{CLKDIV}	CLKDIV maximum frequency	270	262.5	250	125	MHz

Output Serializer/Deserializer Switching Characteristics

Table 38: **OSERDES2 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	–0.03/ 1.02	–0.03/ 1.17	–0.03/ 1.27	–0.02/ 0.23	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	–0.05/ 1.03	–0.05/ 1.13	–0.05/ 1.23	–0.05/ 0.24	ns
T_{OSCCK_OCE}/T_{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.12/ –0.03	0.15/ –0.03	0.24/ –0.03	0.28/ –0.17	ns
T_{OSCCK_TCE}/T_{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.14/ –0.08	0.17/ –0.08	0.27/ –0.08	0.31/ –0.16	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.94	1.11	1.51	1.89	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.94	1.11	1.51	1.91	ns
F_{CLKDIV}	CLKDIV maximum frequency	270	262.5	250	125	MHz

Notes:

1. T_{OSDCK_T2}/T_{OSCKD_T2} (T input setup/hold with respect to CLKDIV) are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 41: **CLB Distributed RAM Switching Characteristics (SLICEM Only)**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Sequential Delays						
T_{SHCKO}	Clock to A – D outputs	1.26	1.55	1.55	2.35	ns, Max
	Clock to A – D outputs (direct output path)	0.96	1.20	1.20	1.87	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS}/T_{DH}	AX – DX or AI – DI inputs to CLK	0.59/ 0.17	0.73/ 0.22	0.73/ 0.22	1.17/ 0.33	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock for XC devices	0.28/ 0.35	0.32/ 0.42	0.32/ 0.42	0.26/ 0.71	ns, Min
	Address An inputs to clock for XA and XQ devices	0.28/ 0.51	N/A	0.32/ 0.51	0.26/ 0.71	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.31/ –0.08	0.37/ –0.08	0.37/ –0.08	0.59/ –0.27	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.31/ –0.08	0.37/ –0.08	0.37/ –0.08	0.59/ –0.27	ns, Min

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 42: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	1.35	1.78	1.78	2.74	ns, Max
	Clock to A – D outputs (direct output path)	1.24	1.65	1.65	2.48	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS}/T_{WH}	WE input to CLK	0.20/ –0.07	0.24/ –0.07	0.24/ –0.07	0.29/ –0.27	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK for XC devices	0.30/ 0.30	0.30/ 0.38	0.30/ 0.38	0.82/ –0.41	ns, Min
	CE input to CLK for XA and XQ devices	0.32/ 0.30	N/A	0.40/ 0.38	0.82/ –0.41	ns, Min
T_{DS}/T_{DH}	AX – DX or AI – DI inputs to CLK	0.07/ 0.11	0.09/ 0.14	0.09/ 0.14	0.11/ 0.23	ns, Min

DSP48A1 Switching Characteristics

Table 44: **DSP48A1 Switching Characteristics**

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade				Units
					-3	-3N	-2	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock									
$T_{DSPDCK\_A\_A1REG}$/ $T_{DSPCKD\_A\_A1REG}$	A input to A1 register CLK	N/A	N/A	N/A	0.15/ 0.09	0.17/ 0.09	0.17/ 0.09	0.32/ 0.09	ns
$T_{DSPDCK\_D\_B1REG}$/ $T_{DSPCKD\_D\_B1REG}$	D input to B1 register CLK	Yes	N/A	N/A	1.90/ –0.07	1.95/ –0.07	1.95/ –0.07	2.82/ –0.07	ns
$T_{DSPDCK\_C\_CREG}$/ $T_{DSPCKD\_C\_CREG}$	C input to C register CLK for XC devices	N/A	N/A	N/A	0.11/ 0.15	0.13/ 0.15	0.13/ 0.15	0.24/ 0.09	ns
	C input to C register CLK for XA and XQ devices				0.11/ 0.19	N/A	0.13/ 0.23	0.24/ 0.09	
$T_{DSPDCK\_D\_DREG}$/ $T_{DSPCKD\_D\_DREG}$	D input to D register CLK for XC devices	N/A	N/A	N/A	0.09/ 0.15	0.10/ 0.15	0.10/ 0.15	0.19/ 0.12	ns
	D input to D register CLK for XA and XQ devices				0.09/ 0.23	N/A	0.10/ 0.27	0.19/ 0.12	
$T_{DSPDCK\_OPMODE\_B1REG}$/ $T_{DSPCKD\_OPMODE\_B1REG}$	OPMODE input to B1 register CLK	Yes	N/A	N/A	1.97/ 0.01	2.00/ 0.01	2.00/ 0.01	2.85/ 0.01	ns
$T_{DSPDCK\_OPMODE\_OPMODEREG}$/ $T_{DSPCKD\_OPMODE\_OPMODEREG}$	OPMODE input to OPMODE register CLK for XC devices	N/A	N/A	N/A	0.18/ 0.12	0.21/ 0.12	0.21/ 0.12	0.40/ 0.12	ns
	OPMODE input to OPMODE register CLK for XA and XQ devices				0.18/ 0.16	N/A	0.21/ 0.22	0.40/ 0.12	
Setup and Hold Times of Data Pins to the Pipeline Register Clock									
$T_{DSPDCK\_A\_MREG}$/ $T_{DSPCKD\_A\_MREG}$	A input to M register CLK	N/A	Yes	N/A	3.06/ –0.40	3.51/ –0.40	3.51/ –0.40	3.97/ –0.40	ns
$T_{DSPDCK\_B\_MREG}$/ $T_{DSPCKD\_B\_MREG}$	B input to M register CLK	Yes	Yes	N/A	3.96/ –0.68	4.58/ –0.68	4.58/ –0.68	7.00/ –0.68	ns
$T_{DSPDCK\_D\_MREG}$/ $T_{DSPCKD\_D\_MREG}$	D input to M register CLK	Yes	Yes	N/A	4.23/ –0.56	4.80/ –0.56	4.80/ –0.56	6.84/ –0.56	ns
$T_{DSPDCK\_OPMODE\_MREG}$/ $T_{DSPCKD\_OPMODE\_MREG}$	OPMODE to M register CLK	Yes	Yes	N/A	4.18/ –0.48	4.80/ –0.48	4.80/ –0.48	6.88/ –0.48	ns
		No	Yes	N/A	2.37/ –0.48	2.70/ –0.48	2.70/ –0.48	4.28/ –0.48	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock									
$T_{DSPDCK\_A\_PREG}$/ $T_{DSPCKD\_A\_PREG}$	A input to P register CLK	N/A	Yes	Yes	4.32/ –0.76	5.06/ –0.76	5.06/ –0.76	7.52/ –0.76	ns
$T_{DSPDCK\_B\_PREG}$/ $T_{DSPCKD\_B\_PREG}$	B input to P register CLK	Yes	Yes	Yes	5.87/ –0.59	6.87/ –0.59	6.87/ –0.59	10.55/ –0.59	ns
		No	Yes	Yes	4.14/ –0.93	4.68/ –0.93	4.68/ –0.93	8.12/ –0.93	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK	N/A	N/A	Yes	2.20/ –0.23	2.25/ –0.23	2.25/ –0.23	3.27/ –0.23	ns
$T_{DSPDCK\_D\_PREG}$/ $T_{DSPCKD\_D\_PREG}$	D input to P register CLK	Yes	Yes	Yes	5.90/ –0.92	6.91/ –0.92	6.91/ –0.92	10.39/ –0.92	ns

Table 45: Device DNA Interface Port Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
T_{DNASSU}	Setup time on SHIFT before the rising edge of CLK	7				ns, Min
T_{DNASH}	Hold time on SHIFT after the rising edge of CLK	1				ns, Min
T_{DNADSU}	Setup time on DIN before the rising edge of CLK	7				ns, Min
T_{DNADH}	Hold time on DIN after the rising edge of CLK	1				ns, Min
T_{DNARSU}	Setup time on READ before the rising edge of CLK	7				ns, Min
		1,000				ns, Max
T_{DNARH}	Hold time on READ after the rising edge of CLK	1				ns, Min
$T_{DNADCKO}$	Clock-to-output delay on DOUT after rising edge of CLK	0.5				ns, Min
		6				ns, Max
$T_{DNACLKF}$(2)	CLK frequency	2				MHz, Max
$T_{DNACLKL}$	CLK Low time	50				ns, Min
$T_{DNACLKH}$	CLK High time	50				ns, Min

Notes:

1. The minimum READ pulse width is 8 ns, the maximum READ pulse width is 1 μs.
2. Also applies to TCK when reading DNA through the boundary-scan port.

Table 46: Suspend Mode Switching Characteristics

Symbol	Description	Min	Max	Units
Entering Suspend Mode				
$T_{SUSPENDHIGH\_AWAKE}$	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter	2.5	14	ns
$T_{SUSPENDFILTER}$	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled	31	430	ns
$T_{SUSPEND\_GWE}$	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior (without glitch filter)	–	15	ns
$T_{SUSPEND\_GTS}$	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements (without glitch filter)	–	15	ns
$T_{SUSPEND\_DISABLE}$	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled (without glitch filter)	–	1500	ns
Exiting Suspend Mode				
$T_{SUSPENDLOW\_AWAKE}$	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM or PLL lock time.	7	75	μs
$T_{SUSPEND\_ENABLE}$	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	7	41	μs
T_{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using **sw_clk:InternalClock** and **sw_gwe_cycle:1**.	–	80	ns
T_{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using **sw_clk:InternalClock** and **sw_gwe_cycle:512**.	–	20.5	μs
T_{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using **sw_clk:InternalClock** and **sw_gts_cycle:1**.	–	80	ns
T_{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using **sw_clk:InternalClock** and **sw_gts_cycle:512**.	–	20.5	μs
T_{SCP_AWAKE}	Rising edge of SCP pins to rising edge of AWAKE pin	7	75	μs

Configuration Switching Characteristics

Table 47: **Configuration Switching Characteristics**[(1)]

Symbol	Description	Speed Grade				Units
		-3	-3N	-2	-1L	
Power-up Timing Characteristics						
T_{PL}[(2)]	PROGRAM_B Latency	4	4	4	5	ms, Max
T_{POR}[(2)]	Power-on reset (50 ms ramp time)[(3)]	5/30	5/34	5/40	5/40	ms, Min/Max
	Power-on reset (10 ms ramp time)	5/25	5/29	5/35	5/40	ms, Min/Max
$T_{PROGRAM}$	PROGRAM_B Pulse Width	500	500	500	500	ns, Min
Slave Serial Mode Programming Switching						
T_{DCCK}/T_{CCKD}	DIN Setup/Hold, slave mode	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
T_{CCO}	CCLK to DOUT	12	12	12	17	ns, Max
F_{SCCK}	Slave mode external CCLK	80	80	80	50	MHz, Max
Slave SelectMAP Mode Programming Switching						
T_{SMDCCK}/T_{SMCCKD}	SelectMAP Data Setup/Hold	6.0/1.0	6.0/1.0	6.0/1.0	8.0/2.0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold	7.0/0.0	7.0/0.0	7.0/0.0	9.0/2.0	ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B Setup/Hold	17.0/1.0	17.0/1.0	17.0/1.0	27.0/2.0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out	16	16	16	26	ns, Max
T_{SMCO}	CCLK to DATA out in readback	13	13	13	25	ns, Max
T_{SMCKBY}	CCLK to BUSY out in readback	12	12	12	17	ns, Max
F_{SMCCK}	Maximum CCLK frequency (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	25	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x8 mode, LX150, and LX150T only)	40	40	40	20	MHz, Max
	Maximum CCLK frequency (LX100 and LX100T in x16 mode only)	35	35	35	20	MHz, Max
F_{RBCCK}	Maximum Readback CCLK frequency, including block RAM (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	20	20	20	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only)	50	50	50	30	MHz, Max
	Maximum Readback CCLK frequency, including block RAM (LX100, LX100T, LX150, and LX150T only)	12	12	12	4	MHz, Max
	Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX100, LX100T, LX150, and LX150T only)	35	35	35	20	MHz, Max
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}	TMS and TDI Setup time before TCK	10	10	10	17	ns, Min
T_{TCKTAP}	TMS and TDI Hold time after TCK	5.5	5.5	5.5	5.5	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid	6.5	6.5	6.5	8	ns, Max
T_{TCKH}	TCK clock minimum High time	12	12	12	21	ns, Min
T_{TCKL}	TCK clock minimum Low time	12	12	12	21	ns, Min
F_{TCK}	Maximum configuration TCK clock frequency	33	33	33	18	MHz, Max
F_{TCKB}	Maximum boundary-scan TCK clock frequency	33	33	33	18	MHz, Max
F_{TCKAES}	Maximum AES key TCK clock frequency	2	2	2	2	MHz, Max

Clock Buffers and Networks

Table 48: **Global Clock Switching Characteristics (BUFGMUX)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T_{GSI}	S pin Setup to I0/I1 inputs	LX devices	0.25	0.31	0.48	0.48	ns
		LXT devices	0.25	0.31	0.48	N/A	ns
T_{GIO}	BUFGMUX delay from I0/I1 to O	LX devices	0.21	0.21	0.21	0.21	ns
		LXT devices	0.21	0.21	0.21	N/A	ns
Maximum Frequency							
F_{MAX}	Global clock tree (BUFGMUX)	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 49: **Input/Output Clock Switching Characteristics (BUFIO2)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
T_{BUFCKO_O}	Clock to out delay from I to O	LX devices	0.67	0.82	1.09	1.50	ns
		LXT devices	0.67	0.82	1.09	N/A	ns
Maximum Frequency							
F_{MAX}	I/O clock tree (BUFIO2)	LX devices	540	525	500	300	MHz
		LXT devices	540	525	500	N/A	MHz

Table 50: **Input/Output Clock Switching Characteristics (BUFIO2FB)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
Maximum Frequency							
F_{MAX}	I/O clock tree (BUFIO2FB)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

Table 51: **Input/Output Clock Switching Characteristics (BUFPLL)**

Symbol	Description	Devices	Speed Grade				Units
			-3	-3N	-2	-1L	
Maximum Frequency							
F_{MAX}	BUFPLL clock tree (BUFPLL)	LX devices	1080	1050	950	500	MHz
		LXT devices	1080	1050	950	N/A	MHz

PLL Switching Characteristics

Table 52: **PLL Specification**

Symbol	Description	Device(1)	Speed Grade				Units
			-3	-3N	-2	-1L	
F_{INMAX}	Maximum Input Clock Frequency from I/O Clock	LX devices	540	525	450	300	MHz
		LXT devices	540	525	450	N/A	MHz
	Maximum Input Clock Frequency from Global Clock	LX devices	400	400	375	250	MHz
		LXT devices	400	400	375	N/A	MHz

Table 56: **Switching Characteristics for the Digital Frequency Synthesizer (DFS) for DCM_SP[(1)]**

Symbol	Description	Speed Grade								Units
		-3		-3N		-2		-1L		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Frequency Ranges										
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	5	375	5	375	5	333	5	200	MHz
Output Clock Jitter[(2)(3)]										
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN < 20 MHz	Use the Clocking Wizard								ps
	Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN > 20 MHz	Typical = ±(1% of CLKFX period + 100)								ps
Duty Cycle[(4)(5)]										
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs including the BUFGMUX and clock tree duty-cycle distortion	Maximum = ±(1% of CLKFX period + 350)								ps
Phase Alignment[(5)]										
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used	–	±200	–	±200	–	±200	–	±250	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used	Maximum = ±(1% of CLKFX period + 200)								ps
LOCKED Time										
LOCK_FX[(2)]	When FCLKIN < 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	–	5	–	5	–	5	–	5	ms
	When FCLKIN > 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time.	–	0.45	–	0.45	–	0.45	–	0.60	ms

Notes:

1. The values in this table are based on the operating conditions described in Table 2 and Table 55.
2. For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
3. Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
5. Some duty cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.

Table 64: **Global Clock Input to Output Delay With DCM in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in System-Synchronous Mode.							
$T_{ICKOFDCM}$	Global Clock and OUTFF *with* DCM	XC6SLX4	4.23	N/A	6.11	6.60	ns
		XC6SLX9	4.23	5.17	6.11	6.60	ns
		XC6SLX16	4.28	4.57	5.34	6.36	ns
		XC6SLX25	3.95	4.18	4.59	6.91	ns
		XC6SLX25T	3.95	4.18	4.59	N/A	ns
		XC6SLX45	4.37	4.70	5.50	6.85	ns
		XC6SLX45T	4.37	4.70	5.50	N/A	ns
		XC6SLX75	3.90	4.23	4.77	6.31	ns
		XC6SLX75T	3.90	4.23	4.77	N/A	ns
		XC6SLX100	3.86	4.16	4.66	7.25	ns
		XC6SLX100T	3.90	4.16	4.66	N/A	ns
		XC6SLX150	4.03	4.33	4.83	6.63	ns
		XC6SLX150T	4.03	4.33	4.83	N/A	ns
		XA6SLX4	4.55	N/A	6.11	N/A	ns
		XA6SLX9	4.55	N/A	6.11	N/A	ns
		XA6SLX16	4.62	N/A	5.33	N/A	ns
		XA6SLX25	4.27	N/A	4.59	N/A	ns
		XA6SLX25T	4.27	N/A	4.69	N/A	ns
		XA6SLX45	4.69	N/A	5.50	N/A	ns
		XA6SLX45T	4.69	N/A	5.50	N/A	ns
		XA6SLX75	4.22	N/A	4.77	N/A	ns
		XA6SLX75T	4.22	N/A	4.77	N/A	ns
		XA6SLX100	N/A	N/A	5.34	N/A	ns
		XQ6SLX75	N/A	N/A	4.77	6.31	ns
		XQ6SLX75T	4.22	N/A	4.77	N/A	ns
		XQ6SLX150	N/A	N/A	4.96	6.63	ns
		XQ6SLX150T	4.62	N/A	4.96	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 74: **Global Clock Setup and Hold With PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.[1]							
T_{PSPLL}/ T_{PHPLL}	No Delay Global Clock and IFF[2] with PLL in System-Synchronous Mode	XC6SLX4	1.37/0.25	N/A	1.52/0.41	2.07/0.69	ns
		XC6SLX9	1.37/0.21	1.48/0.21	1.52/0.26	2.07/0.69	ns
		XC6SLX16	1.33/–0.03	1.53/–0.02	1.60/–0.02	1.57/0.48	ns
		XC6SLX25	1.65/0.28	1.71/0.28	1.91/0.28	2.44/0.76	ns
		XC6SLX25T	1.65/0.28	1.71/0.28	1.91/0.28	N/A	ns
		XC6SLX45	1.55/0.18	1.64/0.18	1.75/0.18	2.02/0.90	ns
		XC6SLX45T	1.55/0.18	1.64/0.18	1.75/0.18	N/A	ns
		XC6SLX75	1.77/0.21	1.89/0.21	2.13/0.21	2.46/0.53	ns
		XC6SLX75T	1.77/0.21	1.89/0.21	2.13/0.21	N/A	ns
		XC6SLX100	1.44/0.32	1.52/0.32	1.70/0.32	1.78/0.86	ns
		XC6SLX100T	1.44/0.32	1.52/0.32	1.70/0.32	N/A	ns
		XC6SLX150	1.39/0.49	1.48/0.49	1.67/0.49	1.94/0.94	ns
		XC6SLX150T	1.39/0.49	1.48/0.49	1.67/0.49	N/A	ns
		XA6SLX4	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX9	1.61/0.10	N/A	1.64/0.28	N/A	ns
		XA6SLX16	1.89/–0.08	N/A	1.72/–0.08	N/A	ns
		XA6SLX25	1.85/0.16	N/A	2.08/0.16	N/A	ns
		XA6SLX25T	1.85/0.16	N/A	2.17/0.16	N/A	ns
		XA6SLX45	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX45T	1.58/0.07	N/A	1.87/0.03	N/A	ns
		XA6SLX75	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XA6SLX100	N/A	N/A	2.34/0.14	N/A	ns
		XQ6SLX75	N/A	N/A	2.25/0.06	2.46/0.53	ns
		XQ6SLX75T	1.80/0.06	N/A	2.25/0.06	N/A	ns
		XQ6SLX150	N/A	N/A	1.79/0.37	1.94/0.94	ns
		XQ6SLX150T	1.43/0.37	N/A	1.79/0.37	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 76: **Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade				Units
			-3	-3N	-2	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
$T_{PSDCMPLL}$/ $T_{PHDCMPLL}$	No Delay Global Clock and IFF(2) with DCM in System-Synchronous Mode and PLL in DCM2PLL Mode.	XC6SLX4	1.16/0.49	N/A	1.39/0.49	2.36/0.59	ns
		XC6SLX9	1.16/0.44	1.37/0.44	1.39/0.44	2.36/0.59	ns
		XC6SLX16	1.44/–0.08	1.49/–0.04	1.62/–0.04	2.06/0.55	ns
		XC6SLX25	1.52/0.42	1.65/0.42	1.83/0.42	2.52/0.43	ns
		XC6SLX25T	1.52/0.42	1.65/0.42	1.83/0.42	N/A	ns
		XC6SLX45	1.54/0.39	1.59/0.39	1.75/0.39	2.48/0.76	ns
		XC6SLX45T	1.54/0.39	1.59/0.39	1.75/0.39	N/A	ns
		XC6SLX75	1.72/0.41	1.80/0.41	1.99/0.41	2.60/0.75	ns
		XC6SLX75T	1.72/0.41	1.80/0.41	1.99/0.41	N/A	ns
		XC6SLX100	1.34/0.51	1.46/0.51	1.64/0.51	2.12/0.90	ns
		XC6SLX100T	1.34/0.51	1.46/0.51	1.64/0.51	N/A	ns
		XC6SLX150	1.30/0.60	1.40/0.60	1.55/0.60	2.57/0.97	ns
		XC6SLX150T	1.30/0.60	1.40/0.60	1.55/0.60	N/A	ns
		XA6SLX4	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX9	1.58/0.37	N/A	1.58/0.37	N/A	ns
		XA6SLX16	2.67/0.35	N/A	2.67/0.17	N/A	ns
		XA6SLX25	1.74/0.27	N/A	1.95/0.27	N/A	ns
		XA6SLX25T	1.74/0.27	N/A	2.03/0.27	N/A	ns
		XA6SLX45	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX45T	1.58/0.29	N/A	1.87/0.29	N/A	ns
		XA6SLX75	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XA6SLX100	N/A	N/A	2.64/0.82	N/A	ns
		XQ6SLX75	N/A	N/A	2.11/0.24	2.60/0.75	ns
		XQ6SLX75T	1.74/0.24	N/A	2.11/0.24	N/A	ns
		XQ6SLX150	N/A	N/A	1.67/0.70	2.57/0.97	ns
		XQ6SLX150T	1.50/0.70	N/A	1.67/0.70	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 77: **Global Clock Setup and Hold With DCM and PLL in Source-Synchronous Mode**

Symbol	**Description**	**Device**	**Speed Grade**				**Units**
			-3	**-3N**	**-2**	**-1L**	
Example Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin,(1) Using DCM, PLL, and Global Clock Buffer for the LVCMOS25 standard.							
$T_{PSDCMPLL\_0}$/ $T_{PHDCMPLL\_0}$	No Delay Global Clock and IFF(2) with DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode.	XC6SLX4	0.43/1.07	N/A	0.43/1.43	1.10/1.67	ns
		XC6SLX9	0.43/1.03	0.45/1.14	0.45/1.43	1.10/1.67	ns
		XC6SLX16	0.74/0.93	0.74/1.12	0.74/1.21	0.77/1.35	ns
		XC6SLX25	0.67/1.02	0.76/1.11	0.84/1.18	1.23/1.46	ns
		XC6SLX25T	0.67/1.02	0.76/1.11	0.84/1.18	N/A	ns
		XC6SLX45	0.65/0.99	0.65/1.04	0.71/1.12	1.18/1.58	ns
		XC6SLX45T	0.65/1.00	0.65/1.04	0.71/1.12	N/A	ns
		XC6SLX75	0.86/1.01	0.88/1.06	0.94/1.14	1.29/1.67	ns
		XC6SLX75T	0.86/1.01	0.88/1.06	0.94/1.14	N/A	ns
		XC6SLX100	0.50/1.10	0.56/1.10	0.61/1.17	0.84/2.24	ns
		XC6SLX100T	0.50/1.10	0.56/1.10	0.61/1.17	N/A	ns
		XC6SLX150	0.45/1.28	0.47/1.28	0.52/1.28	1.27/1.56	ns
		XC6SLX150T	0.45/1.28	0.47/1.28	0.52/1.28	N/A	ns
		XA6SLX4	0.74/1.00	N/A	0.74/1.43	N/A	ns
		XA6SLX9	0.74/1.00	N/A	0.74/1.43	N/A	ns
		XA6SLX16	1.81/1.15	N/A	1.81/1.03	N/A	ns
		XA6SLX25	0.89/1.01	N/A	0.96/1.05	N/A	ns
		XA6SLX25T	0.89/1.01	N/A	1.04/1.15	N/A	ns
		XA6SLX45	0.69/0.95	N/A	0.83/0.96	N/A	ns
		XA6SLX45T	0.69/0.95	N/A	0.83/0.96	N/A	ns
		XA6SLX75	0.88/0.94	N/A	1.06/0.96	N/A	ns
		XA6SLX75T	0.88/0.94	N/A	1.06/0.96	N/A	ns
		XA6SLX100	N/A	N/A	1.55/1.33	N/A	ns
		XQ6SLX75	N/A	N/A	1.06/0.96	1.29/1.67	ns
		XQ6SLX75T	0.88/0.94	N/A	1.06/0.96	N/A	ns
		XQ6SLX150	N/A	N/A	0.64/1.30	1.27/1.56	ns
		XQ6SLX150T	0.58/1.30	N/A	0.64/1.30	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG. Package skew is not included in these measurements.
2. IFF = Input Flip-Flop