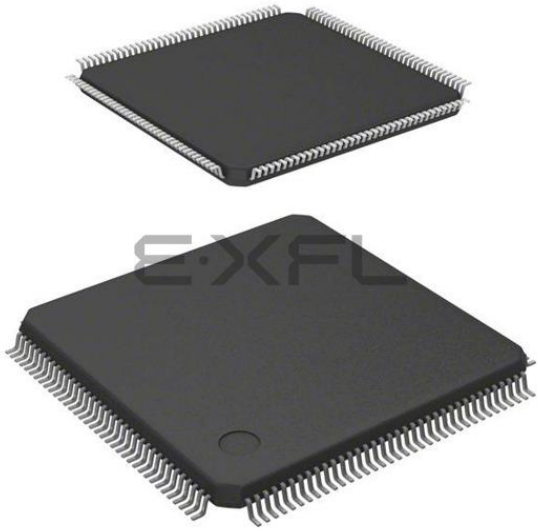

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Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f269z1q3

1 - INTRODUCTION

The ST10F269 is a derivative of the STMicroelectronics ST10 family of 16-bit single-chip CMOS microcontrollers. It combines high CPU performance (up to 20 million instructions per second) with high peripheral functionality and enhanced I/O-capabilities. It also provides on-chip high-speed single voltage Flash memory, on-chip high-speed RAM, and clock generation via PLL.

ST10F269 is processed in 0.35µm CMOS technology. The MCU core and the logic is supplied with a 5V to 3.3V on chip voltage regulator on PQFP144 devices (or 5V to 2.7V on TQFP144 devices). The part is supplied with a single 5V supply and I/Os work at 5V.

The device is upward compatible with the ST10F168 device, with the following set of differences:

– The Multiply/Accumulate unit is available as standard. This MAC unit adds powerful DSP functions to the ST10 architecture, but maintains full compatibility for existing code.

– Flash control interface is now based on STMicroelectronics third generation of stand-alone Flash memories, with an embedded Erase/Program Controller. This completely frees up the CPU during programming or erasing the Flash.

– 128-KByte Flash Option

– Two dedicated pins (DC1 and DC2) on the 144-pin package are used for decoupling the internally generated 3.3V (or 2.7V on TQFP144 devices) core logic supply. **Do not connect these two pins to 5.0V external supply.** Instead, these pins should be connected to a decoupling capacitor (ceramic type, value ≥ 330 nF).

– The A/D Converter characteristics are different from previous ST10 derivatives ones. Refer to *Section 21.3.1* -.

– The AC and DC parameters are adapted to the 40MHz maximum CPU frequency on PQFP144 devices (32MHz on TQFP144 devices). The characterization is performed with C_L = 50pF max on output pins. Refer to *Section 21.3* -.

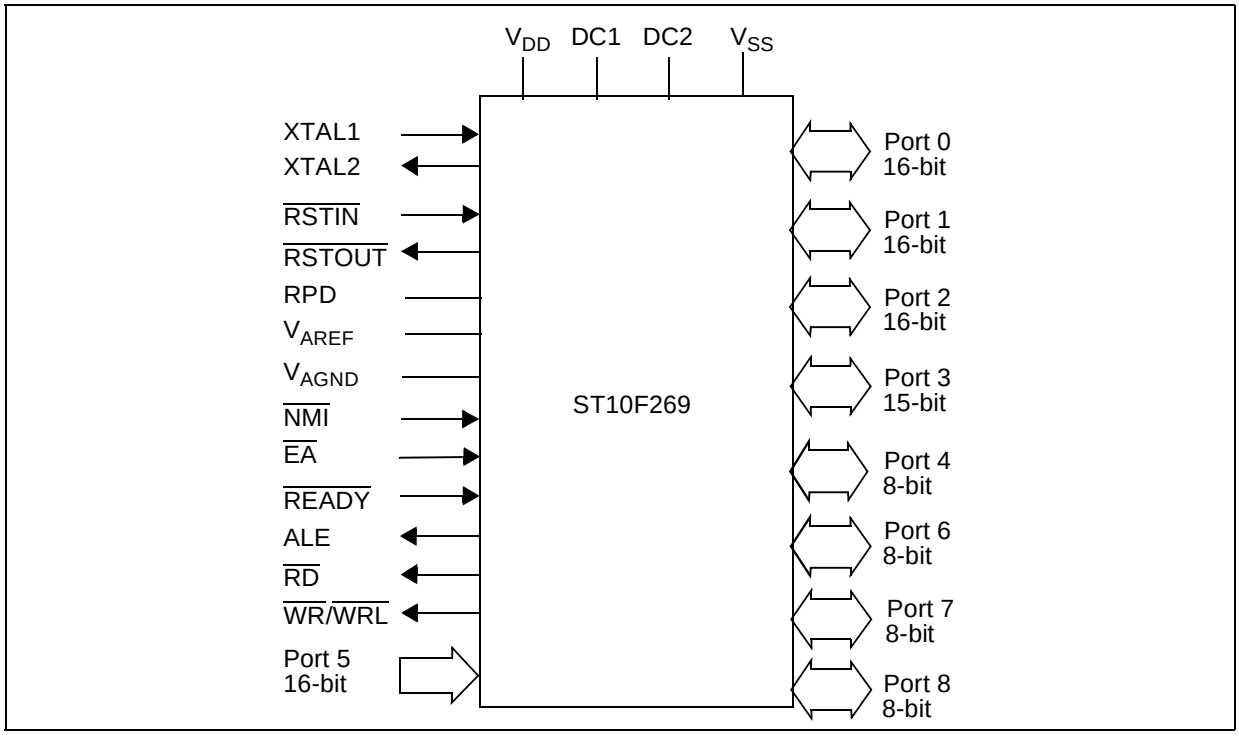
– In order to reduce EMC, the rise/fall time and the sink/source capability of the drivers of the I/O pads are programmable. Refer to *Section 12.2* -.

– The Real Time Clock functionality is added.

– The external interrupt sources can be selected with the EXISEL register.

– The reset source is identified by a dedicated status bit in the WDTCON register.

Figure 1 : Logic Symbol

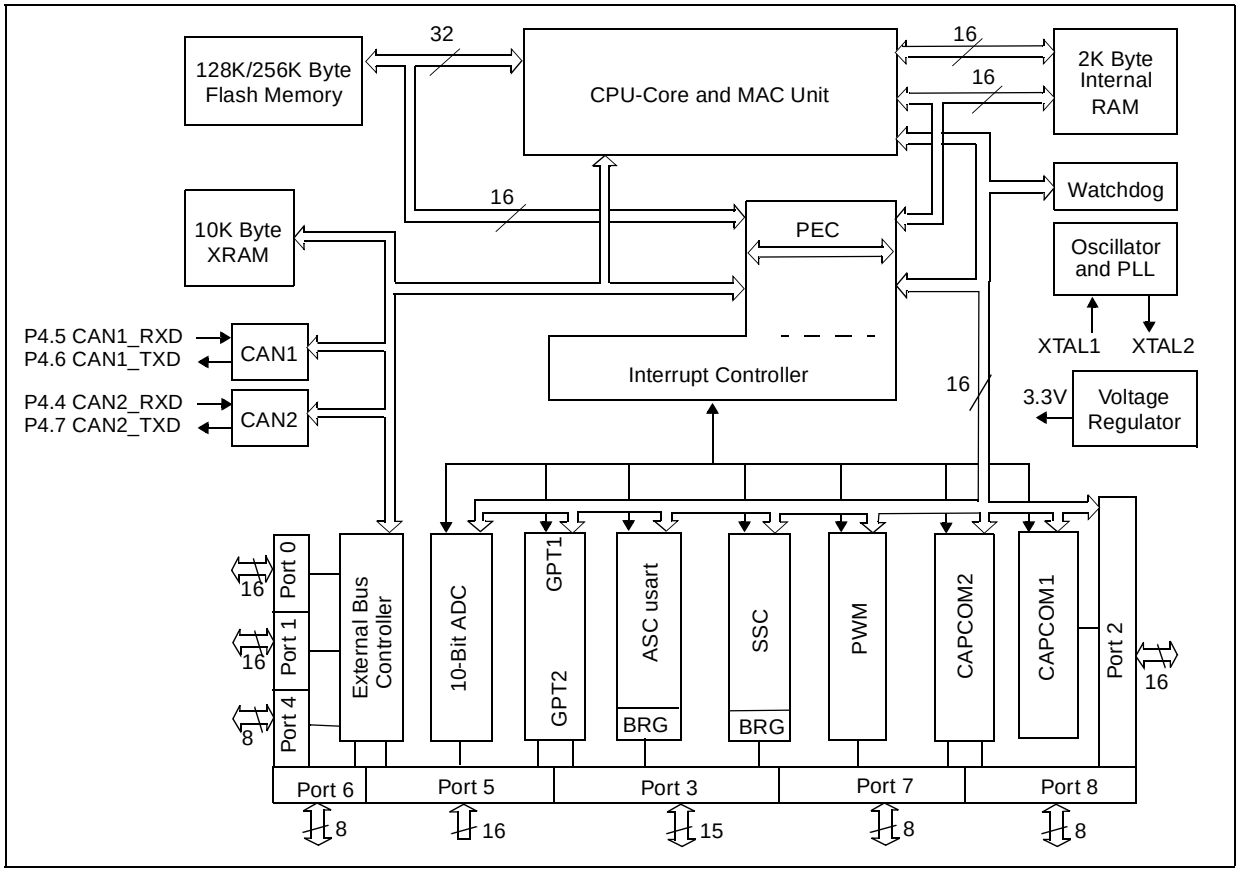


Symbol	Pin	Type	Function
V_{DD}	46, 72, 82,93, 109, 126, 136, 144	-	Digital Supply Voltage: = + 5V during normal operation and idle mode.
V_{SS}	18,45, 55,71, 83,94, 110, 127, 139, 143	-	Digital Ground.
DC1 DC2	56 17	- -	3.3V Decoupling pin (2.7V on TQFP144 devices): a decoupling capacitor of ≥ 330 nF must be connected between this pin and nearest V_{SS} pin.

3 - FUNCTIONAL DESCRIPTION

The architecture of the ST10F269 combines advantages of both RISC and CISC processors and an advanced peripheral subsystem. The block diagram gives an overview of the different on-chip components and the high bandwidth internal bus structure of the ST10F269.

Figure 3 : Block Diagram



If the second command given is not an erase confirm or if the coded cycles are wrong, the instruction aborts, and the device is reset to Read Mode. It is not necessary to program the block with 0000h as the EPC will do this automatically before the erasing to FFFFh. Read operations after the EPC has started, output the Flash Status Register.

During the execution of the erase by the EPC, the device accepts only the Erase Suspend and Read/Reset instructions. Data Polling bit FSB.7 returns ‘0’ while the erasure is in progress, and ‘1’ when it has completed. The Toggle bit FSB.2 and FSB.6 toggle during the erase operation. They stop when erase is completed. After completion, the Error bit FSB.5 returns ‘1’ if there has been an erase failure because erasure has not completed even after the maximum number of erase cycles have been executed by the EPC, in this case, it will be necessary to input a Read/Reset to the Command Interface in order to reset the EPC.

Chip Erase (CE). This instruction uses six write cycles. The Erase Enable command xx80h, must be written at address 1554h after CI-Enable cycles. The Chip Erase command xx10h must be given on the sixth cycle after a second CI-Enable sequence. An error in command sequence will reset the CI to Read mode. It is NOT necessary to program the block with 0000h as the EPC will do this automatically before the erasing to FFFFh. Read operations after the EPC has started output the Flash Status Register. During the execution of the erase by the EPC, Data Polling bit FSB.7 returns ‘0’ while the erasure is in progress, and ‘1’ when it has completed. The FSB.2 and FSB.6 bit toggle during the erase operation. They stop when erase is finished. The FSB.5 error bit returns "1" in case of failure of the erase operation. The error flag is set after the maximum number of erase cycles have been executed by the EPC. In this case, it will be necessary to input a Read/Reset to the Command Interface in order to reset the EPC.

Erase Suspend (ES). This instruction can be used to suspend a Block Erase operation by giving the command xxB0h without any specific address. No CI-Enable cycles is required. Erase Suspend operation allows reading of data from another block and/or the programming in another block while erase is in progress. If this command is given during the time-out period, it will terminate the time-out period in addition to erase Suspend. The Toggle bit FSB.6, when monitored at an address that belongs to the block being erased, stops toggling when Erase Suspend Command is effective, It happens between 0.1µs and 15µs after the Erase Suspend Command has been written. The Flash will then go in normal Read Mode, and read from blocks not being erased is valid, while read from block being erased will output FSB.2 toggling. During a Suspend phase the only instructions valid are Erase Resume and Program Word. A Read / Reset instruction during Erase suspend will definitely abort the Erase and result in invalid data in the block being erased.

Erase Resume (ER). This instruction can be given when the memory is in Erase Suspend State. Erase can be resumed by writing the command xx30h at any address without any CI-enable sequence.

Program during Erase Suspend. The Program Word instruction during Erase Suspend is allowed only on blocks that are not Erase-suspended. This instruction is the same than the Program Word instruction.

Set Protection (SP). This instruction can be used to enable both Block Protection (to protect each block independently from accidental Erasing-Programming Operation) and Code Protection (to avoid code dump). The Set Protection Command must be given after a special CI-Protection Enable cycles (see instruction table). The following Write cycle, will program the Protection Register. To protect the block x (x = 0 to 6), the data bit x must be at ‘0’. To protect the code, bit 15 of the data must be ‘0’. Enabling Block or Code Protection is **permanent** and can be cleared only by STM. Block Temporary Unprotection and Code Temporary Unprotection instructions are available to allow the customer to update the code.

Notes: 1. The new value programmed in protection register will only become active after a reset.

2. Bit that are already at ’0’ in protection register must be confirmed at ’0’ also in data latched during the 4th cycle of set protection command, otherwise an error may occur.

Read Protection Status (RP). This instruction is used to read the Block Protection status and the Code Protection status. To read the protection register (see Table 3), the CI-Protection Enable cycles must be executed followed by the command xx90h at address x2A54h. The following Read Cycles at any odd word address will output the Block Protection Status. The Read/Reset command xxF0h must be written to reset the protection interface.

Note: After a modification of protection register (using Set Protection command), the Read

9 - CAPTURE/COMPARE (CAPCOM) UNITS

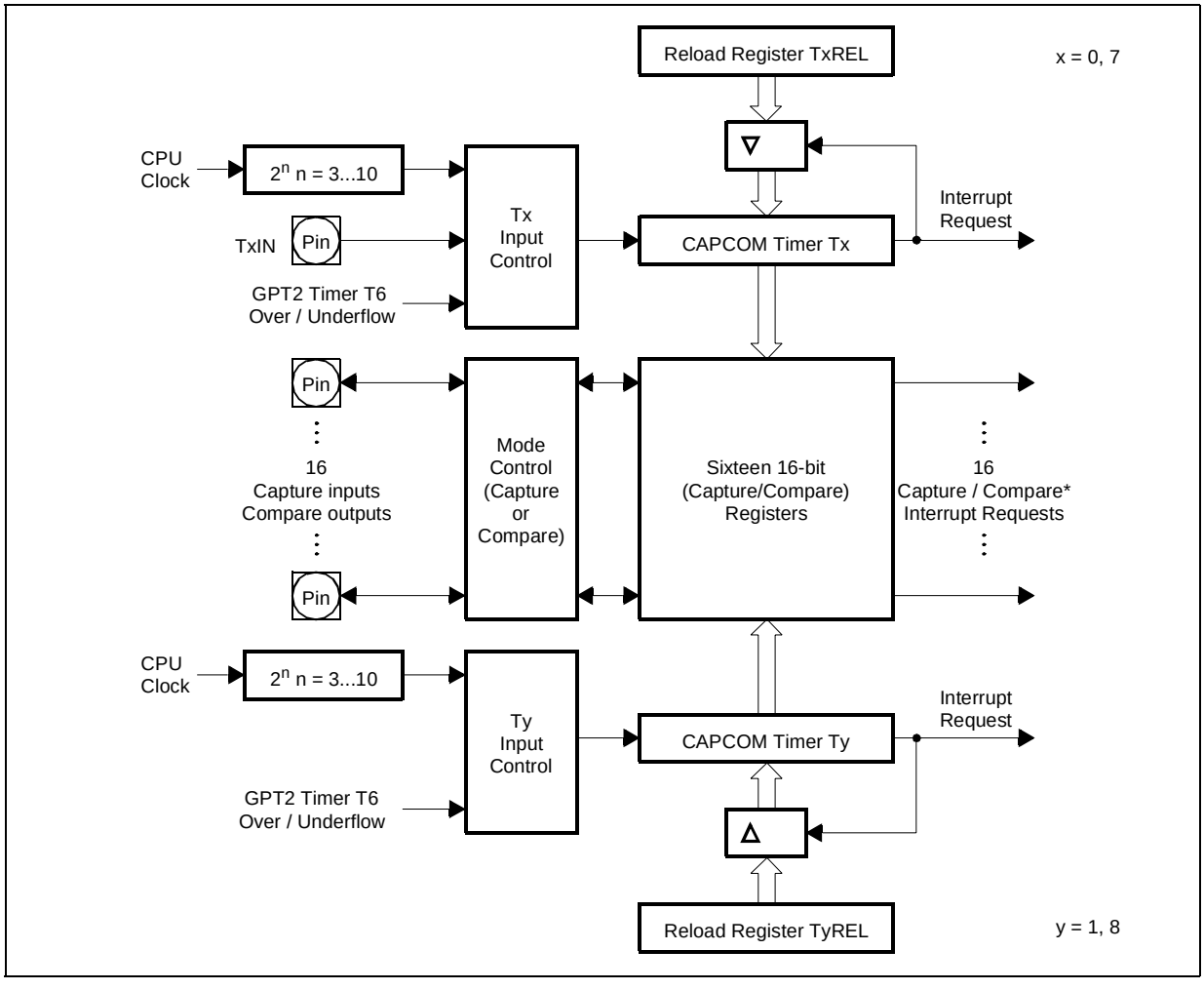
The ST10F269 has two 16 channels CAPCOM units as described in Figure 12. These support generation and control of timing sequences on up to 32 channels with a maximum resolution of 200ns at 40MHz CPU clock on PQFP144 devices and 250ns at 32MHz CPU clock on TQFP144 devices. The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for the capture/compare register array (See Figures *Figure 13* and *Figure 14*).

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/ underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Each of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare functions. Each of the 32 registers has one associated port pin which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event. Figure 12 shows the basic structure of the two CAPCOM units.

Figure 12 : CAPCOM Unit Block Diagram



Resolution and Period (TQFP144 devices) list the timer input frequencies, resolution and periods for each pre-scaler option at 40MHz (or 32MHz) CPU clock. This also applies to the Gated Timer Mode of T6 and to the auxiliary timer T5 in Timer and Gated Timer Mode.

Table 14 : GPT2 Timer Input Frequencies, Resolution and Period (PQFP144 devices)

f_{CPU} = 40MHz	Timer Input Selection T5I / T6I							
	000b	**001b**	**010b**	**011b**	**100b**	**101b**	**110b**	**111b**
Pre-scaler factor	4	8	16	32	64	128	256	512
Input Freq	10MHz	5MHz	2.5MHz	1.25MHz	625kHz	312.5kHz	156.25kHz	78.125kHz
Resolution	100ns	200ns	400ns	0.8µs	1.6µs	3.2µs	6.4µs	12.8µs
Period maximum	6.55ms	13.1ms	26.2ms	52.4ms	104.8ms	209.7ms	419.4ms	838.9ms

Table 15 : GPT2 Timer Input Frequencies, Resolution and Period (TQFP144 devices)

f_{CPU} = 32MHz	Timer Input Selection T5I / T6I							
	000b	**001b**	**010b**	**011b**	**100b**	**101b**	**110b**	**111b**
Pre-scaler factor	4	8	16	32	64	128	256	512
Input Freq	8MHz	4MHz	2MHz	1MHz	500KHz	250KHz	125KHz	62.5KHz
Resolution	125ns	250ns	500ns	1µs	2µs	4µs	8µs	16µs
Period maximum	8.19ms	16.4ms	32.8ms	65.5ms	131ms	262.1ms	524.3ms	1.05s

12.3 - PORT0

The two 8-bit ports P0H and P0L represent the higher and lower part of PORT0, respectively. Both halves of PORT0 can be written (via a PEC transfer) without effecting the other half.

If this port is used for general purpose I/O, the direction of each line can be configured via the corresponding direction registers DP0H and DP0L.

P0L (FF00h / 80h) SFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	P0L.7	P0L.6	P0L.5	P0L.4	P0L.3	P0L.2	P0L.1	P0L.0
								RW	RW	RW	RW	RW	RW	RW	RW

P0H (FF02h / 81h) SFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	P0H.7	P0H.6	P0H.5	P0H.4	P0H.3	P0H.2	P0H.1	P0H.0
								RW	RW	RW	RW	RW	RW	RW	RW

P0X.y	**Port Data Register P0H or P0L Bit y**

DP0L (F100h / 80h) ESFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DP0L.7	DP0L.6	DP0L.5	DP0L.4	DP0L.3	DP0L.2	DP0L.1	DP0L.0
								RW	RW	RW	RW	RW	RW	RW	RW

DP0H (F102h / 81h) ESFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DP0H.7	DP0H.6	DP0H.5	DP0H.4	DP0H.3	DP0H.2	DP0H.1	DP0H.0
								RW	RW	RW	RW	RW	RW	RW	RW

DP0X.y	**Port Direction Register DP0H or DP0L Bit y** DP0X.y = 0: Port line P0X.y is an input (high-impedance) DP0X.y = 1: Port line P0X.y is an output

12.5 - Port 2

If this 16-bit port is used for general purpose I/O, the direction of each line can be configured via the corresponding direction register DP2. Each port line can be switched into push/pull or open drain mode via the open drain control register ODP2.

P2 (FFC0h / E0h) SFR Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.15	P2.14	P2.13	P2.12	P2.11	P2.10	P2.9	P2.8	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

P2.y	**Port Data Register P2 Bit y**

DP2 (FFC2h / E1h) SFR Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DP2 .15	DP2 .14	DP2 .13	DP2 .12	DP2 .11	DP2 .10	DP2 .9	DP2 .8	DP2 .7	DP2 .6	DP2 .5	DP2 .4	DP2 .3	DP2 .2	DP2 .1	DP2 .0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

DP2.y	**Port Direction Register DP2 Bit y** DP2.y = 0: Port line P2.y is an input (high-impedance) DP2.y = 1: Port line P2.y is an output

ODP2 (F1C2h / E1h) ESFR Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ODP2 .15	ODP2 .14	ODP2 .13	ODP2 .12	ODP2 .11	ODP2 .10	ODP2 .9	ODP2 .8	ODP2 .7	ODP2 .6	ODP2 .5	ODP2 .4	ODP2 .3	ODP2 .2	ODP2 .1	ODP2 .0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ODP2.y	**Port 2 Open Drain Control Register Bit y** ODP2.y = 0: Port line P2.y output driver in push/pull mode ODP2.y = 1: Port line P2.y output driver in open drain mode

12.5.1 - Alternate Functions of Port 2

All Port 2 lines (P2.15...P2.0) serve as capture inputs or compare outputs (CC15IO...CC0IO) for the CAPCOM1 unit.

When a Port 2 line is used as a capture input, the state of the input latch, which represents the state of the port pin, is directed to the CAPCOM unit via the line “Alternate Pin Data Input”. If an external capture trigger signal is used, the direction of the respective pin must be set to input.

If the direction is set to output, the state of the port output latch will be read since the pin represents the state of the output latch.

This can be used to trigger a capture event through software by setting or clearing the port latch. Note that in the output configuration, no external device may drive the pin, otherwise conflicts would occur.

When a Port 2 line is used as a compare output (compare modes 1 and 3), the compare event (or the timer overflow in compare mode 3) directly effects the port output latch. In compare mode 1, when a valid compare match occurs, the state of the port output latch is read by the CAPCOM control hardware via the line “Alternate Latch Data Input”, inverted, and written back to the latch via the line “Alternate Data Output”.

The port output latch is clocked by the signal “Compare Trigger” which is generated by the CAPCOM unit. In compare mode 3, when a match occurs, the value '1' is written to the port output latch via the line “Alternate Data Output”. When an overflow of the corresponding timer occurs, a '0' is written to the port output latch. In both cases,

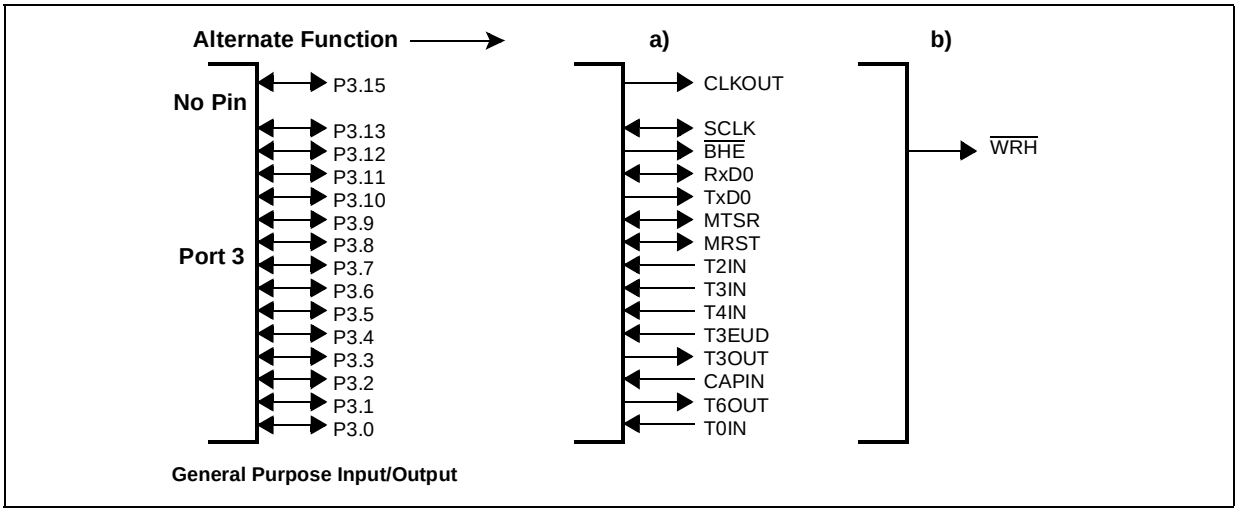
12.6.1 - Alternate Functions of Port 3

The pins of Port 3 serve for various functions which include external timer control lines, the two serial interfaces and the control lines $\overline{BHE}$/$\overline{WRH}$ and CLKOUT.

Table 20 : Port 3 Alternative Functions

Port 3 Pin	Alternate Function	
P3.0	T0IN	CAPCOM1 Timer 0 Count Input
P3.1	T6OUT	Timer 6 Toggle Output
P3.2	CAPIN	GPT2 Capture Input
P3.3	T3OUT	Timer 3 Toggle Output
P3.4	T3EUD	Timer 3 External Up/Down Input
P3.5	T4IN	Timer 4 Count Input
P3.6	T3IN	Timer 3 Count Input
P3.7	T2IN	Timer 2 Count Input
P3.8	MRST	SSC Master Receive / Slave Transmit
P3.9	MTSR	SSC Master Transmit / Slave Receive
P3.10	TxD0	ASC0 Transmit Data Output
P3.11	RxD0	ASC0 Receive Data Input (Output in synchronous mode)
P3.12	$\overline{BHE}$/$\overline{WRH}$	Byte High Enable / Write High Output
P3.13	SCLK	SSC Shift Clock Input/Output
P3.14	---	No pin assigned
P3.15	CLKOUT	System Clock Output

Figure 27 : Port 3 I/O and Alternate Functions



The structure of the Port 3 pins depends on their alternate function (see figures *Figure 28* and *Figure 29*). When the on-chip peripheral associated with a Port 3 pin is configured to use the alternate input function, it reads the input latch, which represents the state of the pin, via the line labeled “Alternate Data Input”. Port 3 pins with alternate input functions are: T0IN, T2IN, T3IN, T4IN, T3EUD and CAPIN.

When the on-chip peripheral associated with a Port 3 pin is configured to use the alternate output function, its “Alternate Data Output” line is ANDed with the port output latch line. When using these alternate functions, the user must set the direction of the port line to output (DP3.y=1) and must set the port output latch (P3.y=1). Otherwise the pin is in its high-impedance state (when configured as input) or the pin is stuck at '0' (when the port output latch is cleared). When the alternate output functions are not used, the “Alternate Data Output” line is in its inactive state, which is a high level ('1').

Port 3 pins with alternate output functions are: T6OUT, T3OUT, TxD0, $\overline{BHE}$ and CLKOUT.

12.10 - Port 7

If this 8-bit port is used for general purpose I/O, the direction of each line can be configured via the corresponding direction register DP7. Each port line can be switched into push-pull or open drain mode via the open drain control register ODP7.

P7 (FFD0h / E8h) SFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	P7.7	P7.6	P7.5	P7.4	P7.3	P7.2	P7.1	P7.0
								RW	RW	RW	RW	RW	RW	RW	RW

P7.y	**Port Data Register P7 Bit y**

DP7 (FFD2h / E9h) SFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DP7.7	DP7.6	DP7.5	DP7.4	DP7.3	DP7.2	DP7.1	DP7.0
								RW	RW	RW	RW	RW	RW	RW	RW

DP7.y	**Port Direction Register DP7 Bit y** DP7.y = 0: Port line P7.y is an input (high impedance) DP7.y = 1: Port line P7.y is an output

ODP7 (F1D2h / E9h) ESFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	ODP7.7	ODP7.6	ODP7.5	ODP7.4	ODP7.3	ODP7.2	ODP7.1	ODP7.0
								RW	RW	RW	RW	RW	RW	RW	RW

ODP7.y	**Port 7 Open Drain Control Register Bit y** ODP7.y = 0: Port line P7.y output driver in push-pull mode ODP7.y = 1: Port line P7.y output driver in open drain mode

13 - A/D CONVERTER

A 10-bit A/D converter with 16 multiplexed input channels and a sample and hold circuit is integrated on-chip. The sample time (for loading the capacitors) and the conversion time is programmable and can be adjusted to the external circuitry.

To remove high frequency components from the analog input signal, a low-pass filter must be connected at the ADC input.

Overrun error detection / protection is controlled by the ADDAT register. Either an interrupt request is generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended until the previous result has been read. For applications which require less than 16 analog input channels, the remaining channel inputs can be used as digital input port pins. The A/D converter of the ST10F269 supports different conversion modes:

– **Single channel single conversion**: the analog level of the selected channel is sampled once and converted. The result of the conversion is stored in the ADDAT register.

– **Single channel continuous conversion**: the analog level of the selected channel is repeatedly sampled and converted. The result of the conversion is stored in the ADDAT register.

– **Auto scan single conversion**: the analog level of the selected channels are sampled once and converted. After each conversion the result is stored in the ADDAT register. The data can be transferred to the RAM by interrupt software management or using the powerful Peripheral Event Controller (PEC) data transfer.

– **Auto scan continuous conversion**: the analog level of the selected channels are repeatedly sampled and converted. The result of the conversion is stored in the ADDAT register. The data can be transferred to the RAM by interrupt software management or using the PEC data transfer.

– **Wait for ADDAT read mode**: when using continuous modes, in order to avoid to overwrite the result of the current conversion by the next one, the ADWR bit of ADCON control register must be activated. Then, until the ADDAT register is read, the new result is stored in a temporary buffer and the conversion is on hold.

– **Channel injection mode**: when using continuous modes, a selected channel can be converted in between without changing the current operating mode. The 10-bit data of the conversion are stored in ADRES field of ADDAT2. The current continuous mode remains active after the single conversion is completed

Table 26 : ADC Sample Clock and Conversion Clock (PQFP144 devices)

ADCTC	Conversion Clock t_{CC}		ADSTC	Sample Clock t_{SC}	
	TCL[1] = 1/2 x f_{XTAL}	At f_{CPU} = 40MHz		t_{SC} =	At f_{CPU} = 40MHz
00	TCL x 24	0.3µs	00	t_{CC}	0.3µs [2]
01	Reserved, do not use	Reserved	01	t_{CC} x 2	0.6µs [2]
10	TCL x 96	1.2 µs	10	t_{CC} x 4	1.2µs [2]
11	TCL x 48	0.6 µs	11	t_{CC} x 8	2.4µs [2]

Notes: 1. Section 21.4.5 -: Direct Drive for TCL definition.
2. t_{CC} = TCL x 24

16.1.5 - RTCAH & RTCAL: RTC ALARM Registers

When the programmable counters reach the 32-bit value stored into RTCAH & RTCAL registers, an alarm is triggered and the interrupt request RTAIR is generated. Those registers are not protected.

RTCAL (EC12h) XBUS Reset Value: XXXXh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTCAL															
RW															

RTCAH (EC14h) XBUS Reset Value: XXXXh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTCAH															
RW															

Note: Those registers are not reset

16.2 - Programming the RTC

RTC interrupt request signals are connected to Port2, pad 10 (RTCSI) and pad 11 (RTCAI). An alternate function Port2 is to generate fast interrupts firq[7:0]. To trigger firq[2] and firq[3] the following configuration has to be set.

EXICON ESFR controls the external interrupt edge selection, RTC interrupt requests are rising edge active.

EXICON (F1C0h) ESFR Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXI7ES		EXI6ES		EXI5ES		EXI4ES		EXI3ES [1 2]		EXI2ES [1 3]		EXI1ES		EXI0ES	
RW		RW		RW		RW		RW		RW		RW		RW	

Notes: 1. EXI2ES and EXI3ES must be configured as "01b" because RCT interrupt request lines are rising edge active.
2. Alarm interrupt request line (RTCAI) is linked with EXI3ES.
3. Timed interrupt request line (RTCSI) is linked with EXI2ES.

EXISEL ESFR enables the Port2 alternate sources. RTC interrupts are alternate sources 2 and 3.

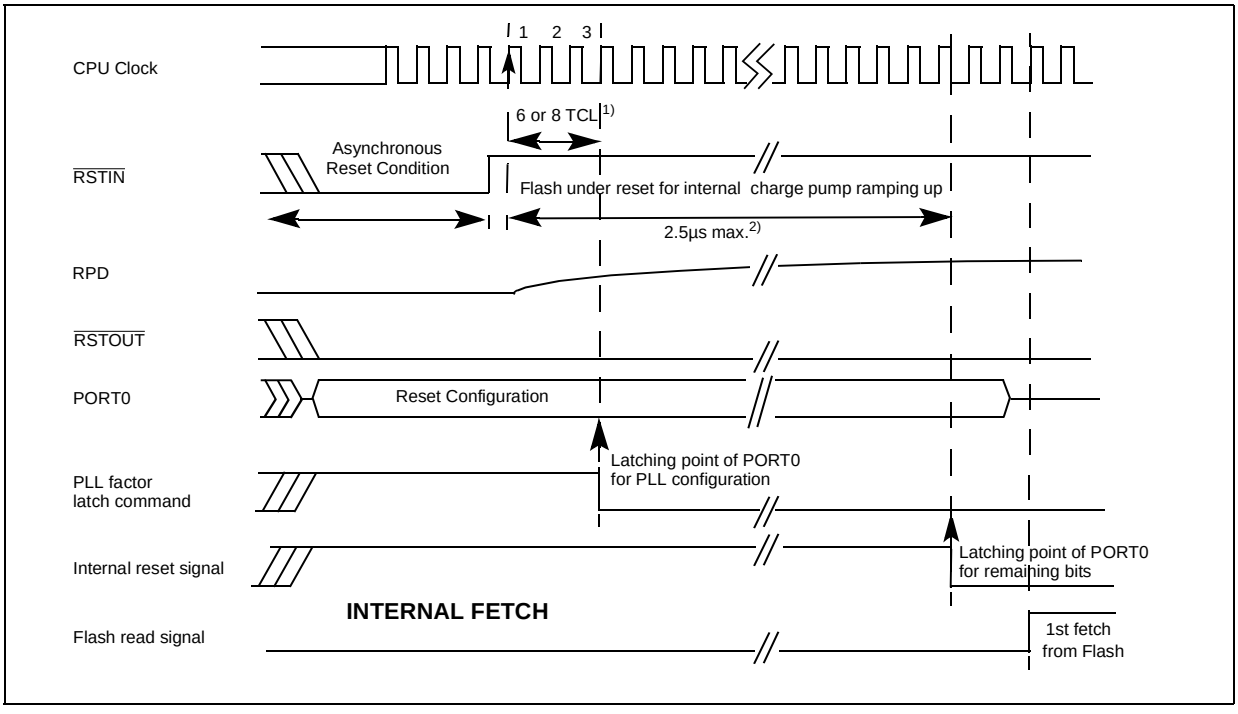
EXISEL (F1DAh) ESFR Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXI7SS		EXI6SS		EXI5SS		EXI4SS		EXI3SS [2]		EXI2SS [3]		EXI1SS		EXI0SS	
RW		RW		RW		RW		RW		RW		RW		RW	

EXIxSS	**External Interrupt x Source Selection (x=7...0)** '00': Input from associated Port 2 pin. '01': Input from "alternate source". [1] '10': Input from Port 2 pin ORed with "alternate source". [1] '11': Input from Port 2 pin ANDed with "alternate source".

Notes: 1. Advised configuration.
2. Alarm interrupt request (RTCAI) is linked with EXI3SS.
3. Timed interrupt request (RTCSI) is linked with EXI2SS.

Figure 55 : Asynchronous Reset Sequence Internal Fetch



Note: 1) RSTIN rising edge to internal latch of PORT0 is 3 CPU clock cycles (6 TCL) if the PLL is bypassed and the prescaler is on ($f_{CPU} = f_{XTAL} / 2$), else it is 4 CPU clock cycles (8 TCL).

2) 2.1µs typical value.

Power-on reset

The asynchronous reset must be used during the power-on of the MCU. Depending on the crystal frequency, the on-chip oscillator needs about 10ms to 50ms to stabilize. The logic of the MCU does not need a stabilized clock signal to detect an asynchronous reset, so it is suitable for power-on conditions. To ensure a proper reset sequence, the **RSTIN pin and the RPD pin must be held at low level** until the MCU clock signal is stabilized and the system configuration value on PORT0 is settled.

Hardware reset

The asynchronous reset must be used to recover from catastrophic situations of the application. It may be triggered by the **hardware of the application**. Internal hardware logic and application circuitry are described in *Section 18.6* - and Figure 58, Figure 59 and Figure 60.

18.1.2 - Synchronous Reset (RSTIN pulse > 1040TCL and RPD pin at high level)

The synchronous reset is a warm reset. It may be generated synchronously to the CPU clock. To be detected by the reset logic, the RSTIN pulse must be low at least for 4 TCL (2 periods of CPU clock). Then the I/O pins are set to high impedance and RSTOUT pin is driven low. After the RSTIN level is detected, a short duration of 12 TCL (6 CPU clocks) maximum elapses, during which pending internal hold states are cancelled and the current internal access cycle, if any, is completed. External bus cycle is aborted.

The internal pull-down of RSTIN pin is activated if bit BDRSTEN of SYSCON register was previously set by software. This bit is always cleared on power-on or after any reset sequence.

The internal sequence lasts for 1024 TCL (512 periods of CPU clock). After this duration the pull-down of RSTIN pin for the bidirectional reset function is released and the RSTIN pin level is sampled. At this step the sequence lasts **1040 TCL** (4 TCL + 12 TCL + 1024 TCL). If the RSTIN pin level is low, the reset sequence is extended until RSTIN level becomes high. Refer to Figure 56

Note If V_{RPD} voltage drops below the RPD pin threshold (typically 2.5V for V_{DD} = 5V) when RSTIN pin is low or when RSTIN pin is internally pulled low, the ST10 reset circuitry disables the bidirectional reset function and RSTIN pin is no more pulled

Figure 62 : Simplified Powerdown Exit Circuitry

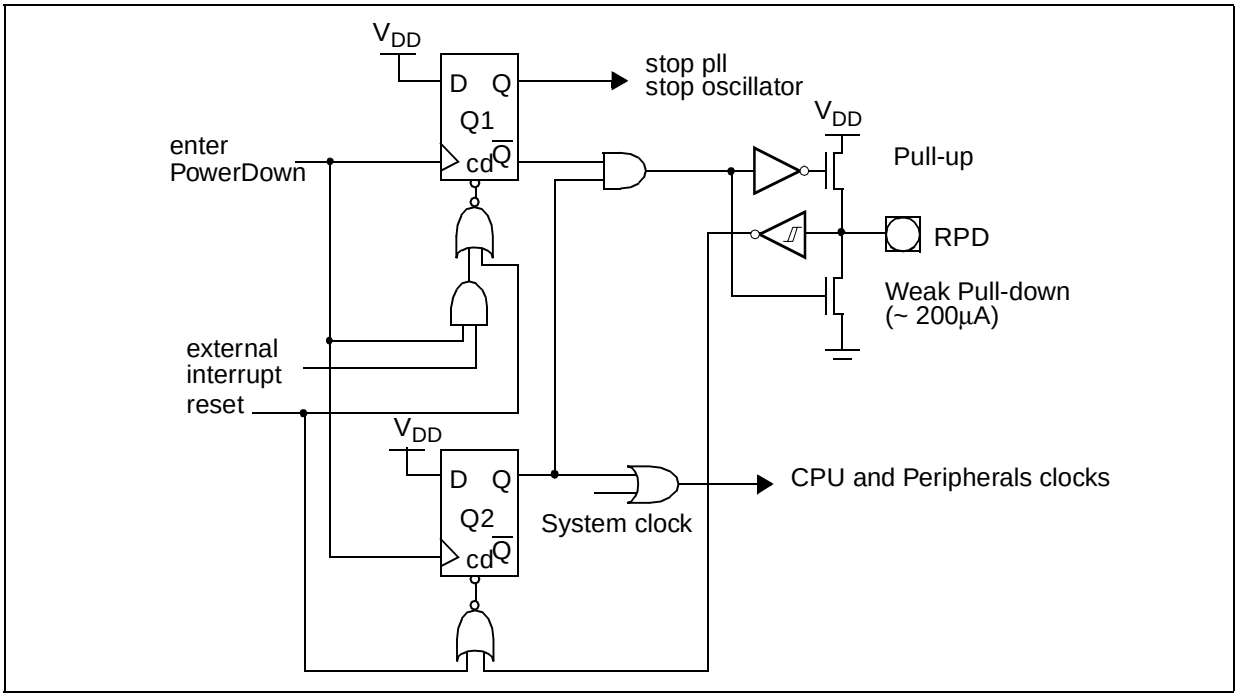
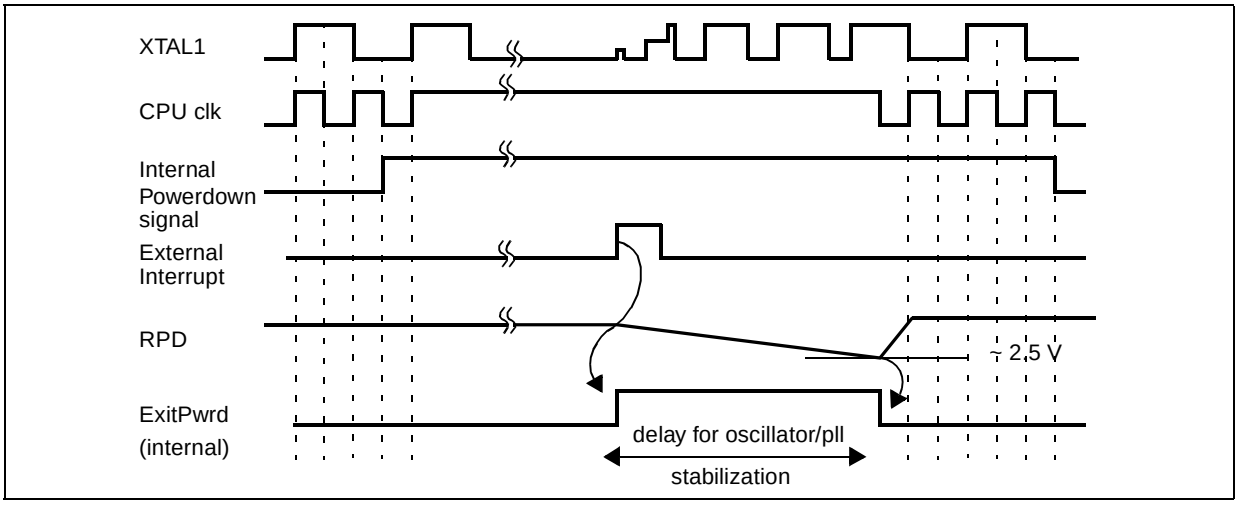


Figure 63 : Powerdown Exit Sequence When Using an External Interrupt (PLL x 2)



Symbol		Parameter		Test Conditions	Min.	Max.	Unit
V_{OL1}	CC	Output low voltage (all other outputs)	1	I_{OL1} = 1.6mA	–	0.45	V
V_{OH}	CC	Output high voltage (PORT0, PORT1, Port4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	1	I_{OH} = -500µA I_{OH} = -2.4mA	0.9 V_{DD} 2.4	– –	V
V_{OH1}	CC	Output high voltage (all other outputs)	1/2	I_{OH} = – 250µA I_{OH} = – 1.6mA	0.9 V_{DD} 2.4	– –	V V
$\lvert I_{OZ1} \rvert$	CC	Input leakage current (Port 5)		$0V < V_{IN} < V_{DD}$	–	200	nA
$\lvert I_{OZ2} \rvert$	CC	Input leakage current (all other)		$0V < V_{IN} < V_{DD}$	–	1	µA
$\lvert I_{OV} \rvert$	SR	Overload current	3/4		–	5	mA
R_{RST}	CC	$\overline{RSTIN}$ pull-up resistor	3	–	50	250	kΩ
I_{RWH}		Read / Write inactive current	5/6	V_{OUT} = 2.4V	–	-40	µA
I_{RWL}		Read / Write active current	5/7	$V_{OUT} = V_{OLmax}$	-500	–	µA
I_{ALEL}		ALE inactive current	5/6	$V_{OUT} = V_{OLmax}$	40	–	µA
I_{ALEH}		ALE active current	5/7	V_{OUT} = 2.4V	–	500	µA
I_{P6H}		Port 6 inactive current	5/6	V_{OUT} = 2.4V	–	-40	µA
I_{P6L}		Port 6 active current	5/7	$V_{OUT} = V_{OL1max}$	-500	–	µA
I_{P0H}		PORT0 configuration current	5/6	$V_{IN} = V_{IHmin}$	–	-10	µA
I_{P0L}			5/7	$V_{IN} = V_{ILmax}$	-100	–	µA
$\lvert I_{IL} \rvert$	CC	XTAL1 input current		$0V < V_{IN} < V_{DD}$	–	20	µA
gm		On-chip oscillator transconductance	3		5	-	mA/V
C_{IO}	CC	Pin capacitance (digital inputs / outputs)	3/5	f = 1MHz, T_A = 25°C	–	10	pF
I_{CC}		Power supply current (PQFP144 devices)	8	RSTIN = V_{IH1} f_{CPU} in [MHz]	–	20 + 2.5 x f_{CPU}	mA
		Power supply current (TQFP144 devices)			–	20 + 2.3 x f_{CPU}	mA
I_{ID}		Idle mode supply current	9	RSTIN = V_{IH1} f_{CPU} in [MHz]	–	20 + f_{CPU}	mA
I_{PD}		Power-down mode supply current	10	V_{DD} = 5.5V T_A = 25°C T_A = 85°C T_A = 125°C	 – – –	 15 [11] 50 [11] 190 [11]	 µA µA µA

Table 43 : ADC Sampling and Conversion Timing (TQFP144 devices)

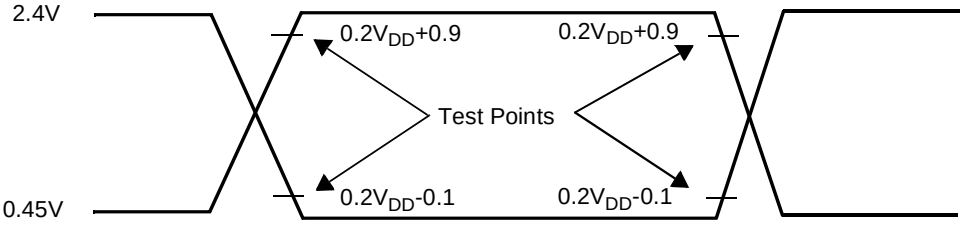
ADCON.15/14 ADCTC	Conversion Clock t_{CC}		ADCON.13/12 ADSTC	Sample Clock t_{SC}	
	TCL = 1/2 x f_{XTAL}	At f_{CPU} = 32MHz		t_{SC} =	At f_{CPU} = 32MHz and ADCTC = 00
00	TCL x 24	0.375µs	00	t_{CC}	0.375µs
01	Reserved, do not use	Reserved	01	t_{CC} x 2	0.75µs
10	TCL x 96	1.5 µs	10	t_{CC} x 4	1.50µs
11	TCL x 48	0.75 µs	11	t_{CC} x 8	3.00µs

A complete conversion will take 14 t_{CC} + 2 t_{SC} + 4 TCL (fastest convertion rate = 6.06µs at 32MHz). This time includes the conversion itself, the sample time and the time required to transfer the digital value to the result register.

21.4 - AC characteristics

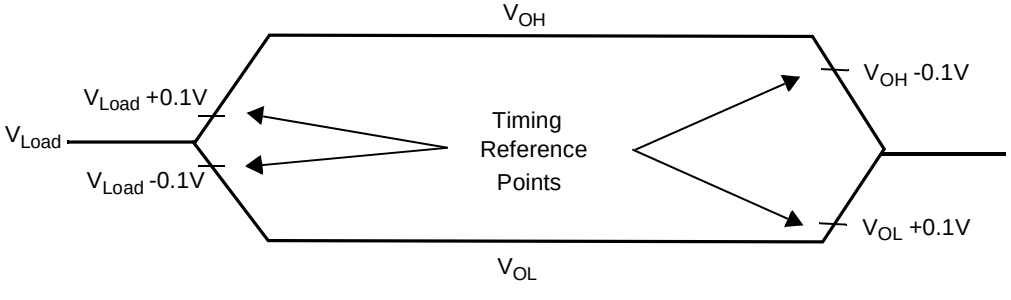
21.4.1 - Test Waveforms

Figure 66 : Input / Output Waveforms



AC inputs during testing are driven at 2.4V for a logic '1' and 0.4V for a logic '0'.
Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

Figure 67 : Float Waveforms



For timing purposes a port pin is no longer floating when V_{LOAD} changes of ±100mV.
It begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20mA).

21.4.2 - Definition of Internal Timing

The internal operation of the ST10F269 is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (for example pipeline) or external (for example bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time

21.4.3 - Clock Generation Modes

The Table 44 associates the combinations of these three bits with the respective clock generation mode.

Table 44 : CPU Frequency Generation (PQFP144 devices)

P0H.7	P0H.6	P0H.5	CPU Frequency $f_{CPU} = f_{XTAL} \times F$	External Clock Input Range[1]	Notes
1	1	1	f_{XTAL} x 4	2.5 to 10MHz	Default configuration
1	1	0	f_{XTAL} x 3	3.33 to 13.33MHz	
1	0	1	f_{XTAL} x 2	5 to 20MHz	
1	0	0	f_{XTAL} x 5	2 to 8MHz	
0	1	1	f_{XTAL} x 1	1 to 40MHz	Direct drive[2]
0	1	0	f_{XTAL} x 1.5	6.66 to 26.66MHz	
0	0	1	f_{XTAL} x 0.5	2 to 80MHz	CPU clock via prescaler[3]
0	0	0	f_{XTAL} x 2.5	4 to 16MHz	

Notes: 1. The external clock input range refers to a CPU clock range of 1...40MHz.
2. The maximum input frequency depends on the duty cycle of the external clock signal.
3. The maximum input frequency is 25MHz when using an external crystal with the internal oscillator; providing that internal serial resistance of the crystal is less than 40Ω. However, higher frequencies can be applied with an external clock source on pin XTAL1, but in this case, the input clock signal must reach the defined levels V_{IL} and V_{IH2}.

.

Table 45 : CPU Frequency Generation (TQFP144 devices)

P0H.7	P0H.6	P0H.5	CPU Frequency $f_{CPU} = f_{XTAL} \times F$	External Clock Input Range[1]	Notes
1	1	1	f_{XTAL} x 4	2.5 to 8MHz	Default configuration
1	1	0	f_{XTAL} x 3	3.33 to 10.67MHz	
1	0	1	f_{XTAL} x 2	5 to 16MHz	
1	0	0	f_{XTAL} x 5	2 to 6.4MHz	
0	1	1	f_{XTAL} x 1	1 to 32MHz	Direct drive[2]
0	1	0	f_{XTAL} x 1.5	6.67 to 21.33MHz	
0	0	1	f_{XTAL} x 0.5	2 to 64MHz	CPU clock via prescaler[3]
0	0	0	f_{XTAL} x 2.5	4 to 12.8MHz	

Notes: 1. The external clock input range refers to a CPU clock range of 1...32MHz.
2. The maximum input frequency depends on the duty cycle of the external clock signal.
3. The maximum input frequency is 32MHz when using an external crystal with the internal oscillator; providing that internal serial resistance of the crystal is less than 40Ω. However, higher frequencies can be applied with an external clock source on pin XTAL1, but in this case, the input clock signal must reach the defined levels V_{IL} and V_{IH2}.

Figure 72 : External Memory Cycle: Multiplexed Bus, With / Without Read / Write Delay, Extended ALE

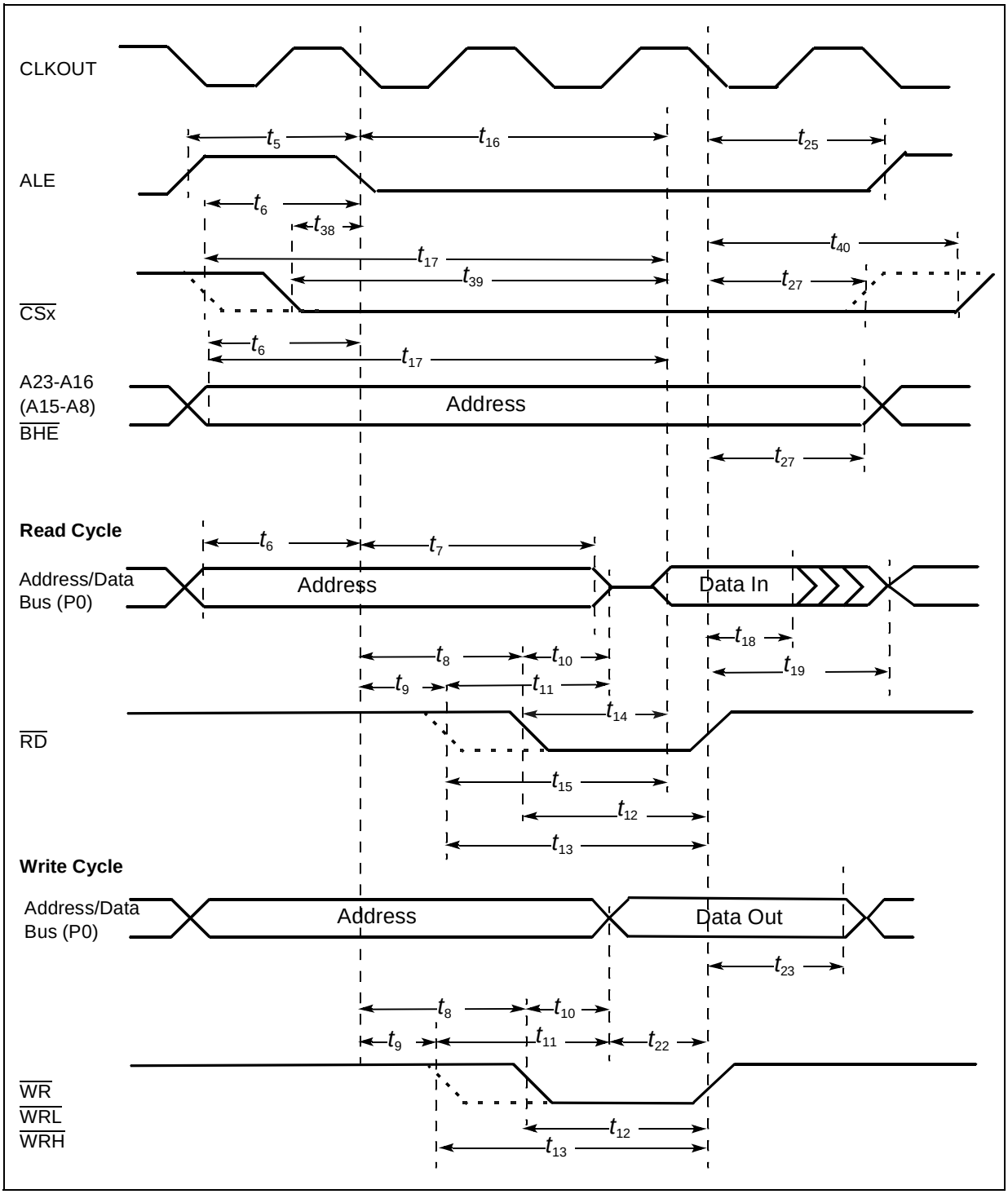
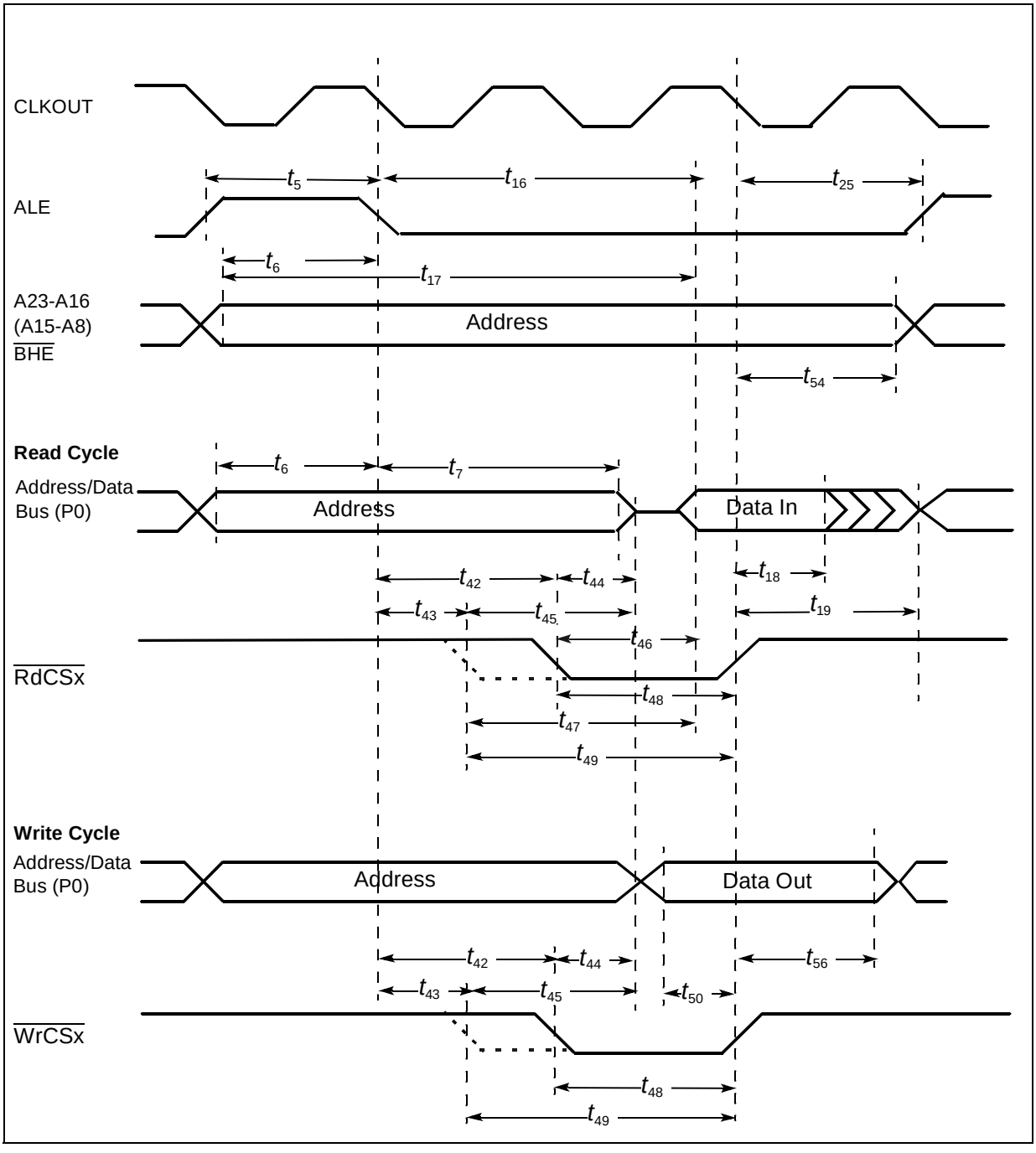


Figure 74 : External Memory Cycle: Multiplexed Bus, With / Without Read / Write Delay, Extended ALE, Read / Write Chip Select



ERRATA SHEET

ST10F269Zxxx-D
LIMITATIONS AND CORRECTIONS

1 - DESCRIPTION

This Errata sheet describes the functional and electrical problems known in the D revision of the ST10F269Zxxx.

The revision number can be found in the third line on the ST10F269 package. It looks like: 'xxxxxxxxx D' where "D" identifies the revision number.

2 - FUNCTIONAL PROBLEMS

The following malfunctions are known in this step:

2.1 - PWRDN.1 - Execution of PWRDN Instruction

When instruction PWRDN is executed while pin $\overline{\text{NMI}}$ is at a high level (if PWRDCFG bit is clear in SYSCON register) or while at least one of the port 2 pins used to exit from power-down mode (if PWRD-CFG bit is set in SYSCON register) is at the active level, power down mode is not entered, and the PWRDN instruction is ignored.

However, under the conditions described below, the PWRDN instruction is not ignored, and no further instructions are fetched from external memory, i.e. the CPU is in a quasi-idle state.

This problem only occurs in the following situations:

a) The instructions following the PWRDN instruction are located in an external memory, and a **multiplexed bus** configuration **with memory tristate waitstate** (bit MT-TCx = 0) is used.

   Or

b) The instruction preceeding the PWRDN instruction **writes** to external memory or an XPeripheral (XRAM,CAN), and the instructions following the PWRDN instruction are located in external memory. In this case, the problem occurs for any bus configuration.

Note: The on-chip peripherals are still working correctly, in particular the Watchdog Timer, if not disabled, resets the device upon an overflow. Interrupts and PEC transfers, however, cannot be processed. In case NMI is asserted low while the device is in this quasi-idle state, power-down mode is entered.

No problem occurs if the $\overline{\text{NMI}}$ pin is low (if PWRDCFG = 0) or if all P2 pins used to exit from power-down mode are at inactive level (if PWRDCFG = 1): the chip normally enters powerdown mode.

Workaround:

Ensure that no instruction that writes to external memory or an XPeripheral preceeds the PWRDN instruction, otherwise insert a NOP instruction in front of PWRDN. When a multiplexed bus with memory tristate wait state is used, the PWRDN instruction must be executed from internal RAM or XRAM.