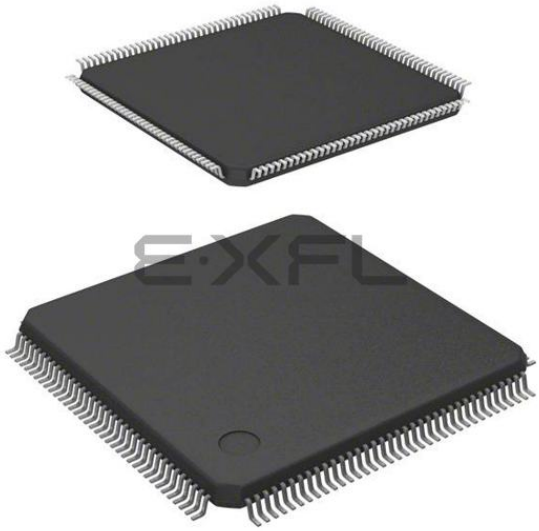

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f269z2q6-tr

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ST10F269

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Symbol	Pin	Type	Function		
P6.0 - P6.7	1 - 8	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 6 outputs can be configured as push-pull or open drain drivers. The following Port 6 pins have alternate functions:		
	1	O	P6.0	$\overline{CS0}$	Chip Select 0 Output
	...	...	...	...	...
	5	O	P6.4	$\overline{CS4}$	Chip Select 4 Output
	6	I	P6.5	$\overline{HOLD}$	External Master Hold Request Input
	7	O	P6.6	$\overline{HLDA}$	Hold Acknowledge Output
	8	O	P6.7	$\overline{BREQ}$	Bus Request Output
P8.0 - P8.7	9-16	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 8 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). The following Port 8 pins have alternate functions:		
	9	I/O	P8.0	CC16IO	CAPCOM2: CC16 Capture Input / Compare Output
	...	...	...	...	...
	16	I/O	P8.7	CC23IO	CAPCOM2: CC23 Capture Input / Compare Output
P7.0 - P7.7	19-26	I/O	8-bit bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 7 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins have alternate functions:		
	19	O	P7.0	POUT0	PWM Channel 0 Output
	...	...	...	...	...
	22	O	P7.3	POUT3	PWM Channel 3 Output
	23	I/O	P7.4	CC28IO	CAPCOM2: CC28 Capture Input / Compare Output
	...	...	...	...	...
	26	I/O	P7.7	CC31IO	CAPCOM2: CC31 Capture Input / Compare Output
P5.0 - P5.9 P5.10 - P5.15	27-36 39-44	I I	16-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 can be the analog input channels (up to 16) for the A/D converter, where P5.x equals ANx (Analog input channel x), or they are timer inputs:		
	39	I	P5.10	T6EUD	GPT2 Timer T6 External Up / Down Control Input
	40	I	P5.11	T5EUD	GPT2 Timer T5 External Up / Down Control Input
	41	I	P5.12	T6IN	GPT2 Timer T6 Count Input
	42	I	P5.13	T5IN	GPT2 Timer T5 Count Input
	43	I	P5.14	T4EUD	GPT1 Timer T4 External Up / Down Control Input
	44	I	P5.15	T2EUD	GPT1 Timer T2 External Up / Down Control Input

10 - GENERAL PURPOSE TIMER UNIT

The GPT unit is a flexible multifunctional timer/ counter structure which is used for time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication. The GPT unit contains five 16-bit timers organized into two separate modules GPT1 and GPT2. Each timer in each module may operate independently in several different modes, or may be concatenated with another timer of the same module.

10.1 - GPT1

Each of the three timers T2, T3, T4 of the GPT1 module can be configured individually for one of four basic modes of operation: **timer**, **gated timer**, **counter mode and incremental interface mode**.

In timer mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler.

In counter mode, the timer is clocked in reference to external events.

Pulse width or duty cycle measurement is supported in gated timer mode where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input.

Table 12 GPT1 Timer Input Frequencies, Resolution and Periods (PQFP144 devices) and Table 13 GPT1 Timer Input Frequencies, Resolution and Periods (TQFP144 devices) list the timer input frequencies, resolution and periods for each pre-scaler option at 40MHz (Table 12 GPT1 Timer Input Frequencies, Resolution and Periods (PQFP144 devices)) or 32MHz (Table 13 GPT1 Timer Input Frequencies, Resolution and Periods (TQFP144 devices)) CPU clock. This also applies to the Gated Timer Mode of T3 and to the auxiliary timers T2 and T4 in Timer and Gated Timer Mode. The count direction (up/down) for each timer is programmable by software or may be altered dynamically by an external signal on a port pin (TxEUD).

In Incremental Interface Mode, the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B by their respective inputs TxIN and TxEUD.

Direction and count signals are internally derived from these two input signals so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has output toggle latches (TxOTL) which changes state on each timer over flow / underflow. The state of this latch may be output on port pins (TxOUT) for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for high resolution of long duration measurements.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN).

Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

Table 12 : GPT1 Timer Input Frequencies, Resolution and Periods (PQFP144 devices)

f_{CPU} = 40MHz	Timer Input Selection T2I / T3I / T4I							
	000b	**001b**	**010b**	**011b**	**100b**	**101b**	**110b**	**111b**
Pre-scaler factor	8	16	32	64	128	256	512	1024
Input Freq	5MHz	2.5MHz	1.25MHz	625kHz	312.5kHz	156.25kHz	78.125kHz	39.1kHz
Resolution	200ns	400ns	0.8µs	1.6µs	3.2µs	6.4µs	12.8µs	25.6µs
Period maximum	13.1ms	26.2ms	52.4ms	104.8ms	209.7ms	419.4ms	838.9ms	1.678s

11 - PWM MODULE

The pulse width modulation module can generate up to four PWM output signals using edge-aligned or centre-aligned PWM. In addition, the PWM module can generate PWM burst signals and single shot outputs. Table 16 and Table 17 show the PWM frequencies for different resolutions. The level of the output signals is selectable and the PWM module can generate interrupt requests.

Figure 17 : Block Diagram of PWM Module

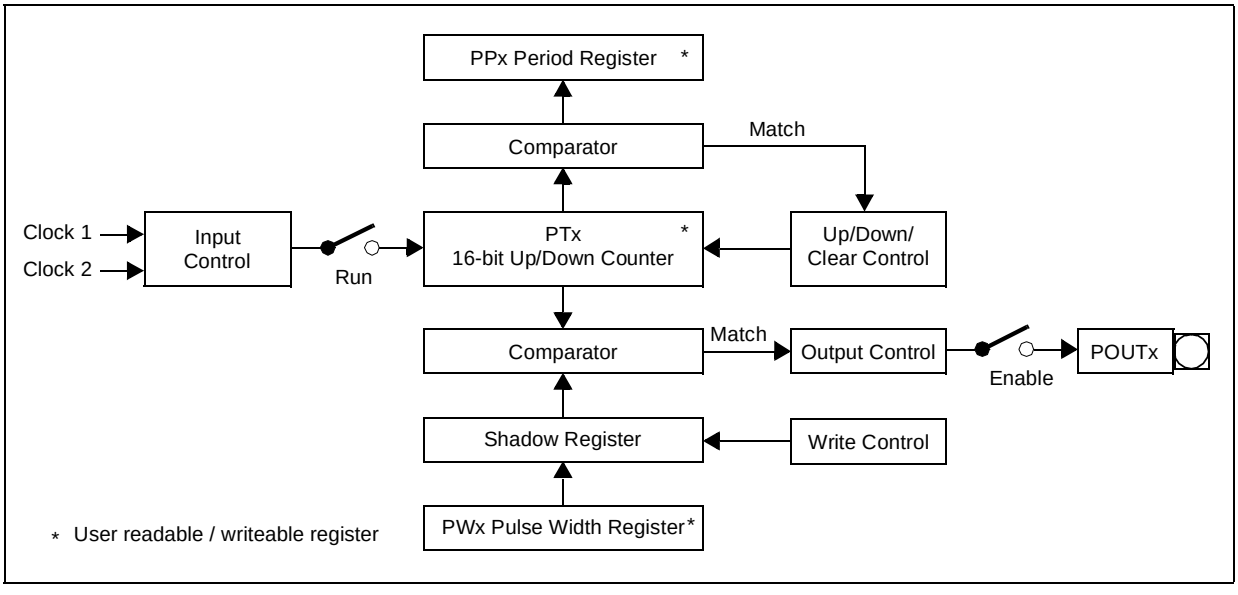


Table 16 : PWM Unit Frequencies and Resolution at 40MHz CPU Clock (PQFP144 devices)

Mode 0	Resolution	8-bit	10-bit	12-bit	14-bit	16-bit
CPU Clock/1	25ns	156.25kHz	39.1kHz	9.77kHz	2.44Hz	610Hz
CPU Clock/64	1.6 s	2.44Hz	610Hz	152.6Hz	38.15Hz	9.54Hz
Mode 1	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU Clock/1	25ns	78.12kHz	19.53kHz	4.88kHz	1.22kHz	305.17Hz
CPU Clock/64	1.6 s	1.22kHz	305.17Hz	76.29Hz	19.07Hz	4.77Hz

Table 17 : PWM Unit Frequencies and Resolution at 32MHz CPU Clock (TQFP144 devices)

Mode 0	Resolution	8-bit	10-bit	12-bit	14-bit	16-bit
CPU Clock/1	31.25ns	125KHz	31.25KHz	7.81KHz	1.953KHz	976.6Hz
CPU Clock/64	2.00 s	1.953KHz	488.3Hz	122.1Hz	30.52Hz	7.63Hz
Mode 1	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU Clock/1	31.25ns	62.5KHz	15.62KHz	3.90KHz	976.6Hz	244.1Hz
CPU Clock/64	2.00 s	976.6Hz	244.1Hz	61Hz	15.26Hz	3.81Hz

12 - PARALLEL PORTS

12.1 - Introduction

The ST10F269 MCU provides up to 111 I/O lines with programmable features. These capabilities bring very flexible adaptation of this MCU to wide range of applications.

ST10F269 has 9 groups of I/O lines gathered as following:

– Port 0 is a 2 time 8-bit port named P0L (Low as less significant Byte) and P0H (high as most significant Byte)

– Port 1 is a 2 time 8-bit port named P1L and P1H

– Port 2 is a 16-bit port

– Port 3 is a 15-bit port (P3.14 line is not implemented)

– Port 4 is a 8-bit port

– Port 5 is a 16-bit port input only

– Port 6, Port 7 and Port 8 are 8-bit port

These ports may be used as general purpose bidirectional input or output, software controlled with dedicated registers.

For example the output drivers of six of the ports (2, 3, 4, 6, 7, 8) can be configured (bit-wise) for push-pull or open drain operation using ODPx registers.

In addition, the sink and the source capability and the rise / fall time of the transition of the signal of some of the push-pull buffers can be programmed to fit the driving requirements of the application and to minimize EMI. This feature is implemented on Port 0, 1, 2, 3, 4, 6, 7 and 8 with the control registers POCONx. The output drivers capabilities of ALE, $\overline{RD}$, $\overline{WR}$ control lines are programmable with the dedicated bits of POCON20 control register.

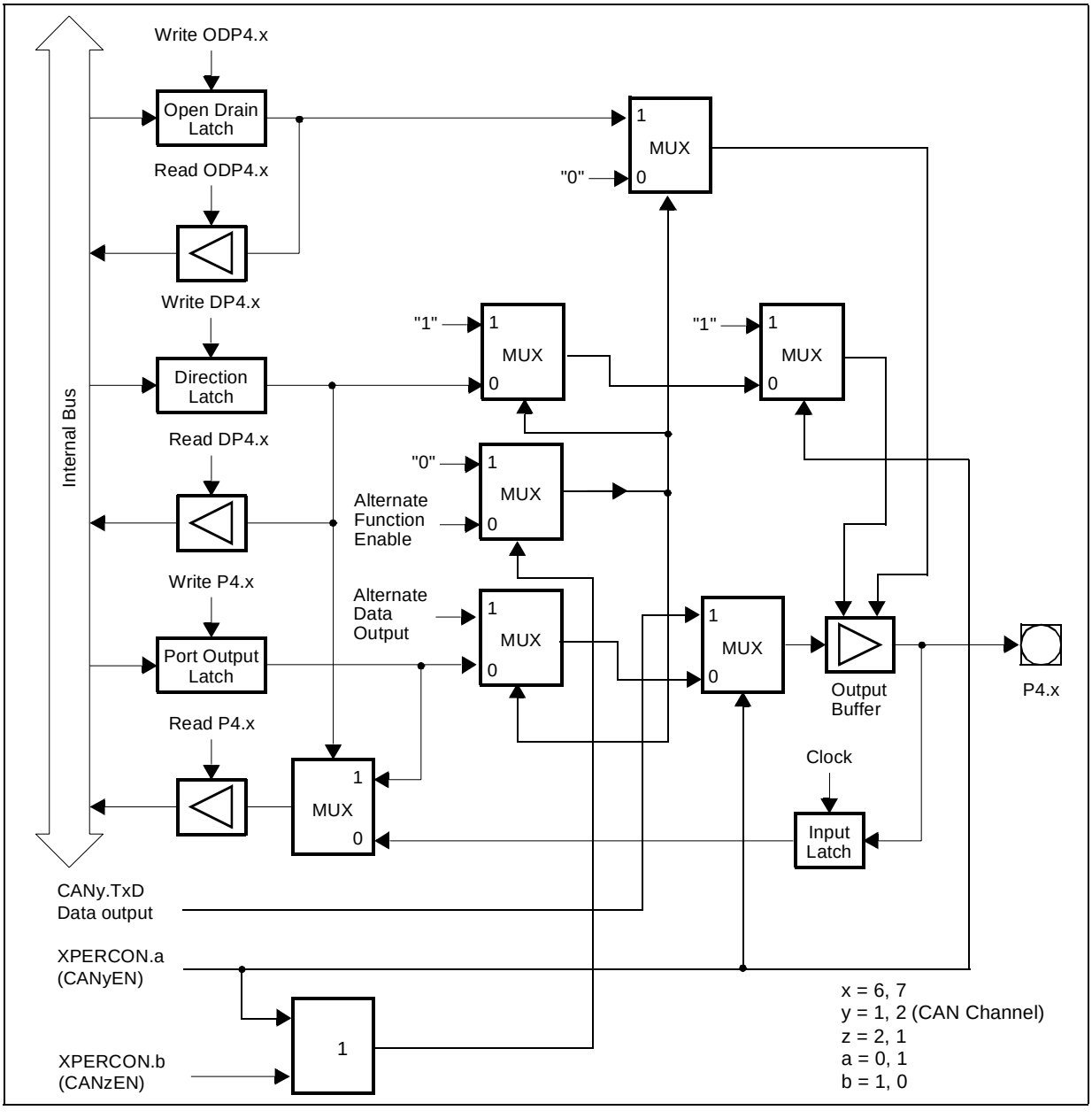
The input threshold levels are programmable (TTL/CMOS) for 5 ports (2, 3, 4, 7, 8). The logic level of a pin is clocked into the input latch once per state time, regardless whether the port is configured for input or output. The threshold is selected with the PICON register control bits.

A write operation to a port pin configured as an input causes the value to be written into the port output latch, while a read operation returns the latched state of the pin itself. A read-modify-write operation reads the value of the pin, modifies it, and writes it back to the output latch.

Writing to a pin configured as an output (DPx.y='1') causes the output latch and the pin to have the written value, since the output buffer is enabled. Reading this pin returns the value of the output latch. A read-modify-write operation reads the value of the output latch, modifies it, and writes it back to the output latch, thus also modifying the level at the pin.

I/O lines support an alternate function which is detailed in the following description of each port.

Figure 33 : Block Diagram of P4.6 and P4.7 Pins



12.8 - Port 5

This 16-bit input port can only read data. There is no output latch and no direction register. Data written to P5 will be lost.

P5 (FFA2h / D1h) SFR Reset Value: XXXXh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P5.15	P5.14	P5.13	P5.12	P5.11	P5.10	P5.9	P5.8	P5.7	P5.6	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

P5.y	**Port Data Register P5 Bit y (Read only)**

12.10 - Port 7

If this 8-bit port is used for general purpose I/O, the direction of each line can be configured via the corresponding direction register DP7. Each port line can be switched into push-pull or open drain mode via the open drain control register ODP7.

P7 (FFD0h / E8h) SFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	P7.7	P7.6	P7.5	P7.4	P7.3	P7.2	P7.1	P7.0
								RW	RW	RW	RW	RW	RW	RW	RW

P7.y	**Port Data Register P7 Bit y**

DP7 (FFD2h / E9h) SFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DP7.7	DP7.6	DP7.5	DP7.4	DP7.3	DP7.2	DP7.1	DP7.0
								RW	RW	RW	RW	RW	RW	RW	RW

DP7.y	**Port Direction Register DP7 Bit y** DP7.y = 0: Port line P7.y is an input (high impedance) DP7.y = 1: Port line P7.y is an output

ODP7 (F1D2h / E9h) ESFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	ODP7.7	ODP7.6	ODP7.5	ODP7.4	ODP7.3	ODP7.2	ODP7.1	ODP7.0
								RW	RW	RW	RW	RW	RW	RW	RW

ODP7.y	**Port 7 Open Drain Control Register Bit y** ODP7.y = 0: Port line P7.y output driver in push-pull mode ODP7.y = 1: Port line P7.y output driver in open drain mode

Table 40 : Special Function Registers Listed by Name (continued)

Name		Physical address		8-bit address	Description	Reset value
T0IC	b	FF9Ch		CEh	CAPCOM Timer 0 Interrupt Control Register	- - 00h
T0REL		FE54h		2Ah	CAPCOM Timer 0 Reload Register	0000h
T1		FE52h		29h	CAPCOM Timer 1 Register	0000h
T1IC	b	FF9Eh		CFh	CAPCOM Timer 1 Interrupt Control Register	- - 00h
T1REL		FE56h		2Bh	CAPCOM Timer 1 Reload Register	0000h
T2		FE40h		20h	GPT1 Timer 2 Register	0000h
T2CON	b	FF40h		A0h	GPT1 Timer 2 Control Register	0000h
T2IC	b	FF60h		B0h	GPT1 Timer 2 Interrupt Control Register	- - 00h
T3		FE42h		21h	GPT1 Timer 3 Register	0000h
T3CON	b	FF42h		A1h	GPT1 Timer 3 Control Register	0000h
T3IC	b	FF62h		B1h	GPT1 Timer 3 Interrupt Control Register	- - 00h
T4		FE44h		22h	GPT1 Timer 4 Register	0000h
T4CON	b	FF44h		A2h	GPT1 Timer 4 Control Register	0000h
T4IC	b	FF64h		B2h	GPT1 Timer 4 Interrupt Control Register	- - 00h
T5		FE46h		23h	GPT2 Timer 5 Register	0000h
T5CON	b	FF46h		A3h	GPT2 Timer 5 Control Register	0000h
T5IC	b	FF66h		B3h	GPT2 Timer 5 Interrupt Control Register	- - 00h
T6		FE48h		24h	GPT2 Timer 6 Register	0000h
T6CON	b	FF48h		A4h	GPT2 Timer 6 Control Register	0000h
T6IC	b	FF68h		B4h	GPT2 Timer 6 Interrupt Control Register	- - 00h
T7		F050h	E	28h	CAPCOM Timer 7 Register	0000h
T78CON	b	FF20h		90h	CAPCOM Timer 7 and 8 Control Register	0000h
T7IC	b	F17Ah	E	BEh	CAPCOM Timer 7 Interrupt Control Register	- - 00h
T7REL		F054h	E	2Ah	CAPCOM Timer 7 Reload Register	0000h
T8		F052h	E	29h	CAPCOM Timer 8 Register	0000h
T8IC	b	F17Ch	E	BFh	CAPCOM Timer 8 Interrupt Control Register	- - 00h
T8REL		F056h	E	2Bh	CAPCOM Timer 8 Reload Register	0000h
TFR	b	FFACh		D6h	Trap Flag Register	0000h
WDT		FEAEh		57h	Watchdog Timer Register (read only)	0000h
WDTCON	b	FFAEh		D7h	Watchdog Timer Control Register	00xxh [2]
XP0IC	b	F186h	E	C3h	CAN1 Module Interrupt Control Register	- - 00h [3]
XP1IC	b	F18Eh	E	C7h	CAN2 Module Interrupt Control Register	- - 00h [3]
XP2IC	b	F196h	E	CBh	Flash ready/busy interrupt control register	- - 00h [3]
XP3IC	b	F19Eh	E	CFh	PLL unlock Interrupt Control Register	- - 00h [3]
XPERCON		F024h	E	12h	XPER Configuration Register	- - 05h
ZEROS	b	FF1Ch		8Eh	Constant Value 0's Register (read only)	0000h

Notes: 1. The system configuration is selected during reset.

2. Bit WDTR indicates a watchdog timer triggered reset.

3. The XPnIC Interrupt Control Registers control interrupt requests from integrated X-Bus peripherals. Some software controlled interrupt requests may be generated by setting the XPnIR bits (of XPnIC register) of the unused X-peripheral nodes.

20.1 - Identification Registers

The ST10F269 has four Identification registers, mapped in ESFR space. These registers contain:

– A manufacturer identifier,

– A chip identifier, with its revision,

– A internal memory and size identifier and programming voltage description.

Note: 256K and 128K versions of ST10F269 have the same IDMEM corresponding to 256K.

Both versions are based on the same device with the only difference that the two upper banks of Flash are not tested on 128K versions. Therefore, there is no way to detect by software if a device is a 128K version or a 256K version.

IDMANUF (F07Eh / 3Fh) [1] ESFR Reset Value: 0401h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MANUF											0	0	0	0	1
R															

MANUF	**Manufacturer Identifier** - 020h: STMicroelectronics Manufacturer (JTAG worldwide normalization).

IDCHIP (F07Ch / 3Eh) [1] ESFR Reset Value: 10DXh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHIPID												REVID			
R												R			

REVID	**Device Revision Identifier**
CHIPID	**Device Identifier** - 10Dh: ST10F269 identifier.

IDMEM (F07Ah / 3Dh) [1] ESFR Reset Value: 3040h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEMTYP				MEMSIZE											
R				R											

MEMSIZE	**Internal Memory Size** is calculated using the following formula: Size = 4 x [MEMSIZE] (in K Byte) - 040h for ST10F269 (256K Byte)
MEMTYP	**Internal Memory Type** - 3h for ST10F269 (Flash memory).

IDPROG (F078h / 3Ch) [1] ESFR Reset Value: 0040h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROGVPP								PROGVDD							
R								R							

PROGVDD	**Programming V_{DD} Voltage** V_{DD} voltage when programming EPROM or FLASH devices is calculated using the following formula: V_{DD} = 20 x [PROGVDD] / 256 (volts) - 40h for ST10F269 (5V).
PROGVPP	**Programming V_{PP} Voltage** (no need of external V_{PP}) - 00h

Note : 1. All identification words are read only registers.

Symbol	Parameter		Test Conditions	Min.	Max.	Unit
I_{PD2}	Power-down mode supply current (Real time clock enabled, oscillator enabled)	10 12	V_{DD} = 5.5V T_A = 55°C f_{OSC} = 25MHz	–	2 + f_{OSC} / 4	mA

Notes: 1. ST10F269 pins are equipped with low-noise output drivers which significantly improve the device's EMI performance. These low-noise drivers deliver their maximum current only until the respective target output level is reached. After this, the output current is reduced. This results in increased impedance of the driver, which attenuates electrical noise from the connected PCB tracks. The current specified in column "Test Conditions" is delivered in any cases.

2. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.
3. Partially tested, guaranteed by design characterization.

4. Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$+0.5V or $V_{OV} < -0.5V$). The absolute sum of input overload currents on all port pins may not exceed 50mA. The supply voltage must remain within the specified limits.

5. This specification is only valid during Reset, or during Hold-mode or Adapt-mode. Port 6 pins are only affected if they are used for $\overline{CS}$ output and if their open drain function is not enabled.

6. The maximum current may be drawn while the respective signal line remains inactive.

7. The minimum current must be drawn in order to drive the respective signal line active.

8. The power supply current is a function of the operating frequency. This dependency is illustrated in Figure 65 and Figure 65. These parameters are tested at V_{DD}max and 40MHz (or 32MHz) CPU clock with all outputs disconnected and all inputs at VIL or VIH. The chip is configured with a demultiplexed 16-bit bus, direct clock drive, 5 chip select lines and 2 segment address lines, $\overline{EA}$ pin is low during reset. After reset, PORT 0 is driven with the value '00CCh' that produces infinite execution of NOP instruction with 15 wait-states, R/W delay, memory tristate wait state, normal ALE. Peripherals are not activated.

9. Idle mode supply current is a function of the operating frequency. This dependency is illustrated in the Figure 65. These parameters are tested at V_{DD}max and 40MHz (or 32MHz) CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

10. This parameter value includes leakage currents. With all inputs (including pins configured as inputs) at 0V to 0.1V or at V_{DD} – 0.1V to V_{DD}, V_{REF} = 0V, all outputs (including pins configured as outputs) disconnected.

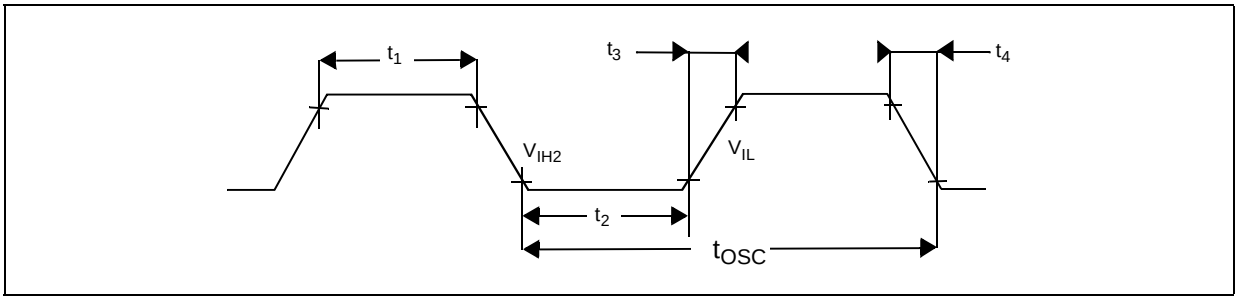
11. Typical I_{PD} value is 5µA @ T_A=25°C, 20µA @ T_A=85°C and 60µA @ T_A=125°C.
12. Partially tested, guaranteed by design characterization using 22pF loading capacitors on crystal pins.

V_{DD} = 5V 10%, V_{SS} = 0V, T_A = -40 to +125 °C (TQFP144 devices)

Parameter	Symbol		$f_{CPU} = f_{XTAL}$		$f_{CPU} = f_{XTAL} / 2$		$f_{CPU} = f_{XTAL} \times F$ F = 1.5/2,/2.5/3/4/5		Unit
			Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
Oscillator period	t_{OSC}	SR	31.25[1]	–	15.625	–	31.25 x N	–	ns
High time	t_1	SR	12.5[2]	–	6.25[2]	–	12.5[2]	–	ns
Low time	t_2	SR	12.5[2]	–	6.25[2]	–	12.5[2]	–	ns
Rise time	t_3	SR	–	3.125[2]	–	1.56[2]	–	3.125[2]	ns
Fall time	t_4	SR	–	3.125[2]	–	1.56[2]	–	3.125[2]	ns

1. Theoretical minimum. The real minimum value depends on the duty cycle of the input clock signal. 32MHz is the maximum input frequency when using an external crystal oscillator. However, 32MHz can be applied with an external clock source.
2. The input clock signal must reach the defined levels V_{IL} and V_{IH2}.

Figure 70 : External Clock Drive XTAL1



21.4.9 - Memory Cycle Variables

The tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Description	Symbol	Values
ALE Extension	t_A	TCL x [ALECTL]
Memory Cycle Time wait states	t_C	2TCL x (15 - [MCTC])
Memory Tri-state Time	t_F	2TCL x (1 - [MTTC])

Symbol		Parameter	Maximum CPU Clock = 32MHz		Variable CPU Clock 1/2 TCL = 1 to 32MHz		Unit
			Minimum	Maximum	Minimum	Maximum	
t_{81}	CC	Address/Unlatched $\overline{CS}$ setup to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	5.625 + $2t_A$	–	TCL -10 + $2t_A$	–	ns
t_{12}	CC	$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	21.25 + t_C	–	2TCL - 10 + t_C	–	ns
t_{13}	CC	$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	36.875 + t_C	–	3TCL - 10 + t_C	–	ns
t_{14}	SR	$\overline{RD}$ to valid data in (with RW-delay)	–	11.25 + t_C	–	2TCL - 20 + t_C	ns
t_{15}	SR	$\overline{RD}$ to valid data in (no RW-delay)	–	26.875 + t_C	–	3TCL - 20 + t_C	ns
t_{16}	SR	ALE low to valid data in	–	26.875 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
t_{17}	SR	Address/Unlatched $\overline{CS}$ to valid data in	–	32.5 + $2t_A$ + t_C	–	4TCL - 30 + $2t_A$ + t_C	ns
t_{18}	SR	Data hold after $\overline{RD}$ rising edge	0	–	0	–	ns
t_{20}	SR	Data float after $\overline{RD}$ rising edge (with RW-delay)[1 - 3]	–	26 + t_F	–	2TCL - 14 + t_F + $2t_A$[1]	ns
t_{21}	SR	Data float after $\overline{RD}$ rising edge (no RW-delay) [1 - 3]	–	5.625 + t_F	–	TCL - 10 + t_F + $2t_A$[1]	ns
t_{22}	CC	Data valid to $\overline{WR}$	11.25 + t_C	–	2TCL- 20 + t_C	–	ns
t_{24}	CC	Data hold after $\overline{WR}$	5.625 + t_F	–	TCL - 10+ t_F	–	ns
t_{26}	CC	ALE rising edge after $\overline{RD}$, $\overline{WR}$	-10 + t_F	–	-10 + t_F	–	ns
t_{28}	CC	Address/Unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$ [2]	0 (no t_F) -5 + t_F (t_F > 0)	–	0 (no t_F) -5 + t_F (t_F > 0)	–	ns
t_{28h}	CC	Address/Unlatched $\overline{CS}$ hold after $\overline{WRH}$	-5 + t_F	–	-5 + t_F	–	ns
t_{38}	CC	ALE falling edge to Latched $\overline{CS}$	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
t_{39}	SR	Latched $\overline{CS}$ low to Valid Data In	–	26.875 + t_C+ $2t_A$	–	3TCL - 20 + t_C + $2t_A$	ns
t_{41}	CC	Latched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	1.625 + t_F	–	TCL - 14 + t_F	–	ns
t_{82}	CC	Address setup to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	17.25 + $2t_A$	–	2TCL - 14 + $2t_A$	–	ns
t_{83}	CC	Address setup to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	1.625 + $2t_A$	–	TCL -14 + $2t_A$	–	ns
t_{46}	SR	$\overline{RdCS}$ to Valid Data In (with RW-delay)	–	7.25 + t_C	–	2TCL - 24 + t_C	ns
t_{47}	SR	$\overline{RdCS}$ to Valid Data In (no RW-delay)	–	22.875 + t_C	–	3TCL - 24 + t_C	ns

21.4.14 - High-Speed Synchronous Serial Interface (SSC) Timing

21.4.14.1 Master Mode

V_{CC} = 5V ±10%, V_{SS} = 0V, CPU clock = 40MHz, T_A = -40 to +125°C, C_L = 50pF (PQFP144 devices)

Symbol		Parameter	Maximum Baud rate = 10M Baud (<SSCBR> = 0001h)		Variable Baud rate (<SSCBR>=0001h-FFFFh)		Unit
			Minimum	Maximum	Minimum	Maximum	
t_{300}	CC	SSC clock cycle time	100	100	8 TCL	262144 TCL	ns
t_{301}	CC	SSC clock high time	40	–	t_{300}/2 - 10	–	ns
t_{302}	CC	SSC clock low time	40	–	t_{300}/2 - 10	–	ns
t_{303}	CC	SSC clock rise time	–	10	–	10	ns
t_{304}	CC	SSC clock fall time	–	10	–	10	ns
t_{305}	CC	Write data valid after shift edge	–	15	–	15	ns
t_{306}	CC	Write data hold after shift edge [1]	-2	–	-2	–	ns
t_{307p}	SR	Read data setup time before latch edge, phase error detection on (SSCPEN = 1)	37.5	–	2TCL+12.5	–	ns
t_{308p}	SR	Read data hold time after latch edge, phase error detection on (SSCPEN = 1)	50	–	4TCL	–	ns
t_{307}	SR	Read data setup time before latch edge, phase error detection off (SSCPEN = 0)	25	–	2TCL	–	ns
t_{308}	SR	Read data hold time after latch edge, phase error detection off (SSCPEN = 0)	0	–	0	–	ns

Note: 1. Timing guaranteed by design.

The formula for SSC Clock Cycle time is: t_{300} = 4 TCL * (<SSCBR> + 1)
Where <SSCBR> represents the content of the SSC Baud rate register, taken as unsigned 16-bit integer.

V_{CC} = 5V ±10%, V_{SS} = 0V, CPU clock = 32MHz, T_A = -40 to +125°C, C_L = 50pF (TQFP144 devices)

Symbol		Parameter	Maximum Baud rate=6.25MBd (<SSCBR> = 0001h)		Variable Baud rate (<SSCBR>=0001h-FFFFh)		Symbol
			Minimum	Maximum	Minimum	Maximum	
t_{310}	SR	SSC clock cycle time	125	–	8 TCL	262144 TCL	t_{310}
t_{311}	SR	SSC clock high time	52.5	–	t_{310}/2 - 10	–	t_{311}
t_{312}	SR	SSC clock low time	52.5	–	t_{310}/2 - 10	–	t_{312}
t_{313}	SR	SSC clock rise time	–	10	–	10	t_{313}
t_{314}	SR	SSC clock fall time	–	10	–	10	t_{314}
t_{315}	CC	Write data valid after shift edge	–	45.25	–	2 TCL + 14	t_{315}
t_{316}	CC	Write data hold after shift edge	0	–	0	–	t_{316}
t_{317p}	SR	Read data setup time before latch edge, phase error detection on (SSCPEN = 1)	78.125	–	4TCL + 15.625	–	t_{317p}
t_{318p} [1]	SR	Read data hold time after latch edge, phase error detection on (SSCPEN = 1)	109.375	–	6TCL + 15.625	–	t_{318p} [1]
t_{317}	SR	Read data setup time before latch edge, phase error detection off (SSCPEN = 0)	6	–	6	–	t_{317}