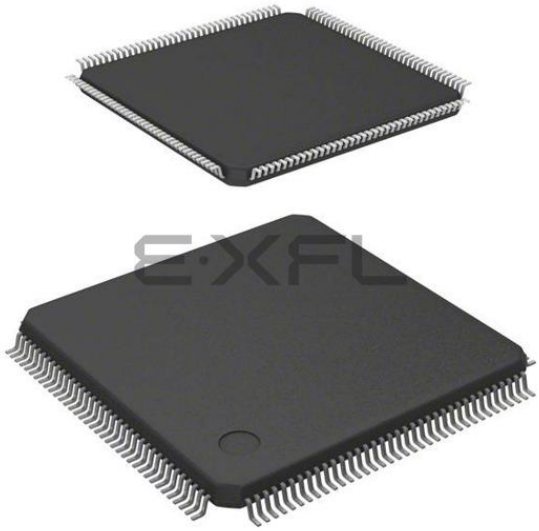


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f269z2q6

4 - MEMORY ORGANIZATION

The memory space of the ST10F269 is configured in a unified memory architecture. Code memory, data memory, registers and I/O ports are organized within the same linear address space of 16M Bytes. The entire memory space can be accessed Byte wise or Word wise. Particular portions of the on-chip memory have additionally been made directly bit addressable.

Flash: 128K or 256K Bytes of on-chip Flash memory.

IRAM: 2K Bytes of on-chip internal RAM (dual-port) is provided as a storage for data, system stack, general purpose register banks and code. A register bank is 16 Wordwide (R0 to R15) and / or Bytewide (RL0, RH0, …, RL7, RH7) general purpose registers.

XRAM: 10K Bytes of on-chip extension RAM (single port XRAM) is provided as a storage for data, user stack and code.

The XRAM is divided into 2 areas, the first 2K Bytes named XRAM1 and the second 8K Bytes named XRAM2, connected to the internal XBUS and are accessed like an external memory in 16-bit demultiplexed bus-mode without wait state or read/write delay (50ns access at 40MHz CPU clock on PQFP144 devices and 62.5ns access at 32MHz CPU clock on TQFP144 devices). Byte and Word accesses are allowed.

The XRAM1 address range is 00'E000h - 00'E7FFh if XPEN (bit 2 of SYSCON register), and XRAM1EN (bit 2 of XPERCON register) are set. If XRAM1EN or XPEN is cleared, then any access in the address range 00'E000h - 00'E7FFh will be directed to external memory interface, using the BUSCONx register corresponding to address matching ADDRSELx register

The XRAM2 address range is 00'C000h - 00'DFFFh if XPEN (bit 2 of SYSCON register), and XRAM2 (bit 3 of XPERCON register are set). If bit XRAM2EN or XPEN is cleared, then any access in the address range 00'C000h - 00'DFFFh will be directed to external memory interface, using the BUSCONx register corresponding to address matching ADDRSELx register.
As the XRAM appears like external memory, it cannot be used as system stack or as register banks. The XRAM is not provided for single bit storage and therefore is not bit addressable.

SFR/ESFR: 1024 Bytes (2 x 512 Bytes) of address space is reserved for the special function register areas. SFRs are Wordwide registers which are used to control and to monitor the function of the different on-chip units.

CAN1: Address range 00'EF00h - 00'EFFFh is reserved for the CAN1 Module access. The CAN1 is enabled by setting XPEN bit 2 of the SYSCON register and by setting CAN1EN bit 0 of the new XPERCON register. Accesses to the CAN Module use demultiplexed addresses and a 16-bit data bus (Byte accesses are possible). Two wait states give an access time of 100ns at 40MHz CPU clock on PQFP144 devices (or 125ns at 32MHz CPU clock on TQFP144 devices). No tri-state wait states are used.

CAN2: Address range 00'EE00h - 00'EEFFh is reserved for the CAN2 Module access. The CAN2 is enabled by setting XPEN bit 2 of the SYSCON register and by setting CAN2EN bit 1 of the new XPERCON register. Accesses to the CAN Module use demultiplexed addresses and a 16-bit data bus (Byte accesses are possible). Two wait states give an access time of 100ns at 40MHz CPU clock on PQFP144 devices (or 125ns at 32MHz CPU clock on TQFP144 devices). No tri-state wait states are used.

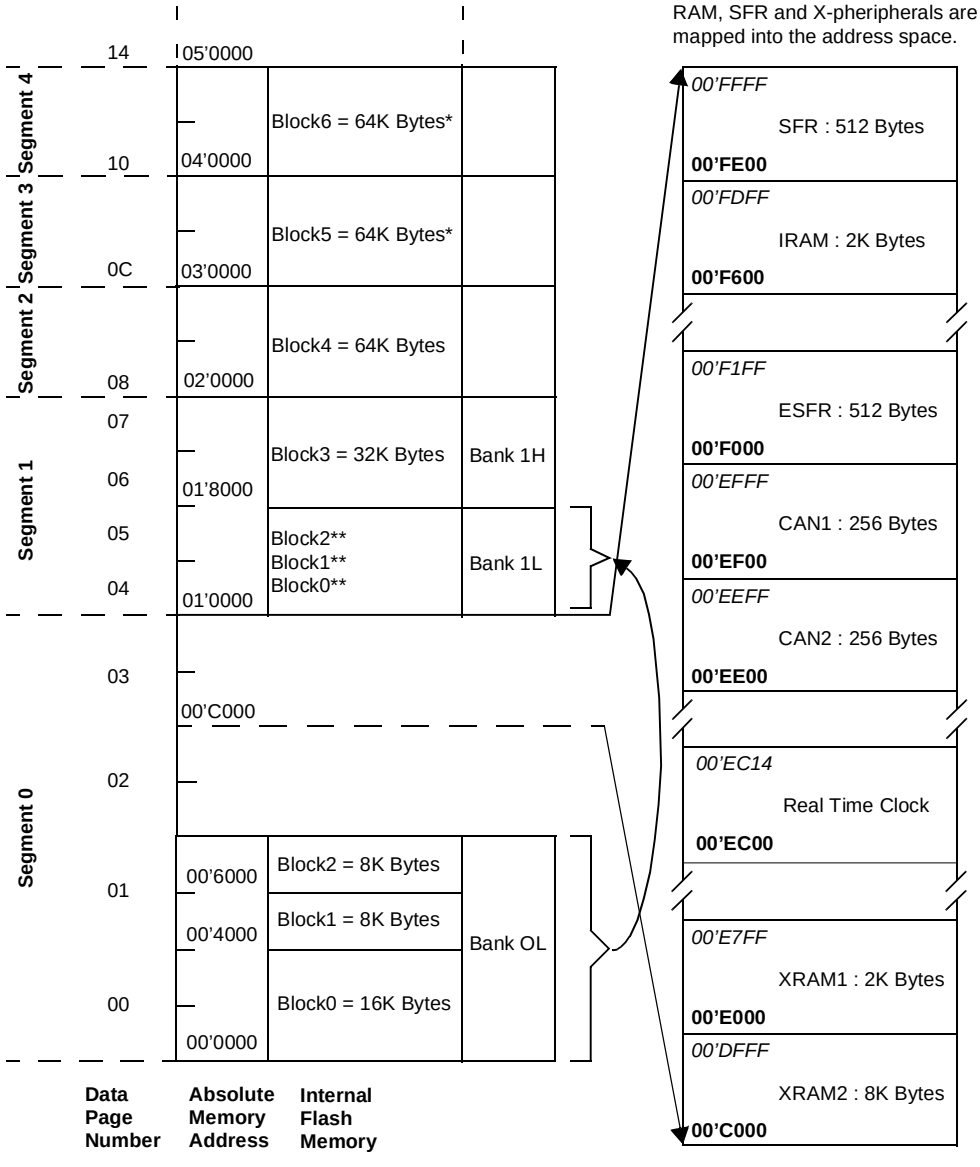
In order to meet the needs of designs where more memory is required than is provided on chip, up to 16M Bytes of external RAM and/or ROM can be connected to the microcontroller.

Note If one or the two CAN modules are used, Port 4 cannot be programmed to output all 8 segment address lines. Thus, only 4 segment address lines can be used, reducing the external memory space to 5M Bytes (1M Byte per $\overline{CS}$ line).

Visibility of XBUS Peripherals

In order to keep the ST10F269 compatible with the ST10C167 and with the ST10F167, the XBUS peripherals can be selected to be visible and / or accessible on the external address / data bus. CAN1EN and CAN2EN bits of XPERCON register must be set. If these bits are cleared before the global enabling with XPEN-bit in SYSCON register, the corresponding address space, port pins and interrupts are not occupied by the peripheral, thus the peripheral is not visible and not available. Refer to Chapter : *Special Function Register Overview* on page 125.

Figure 4 : ST10F269 On-chip Memory Mapping



*Reserved area for 128K versions.

** Bank 0L may be remapped from segment 0 to segment 1 (Bank 1L) by setting SYSCON-ROMS1 (before EINIT)
Data Page Number and Absolute Memory Address are hexadecimal values.

be temporarily unlocked for update (write) operations.

With the two possibilities for write protection - whole memory or block specific - a flexible installation of write protection is supported to protect the Flash memory or parts of it from unauthorized programming or erase accesses and to provide virus-proof protection for all system code blocks. All write protection also is enabled during boot operation.

Power Supply, Reset

The Flash module uses a single power supply for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations from 5V supply. Once a program or erase cycle has been completed, the device resets to the standard read mode. At power-on, the Flash memory has a setup phase of some microseconds (dependent on the power supply ramp-up). During this phase, Flash can not be read. Thus, if $\overline{EA}$ pin is high (execution will start from Flash memory), the CPU will remains in reset state until the Flash can be accessed.

5.3 - Architectural Description

The Flash module distinguishes two basic operating modes, the standard read mode and the command mode. The initial state after power-on and after reset is the standard read mode.

5.3.1 - Read Mode

The Flash module enters the standard operating mode, the read mode:

– After Reset command
– After every completed erase operation
– After every completed programming operation
– After every other completed command execution
– Few microseconds after a CPU-reset has started
– After incorrect address and data values of command sequences or writing them in an improper sequence
– After incorrect write access to a read protected Flash memory

The read mode remains active until the last command of a command sequence is decoded which starts directly a Flash array operation, such as:

– erase one or several blocks
– program a word into Flash array
– protect / temporary unprotect a block.

In the standard read mode read accesses are directly controlled by the Flash memory array, delivering a 32-bit double Word from the addressed position. Read accesses are always aligned to double Word boundaries. Thus, both low order address bit A1 and A0 are not used in the Flash array for read accesses. The high order address bit A17/A16 define the physical 64K Byte segment being accessed within the Flash array.

5.3.2 - Command Mode

Every operation besides standard read operations is initiated by commands written to the Flash command register. The addresses used for command cycles define in conjunction with the actual state the specific step within command sequences. With the last command of a command sequence, the Erase-Program Controller (EPC) starts the execution of the command. The EPC status is indicated during command execution by:

– The Status Register,

– The Ready/Busy signal.

5.3.3 - Ready/Busy Signal

The Ready/Busy ($\overline{R}$/B) signal is connected to the XPER2 interrupt node (XP2IC). When $\overline{R}$/B is high, the Flash is busy with a Program or Erase operation and will not accept any additional program or erase instruction. When $\overline{R}$/B is Low, the Flash is ready for any Read/Write or Erase operation. The $\overline{R}$/B will also be low when the memory is put in Erase Suspend mode.

This signal can be polled by reading XP2IC register, or can be used to trigger an interrupt when the Flash goes from Busy to Ready.

5.3.4 - Flash Status Register

The Flash Status register is used to flag the status of the Flash memory and the result of an operation. This register can be accessed by Read cycles during the program-Erase Controller operations. The program or erase operation can be controlled by data polling on bit FSB.7 of Status Register, detection of Toggle on FSB.6 and FSB.2, or Error on FSB.5 and Erase Time-out on FSB.3 bit. Any read attempt in Flash during EPC operation will automatically output these five bits. The EPC sets bit FSB.2, FSB.3, FSB.5, FSB.6 and FSB.7. Other bits are reserved for future use and should be masked.

Flash Status (see note for address)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	**FSB.7**	**FSB.6**	**FSB.5**	-	**FSB.3**	**FSB.2**	-	-
								R	R	R		R	R		

FSB.7	**Flash Status bit 7: Data Polling Bit** Programming Operation: this bit outputs the complement of the bit 7 of the word being programmed, and after completion, will output the bit 7 of the word programmed. Erasing Operation: outputs a ‘0’ during erasing, and ‘1’ after erasing completion. If the block selected for erasure is (are) protected, FSB.7 will be set to ‘0’ for about 100 µs, and then return to the previous addressed memory data value. FSB.7 will also flag the Erase Suspend Mode by switching from ‘0’ to ‘1’ at the start of the Erase Suspend. During Program operation in Erase Suspend Mode, FSB.7 will have the same behaviour as in normal Program execution outside the Suspend mode.
FSB.6	**Flash Status bit 6: Toggle Bit** Programming or Erasing Operations: successive read operations of Flash Status register will deliver complementary values. FSB.6 will toggle each time the Flash Status register is read. The Program operation is completed when two successive reads yield the same value. The next read will output the bit last programmed, or a ‘1’ after Erase operation FSB.6 will be set to‘1’ if a read operation is attempted on an Erase Suspended block. In addition, an Erase Suspend/Resume command will cause FSB.6 to toggle.
FSB.5	**Flash Status bit 5: Error Bit** This bit is set to ‘1’ when there is a failure of Program, block or chip erase operations.This bit will also be set if a user tries to program a bit to ‘1’ to a Flash location that is currently programmed with ‘0’. The error bit resets after Read/Reset instruction. In case of success, the Error bit will be set to ‘0’ during Program or Erase and then will output the bit last programmed or a ‘1’ after erasing
FSB.3	**Flash Status bit 3: Erase Time-out Bit** This bit is cleared by the EPC when the last Block Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the time-out period is finished, after 96 µs, FSB.3 returns back to ‘1’.
FSB.2	**Flash Status bit 2: Toggle Bit** This toggle bit, together with FSB.6, can be used to determine the chip status during the Erase Mode or Erase Suspend Mode. It can be used also to identify the block being Erased Suspended. A Read operation will cause FSB.2 to Toggle during the Erase Mode. If the Flash is in Erase Suspend Mode, a Read operation from the Erase suspended block or a Program operation into the Erase suspended block will cause FSB.2 to toggle. When the Flash is in Program Mode during Erase Suspend, FSB.2 will be read as ‘1’ if address used is the address of the word being programmed. After Erase completion with an Error status, FSB.2 will toggle when reading the faulty sector.

Note: The Address of Flash Status Register is the address of the word being programmed when Programming operation is in progress, or an address within block being erased when Erasing operation is in progress.

Table 7 : Interrupt Sources (continued)

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Timer 1	T1IR	T1IE	T1INT	00'0084h	21h
CAPCOM Timer 7	T7IR	T7IE	T7INT	00'00F4h	3Dh
CAPCOM Timer 8	T8IR	T8IE	T8INT	00'00F8h	3Eh
GPT1 Timer 2	T2IR	T2IE	T2INT	00'0088h	22h
GPT1 Timer 3	T3IR	T3IE	T3INT	00'008Ch	23h
GPT1 Timer 4	T4IR	T4IE	T4INT	00'0090h	24h
GPT2 Timer 5	T5IR	T5IE	T5INT	00'0094h	25h
GPT2 Timer 6	T6IR	T6IE	T6INT	00'0098h	26h
GPT2 CAPREL Register	CRIR	CRIE	CRINT	00'009Ch	27h
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	00'00A0h	28h
A/D Overrun Error	ADEIR	ADEIE	ADEINT	00'00A4h	29h
ASC0 Transmit	S0TIR	S0TIE	S0TINT	00'00A8h	2Ah
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	00'011Ch	47h
ASC0 Receive	S0RIR	S0RIE	S0RINT	00'00ACh	2Bh
ASC0 Error	S0EIR	S0EIE	S0EINT	00'00B0h	2Ch
SSC Transmit	SCTIR	SCTIE	SCTINT	00'00B4h	2Dh
SSC Receive	SCRIR	SCRIE	SCRINT	00'00B8h	2Eh
SSC Error	SCEIR	SCEIE	SCEINT	00'00BCh	2Fh
PWM Channel 0...3	PWMIR	PWMIE	PWMINT	00'00FCh	3Fh
CAN1 Interface	XP0IR	XP0IE	XP0INT	00'0100h	40h
CAN2 Interface	XP1IR	XP1IE	XP1INT	00'0104h	41h
FLASH Ready / Busy	XP2IR	XP2IE	XP2INT	00'0108h	42h
PLL Unlock/OWD	XP3IR	XP3IE	XP3INT	00'010Ch	43h

Hardware traps are exceptions or error conditions that arise during run-time. They cause immediate non-maskable system reaction similar to a standard interrupt service (branching to a dedicated vector table location).

The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any other program execution. Hardware trap services cannot not be interrupted by standard interrupt or by PEC interrupts.

8.3 - Interrupt Control Registers

All interrupt control registers are identically organized. The lower 8 bits of an interrupt control register contain the complete interrupt status information of the associated source, which is required during one round of prioritization, the upper 8 bits of the respective register are reserved. All interrupt control registers are bit addressable and all bits can be read or written via software.

This allows each interrupt source to be programmed or modified with just one instruction. When accessing interrupt control registers through instructions which operate on Word data types, their upper 8 bits (15...8) will return zeros, when read, and will discard written data.

The layout of the Interrupt Control registers shown below applies to each xxIC register, where xx stands for the mnemonic for the respective source.

12.4 - PORT1

The two 8-bit ports P1H and P1L represent the higher and lower part of PORT1, respectively. Both halves of PORT1 can be written (via a PEC transfer) without effecting the other half.

If this port is used for general purpose I/O, the direction of each line can be configured via the corresponding direction registers DP1H and DP1L.

P1L (FF04h / 82h) SFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	P1L.7	P1L.6	P1L.5	P1L4	P1L.3	P1L.2	P1L.1	P1L.0
								RW	RW	RW	RW	RW	RW	RW	RW

P1H (FF06h / 83h) SFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	P1H.7	P1H.6	P1H.5	P1H.4	P1H.3	P1H.2	P1H.1	P1H.0
								RW	RW	RW	RW	RW	RW	RW	RW

P1X.y	**Port Data Register P1H or P1L Bit y**

DP1L (F104h / 82h) ESFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DP1L.7	DP1L.6	DP1L.5	DP1L.4	DP1L.3	DP1L.2	DP1L.1	DP1L.0
								RW	RW	RW	RW	RW	RW	RW	RW

DP1H (F106h / 83h) ESFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DP1H.7	DP1H.6	DP1H.5	DP1H.4	DP1H.3	DP1H.2	DP1H.1	DP1H.0
								RW	RW	RW	RW	RW	RW	RW	RW

DP1X.y	**Port Direction Register DP1H or DP1L Bit y** DP1X.y = 0: Port line P1X.y is an input (high-impedance) DP1X.y = 1: Port line P1X.y is an output

12.4.1 - Alternate Functions of PORT1

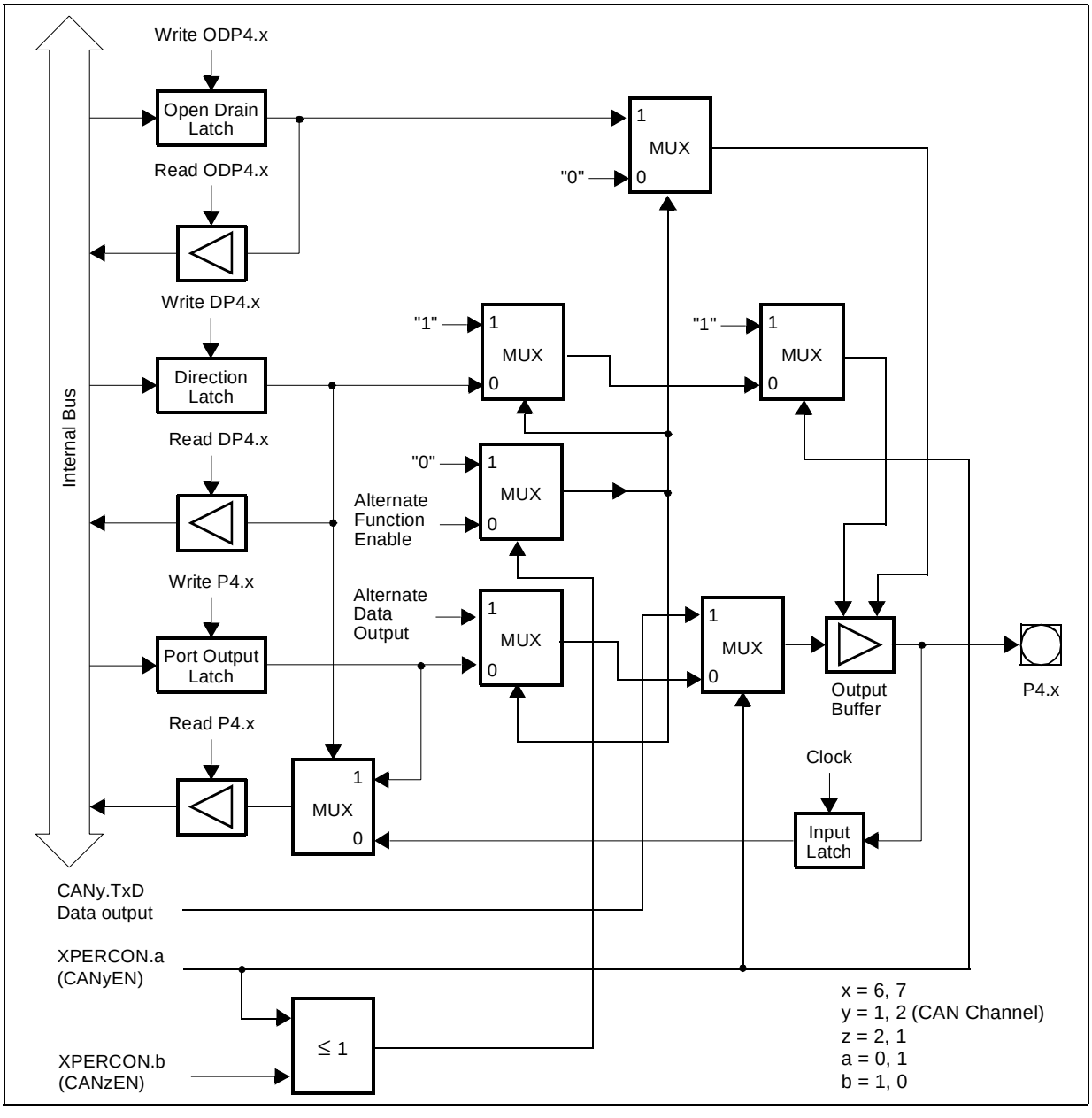
When a demultiplexed external bus is enabled, PORT1 is used as address bus.
Note: Demultiplexed bus modes use PORT1 as a 16-bit port. Otherwise all 16 port lines can be used for general purpose I/O.

The upper 4 pins of PORT1 (P1H.7...P1H.4) are used as capture input lines (CC27IO...CC24IO).

During external accesses in demultiplexed bus modes PORT1 outputs the 16-bit intra-segment address as an alternate output function.

During external accesses in multiplexed bus modes, when no BUSCON register selects a demultiplexed bus mode, PORT1 is not used and is available for general purpose I/O.

Figure 33 : Block Diagram of P4.6 and P4.7 Pins



12.8 - Port 5

This 16-bit input port can only read data. There is no output latch and no direction register. Data written to P5 will be lost.

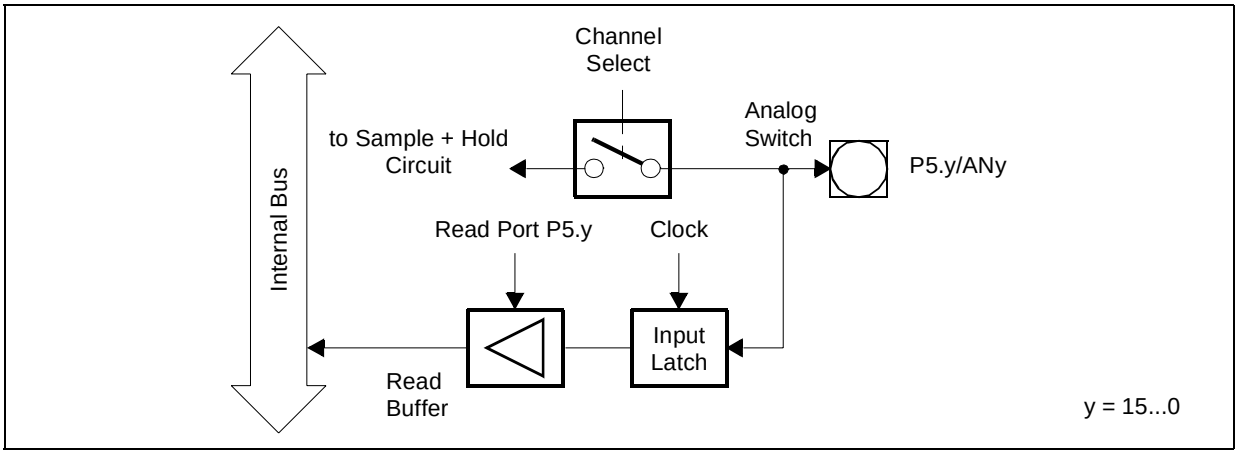
P5 (FFA2h / D1h) SFR Reset Value: XXXXh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P5.15	P5.14	P5.13	P5.12	P5.11	P5.10	P5.9	P5.8	P5.7	P5.6	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

P5.y	**Port Data Register P5 Bit y (Read only)**

Port 5 pins have a special port structure (see Figure 35), first because it is an input only port, and second because the analog input channels are directly connected to the pins rather than to the input latches.

Figure 35 : Block Diagram of a Port 5 Pin



12.8.2 - Port 5 Schmitt Trigger Analog Inputs

A Schmitt trigger protection can be activated on each pin of Port 5 by setting the dedicated bit of register P5DIDIS.

P5DIDIS (FFA4h / D2h) SFR Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P5DI DIS.15	P5DI DIS.14	P5DI DIS.13	P5DI DIS.12	P5DI DIS.11	P5DI DIS.10	P5DI DIS.9	P5DI DIS.8	P5DI DIS.7	P5DI DIS.6	P5DI DIS.5	P5DI DIS.4	P5DI DIS.3	P5DI DIS.2	P5DI DIS.1	P5DI DIS.0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

P5DIDIS.y	**Port 5 Digital Disable Register Bit y** P5DIDIS.y = 0: Port line P5.y digital input is enabled (Schmitt trigger enabled) P5DIDIS.y = 1: Port line P5.y digital input is disabled (Schmitt trigger disabled, necessary for input leakage current reduction)

12.9 - Port 6

If this 8-bit port is used for general purpose I/O, the direction of each line can be configured via the corresponding direction register DP6. Each port line can be switched into push/pull or open drain mode via the open drain control register ODP6.

P6 (FFCCh / E6h) SFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	P6.7	P6.6	P6.5	P6.4	P6.3	P6.2	P6.1	P6.0
								RW	RW	RW	RW	RW	RW	RW	RW

P6.y	**Port Data Register P6 Bit y**

DP6 (FFCEH / E7H) SFR Reset Value: --00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	DP6.7	DP6.6	DP6.5	DP6.4	DP6.3	DP6.2	DP6.1	DP6.0
								RW	RW	RW	RW	RW	RW	RW	RW

The chip select lines of Port 6 have an internal weak pull-up device. This device is switched on during reset. This feature is implemented to drive the chip select lines high during reset in order to avoid multiple chip selection.
After reset the $\overline{CS}$ function must be used, if selected so. In this case there is no possibility to program any port latches before. Thus the alternate function ($\overline{CS}$) is selected automatically in this case.

Note: The open drain output option can only be selected via software earliest during the initialization routine; at least signal $\overline{CS0}$ will be in push/pull output driver mode directly after reset.

Figure 37 : Block Diagram of Port 6 Pins with an Alternate Output Function

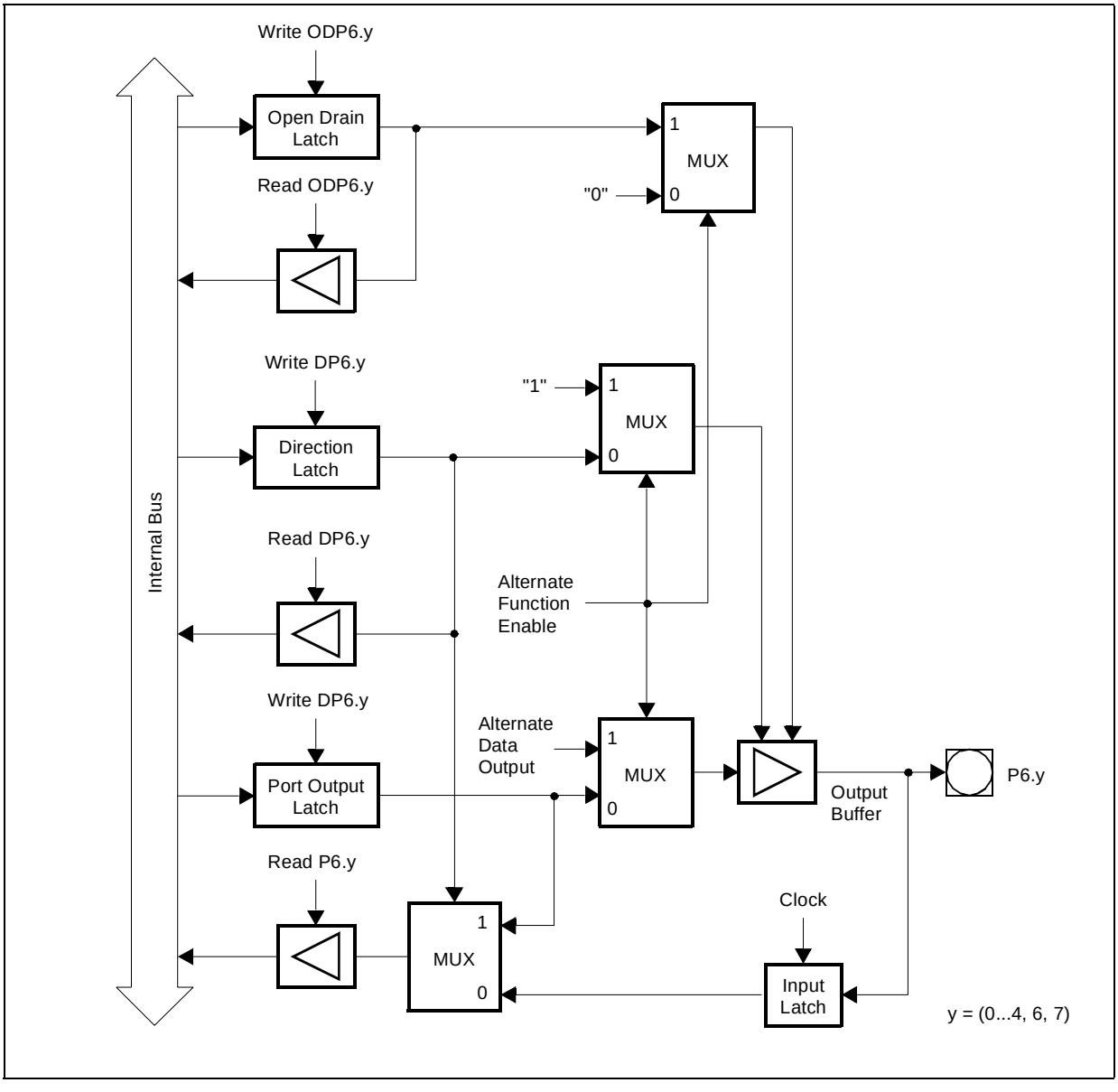
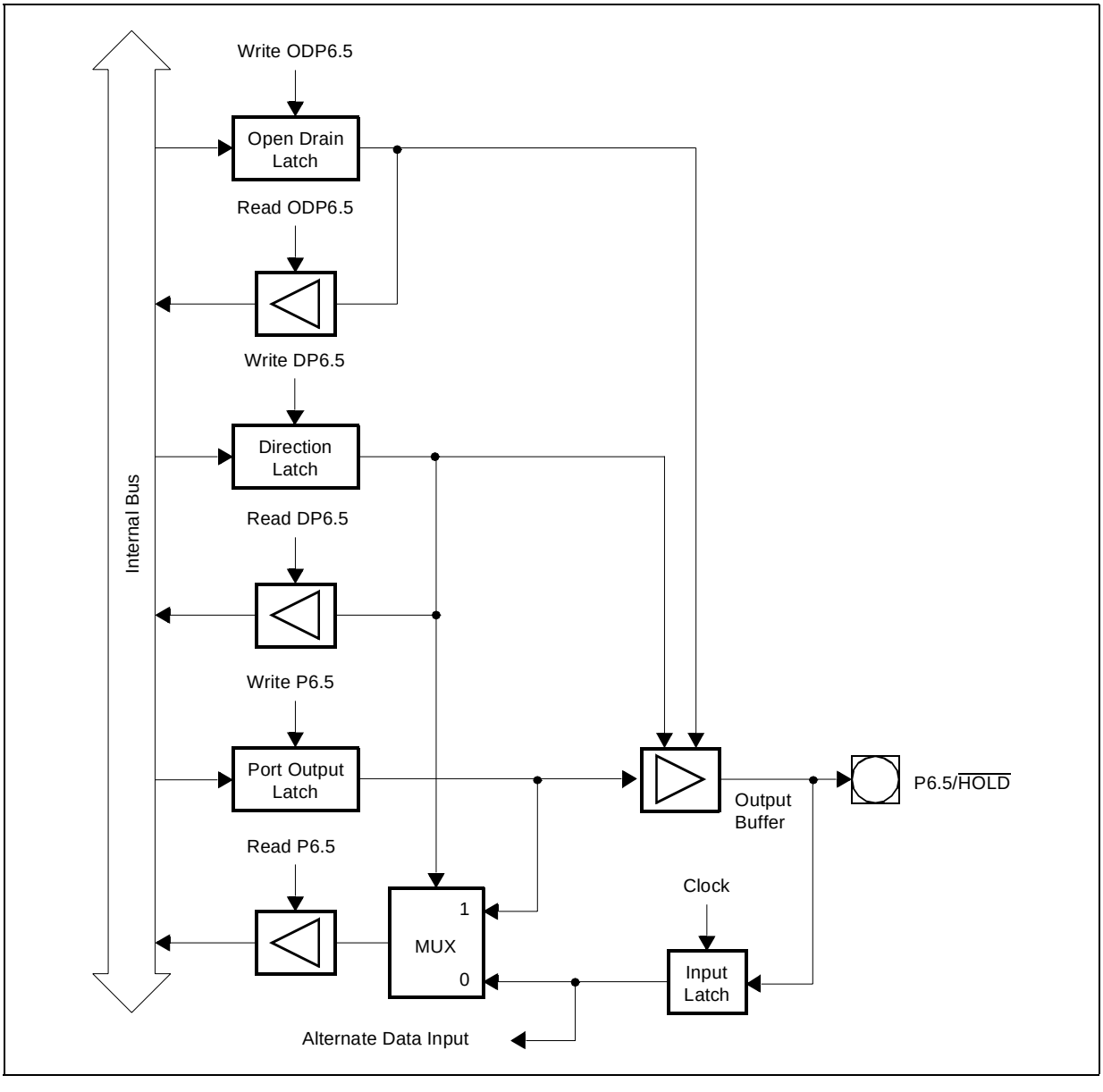


Figure 38 : Block Diagram of Pin P6.5 ($\overline{\text{HOLD}}$)



13 - A/D CONVERTER

A 10-bit A/D converter with 16 multiplexed input channels and a sample and hold circuit is integrated on-chip. The sample time (for loading the capacitors) and the conversion time is programmable and can be adjusted to the external circuitry.

To remove high frequency components from the analog input signal, a low-pass filter must be connected at the ADC input.

Overrun error detection / protection is controlled by the ADDAT register. Either an interrupt request is generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended until the previous result has been read. For applications which require less than 16 analog input channels, the remaining channel inputs can be used as digital input port pins. The A/D converter of the ST10F269 supports different conversion modes:

– **Single channel single conversion**: the analog level of the selected channel is sampled once and converted. The result of the conversion is stored in the ADDAT register.

– **Single channel continuous conversion**: the analog level of the selected channel is repeatedly sampled and converted. The result of the conversion is stored in the ADDAT register.

– **Auto scan single conversion**: the analog level of the selected channels are sampled once and converted. After each conversion the result is stored in the ADDAT register. The data can be transferred to the RAM by interrupt software management or using the powerful Peripheral Event Controller (PEC) data transfer.

– **Auto scan continuous conversion**: the analog level of the selected channels are repeatedly sampled and converted. The result of the conversion is stored in the ADDAT register. The data can be transferred to the RAM by interrupt software management or using the PEC data transfer.

– **Wait for ADDAT read mode**: when using continuous modes, in order to avoid to overwrite the result of the current conversion by the next one, the ADWR bit of ADCON control register must be activated. Then, until the ADDAT register is read, the new result is stored in a temporary buffer and the conversion is on hold.

– **Channel injection mode**: when using continuous modes, a selected channel can be converted in between without changing the current operating mode. The 10-bit data of the conversion are stored in ADRES field of ADDAT2. The current continuous mode remains active after the single conversion is completed

Table 26 : ADC Sample Clock and Conversion Clock (PQFP144 devices)

ADCTC	Conversion Clock t_{CC}		ADSTC	Sample Clock t_{SC}	
	TCL[1] = 1/2 x f_{XTAL}	At f_{CPU} = 40MHz		t_{SC} =	At f_{CPU} = 40MHz
00	TCL x 24	0.3µs	00	t_{CC}	0.3µs [2]
01	Reserved, do not use	Reserved	01	t_{CC} x 2	0.6µs [2]
10	TCL x 96	1.2 µs	10	t_{CC} x 4	1.2µs [2]
11	TCL x 48	0.6 µs	11	t_{CC} x 8	2.4µs [2]

Notes: 1. Section 21.4.5 -: Direct Drive for TCL definition.
2. t_{CC} = TCL x 24

14.1.2 - ASCO in Synchronous Mode

In synchronous mode, data are transmitted or received synchronously to a shift clock which is generated by the ST10F269. Half-duplex communication up to 5M Baud (at 40MHz f_{CPU}) or 4M Baud (at 32MHz) is possible in this mode.

Figure 45 : Synchronous Mode of Serial Channel ASC0

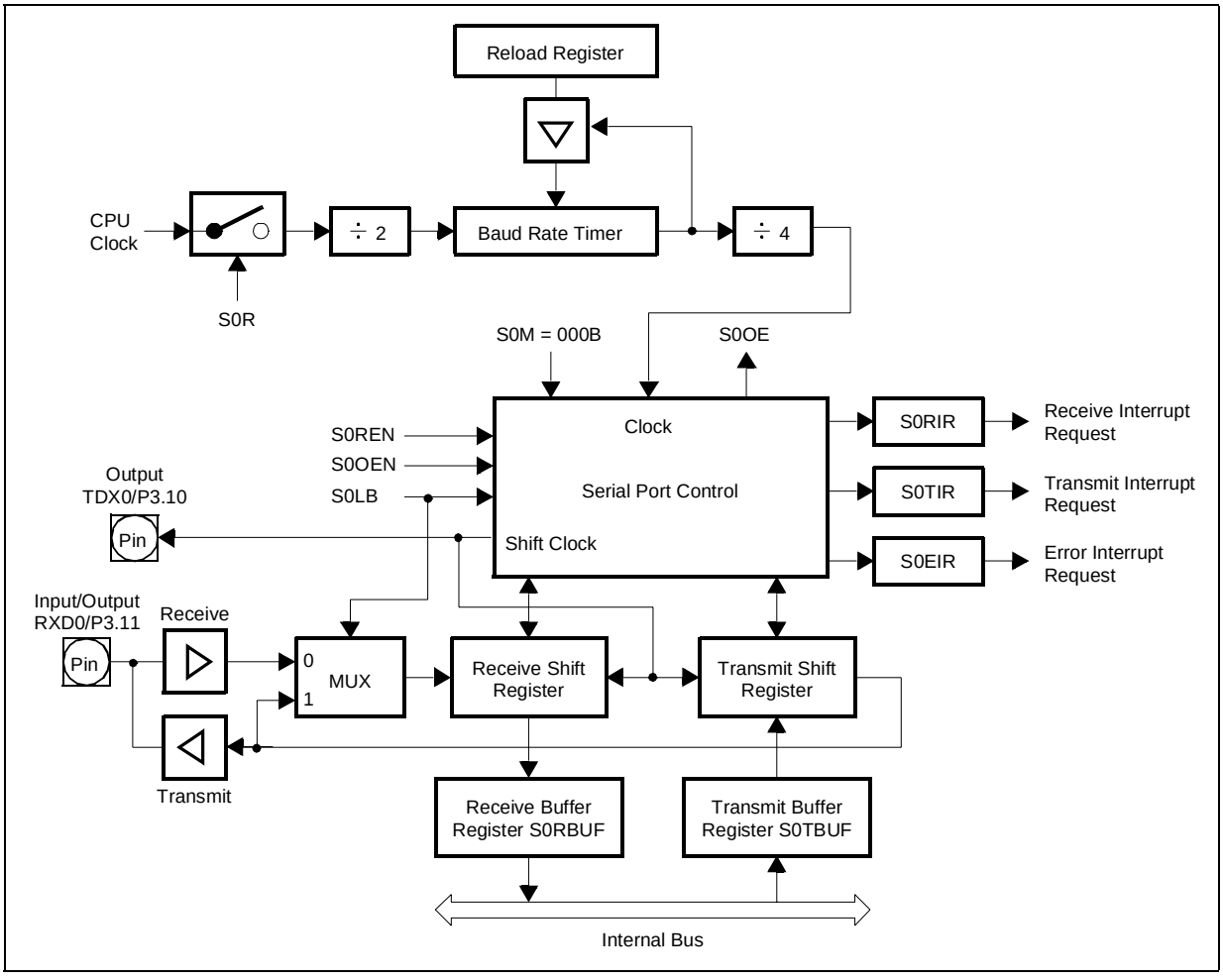


Figure 59 : Minimum External Reset Circuitry

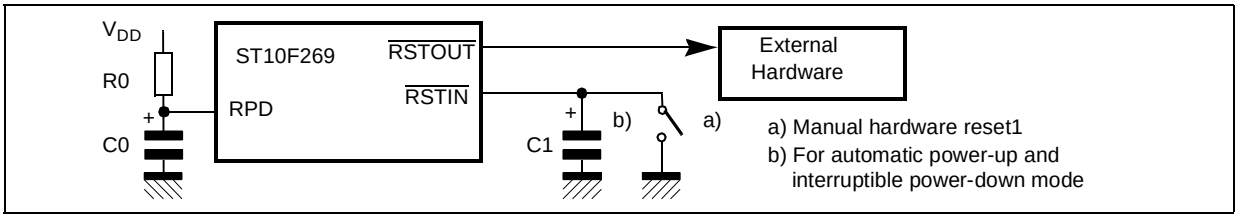


Figure 60 : External Reset Hardware Circuitry

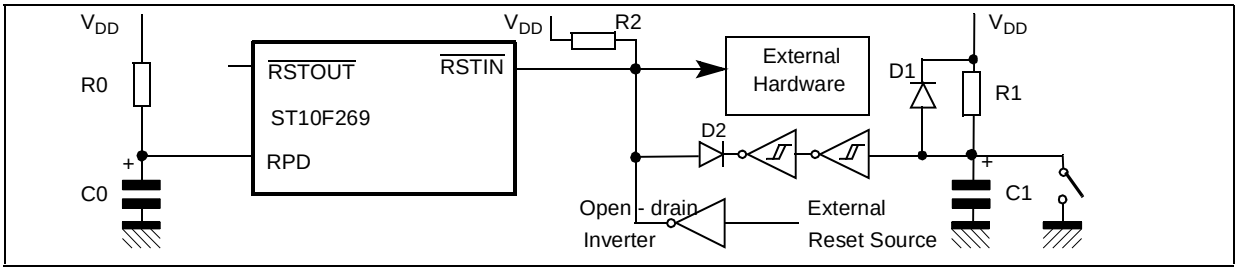


Table 38 : PORT0 Latched Configuration for the Different Resets

X: Pin is sampled -: Pin is not sampled	PORT0															
	Clock Options			Seem. Add. Lines		Chip Selects		WR confide.	Bus Type		Reserved	BSL	Reserved	Reserved	Adapt Mode	Emu Mode
Sample event	**P0H.7**	**P0H.6**	**P0H.5**	**P0H.4**	**P0H.3**	**P0H.2**	**P0H.1**	**P0H.0**	**P0L.7**	**P0L.6**	**P0L.5**	**P0L.4**	**P0L.3**	**P0L.2**	**P0L.1**	**P0L.0**
Software Reset	-	-	-	X	X	X	X	X	X	X	-	-	-	-	-	-
Watchdog Reset	-	-	-	X	X	X	X	X	X	X	-	-	-	-	-	-
Short Hardware Reset	-	-	-	X	X	X	X	X	X	X	X	X	X	X	X	X
Long Hardware Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Power-On Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 39 : PORT0 Bits Latched into the Different Registers After Reset

PORT0 bit Nebr.	**h7**	**h6**	**h5**	**h4**	**h3**	**h2**	**h1**	**h0**	**l7**	**l6**	**l5**	**l4**	**l3**	**l2**	**l1**	**l0**
PORT0 bit Name	CLKCFG	CLKCFG	CLKCFG	SALSEL	SALSEL	CSSEL	CSSEL	WRC	BUSTYP	BUSTYP	R	BSL	R	R	ADP	EMU
RP0H [2]	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	CLKCFG	CLKCFG	CLKCFG	SALSEL	SALSEL	CSSEL	CSSEL	WRC
SYSCON	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	BYTDIS [3]	X [1]	WRCFG [3]	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]
BUSCON0	X [1]	X [1]	X [1]	X [1]	-	BUS ACT0 [4]	ALE CTL0 [4]	-	BTYP	BTYP	X [1]	X [1]	X [1]	X [1]	X [1]	X [1]
Internal Logic	To Clock Generator			To Port 4 Logic		To Port 6 Logic		X [1]	X [1]	X [1]	X [1]	Internal	X [1]	X [1]	Internal	Internal

Notes: 1. Not latched from PORT0.

2. Only RP0H low byte is used and the bit-fields are latched from PORT0 high byte to RP0H low byte.

Figure 62 : Simplified Powerdown Exit Circuitry

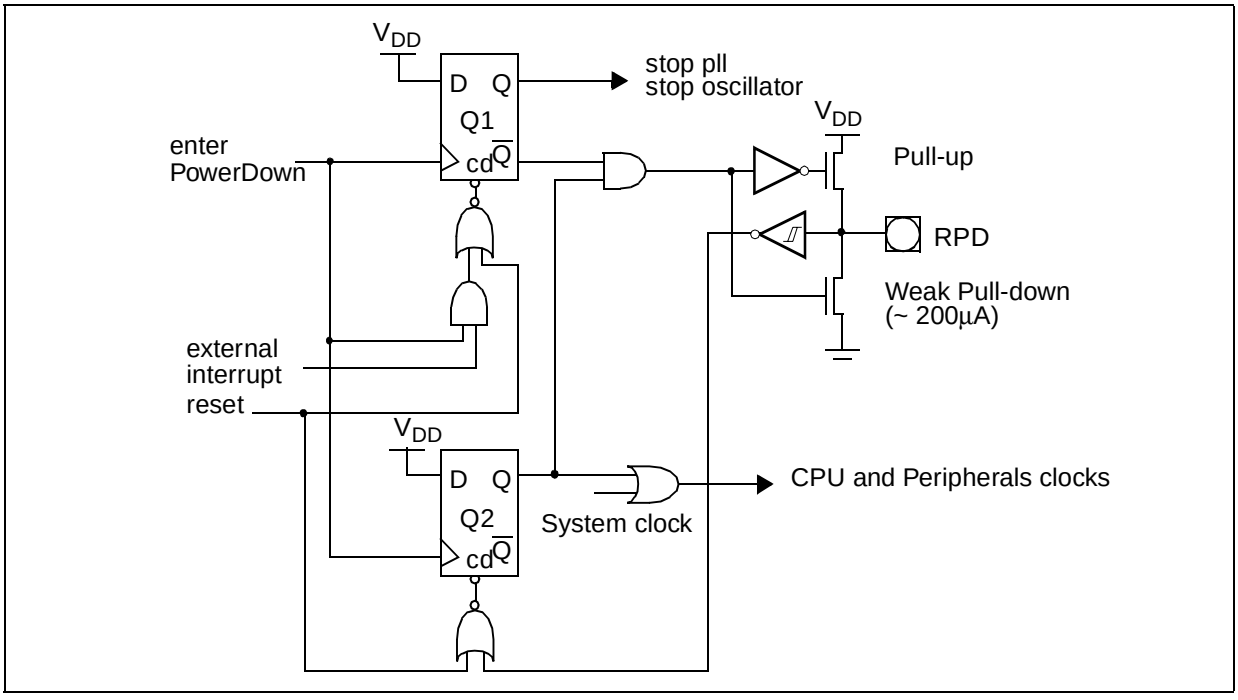


Figure 63 : Powerdown Exit Sequence When Using an External Interrupt (PLL x 2)

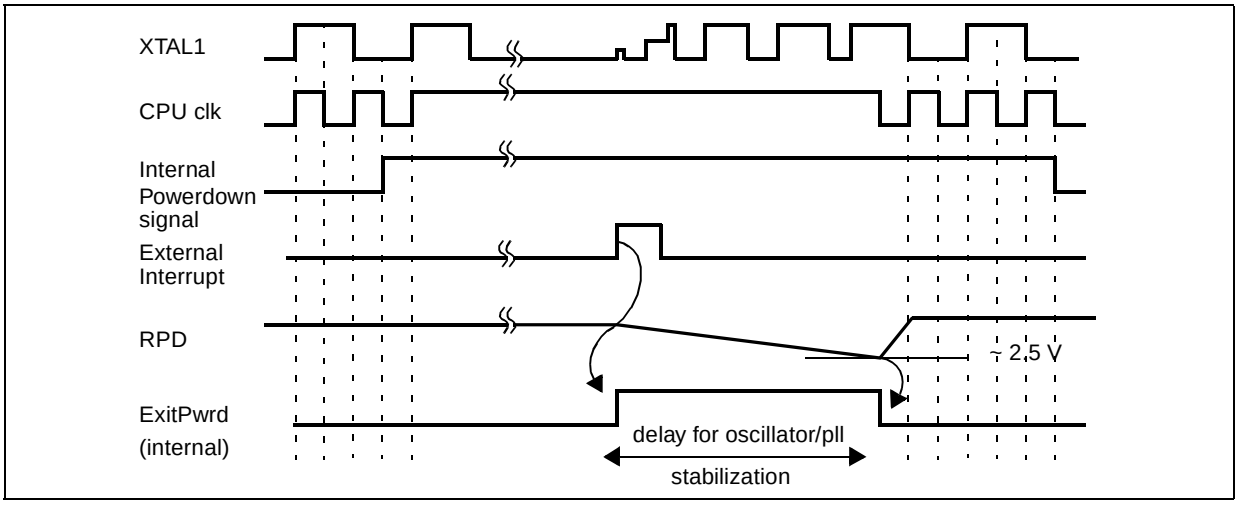


Table 40 : Special Function Registers Listed by Name (continued)

Name		Physical address		8-bit address	Description	Reset value
T0IC	b	FF9Ch		CEh	CAPCOM Timer 0 Interrupt Control Register	- - 00h
T0REL		FE54h		2Ah	CAPCOM Timer 0 Reload Register	0000h
T1		FE52h		29h	CAPCOM Timer 1 Register	0000h
T1IC	b	FF9Eh		CFh	CAPCOM Timer 1 Interrupt Control Register	- - 00h
T1REL		FE56h		2Bh	CAPCOM Timer 1 Reload Register	0000h
T2		FE40h		20h	GPT1 Timer 2 Register	0000h
T2CON	b	FF40h		A0h	GPT1 Timer 2 Control Register	0000h
T2IC	b	FF60h		B0h	GPT1 Timer 2 Interrupt Control Register	- - 00h
T3		FE42h		21h	GPT1 Timer 3 Register	0000h
T3CON	b	FF42h		A1h	GPT1 Timer 3 Control Register	0000h
T3IC	b	FF62h		B1h	GPT1 Timer 3 Interrupt Control Register	- - 00h
T4		FE44h		22h	GPT1 Timer 4 Register	0000h
T4CON	b	FF44h		A2h	GPT1 Timer 4 Control Register	0000h
T4IC	b	FF64h		B2h	GPT1 Timer 4 Interrupt Control Register	- - 00h
T5		FE46h		23h	GPT2 Timer 5 Register	0000h
T5CON	b	FF46h		A3h	GPT2 Timer 5 Control Register	0000h
T5IC	b	FF66h		B3h	GPT2 Timer 5 Interrupt Control Register	- - 00h
T6		FE48h		24h	GPT2 Timer 6 Register	0000h
T6CON	b	FF48h		A4h	GPT2 Timer 6 Control Register	0000h
T6IC	b	FF68h		B4h	GPT2 Timer 6 Interrupt Control Register	- - 00h
T7		F050h	E	28h	CAPCOM Timer 7 Register	0000h
T78CON	b	FF20h		90h	CAPCOM Timer 7 and 8 Control Register	0000h
T7IC	b	F17Ah	E	BEh	CAPCOM Timer 7 Interrupt Control Register	- - 00h
T7REL		F054h	E	2Ah	CAPCOM Timer 7 Reload Register	0000h
T8		F052h	E	29h	CAPCOM Timer 8 Register	0000h
T8IC	b	F17Ch	E	BFh	CAPCOM Timer 8 Interrupt Control Register	- - 00h
T8REL		F056h	E	2Bh	CAPCOM Timer 8 Reload Register	0000h
TFR	b	FFACh		D6h	Trap Flag Register	0000h
WDT		FEAEh		57h	Watchdog Timer Register (read only)	0000h
WDTCON	b	FFAEh		D7h	Watchdog Timer Control Register	00xxh [2]
XP0IC	b	F186h	E	C3h	CAN1 Module Interrupt Control Register	- - 00h [3]
XP1IC	b	F18Eh	E	C7h	CAN2 Module Interrupt Control Register	- - 00h [3]
XP2IC	b	F196h	E	CBh	Flash ready/busy interrupt control register	- - 00h [3]
XP3IC	b	F19Eh	E	CFh	PLL unlock Interrupt Control Register	- - 00h [3]
XPERCON		F024h	E	12h	XPER Configuration Register	- - 05h
ZEROS	b	FF1Ch		8Eh	Constant Value 0's Register (read only)	0000h

Notes: 1. The system configuration is selected during reset.

2. Bit WDTR indicates a watchdog timer triggered reset.

3. The XPnIC Interrupt Control Registers control interrupt requests from integrated X-Bus peripherals. Some software controlled interrupt requests may be generated by setting the XPnIR bits (of XPnIC register) of the unused X-peripheral nodes.

21.3.1 - A/D Converter Characteristics

V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = -40 to +85°C or -40 to +125°C, 4.0V ≤ V_{AREF} ≤ V_{DD} + 0.1V; V_{SS}0.1V ≤ V_{AGND} ≤ V_{SS} + 0.2V

Table 41 : A/D Converter Characteristics

Symbol		Parameter	Test Condition	Limit Values		Unit
				minimum	maximum	
V_{AREF}	SR	Analog Reference voltage		4.0	V_{DD} + 0.1	V
V_{AIN}	SR	Analog input voltage	1 - 8	V_{AGND}	V_{AREF}	V
I_{AREF}	CC	Reference supply current running mode power-down mode	7	 – –	 500 1	 µA µA
C_{AIN}	CC	ADC input capacitance Not sampling Sampling	7	 – –	 10 15	 pF pF
t_S	CC	Sample time	2 - 4	48 TCL	1 536 TCL	
t_C	CC	Conversion time	3 - 4	388 TCL	2 884 TCL	
DNL	CC	Differential Nonlinearity	5	-0.5	+0.5	LSB
INL	CC	Integral Nonlinearity	5	-1.5	+1.5	LSB
OFS	CC	Offset Error	5	-1.0	+1.0	LSB
TUE	CC	Total unadjusted error	5	-2.0	+2.0	LSB
R_{ASRC}	SR	Internal resistance of analog source	t_S in [ns] 2 - 7	–	(t_S / 150) - 0.25	kΩ
K	CC	Coupling Factor between inputs	6 - 7	–	1/500	

Notes: 1. V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be X000h or X3FFh, respectively.

2. During the t_S sample time the input capacitance C_{ain} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within the t_S sample time. After the end of the t_S sample time, changes of the analog input voltage have no effect on the conversion result. Values for the t_{SC} sample clock depend on the programming. Referring to the t_C conversion time formula of Section 21.3.2 - 'Conversion Timing Control' on page 145 and to Table 42 on page 145:
- t_S min. = 2 t_{SC} min. = 2 t_{CC} min. = 2 x 24 x TCL = 48 TCL
- t_S max = 2 t_{SC} max = 2 x 8 t_{CC} max = 2 x 8 x 96 TCL = 1536 TCL
TCL is defined in Section 21.4.2 -, Section 21.4.4 -, and Section 21.4.5 - 'Direct Drive' on page 149:

3. The conversion time formula is:
- t_C = 14 t_{CC} + t_S + 4 TCL (= 14 t_{CC} + 2 t_{SC} + 4 TCL)
The t_C parameter includes the t_S sample time, the time for determining the digital result and the time to load the result register with the result of the conversion. Values for the t_{CC} conversion clock depend on the programming. Referring to Table 42 on page 145:
- t_C min. = 14 t_{CC} min. + t_S min. + 4 TCL = 14 x 24 x TCL + 48 TCL + 4 TCL = 388 TCL
- t_C max = 14 t_{CC} max + t_S max + 4 TCL = 14 x 96 TCL + 1536 TCL + 4 TCL = 2884 TCL

4. This parameter is fixed by ADC control logic.

5. DNL, INL, TUE are tested at V_{AREF} = 5.0V, V_{AGND} = 0V, V_{CC} = 4.9V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
'LSB' has a value of V_{AREF} / 1024.
The specified TUE is guaranteed only if an overload condition (see I_{OV} specification) occurs on maximum 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10mA.

6. The coupling factor is measured on a channel while an overload condition occurs on the adjacent not selected channel with an absolute overload current less than 10mA.

7. Partially tested, guaranteed by design characterization.

8.To remove noise and undesirable high frequency components from the analog input signal, a low-pass filter must be connected at the ADC input. The cut-off frequency of this filter should avoid 2 opposite transitions during the t_s sampling time of the ST10 ADC:
- $f_{cut\text{-}off}$ ≤ 1 / 5 t_s to 1/10 t_s
where t_s is the sampling time of the ST10 ADC and is not related to the Nyquist frequency determined by the t_c conversion time.

21.4.4 - Prescaler Operation

When pins P0.15-13 (P0H.7-5) equal '001' during reset, the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{XTAL} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{XTAL}.

The timings listed in the AC Characteristics that refer to TCL therefore can be calculated using the period of f_{XTAL} for any TCL.

Note that if the bit OWDDIS in SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

21.4.5 - Direct Drive

When pins P0.15-13 (P0H.7-5) equal '011' during reset the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.

The frequency of f_{CPU} directly follows the frequency of f_{XTAL} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{XTAL}.

Therefore, the timings given in this chapter refer to the minimum TCL. This minimum value can be calculated by the following formula:

$$TCL_{min} = 1/f_{XTAL} \times DC_{min}$$

$$DC = \text{duty cycle}$$

For two consecutive TCLs, the deviation caused by the duty cycle of f_{XTAL} is compensated, so the duration of 2TCL is always $1/f_{XTAL}$.

The minimum value TCL_{min} has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula:

$$2TCL = 1/f_{XTAL}$$

Note: The address float timings in Multiplexed bus mode (t_{11} and t_{45}) use the maximum duration of TCL ($TCL_{max} = 1/f_{XTAL} \times DC_{max}$) instead of TCL_{min}.
If the bit OWDDIS in SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

21.4.6 - Oscillator Watchdog (OWD)

An on-chip watchdog oscillator is implemented in the ST10F269. This feature is used for safety operation with external crystal oscillator (using direct drive mode with or without prescaler). This watchdog oscillator operates as following:

The reset default configuration enables the watchdog oscillator. It can be disabled by setting the OWDDIS (bit 4) of SYSCON register.

When the OWD is enabled, the PLL runs at its free-running frequency, and it increments the watchdog counter. The PLL free-running frequency is between 2 and 10MHz. On each transition of external clock, the watchdog counter is cleared. If an external clock failure occurs, then the watchdog counter overflows (after 16 PLL clock cycles).

The CPU clock signal will be switched to the PLL free-running clock signal, and the oscillator watchdog Interrupt Request (XP3INT) is flagged. The CPU clock will not switch back to the external clock even if a valid external clock exits on XTAL1 pin. Only a hardware reset can switch the CPU clock source back to direct clock input.

When the OWD is disabled, the CPU clock is always external oscillator clock and the PLL is switched off to decrease consumption supply current.

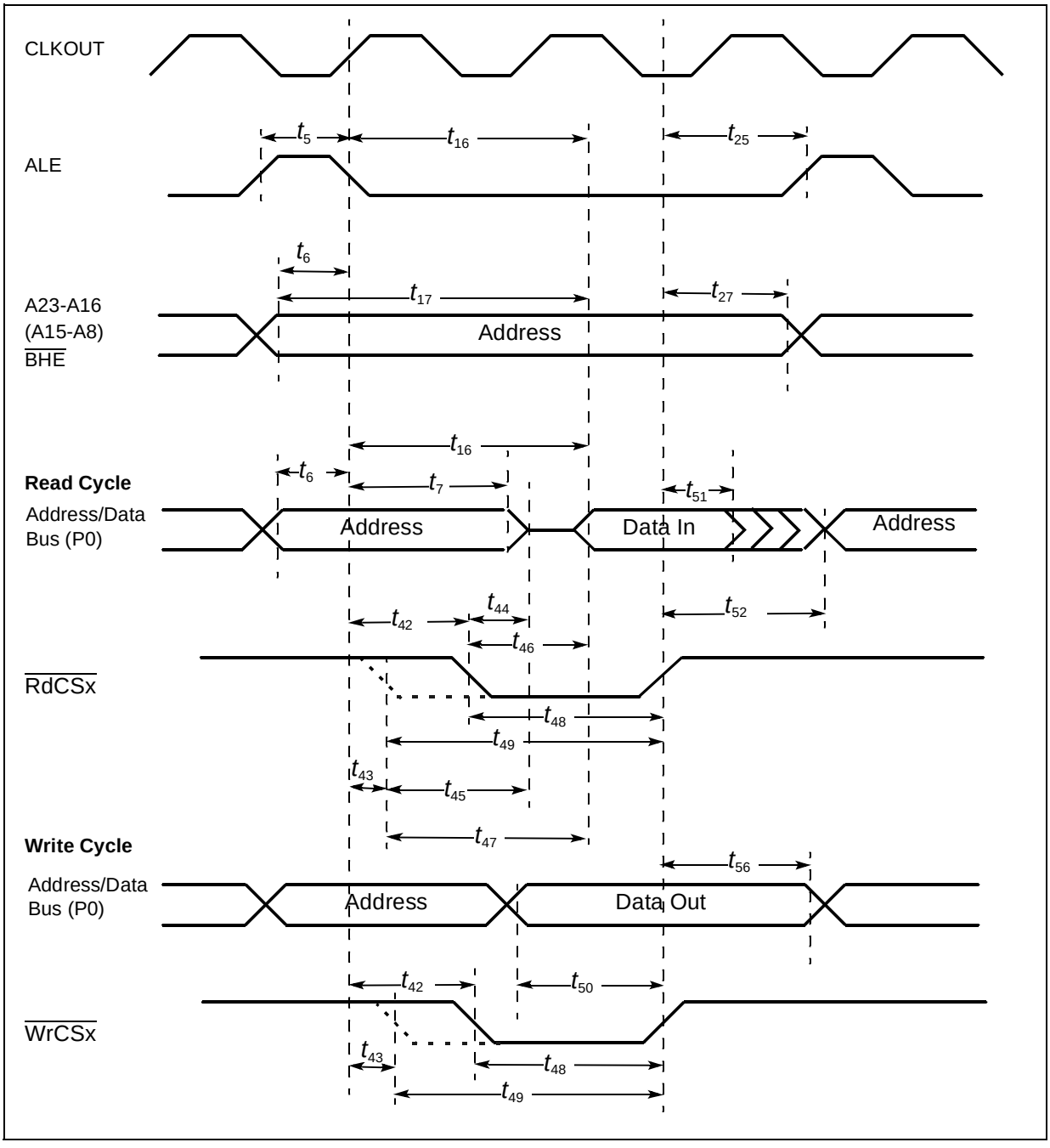
21.4.7 - Phase Locked Loop

For all other combinations of pins P0.15-13 (P0H.7-5) during reset the on-chip phase locked loop is enabled and it provides the CPU clock (see Table 44 and Table 45). The PLL multiplies the input frequency by the factor F which is selected via the combination of pins P0.15-13 ($f_{CPU} = f_{XTAL} \times F$). With every F'th transition of f_{XTAL} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, so the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{XTAL}. The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

Figure 73 : External Memory Cycle: Multiplexed Bus, With / Without Read / Write Delay, Normal ALE, Read / Write Chip Select

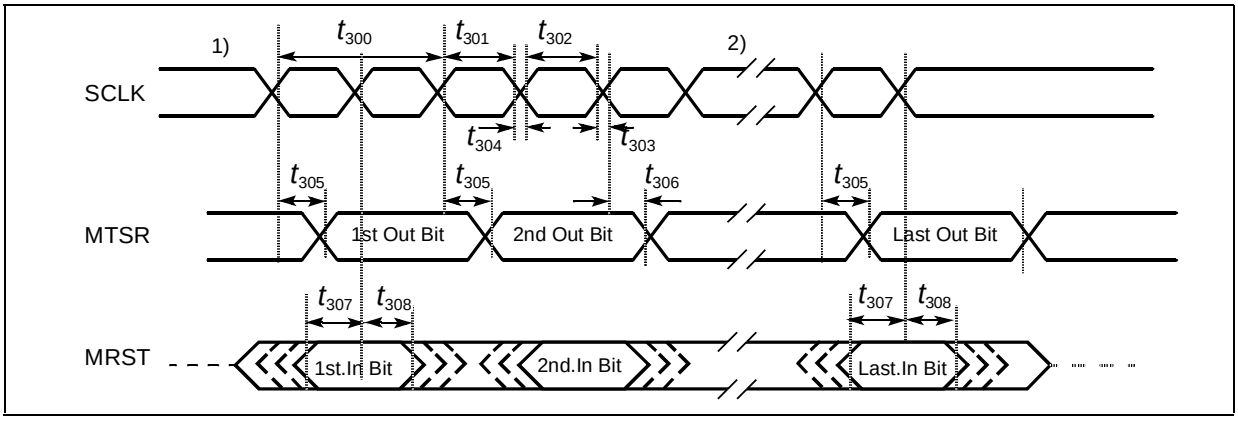


Symbol		Parameter	Maximum Baud rate=6.25MBd (<SSCBR> = 0001h)		Variable Baud rate (<SSCBR>=0001h-FFFFh)		Symbol
			Minimum	Maximum	Minimum	Maximum	
t_{318}	SR	Read data hold time after latch edge, phase error detection off (SSCPEN = 0)	41.25	–	2TCL + 10	–	t_{318}

Note: 1. Timing guaranteed by design.

*The formula for SSC Clock Cycle time is : t_{300} = 4 TCL * (<SSCBR> + 1)*
Where <SSCBR> represents the content of the SSC Baud rate register, taken as unsigned 16-bit integer

Figure 82 : SSC Master Timing



Notes: 1. The phase and polarity of shift and latch edge of SCLK is programmable. This figure uses the leading clock edge as shift edge (drawn in bold), with latch on trailing edge (SSCPH = 0b), Idle clock line is low, leading clock edge is low-to-high transition (SSCPO = 0b).
2. The bit timing is repeated for all bits to be transmitted or received.

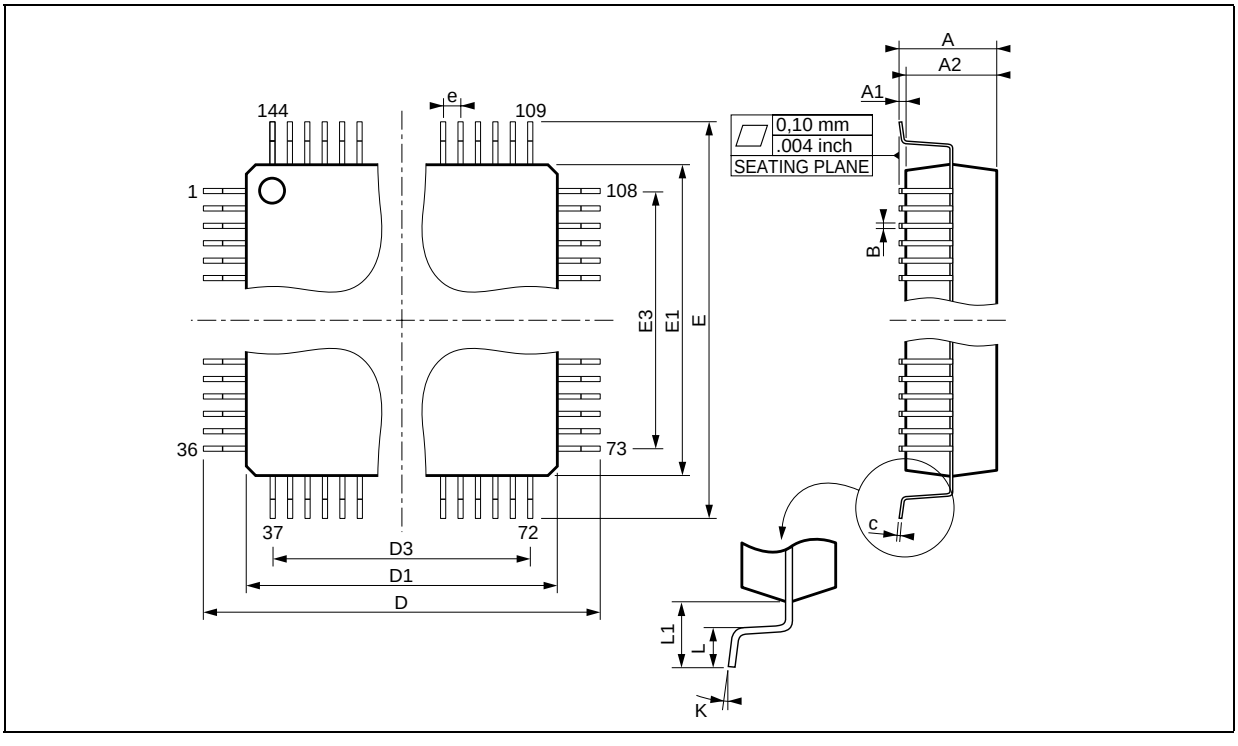
21.4.14.2 Slave mode

V_{CC} = 5V ±10%, V_{SS} = 0V, CPU clock = 40MHz, T_A = -40 to +125°C, C_L = 50pF (PQFP144 devices)

Symbol		Parameter	Maximum Baud rate=10MBd (<SSCBR> = 0001h)		Variable Baud rate (<SSCBR>=0001h-FFFFh)		Unit
			Minimum	Maximum	Minimum	Maximum	
t_{310}	SR	SSC clock cycle time	100	100	8 TCL	262144 TCL	ns
t_{311}	SR	SSC clock high time	40	–	t_{310}/2 - 10	–	ns
t_{312}	SR	SSC clock low time	40	–	t_{310}/2 - 10	–	ns
t_{313}	SR	SSC clock rise time	–	10	–	10	ns
t_{314}	SR	SSC clock fall time	–	10	–	10	ns
t_{315}	CC	Write data valid after shift edge	–	39	–	2 TCL + 14	ns
t_{316}	CC	Write data hold after shift edge	0	–	0	–	ns
t_{317p}	SR	Read data setup time before latch edge, phase error detection on (SSCPEN = 1)	62	–	4TCL + 12	–	ns
t_{318p}[1]	SR	Read data hold time after latch edge, phase error detection on (SSCPEN = 1)	87	–	6TCL + 12	–	ns

22 - PACKAGE MECHANICAL DATA

Figure 84 : Package Outline PQFP144 (28 x 28mm)



Dimensions	Millimeters [1]			Inches (approx)		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
A			4.07			0.160
A1	0.25			0.010		
A2	3.17	3.42	3.67	0.125	0.133	0.144
B	0.22		0.38	0.009		0.015
c	0.13		0.23	0.005		0.009
D	30.95	31.20	31.45	1.219	1.228	1.238
D1	27.90	28.00	28.10	1.098	1.102	1.106
D3		22.75			0.896	
e		0.65			0.026	
E	30.95	31.20	31.45	1.219	1.228	1.238
E1	27.90	28.00	28.10	1.098	1.102	1.106
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0° (Minimum), 7° (Maximum)					

Note: 1. Package dimensions are in mm. The dimensions quoted in inches are rounded.